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A document starting from the next page has been made as a new annex regarding frame process and delay according to the last CarCOM meeting.

New changes:

1. Some incorrect or broken parts mainly in Figure X.4 have been fixed and the document has been stored in \*.docx format to avoid such troubles.

Annex X

Frame process and Delay

## General

This Annex provides definition and handling of delay for frame process subsystems.

Typical speech enhancement subsystems have spectral analysis/synthesis processes to realize good noise reduction or echo cancellation. Time domain input signal in a fixed length of window is applied, analyzed, enhanced, then synthesized by overlap-add method. The windowing period is often called “frame shift”.

Typical data transport subsystems also take frame processes for efficient data compression or error correction. A unit of the data transferred is called a “packet”.

When two subsystems, sender and receiver, having different frame data interval interfaces to each other, a special data buffer must be inserted to arbitrate the difference of intervals. Several definitions about delay and framing process should be given to such processing. This Annex provides the definitions for such parameters.

## Frame interval

**Frame interval** is defined as a logical time interval of input or output frame data. Frame interval of time domain data is regarded as 1 sample period. Subsystem having framed input or output signals shall specify the frame interval.

**Frame rate** is the reciprocal of frame interval.

## Delay

Subsystem having framed input or output signals may have two types of delays, **buffer delay** and **input/output delay**. If the subsystem is composed of software, **algorithmic delay** is defined, and **computational delay** is also defined after the software implementation. Table X.1 provides the definition of these delays. A subsystem supplier shall specify the correspondent delay time.

Table X.1 – Definition of delays

|  |  |  |
| --- | --- | --- |
| Category | | Definition |
| Buffer delay | | Additional delay time when a buffer is introduced at interface to arbitrate frame size difference. |
| Input/output delay | | Subsystem’s physical delay time from data input to output. |
| Software | Algorithmic delay | Subsystem’s logical delay time in case the subsystem is realized by software. |
| Computational delay | Additional computational delay time from data input to output caused by a processor. It is applied in case the software subsystem is implemented onto the processor. |

Figure X.1 shows a system integrating two framed software subsystems on a processor. Input buffer A is placed before subsystem A to convert input sampled data to framed data. If Subsystems A and B has the same frame interval, a buffer between these subsystems should not be necessary. After subsystem B, the output framed data is converted to sampled data by output buffer B which can be regarded as no delay.

The overall delay of this system is calculated by summing buffer delay A, algorithmic delay A, algorithmic delay B and computational delay.

Overall system delay =

(Buffer delay A) + (Algorithmic delay A) + (Algorithmic delay B) + (Computational delay)

[Processor]

[Software]

Subsystem A

[Software]

Subsystem B

Buffer

delay A

No buffer here

Sampled data

Framed

data

No buffer

delay

Input buffer A

Algorithmic

delay A

Output buffer B

Algorithmic

delay B

Framed

data

Framed

data

Sampled data

Computational

delay

Figure X.1: Framing and Delays

## Arbitration between two subsystems having different frame intervals

When a receiver subsystem interfaces with sender subsystem having different frame interval, a data buffer shall be shall be categorized into following cases.

## Sender’s and receiver’s frame intervals are identical

No additional delay is to be inserted.

## Sender’s frame interval is a multiple of receiver’s frame interval

No delay will be added at the receiver. The total delay equals to the sender’s delay. Figure X.2 shows an example that sender’s frame interval is 15 msec and receiver’s is 5 msec. Algorithmic delay and computational delay are omitted. In Figure X.1, subsystem A can be regarded as the sender, subsystem B as the receiver, buffer A as the sender’s input buffer, and buffer B as the receiver’s output buffer.

Sender:

Receiver:

Buffer delay = 15 ms

Buffer delay = 0 ms

Total delay = 15 ms

0 .......... 5 .......... 10 ..........14ms

0 ... 4ms

5 ... 9ms

15 ... 19ms

10 ... 14ms

15 ........ 20 ........ 25 ........ 29ms

30 ........ 35 ....

Sender’s input buffer:

Receiver’s output buffer:

0 ... 14ms

15 ... 29ms

0 ... 4ms

5 ... 9ms

10...14ms

15...19ms

20...24ms

Figure X.2: Example of Case 2

## Receiver’s frame interval is a multiple of sender’s frame interval

Receiver’s delay buffer size is equal to its frame interval minus sender’s frame interval. However, the total buffer delay is equal to the receiver’s frame interval. Figure X.3 shows an example that sender’s frame interval is 5 msec and receiver’s frame interval is 15 msec.

Buffer delay = 5 ms

Sender:

Receiver:

Buffer delay = 10 ms

Total delay = 15 ms

0 ........ 5 ........ 10 ........ 14ms

15 .......

0 ... 4ms

5 ... 9ms

15 ... 19ms

20 ... 24ms

25 ... 29ms

30 ... 34ms

10 ... 14ms

Sender’s input buffer:

Receiver’s output buffer:

0 ... 14ms

15 ... 29ms

0 ... 4ms

5 ... 9ms

10...14ms

15...19ms

20...24ms

25...29ms

30...34ms

Figure X.3: Example of Case 3

## Other cases

In general case, an arbitration buffer is inserted between two subsystems. Receiver has to read the buffer with the delay equal to its frame interval. It coincides with the case that the data is transferred with time domain signal. The resultant buffering delay is equal to the sum of frame intervals of two subsystems. Figure X.4 shows an example that sender’s frame interval is 5 msec and receiver’s is 8 msec.

Figure X.4: Example of Case 4

Sender:

Receiver:

Buffer delay = 8 ms

Total delay = 13 ms

0 ... 4ms

5 ... 9ms

15 ... 19ms

20 ... 24ms

25 ... 29ms

30 ... 34ms

10 ... 14ms

Sender’s input buffer:

Receiver’s output buffer:

0

Buffer delay = 5 ms

0 ... 7ms

8 ... 15ms

16 ... 23ms

Arbitration buffer:

1

2

3

4

-5

-4

-3

-2

-1

5

6

7

8

9

10

11

12

13

14

15

16

17

18

19

20

21

22

23

24

25

26

27

28

29

0 ... 4ms

5 ... 9ms

10...14ms

15...19ms

20...24ms

25...29ms

30...34ms

0 ... 7ms

30

8 ... 15ms

16 ... 23ms

In special cases where two subsystems are operating on asynchronous clocks, a drop/insert buffer with a unit or the multiples of frame size should be used to arbitrate them.

## Example

An example of wideband mode SRW/hands-free system is shown. Examples of frame process are shown in Table X.2.

Table X.2 –Frame intervals of subsystems

|  |  |
| --- | --- |
| Subsystem | Frame interval |
| Signal enhancement | 15 ms (to meet SRW frame interval) |
| SRW | 1.25, 2.5, 3.75 ms (CVSD) for Narrow band  7.5, 15 ms (mSBC) for Wideband |
| Cell phone | 20 ms (Speech codec) |

An example of subsystems composing of an automotive hands-free send system is shown in Figure X.5. The upper boxes specify frame intervals and delays of each subsystem. The total send delay is calculated by summing all delays surrounded by red circles excepted for cell phone factors which are out of send delay specified by P.1100 or P.1110. According to Case 2 in clause X.4, buffer delay at input of SRW is omitted.

2 + 0.5 + 15 + 25 + 7.5 + 15? = 65 msec

Cell phone

Frame interval: 1 sample period

Delay: 0.5 ms

Frame interval: 15ms

Delay: 25 ms

Frame interval:7.5ms

Delay: 15? ms

Processor

MIC

Signal enhancement

SRW

Speech CODEC

Buffer delay: 15 ms

Buffer delay: 20 ms

Acoustic delay: 2 ms

MRP

Frame interval: 20ms

Delay: don’t care

Computational delay: 7.5 ms

Figure X.5: An example of automotive hands-free send system

In the same way, the subsystems composing of the receive system is shown in Figure X.6. The total receive delay is calculated by summing all delays surrounded by red circles excepted for cell phone factors. According to Case 3 in clause X.4, buffer delay at input of SRW is omitted.

15? + 15 +15 + 7.5 + 0.5 + 2 = 55 msec

Cell phone

Frame interval: 1 sample period

Delay: 0.5 ms

Frame interval: 15ms

Delay: 15 ms

Frame interval:7.5ms

Delay: 15? ms

Processor

Audio

Signal enhancement

SRW

Speech CODEC

Buffer delay: 7.5 ms

Computational delay: 7.5 ms

Acoustic delay: 2 ms

DRP

Frame interval: 20ms

Delay: don’t care

Buffer delay: 15 ms

Figure X.6: An example of automotive hands-free receive system

In this scenario, the round trip delay is equal to 120 msec, which meets P.1110.

The next examples are the typical cases that the signal enhancement subsystems of automotive hands-free send system and receive system are implemented without special care for delay or realized as an independant chip from SRW and having 16 msec frame interval. Since the interval is not simple multiple of SRW frame interval, those processes are implemented as asynchronous tasks. Figure X.7 shows the send system. The total delay of the send system is calculated as below. According to Case 4 in clause X.4, buffer delay at input of SRW is also added.

2 + 0.5 + 16 + 16 + 26 + 7.5 + 7.5 + 15? = 90.5 msec

Cell phone

Frame interval: 1 sample period

Delay: 0.5 ms

Frame interval: 16ms

Delay: 26 ms

Frame interval:7.5ms

Delay: 15? ms

Processor

MIC

Signal enhancement

SRW

Speech CODEC

Buffer delay: 16 ms

Buffer delay: 20 ms

Computational delay: 7.5 ms

Acoustic delay: 2 ms

MRP

Frame interval: 20ms

Delay: don’t care

Buffer delay: 7.5 ms

Computational delay: 16 ms

Figure X.7: A bad example of automotive hands-free send system

The receive system is shown in Figure X.8. The total receive delay is calculated as below. According to Case 4 in clause X.4, buffer delay at input of SRW is also added.

7.5 + 15? + 7.5 + 16 + 16 + 16 + 0.5 + 2 = 80.5 msec

Cell phone

Frame interval: 1 sample period

Delay: 0.5 ms

Frame interval: 16ms

Delay: 16 ms

Frame interval:7.5ms

Delay: 15? ms

Processor

Audio

Signal enhancement

SRW

Speech CODEC

Buffer delay: 7.5 ms

Computational delay: 16 ms

Acoustic delay: 2 ms

DRP

Frame interval: 20ms

Delay: don’t care

Buffer delay: 16 ms

Computational delay: 7.5 ms

Figure X.8: A bad example of automotive hands-free receive system

In this scenario, the round trip delay is equal to 171 msec, which cannot meet P.1110.

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