Joint ITU-T / IEEE Workshop on Next Generation Optical Access Systems

Overview of Mass-Market Silicon Development Economics

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The Questions?

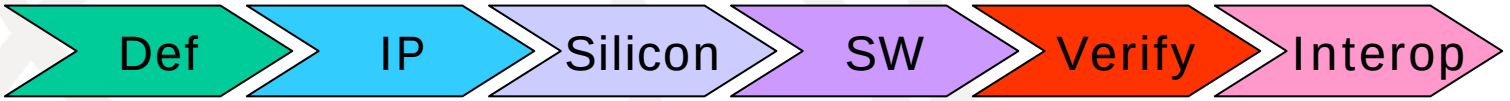
- What is the impact of supporting multiple standards?
- What does history tell us?
- Conclusions

Breakdown of Costs

- Product Development
  - Definition
  - IP development
  - Silicon Development
  - Software Development
  - Verification
  - Interoperability (is also an ongoing cost)
- Device
  - Die
  - Package
  - Final Assembly
- Other Factors
  - Ongoing Costs
  - Volume
  - Availability Vs Development Time
  - Customers Viewpoint

Product Development

- Lets consider two scenarios and calculate the overall impact to development cost
  - Develop two different devices
  - Develop a single chip to support two standards



% Total	5%	20%	25%	25%	5%	20%
2nd Device	90%	100%	100%	50%	100%	100%
2:1 Device	150%	120%	20%	50%	100%	100%

- Assume the cost of developing a single device is US$20M
- Second device is US$17.4 M, Total = US$37.4M
- Single chip with two standards US$34.8M

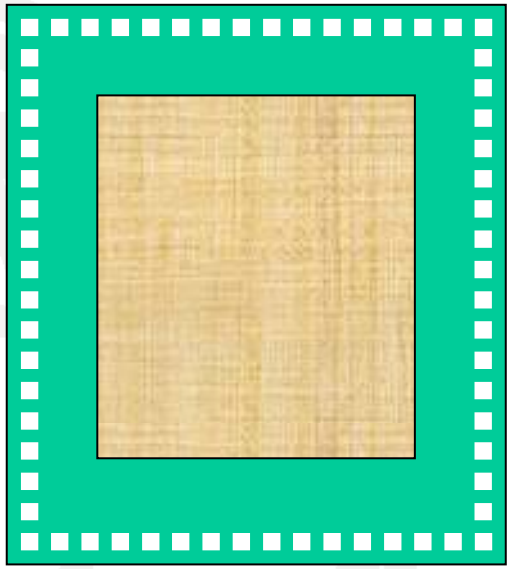
Taken from a sample of 10 similar TI SoC projects

Dual Standard Design Impact

- Multiple clocking schemes
- Multiplexed or reconfigured I/O
- Memory size
- Powering down unused blocks
- complex power supply
- Complex configuration registers
- Design compromises

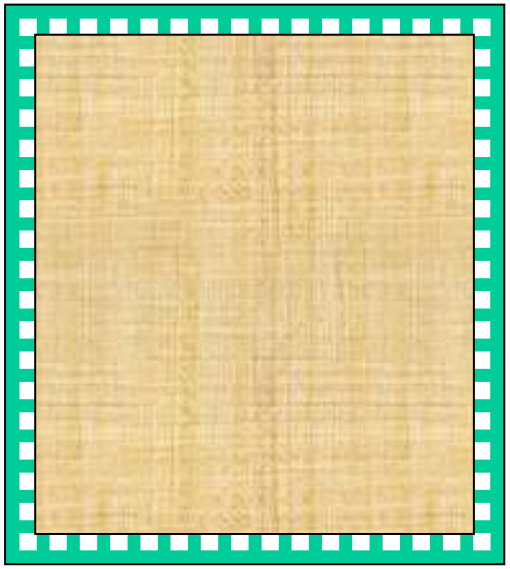
Device Cost - Die

- Die area of a device is driven by the number of gates and I/O
- With geometries shrinking to 45nm and added functionality increasing I/O, most devices are pad limited



Pad Limited – less silicon gates than pads

Not Pad Limited



Device Cost - Package

- The package cost is defined by many factors:
  - Application (operational, environment etc)
  - Power Dissipation
  - Die Size
  - Pin count
- Multiple standards effect all of these factors!

Device Cost – Final Assembly

- The final assembly costs are driven by several factors:
  - Yield
  - Wafer and Final Test
  - Packaging
- Supporting multiple standards will affect test times, mostly at final test which is a functional test of the device

Other Factors

- Ongoing Costs
  - Software Feature Support
  - Interoperability
- Availability Vs Development Time
  - Time to Revenue is longer for a single device with two standards than developing two single devices, whether in parallel or in series. (The penalty is device cost)
- Volume
  - There is a large penalty for sharing the volume (as much as 10%)

Impact Conclusion

- Multiple standards affect the price
  - Development cost
  - Device cost
  - Ongoing support costs
  - Willingness to pay for functionality not used
- Multiple standards affect availability
- Multiple standards affects the attractiveness of the market
  - Manufacturers and buyers sit on the fence, waiting for the winner
  - Competition needed to lower prices

What Does History Tell Us?

- There are winners and losers
  - ISDN encoding 2B1Q Vs 4B3T
  - Token Ring Vs Ethernet
  - VHS Vs Betamax
  - Blu-ray Vs HD
- General observations
  - It is hard to sell a dual standard device as no-one wants to pay for unused silicon for their application
  - Decisions are not necessarily based upon the best technology
    - Sometimes the buyers or end users end up making the decision based on marketing dollars spent
  - The volume market did not take off
    - Sometimes never or not until a winner was identified
  - When the decision was finally made the industry rallied around the chosen and there were only winners

Overall Conclusions

- There is a development and device cost to develop and maintain multiple standard silicon
- There is development cost and a volume impact to develop two different devices
- This deters competition
- History tells us that the turning point is when a single standard is adopted

Q&A

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