Electrical interfaces: Charting a course to the next generation

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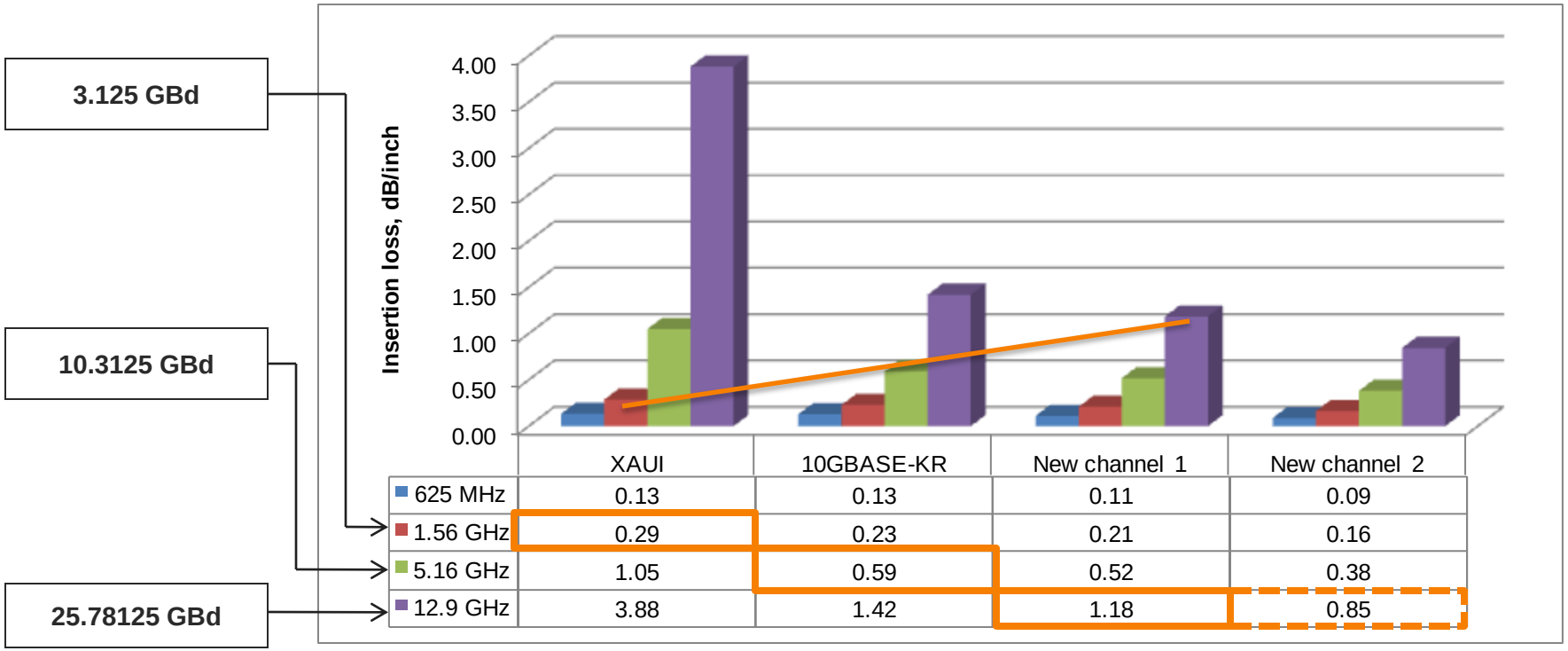
Landscape for electrical interfaces

- Industry convergence on next generation interfaces based on operation in the range of 25 to 28 Gb/s per lane
  - Ethernet – 100GBASE-LR4 (-ER4)
  - Fibre Channel – 32GFC
  - Infiniband – EDR
  - ITU-T – OTL4.4
- A variety of interface types
  - Chip-to-chip or chip-to-module
  - Board-to-board, backplane
  - Direct attach copper cable
- Different requirements for different interfaces and applications
  - e.g. interface reach, backwards compatibility
  - On-going efforts to drive commonality where appropriate

Headwinds for increasing speed: Channel performance



	XAUI	10GBASE-KR	New channel 1	New channel 2
625 MHz	0.13	0.13	0.11	0.09
1.56 GHz	0.29	0.23	0.21	0.16
5.16 GHz	1.05	0.59	0.52	0.38
12.9 GHz	3.88	1.42	1.18	0.85

- Channel insertion loss is roughly doubling for each new speed <u>despite</u> improvements in channel technology
- Thus for a fixed insertion loss budget the link distance is <u>halved</u>
  - Even “holding the line” on the budget presents challenges with increasing speeds
- Further improvements in channel performance may not be “mainstream”
  - Cost pressures are unrelenting

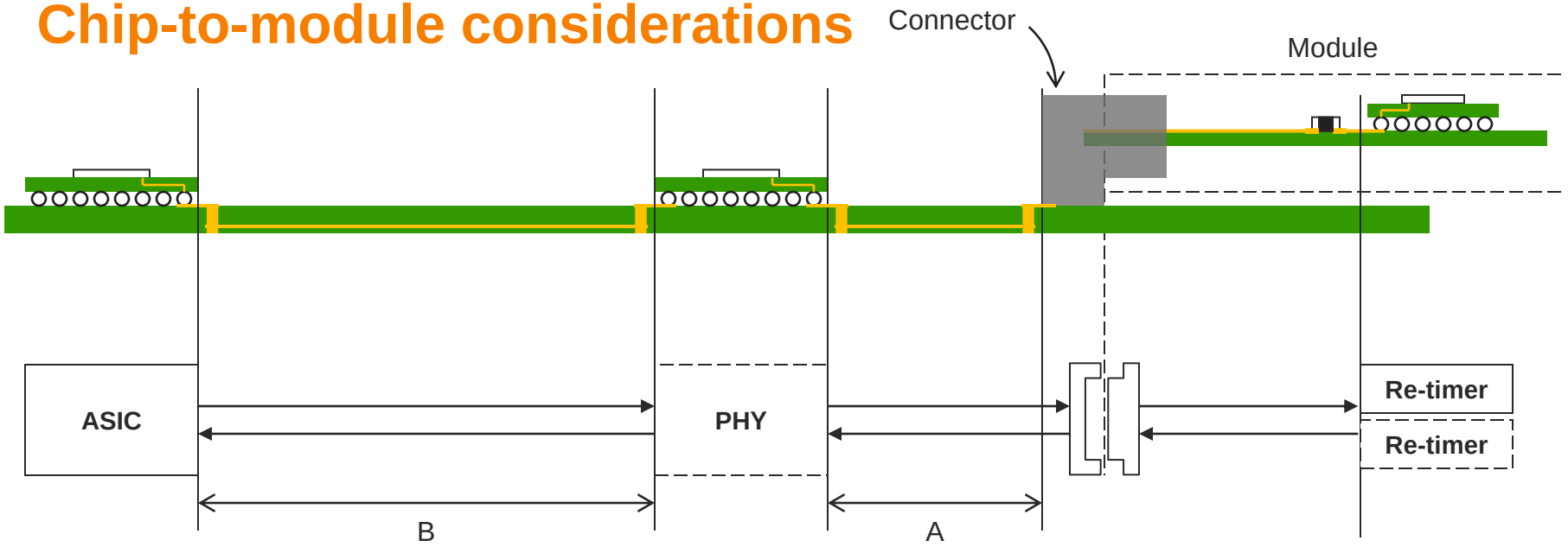
Modulation

Lessons learned from 10 Gb/s Ethernet operation over electrical backplanes…

Modulation	Symbol rate	Symbol distance	Equalization
NRZ	1	1	• Requires highest equalization gain
Duobinary	1	1/2	• Requires lower equalization gain due to 1+D target • Requires more precise equalization to compensate for reduced symbol distance
PAM-4	1/2	1/3	• Requires lower equalization gain due to reduced loss • Requires more precise equalization to compensate for reduced symbol distance • Higher jitter when symbol transitions are unconstrained

- For channels of interest at 10 Gb/s, NRZ yielded the largest absolute margins
  - Receiver assumed to be based on decision feedback equalizer technology
- Considering higher speeds, improving the modulation efficiency reduces the symbol rate and offers the potential to use more advanced signal processing
  - Operation at lower signal-to-noise ratios
- Total solution cost and application constraints must be considered (channel, power, area, latency)

Chip-to-module considerations



- Desire continuity of modulation between electrical and optical domains
- Embed a re-timer in the module transmit path
  - Transmitted jitter has an influence on optical reach
- Limitations of thermal management imply limits on the power dissipation of electronics embedded in the modules
  - Re-timer in the receive path may not available and the burden would be passed to PHY (or ASIC) receiver
- Chip to module reach may constrained to “A” by channel insertion loss and module architecture
- Extend reach to “A + B” using an intermediate PHY device

Looking ahead

Bit rate, Gb/s	Bit rate per lane, Gb/s	Number of lanes	Comments
100	10	10	Starting point for 100 Gb/s
100	25	4	
400	25	16	
400	40	10	Intersects with serial 40 Gb/s Ethernet
400	50	8	2 x 25 Gb/s
1000	50	20	

- Trends indicate that the distance supported by NRZ will continue to shrink with increasing speed
  - Assumes that the circuit implementation challenges can be met and the loss budget remains constant
- Intermediate re-timing circuitry and (or) very high performance channels may not yield the best total solution cost
- A paradigm shift may be required to enable these higher speed interfaces
  - The analysis performed for 10 Gb/s must be revisited for each new speed
  - New options should be considered

Closing thoughts

- There are strong incentives to minimize the number of lanes on the electrical interface
  - Considerable pressure to move from 10 x 10 Gb/s to 4 x 25 Gb/s
- Increasing the bit rate per lane presents multiple challenges at the system level
  - High speed circuit implementation, signal integrity, thermal management
  - Total solution cost relative to the application requirements
- Approaches to these challenges are currently being considered for 25 Gb/s
  - Partition the link into multiple segments using re-timers (chip-to-module)
  - Other solutions are yet to be explored
- These things take time
  - Building blocks for lower-cost higher-density 100 Gb/s Ethernet are just being developed
  - Also fundamental for the next Ethernet speed