International Telecommunication Union

ITU-R

Radiocommunication Sector of ITU

Recommendation ITU-R BT.1120-8
(01/2012)

Digital interfaces for HDTV studio signals

BT Series
Broadcasting service (television)

International Telecommunication Union

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Note: *This ITU-R Recommendation was approved in English under the procedure detailed in Resolution ITU-R 1.*

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RECOMMENDATION ITU-R BT.1120-8*

Digital interfaces for HDTV studio signals

(Question ITU-R 130/6)

(1994-1998-2000-2003-2004-2005-2007-2012)

Scope

This HDTV interface operates at two nominal clock frequencies, 1.485 GHz and 2.97 GHz, and conveys the uncompressed payload defined in Part 2 of Recommendation ITU-R BT.709. The interface may also be used for carrying packetized data.

The ITU Radiocommunication Assembly,

considering

a) that Recommendation ITU-R BT.709 provides the image format parameters and values for HDTV production and international programme exchange and contains the following HDTV studio standard to cover a wide range of applications:

– 1 125 total lines and 1 080 active lines;

– picture rates of 60[1], 50, 30[1], 25 and 24[1] Hz, including progressive, interlaced and segmented frame transport;

b) that a wide range of equipment based on the above systems has been developed and is commercially available;

c) that many programmes are being produced in the above systems using the above equipments and that in the development of broadcasting and other services there is an increasing need for HDTV production installations;

d) that serial digital interconnection has been developed to provide reliable transparent digital interconnections,

recommends

1 that the specifications described in this Recommendation should be used as bit-serial digital interfaces for HDTV studio signals;

2 that Note 1 is considered as part of the Recommendation.

NOTE 1 – Compliance with this Recommendation is voluntary. However, the Recommendation may contain certain mandatory provisions (e.g. to ensure interoperability or applicability) and compliance with the Recommendation is achieved when all of these mandatory provisions are met. The words “shall” or some other obligatory language such as “must” and the negative equivalents are used to express requirements.

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* Radiocommunication Study Group 6 made editorial amendments to this Recommendation in May 2012 in accordance with Resolution ITU-R 1.

[1] Frame rates of 60/1.001, 30/1.001 and 24/1.001 Hz are also included.

Annex 1

Interfaces for HDTV signals conforming to Recommendation ITU-R BT.709, Part 2[2]

This Annex specifies digital interfaces for the systems listed in Table 1. Digital coding parameters are listed in Table 2. For the 60, 30 and 24 Hz systems, picture rates having those values divided by 1.001 are also included. Parameter values for these systems are presented in parentheses.

TABLE 1

HDTV systems based on CIF

System	Capture (Hz)	Transport
60/P	60 progressive	Progressive
30/P	30 progressive	Progressive
30/PsF	30 progressive	Segmented frame
60/I	30 interlaced	Interlaced
50/P	50 progressive	Progressive
25/P	25 progressive	Progressive
25/PsF	25 progressive	Segmented frame
50/I	25 interlaced	Interlaced
24/P	24 progressive	Progressive
24/PsF	24 progressive	Segmented frame

1 Digital representation

1.1 Coding characteristics

The HDTV signals to be transported shall comply with the characteristics described in Recommendation ITU-R BT.709, Part 2.

2 Digital interface

The interface provides a unidirectional interconnection. The data signals are in the form of binary information and are coded accordingly:

– video data (10-bit words);

– timing reference and identification codes (10-bit words);

– ancillary data (see Recommendation ITU-R BT.1364).

When 8-bit video data are used, two LSBs of zeros are to be appended to the 8-bit words to form 10-bit words.

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[2] Legacy signals complying with Recommendation ITU-R BT.709, Part 1: See Appendix 3 to Annex 1.

2.1 Serial video data

Y, C_B and C_R signals are handled as 20-bit words by time-multiplexing C_B and C_R components. Each 20-bit word corresponds to a colour-difference sample and a luminance sample. The multiplex is organized as:

$$(C_{B0}\ Y_0)\,(C_{R0}\ Y_1)\,(C_{B1}\ Y_2)\,(C_{R1}\ Y_3)\ ...$$

where Y_i indicates the i-th active luminance sample of a line, while C_{Bj} and C_{Rj} indicate the j-th active colour-difference samples of C_B and C_R components. C_{Bj} and C_{Rj} samples are co-sited with the even numbered Y_i sample due to the half-rate sampling of the colour-difference signals.

The data words corresponding to digital levels $0_{(10)}$ through $3_{(10)}$ and 1 $020_{(10)}$ through 1 $023_{(10)}$ are reserved for data identification purposes and must not appear as video data.

R, G, B signals are handled as 30-bit words in addition to the above 20-bit words for Y, C_B, C_R signals.

TABLE 2

Digital coding parameters

Item	**Parameter**	**System**									
		60/P	**30/P**	**30/PsF**	**60/I**	**50/P**	**25/P**	**25/PsF**	**50/I**	**24/P**	**24/PsF**
1	Coded signals Y, C_B, C_R or R, G, B	These signals are obtained from gamma pre-corrected signals, namely E'_Y, E'_{C_B}, E'_{C_R} or E'_R, E'_G, E'_B. Also see Recommendation ITU-R BT.709, Part 2									
2	Sampling lattice – R, G, B, Y	Orthogonal, line and picture repetitive									
3	Sampling lattice – C_B, C_R	Orthogonal, line and picture repetitive, co-sited with each other and with alternate(1) Y samples									
4	Number of active lines	1 080									
5	Sampling frequency(2) (MHz) – R, G, B, Y – C_B, C_R(3)	148.5 (148.5/1.001) 74.25 (74.25/1.001)	74.25 (74.25/1.001) 37.125 (37.125/1.001)			148.5 74.25	74.25 37.125			74.25 (74.25/1.001) 37.125 (37.125/1.001)	
6	Number of samples/line – R, G, B, Y – C_B, C_R	2 200 1 100				2 640 1 320				2 750 1 375	
7	Number of active samples/line – R, G, B, Y – C_B, C_R	1 920 960									
8	Position of the first active Y, C_B, C_R sampling instants with respect to the analogue sync timing reference O_H(4) (see Fig. 1)	192 T									

TABLE 2 (*end*)

Item	Parameter	System									
		60/P	30/P	30/PsF	60/I	50/P	25/P	25/PsF	50/I	24/P	24/PsF
9	Coding format	Uniformly quantized PCM for each of the video component signals 8- or 10-bit/sample									
10	Quantization level assignment [5] – Video data – Timing reference	 $1_{(8)}$ through $254_{(8)}$ or $4_{(10)}$ through 1 $019_{(10)}$ $0_{(8)}$ and $255_{(8)}$ or $0_{(10)}$ thru $3_{(10)}$ and 1 020 $_{(10)}$ thru1 $023_{(10)}$									
11	Quantization levels [6] – Black level *R*, *G*, *B*, *Y* – Achromatic level C_B, C_R – Nominal peak – *R*, *G*, *B*, *Y* – C_B, C_R	 $16_{(8)}$ or $64_{(10)}$ $128_{(8)}$ or $512_{(10)}$ $235_{(8)}$ or $940_{(10)}$ $16_{(8)}$ and $240_{(8)}$ or $64_{(10)}$ and $960_{(10)}$									
12	Filter characteristics	See Recommendation ITU-R BT.709									

(1) The first active colour-difference samples are co-sited with the first active Y sample.

(2) The sampling clock must be locked to the line frequency. The tolerance on frequency is ±0.001%.

(3) CB, CR sampling frequency is half of luminance sampling frequency.

(4) T denotes the duration of the luminance sampling clock or the reciprocal of the luminance sampling frequency.

(5) When 8-bit words are treated in 10-bit system, two LSBs of zeros are to be appended to the 8-bit words.

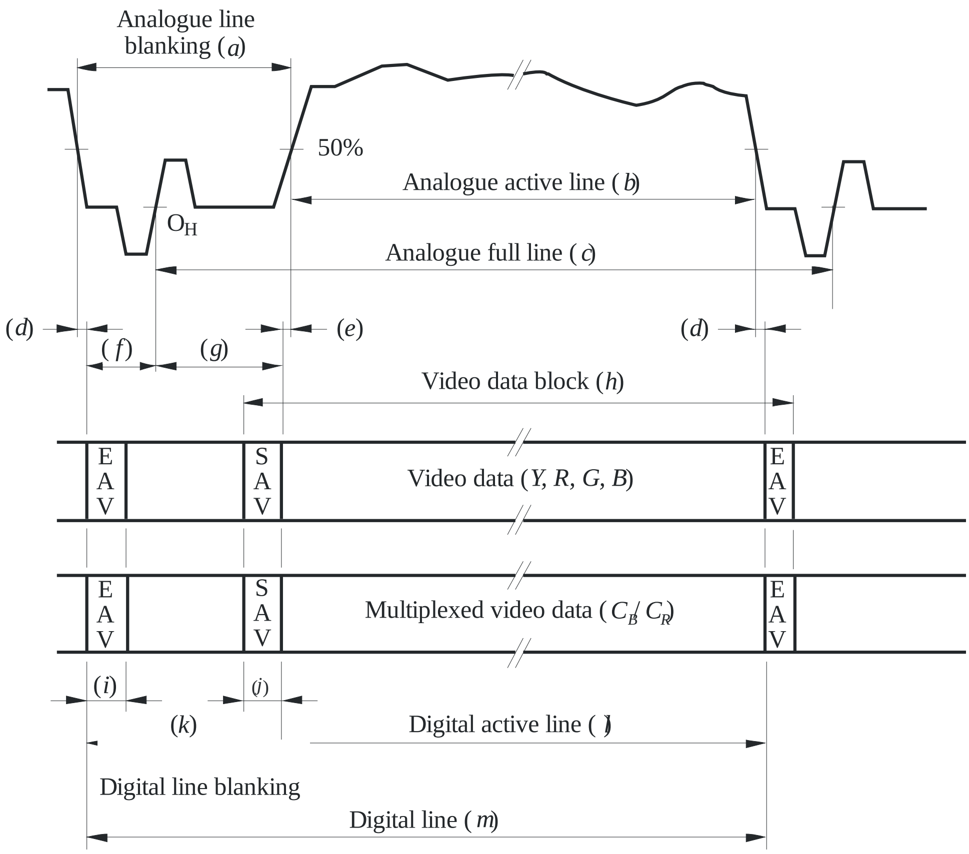
(6) These levels refer to precise nominal video levels. Signal processing may occasionally cause the signal level to deviate outside these ranges.

2.2 Video timing relationship with analogue waveform

The digital line occupies m clock periods. It begins at *f* clock periods prior to the reference transition (O_H) of the analogue synchronizing signal in the corresponding line. The digital active line begins at *g* clock periods after the reference transition (O_H). The values for *m*, *f* and *g* are listed in Table 3. See Fig. 1 and Table 3 for detailed timing relationships in the line interval.

FIGURE 1

Data format and timing relationship to analogue waveform



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For interlaced and segmented frame systems, the start of digital field/segment is fixed by the position specified for the start of the digital line. See Fig. 2a) and Table 4a) for detailed relationships in the field/segment interval.

For progressive systems, the start of the digital frame is fixed by the position specified for the start of the digital line. See Fig. 2b) and Table 4b) for detailed relationships in the frame interval.

2.3 Video timing reference codes SAV and EAV

There are two timing reference codes, one at the beginning of each video data block SAV and the other at the end of each video data block EAV. These codes are contiguous with the video data, and continue during the field/frame/segment blanking interval, as shown in Fig. 2.

TABLE 3

Line interval timing specifications

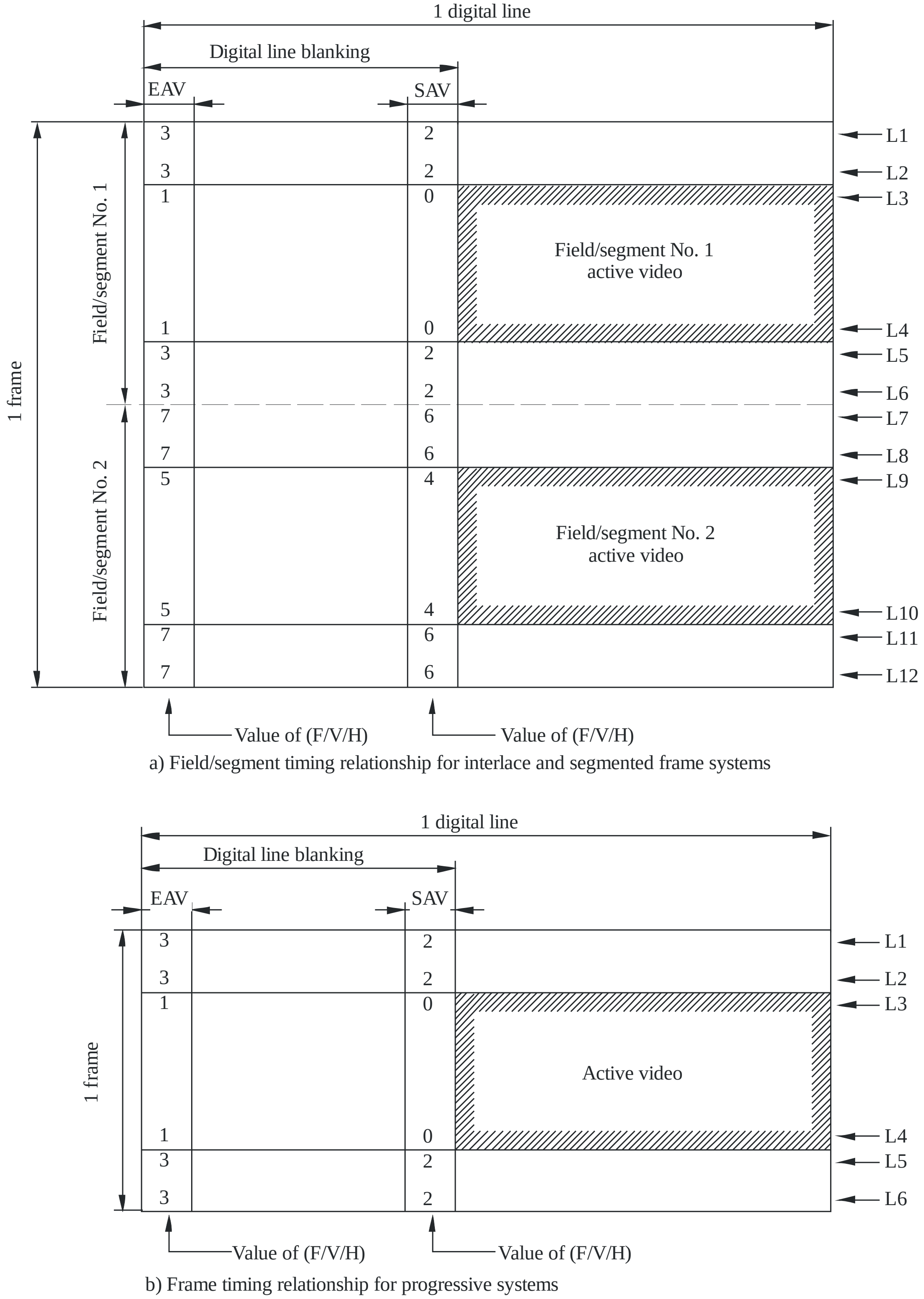
Symbol	Parameter	Value									
		60/P	**30/P**	**30/PsF**	**60/I**	**50/P**	**25/P**	**25/PsF**	**50/I**	**24/P**	**24/PsF**
	Number of active *Y* samples per line	1920									
	Luminance sampling frequency (MHz)	148.5 (148.5/ 1.001)	74.25 (74.25/1.001)			148.5	74.25			74.25 (74.25/1.001)	
a	Analogue line blanking (*T*)	+12 280 –0				+12 280 –0				+12 280 –0	
b	Analogue active line (*T*)	+0 1 920 –12									
c	Analogue full line (*T*)	2 200				2 640				2 750	
d	Duration between end of analogue active video and start of EAV (*T*)	0-6									
e	Duration between end of SAV and start of analogue active video (*T*)	0-6									
f	Duration between start of EAV and analogue timing reference O_H (*T*)	88				528				638	
g	Duration between analogue timing reference O_H and end of SAV (*T*)	192									
h	Video data block (*T*)	1 928									
i	Duration of EAV (*T*)	4									
j	Duration of SAV (*T*)	4									
k	Digital line blanking (*T*)	280				720				830	
l	Digital active line (*T*)	1 920									
m	Digital line (*T*)	2 200				2 640				2 750	

NOTE 1 – The parameter values for analogue specifications expressed by the symbols *a*, *b* and *c* indicate the nominal values.

NOTE 2 – T denotes the duration of the luminance clock or the reciprocal of the luminance sampling frequency.

FIGURE 2

Video timing reference codes SAV and EAV



Note 1 – The values of (F/V/H) for EAV and SAV represent the status of bits for F, V, and H; in a way that the three-bit word composed of F, V, H represents a binary number expressed in decimal notation (F corresponding to MSB and H to LSB). For example, the value 3 represents the bits of F = 0, V = 1 and H = 1.

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Each code consists of a four-word sequence. The bit assignment of the word is given in Table 5. The first three words are fixed preamble and the fourth word carries the information that defines field identification (F), field/frame blanking period (V), and line blanking period (H). In an 8-bit implementation bits Nos. 9 to 2 inclusive are used.

The bits F and V change state synchronously with EAV at the beginning of the digital line.

The value of protection bits, P_0 to P_3, depends on the F, V and H as shown in Table 6. The arrangement permits one-bit errors to be corrected and two-bit errors to be detected at the receiver, but only in the 8 MSBs, as shown in Table 7.

TABLE 4

a) Field/segment interval timing specifications for interlaced and segmented frame systems

Symbol	Definition	Interface digital line number
	Number of active lines	1 080
L1	First line of field/segment No. 1	1
L2	Last line of digital field/segment blanking No. 1	20
L3	First line of field/segment No. 1 active video	21
L4	Last line of field/segment No. 1 active video	560
L5	First line of digital field/segment blanking No. 2	561
L6	Last line of field/segment No. 1	563
L7	First line of field/segment No. 2	564
L8	Last line of digital field/segment blanking No. 2	583
L9	First line of field/segment No. 2 active video	584
L10	Last line of field/segment No. 2 active video	1 123
L11	First line of digital field/segment blanking No. 1	1 124
L12	Last line of field/segment No. 2	1 125

NOTE 1 – Digital field/segment blanking No. 1 denotes the field/segment blanking period that is prior to the active video of field/segment No. 1, and digital field/segment blanking No. 2 denotes that prior to the active video of field/segment No. 2.

b) Frame interval timing specifications for progressive systems

Symbol	Definition	Interface digital line number
	Number of active lines	1 080
L1	First line of frame	1
L2	Last line of digital frame blanking	41
L3	First line of active video	42
L4	Last line of active video	1 121
L5	First line of digital frame blanking	1 122
L6	Last line of frame	1 125

TABLE 5

Bit assignment for video timing reference codes

Word	**Bit number**									
	9 (MSB)	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0 (LSB)**
First	1	1	1	1	1	1	1	1	1	1
Second	0	0	0	0	0	0	0	0	0	0
Third	0	0	0	0	0	0	0	0	0	0
Fourth	1	F	V	H	P_3	P_2	P_1	P_0	0	0
Interlaced and segmented frame system		F = 1 during field/segment No. 2 = 0 during field/segment No. 1		V= 1 during field/segment blanking = 0 elsewhere					H= 1 in EAV = 0 in SAV	
Progressive system		F = 0		V = 1 during frame blanking = 0 elsewhere					H= 1 in EAV = 0 in SAV	

NOTE 1 – P_0, P_1, P_2, P_3 in the fourth word are the protection bits (see Table 6).

TABLE 6

Protection bits for SAV and EAV

	SAV/EAV bit status			**Protection bits**					
Bit 9 (fixed)	**8 (F)**	**7 (V)**	**6 (H)**	**5 (P_3)**	**4 (P_2)**	**3 (P_1)**	**2 (P_0)**	**1 (fixed)**	**0 (fixed)**
1	0	0	0	0	0	0	0	0	0
1	0	0	1	1	1	0	1	0	0
1	0	1	0	1	0	1	1	0	0
1	0	1	1	0	1	1	0	0	0
1	1	0	0	0	1	1	1	0	0
1	1	0	1	1	0	1	0	0	0
1	1	1	0	1	1	0	0	0	0
1	1	1	1	0	0	0	1	0	0

TABLE 7

Error corrections using protection bits (P_3-P_0)

Received bits 5-2 for P_3-P_0	Received bits 8-6 for F, V and H							
	000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
0000	000	000	000	–	000	–	–	111
0001	000	–	–	111	–	111	111	111
0010	000	–	–	011	–	101	–	–
0011	–	–	010	–	100	–	–	111
0100	000	–	–	011	–	–	110	–
0101	–	001	–	–	100	–	–	111
0110	–	011	011	011	100	–	–	011
0111	100	–	–	011	100	100	100	–
1000	000	–	–	–	–	101	110	–
1001	–	001	010	–	–	–	–	111
1010	–	101	010	–	101	101	–	101
1011	010	–	010	010	–	101	010	–
1100	–	001	110	–	110	–	110	110
1101	001	001	–	001	–	001	110	–
1110	–	–	–	011	–	101	110	–
1111	–	001	010	–	100	–	–	–

NOTE 1 – The error correction applied provides a DEDSEC (double error detection – single error correction) function. The received bits denoted by "–" in the table, if detected, indicate that an error has occurred but cannot be corrected.

2.4 Ancillary data

Ancillary data may optionally be included in the blanking intervals of a digital interface according to this Recommendation. The ancillary signals shall comply with the general rules of Recommendation ITU-R BT.1364.

The horizontal blanking interval between the end of the error detection code words and the start of SAV may be employed to convey ancillary data packets.

Ancillary data packets may be conveyed in the vertical blanking interval between the end of SAV and the start of EAV as follows:

– in a progressive system during lines 1 through 41 inclusive, and 1 122 through 1 125 inclusive;

– in an interlaced system during lines 1 through 20 inclusive, and lines 561 through 583 inclusive, and 1 124, 1 125 inclusive;

– on any line that is outside the vertical extent of the picture as noted above and that is not employed to convey vertical blanking interval signals that can be represented in the analogue domain through direct (D/A) conversion;

– ancillary data packets should not be placed in the area which may be affected by switching as defined in Table 2, Appendix 3 to Annex 1, Recommendation ITU-R BT.1364.

2.5 Data words during blanking

The data words occurring during digital blanking intervals that are not used for the timing reference codes (SAV and EAV), line number data, the error detection codes or ancillary data (ANC) are filled with words corresponding to the following blanking levels, appropriately placed in the multiplexed data:

$64_{(10)}$ for *Y*, *R*, *G*, *B* signals

$512_{(10)}$ for C_B,C_R (time-multiplexed colour-difference signal).

3 Bit-parallel interface

The bit-parallel interface defined in previous versions of this Recommendation is no longer in use and its use is deprecated.

4 Bit-serial interface

4.1 Data format

The bit-serial data consists of video data, video timing reference codes, line number data, error detection codes, ancillary data and blanking data. Each data has a word-length of 10 bits, and is represented as parallel data before serialization. Two parallel streams (i.e. luminance data *Y* and colour-difference data C_B/C_R) are multiplexed and serialized in accordance with § 4.2.

4.1.1 Video data

The video data shall be 10-bit words representing *Y*, C_B/C_R of the video systems defined in § 1.

4.1.2 Video timing reference codes

The video timing reference codes, SAV and EAV shall have the same format as that defined in § 2.

4.1.3 Interface line number data

The line number data is composed of two words indicating the line number. The bit assignment of the line number data is shown in Table 8. The line number data shall be located immediately after EAV.

TABLE 8

Bit assignment of the line number data

Word	**b9 (MSB)**	**b8**	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0 (LSB)**
LN0	Not b8	L6	L5	L4	L3	L2	L1	L0	R	R
LN1	Not b8	R	R	R	L10	L9	L8	L7	R	R

L0 (LSB)-L10 (MSB): line number in binary code.

R: reserved (set to zero).

4.1.4 Error detection codes

The error detection codes, cyclic redundancy check codes (CRCC), which are used to detect errors in active digital line, EAV and line number data, consist of two words and are determined by the following polynomial generator equation:

$$EDC(x) = x^{18} + x^5 + x^4 + 1$$

Initial value of the codes is set to zero. The calculation starts at the first word of the digital active line and ends at the final word of the line number data. Two error detection codes are calculated, one for luminance data (YCR) and one for colour-difference data (CCR). The bit assignment of the error detection codes is shown in Table 9. The error detection codes shall be located immediately after the line number data.

TABLE 9

Bit assignment for error detection codes

Word	**b9 (MSB)**	**b8**	**b7**	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0 (LSB)**
YCR0	Not b8	CRC8	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0
YCR1	Not b8	CRC17	CRC16	CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9
CCR0	Not b8	CRC8	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0
CCR1	Not b8	CRC17	CRC16	CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9

NOTE 1 – CRC0 is the MSB of error detection codes.

4.1.5 Ancillary data

The ancillary data shall have the same rules as that defined in § 2.4.

4.1.6 Blanking data

The blanking data words during digital blanking intervals that are not used for SAV, EAV, the line number data, the error detection codes and the ancillary data, shall be filled with the 10-bit words as defined in § 2.5.

4.2 Transmission format

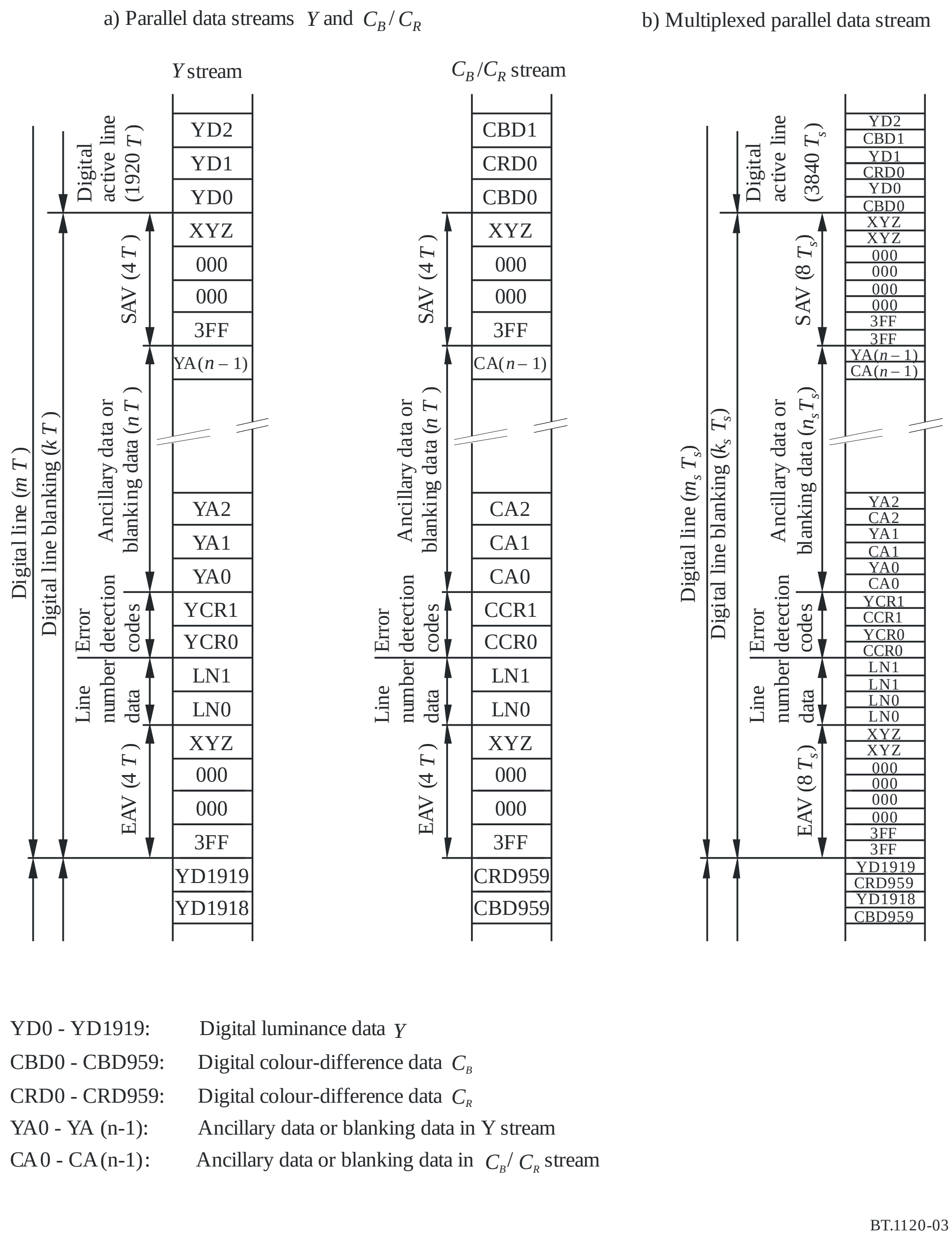
The two parallel data streams are transmitted over a single channel in bit-serial form after word-multiplexing, parallel-to-serial conversion and scrambling.

4.2.1 Word-multiplexing

The two parallel streams shall be multiplexed word by word into a single 10-bit parallel stream in the order of C_B, Y, C_R, Y, C_B, Y, C_R, Y ... (See Fig. 3 and Table 11).

FIGURE 3

Data stream mapping



In the case of 50/P or 60/P, an alternate format is also available. See § 4.5 and § 4.6.

4.2.2 Serializing

The LSB of each 10-bit word in the word-multiplexed parallel stream shall be transmitted first in the bit-serial format.

4.2.3 Channel coding

The channel coding scheme shall be scrambled NRZ inverted (NRZI). The serialized bit stream shall be scrambled using the following generator polynomial equation:

$$G(x) = (x^9 + x^4 + 1)\ (x + 1)$$

The input signal to the scrambler shall be positive logic. (The highest voltage represents data 1 and the lowest voltage represents data 0.)

4.2.4 Serial clock

TABLE 10

Serial clock frequency values

Parameter	Value									
	60/P	**30/P**	**30/PsF**	**60/I**	**50/P**	**25/P**	**25/PsF**	**50/I**	**24/P**	**24/PsF**
Serial clock frequency (GHz)	1.485 for dual-link operation 2.97 for single-link operation (2.97/1.001)	1.485 (1.485/1.001)			1.485 for dual-link operation 2.97 for single-link operation	1.485			1.485 (1.485/1.001)	

TABLE 11

Data stream timing specifications (see Fig. 3)

Symbol	Parameter	Value									
		60/P	**30/P**	**30/PsF**	**60/I**	**50/P**	**25/P**	**25/PsF**	**50/I**	**24/P**	**24/PsF**
T	Parallel clock period (ns)	1 000/148.5 (1 001/148.5)	1 000/74.25 (1 001/74.25)			1 000/148.5	1 000/74.25			1 000/74.25 (1 001/74.25)	
T_s	Multiplexed parallel data clock period	T/2									
m	Digital line in parallel data stream	2 200				2 640				2 750	
k	Digital line blanking in parallel data stream	280				720				830	
n	Ancillary data or blanking data in parallel data stream	268				708				818	
m_s	Digital line in multiplexed parallel data stream	4 400				5 280				5 500	
k_s	Digital line blanking in multiplexed parallel data stream	560				1 440				1 660	
n_s	Ancillary data or blanking data in multiplexed parallel data stream	536				1 416				1 636	

4.2.5 Bit-serial digital check field

Digital test signals suitable for testing cable equalization and phase locked loop (PLL) lock-in are described in Annex 2.

4.2.6 Payload identifier

A payload identifier is optional for a single 1.5 Gbit/s interface and mandatory for a single 3 Gbit/s interface and dual-link 1.5 Gbit/s interface, and when present should be inserted into the horizontal ancillary data space of the Y channel. The reserved values shall be set to 0 unless otherwise specified.

This payload identifier shall be in conformance with the payload identifier data format defined in Recommendation ITU-R BT.1614. The 4-byte payload identifier when present shall be mapped into the horizontal blanking area of the interface immediately following an EAV-LN-CRC word sequence.

For digital interfaces having 1 125 lines with interlaced (I) and progressive segmented-frame (PsF) scanning structures, the ancillary data packet shall be added once per field on the Y-channel. The recommended location of the ancillary data packet, if ancillary data space is available, shall be on the following lines:

1 125I (field 1): Line 10

1 125I (field 2): Line 572.

These line numbers also apply to dual-link HD-SDI when using interlaced and progressive segmented-frame scanning.

For digital interfaces having 1 125 lines with a progressive (P) scanning structure, the ancillary data packet shall be added once per frame on the Y-channel. The recommended location of the ancillary data packet, if ancillary data space is available, shall be on the following line:

1 125P: Line 10.

TABLE 12A

Payload identifier definitions for 1 080-line payloads on a 1.5 Gbit/s (nominal) serial digital interface

	Byte 1	Byte 2	Byte 3	Byte 4
Bit 7	1	Interlaced (0) or progressive (1) transport	Reserved	Reserved
Bit 6	0	Interlaced (0) or progressive (1) picture	Horizontal pixel count 1 920 (0) reserved (1)	Reserved
Bit 5	0	Reserved	Aspect ratio 16:9 (1), unknown (0)	Reserved
Bit 4	0	Reserved	Reserved	Reserved
Bit 3	0	Picture rates 25 Hz (5h), 24/1.001 Hz (2h), 30/1.001 Hz (6h), 24Hz (3h)	Sampling structure 4:2:2 Y,C_B,C_R (0h)	Reserved
Bit 2	1			Reserved
Bit 1	0			Reserved
Bit 0	1			Bit depth 8-bit (0) or 10-bit (1)

TABLE 12B

Payload identifier definitions for 1 080-line payloads on a 3Gbit/s[3] (nominal) serial digital interface

<table>
<tr><th></th><th>Byte 1</th><th>Byte 2</th><th>Byte 3</th><th>Byte 4</th></tr>
<tr><td>Bit 7</td><td>1</td><td>Interlaced (0) or progressive (1) transport</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>Bit 6</td><td>0</td><td>Interlaced (0) or progressive (1) picture</td><td>Horizontal pixel count
1 920 (0) reserved (1)</td><td>Reserved</td></tr>
<tr><td>Bit 5</td><td>0</td><td>Reserved</td><td>Aspect ratio
16:9 (1), unknown (0)</td><td>Reserved</td></tr>
<tr><td>Bit 4</td><td>0</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>Bit 3</td><td>1</td><td rowspan="4">Picture rates
50 Hz (9h), 60/1.001 Hz (Ah), 60Hz (Bh)</td><td rowspan="4">Sampling structure
4:2:2 Y,C_B,C_R (0h)</td><td>Reserved</td></tr>
<tr><td>Bit 2</td><td>0</td><td>Reserved</td></tr>
<tr><td>Bit 1</td><td>0</td><td>Reserved</td></tr>
<tr><td>Bit 0</td><td>1</td><td>Bit depth
8-bit (0) or 10-bit (1)</td></tr>
</table>

Byte 1 Shall have a value of (85h) for 1.5 Gbit/s

Byte 2 Shall have a value of (89h) for 3 Gbit/s

The second byte shall be used to identify the picture rate and the picture and transport structure.

Bit b7 shall be used to identify whether the digital interface uses a progressive or interlaced transport structure such that:

b7 =(0) identifies an interlaced transport

b7 = (1) identifies a progressive transport.

Bit b6 shall be used to identify whether the picture has a progressive or interlaced structure such that:

b6 = (0) identifies an interlaced structure

b6 = (1) identifies a progressive structure.

NOTE – PsF video payloads are identified by a progressive picture transported over an interlaced digital interface. The transport carrying the progressive video payload as a first and second picture segment within the transport frame duration. These first and second picture segments are indicated by the first and second field indicators in the digital interface transport.

Bits b5 to b4 shall be set to (0).

Bits b3 to b0 shall be used to identify the picture rate in Hz and shall be restricted to the frame rates defined in Recommendation ITU-R BT.709 Part 2.

(2h) identifies 24/1.001 frames/sec

(3h) identifies 24 frames/sec

(5h) identifies 25 frame/sec

(6h) identifies 30/1.001 frames/sec

(9h) identifies 50 frames/sec

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[3] 3Gbit/s is typical terminology actual rate is 2.97Gb/s and 2.97/1.001 Gbit/s.

(Ah) identifies 60/1.001 frames/sec

(Bh) identifies 60 frames/sec

(7h) identifies 30 frame/sec.

Byte 3

The third byte shall be used to identify the aspect ratio and sampling structure of the video payload.

Bit b6 shall be used to identify horizontal pixel count:

(0) 1 920 pixels

(1) reserved.

Bit b5 shall be used to identify the image aspect ratio:

(0) aspect ratio unknown

(1) 16:9 image.

Bits b3 to b0 of byte 3 shall be used to identify the horizontal sampling structure. This Recommendation is constrained to value (0h); Bits b7 and b4 shall be reserved and set to (0).

Byte 4

Bits b7 to b1 are reserved and set to (0).

Bit b0 shall be used to identify the bit depth.

(0) identifies 8 bits per sample

(1) identifies 10 bits per sample.

4.3 Coaxial cable interfaces

The coaxial cable interfaces consist of one source and one destination in a point-to-point connection. The coaxial cable interfaces specify the characteristics of line driver (source), line receiver (destination), transmission line and connectors.

4.3.1 Line driver characteristics (source)

Table 13 specifies the line driver characteristics. The line driver shall have an unbalanced output circuit.

TABLE 13

Line driver characteristics

Item	Parameter	Value	
		1.485 Gbit/s	2.97 Gbit/s
1	Output impedance	75 Ω nominal	
2	DC offset(1)	0.0 V ± 0.5 V	
3	Signal amplitude(2)	800 mV_{p-p} ± 10%	
4	Return loss	≥ 15 dB(3), ≥ 10 dB(4)	
5	Rise and fall times(5)	< 270 ps (20% to 80%)	< 135 ps (20% to 80%)
6	Difference between rise and fall time	≤ 100 ps	≤ 50 ps

TABLE 13 (*end*)

Item	Parameter	Value	
		1.485 Gbit/s	2.97 Gbit/s
7	Output jitter(6)	f_1 = 10 Hz f_3 = 100 kHz f_4 = 1/10 of the clock rate $A1$ = 1 UI (UI: unit interval) $A2$ = 0.2 UI	f_1 = 10 Hz f_3 = 100 kHz f_4 = 1/10 of the clock rate $A1$ = 2 UI $A2$ = 0.3 UI

(1) Defined by mid-amplitude point of the signal.

(2) Measured across a 75 Ω resistive load connected through a 1 m coaxial cable.

(3) In the frequency range of 5 MHz to fc/2. (fc: serial clock frequency)

(4) In the frequency range of fc/2 to fc.

(5) Determined between the 20% and 80% amplitude points and measured across a 75 Ω resistive load. Overshoot of the rising and falling edges of the waveform shall not exceed 10% of the amplitude.

(6) 1 UI corresponds to 1/fc. Specification of jitter and jitter measurements methods shall comply with Recommendation ITU-R BT.1363 – Jitter specifications and methods for jitter measurement of bit-serial signals conforming to Recommendations ITU-R BT.656, ITU-R BT.799 and ITU-R BT.1120.

Output amplitude excursions due to signals with a significant dc component occurring for a horizontal line (pathological signals) shall not exceed 50 mV above or below the average peak-peak signal envelope. (In effect, this specification defines a minimum output coupling time constant.)

4.3.2 Line receiver characteristics (destination)

Table 14 specifies the line receiver characteristics. The line receiver shall have an unbalanced input circuit. It must sense correctly the received data when connected to a line driver operating at the extreme voltage limits permitted by § 4.3.1, and when connected through a cable having the worst condition permitted by § 4.3.3.

TABLE 14

Line receiver characteristics

Item	Parameter	Value	
1	Input impedance	75 Ω nominal	
2	Return loss	≥ 15 dB(1), ≥ 10 dB(2)	
3	Interfering signal(3)	±2.5 V_{max}	DC
		< 2.5 V_{p-p}	Below 5 kHz
		< 100 mV_{p-p}	5 kHz to 27 MHz
		< 40 mV_{p-p}	Above 27 MHz

(1) In the frequency range of 5 MHz to fc/2.

(2) In the frequency range of fc/2 to fc.

(3) The values are shown as a guideline.

4.3.3 Transmission line characteristics

Relevant specifications are given in Table 15.

TABLE 15

Transmission line characteristics

Item	Parameter	Value	
1	Transmission loss[(1)]	≤ 20 dB at 1/2 clock frequency	
2	Return loss	≥ 15 dB[(2)], ≥ 10 dB[(3)]	
3	Impedance	75 Ω nominal	

(1) Loss characteristics of $\sqrt{f}$.

(2) In the frequency range of 5 MHz to fc/2.

(3) In the frequency range of fc/2 to fc.

4.3.4 Connector

The male and female connectors shall be 75-ohm BNC, as defined in IEC 61169-8, Part 8, Annex A.

4.4 Optical fibre interfaces

Optical interfaces shall use single mode optical interfaces only and should comply with general rules of Recommendation ITU-R BT.1367 – Serial digital fibre transmission system for signals conforming to Recommendations ITU-R BT.656, ITU-R BT.799 and ITU-R BT.1120.

To make use of this Recommendation the following specifications are necessary.

Item	Parameter	Value	
		1.485 Gbit/s	**2.97 Gbit/s**
1	Rise and fall times	< 270 ps (20% to 80%)	< 135 ps (20% to 80%)
2	Output jitter[(1)]	f_1 = 10 Hz f_3 = 100 kHz f_4 = 1/10 of the clock rate $A1$ = 1 UI (UI: unit interval) $A2$ = 0.2 UI	f_1 = 10 Hz f_3 = 100 kHz f_4 = 1/10 of the clock rate $A1$ = 2 UI $A2$ = 0.3 UI

(1) Specification of jitter and jitter measurement methods shall comply with Recommendation ITU-R BT.1363. Input jitter is measured with a short cable (2 m).

4.5 Bit-serial interface for 60/P and 50/P dual-link operation

The interface consists of two unidirectional interconnections between one device and another. The interconnections carry the data corresponding to the high definition television signal and associated data. The two interconnections are referred to as link A and link B. The term “link” is intended to define a serial bit stream formatted according to the specification in § 4. The total data rate of the dual-link interface is 2.970 Gbit/s or 2.970/1.001 Gbit/s.

4.5.1 Source sample numbering

Each line of the *Y* component consists of 2 640 (50/P) or 2 200 (60/P) total samples, and each line of C_B and C_R components consists of 1 320 (50/P) or 1 100 (60/P) total samples, as shown in Table 2. The samples are designated 0-2 639 or 0-2 199 for *Y* component and 0-1 319 or 0-1 099 for C_B and C_R components, and the individual samples are designated by suffixes such as sample *Y*135 or sample C_B429.

4.5.2 Interface data streams and multiplex structure

The picture data is divided into two data streams conveyed through link A and link B. The serial data stream of one link contains two channels, first channel (*Y* channel) and second channel (C_B/C_R channel). Data is mapped into these channels. The term “channel” is intended to define how the first and second channels of the link are utilized.

Mapping of the data created by the 4:2:2 picture sampling structure is shown in Figs 4 and 5. Each line of the source picture is alternately mapped between link A and link B of the dual-link interface.

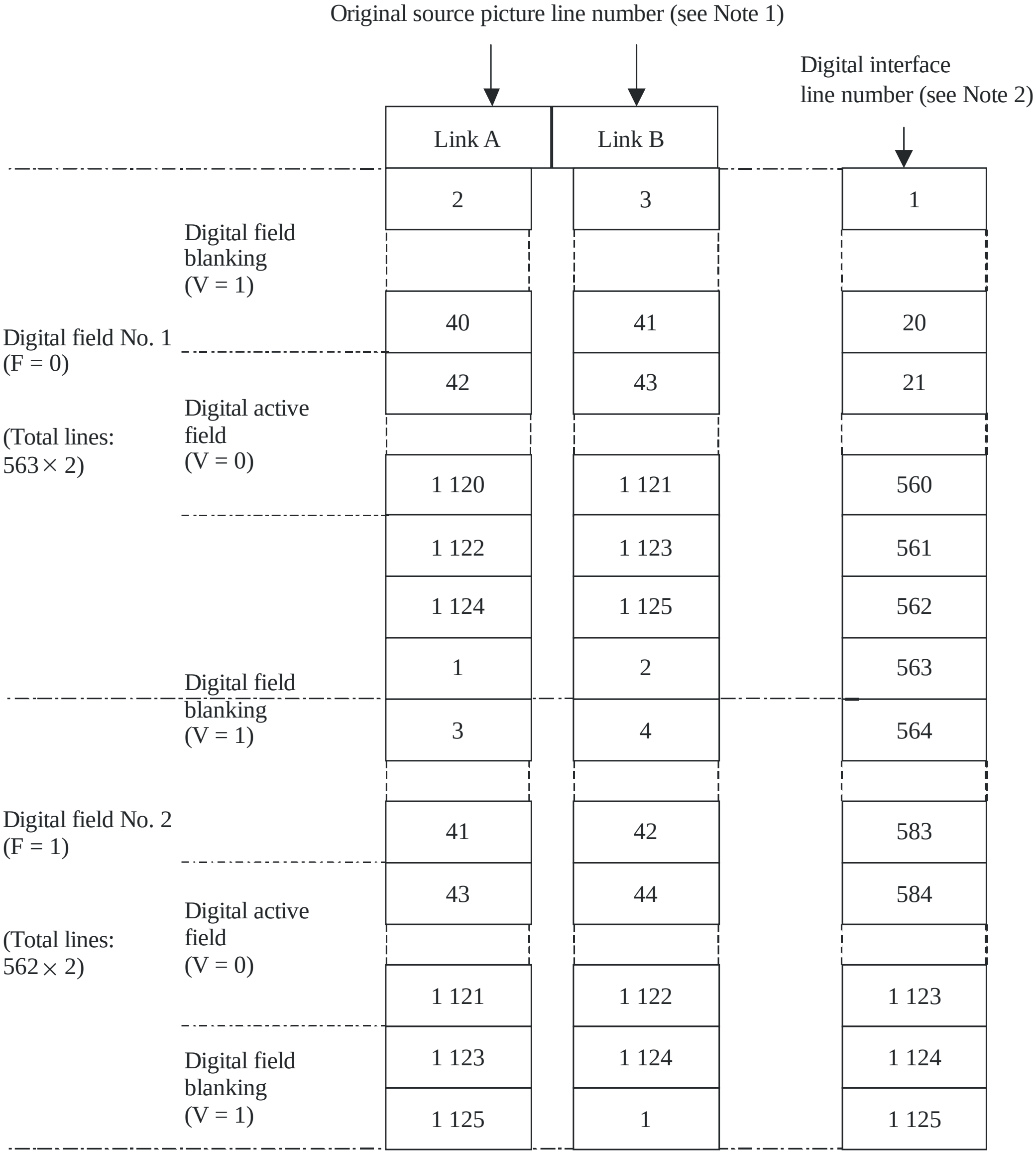
4.5.3 Timing reference signals and line numbers

The F (field/frame), V (vertical), H (horizontal), bits and the interface line numbers of link A and link B shall be as shown in Fig. 4.

NOTE 1 – Buffering having a minimum duration of one horizontal line is required by this process at each interface, making a minimum transmission delay of two horizontal lines.

FIGURE 4

Dual-link interface line numbering and packaging



Note 1 – 1 125 progressive line number as defined in Recommendation ITU-R BT.709, Part 2.
Note 2 – 1 125 interlaced digital line numbers are defined in Recommendation ITU-R BT.709, Part 2. The line number carried on the interface shall be the interface line number, not the source picture line.
Note 3 – The V flag on source picture lines 42 and 1 122 change when they are mapped onto Link B. Interlace Line 583 of Link B carries active video data but V = 1, and interface line 1 123 of Link B does not carry active video data however V = 0.

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4.5.4 Signal timing considerations

The timing difference between link A and link B shall not exceed 400 ns at the source.

4.5.5 Link A and link B identification

A payload identifier shall be present for this application and shall be inserted into the horizontal ancillary data space of the Y channel of both Link A and Link B.

Link A and link B shall be identified by the payload identifier in conformance with Recommendation ITU-R BT.1614 associated with the definition in Table 16.

TABLE 16

Payload identifier definitions for 1 920 × 1 080 video payloads on dual link high definition digital interfaces

<table>
<tr><th>Bits</th><th>Byte 1</th><th>Byte 2</th><th>Byte 3</th><th>Byte 4</th></tr>
<tr><td>Bit 7</td><td>1</td><td>Interlaced (0) or
Progressive (1) transport</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>Bit 6</td><td>0</td><td>Interlaced (0) or
Progressive (1) picture</td><td>Horizontal pixel count
1 920 (0) or reserved (1)</td><td>Channel assignment of dual link
Link A (0) or Link B (1)</td></tr>
<tr><td>Bit 5</td><td>0</td><td>Reserved</td><td>Aspect ratio
16:9 (1) or unknown (0)</td><td>Reserved</td></tr>
<tr><td>Bit 4</td><td>0</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>Bit 3</td><td>0</td><td rowspan="4">Picture rates
50 Hz (9h), 60 Hz (Bh)
60/1.001 Hz (Ah)</td><td rowspan="4">Sampling structure
4:2:2 Y,C_B,C_R (0h)</td><td>Reserved</td></tr>
<tr><td>Bit 2</td><td>1</td><td>Reserved</td></tr>
<tr><td>Bit 1</td><td>1</td><td rowspan="2">Bit depth
8-bit (0h), 10-bit (1h),
Reserved (2h, 3h)</td></tr>
<tr><td>Bit 0</td><td>1</td></tr>
</table>

When identifying 1 080-line progressive payloads mapped onto a dual-link 1.485 Gbit/s serial digital interface, the following constraints shall apply:

– Byte 1 shall have a value of (87h).

– The picture rate shall always be set to the rate at which the pictures were intended to be presented, regardless of the interface frame rate.

– In the case of 60 Hz, 60/1.001 Hz and 50 Hz progressive signals and all PsF signals, the transport type shall be set to interlaced (Bit b7 of byte 2 = 0) and the picture type shall be set to progressive (Bit b6 of byte 2 = 1).

– Bit b6 of byte 3 shall be used to identify active Y samples as defined by the horizontal sample count, and shall be constrained to (0).

– the channel number in Bit b6 of byte 4 shall be set to a value of 0 for Link A and to 1 for Link B.

– Bits b0 and b1 of byte 4 shall be set as follows, 8 Bit Pixel depth (0h), 10 bit pixel depth (1h).

4.5.6 Ancillary data

The ancillary data shall be mapped into the blanking area of link A and link B, and shall be in conformance with Recommendation ITU-R BT.1364. The ancillary data mapping onto link A shall be prior to the mapping onto link B.

4.5.7 Audio data

If present, the audio data shall be mapped into the ancillary data space of link A and link B, and shall be in conformance with Recommendation ITU-R BT.1365. The audio data mapping onto link A shall be prior to the mapping onto link B.

– *Example 1*: When 12 channels of audio data are mapped onto the dual link interface, all of the 12 channels shall be mapped onto link A – it is prohibited to map 8 channels onto link A and 4 channels onto link B.

– *Example 2*: When 20 channels of audio data are mapped, 16 channels shall be mapped onto link A and 4 channels shall be mapped onto link B.

4.5.8 Time code

If present, the time code shall be mapped into the ancillary data space of link A, and shall be in conformance with Recommendation ITU-R BT.1366.

4.6 Single link 3Gbit/s mapping – Dual link source

Two parallel 10-bit interfaces of the same line and frame structure, having bit synchronization and constructed in conformance with § 4 of this Recommendation, shall be mapped into a 20-bit virtual interface consisting of two data streams – data stream one and data stream two.

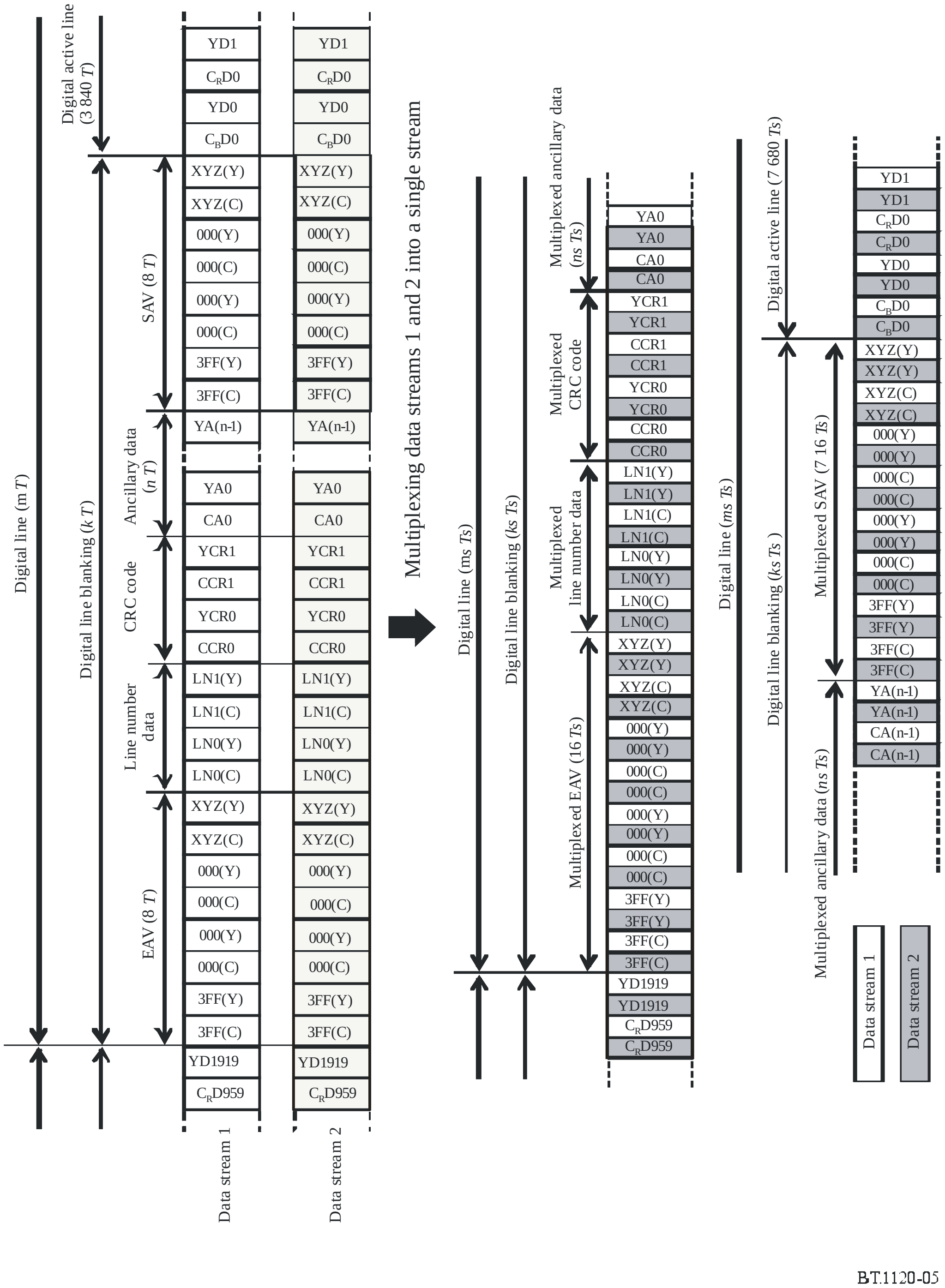
Data-stream one shall contain all of the 10-bit data words of the Link A interface and data stream two shall contain all of the data words of the Link B interface as shown in Fig. 5.

The 10-bit interfaces so constructed shall contain timing reference code words (SAV/EAV, line numbers and line-based CRCs as defined in this Recommendation.

Each parallel 10-bit interface shall be line- and word-aligned, having an interface frequency of 148.5 MHz or 148.5/1.001 MHz.

FIGURE 5

Structure of a single 3 Gbit/s link mapping *Y*, C_B, C_R



YD0 – YD1919: Digital luminance data *Y*
CBD0 – CBD959: Digital colour-difference data C_B
CRD0 – CRD959: Digital colour-difference data C_R
YA0 – YA(n-1): Ancillary data or blanking data in *Y*-channel
CA0 – CA(n-1): Ancillary data or blanking data in C_B/C_R-channel

See Table 17 for sample values not indicated as numbers.

TABLE 17

Data stream timing specifications (see Fig. 5)

Symbol	Parameter	Value	
		60/P	**50/P**
T	Parallel clock period (ns)	1 000/148.5 (1 001/148.5)	1 000/148.5
T_s	Multiplexed parallel data clock period	T/2	
m	Digital line in parallel data stream	4 400	5 280
k	Digital line blanking in parallel data stream	560	1 440
n	Ancillary data or blanking data in parallel data stream	536	1 416
m_s	Digital line in multiplexed parallel data stream	8 800	10 560
k_s	Digital line blanking in multiplexed parallel data stream	1 120	2 880
n_s	Ancillary data or blanking data in multiplexed parallel data stream	1 072	2 832

4.6.1 Single link 3 Gbit/s payload identifier (Dual link source)

A payload identifier shall be present for this application and shall be inserted into the horizontal ancillary data space of the Y channel of both Data stream one and Data stream two.

This payload identifier shall be in conformance with the payload identifier data format defined in Recommendation ITU-R BT.1614 associated with the definition in Table 18. The 4-byte payload identifier shall be mapped into the horizontal blanking area of the interface immediately following an EAV-LN-CRC word sequence.

1 125I (field 1): Line 10

1 125I (field 2): Line 572.

TABLE 18

Single 3 Gbit/s mapping - dual link payload identifier

<table>
<tr><th></th><th>Byte 1</th><th>Byte 2</th><th>Byte 3</th><th>Byte 4</th></tr>
<tr><td>Bit 7</td><td>1</td><td>Interlaced (0) or progressive (1) transport</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>Bit 6</td><td>0</td><td>Interlaced (0) or progressive (1) picture</td><td>Horizontal pixel count
1 920 (0) Reserved (1)</td><td>Channel assignment of dual link
Link A (0) or Link B (1)</td></tr>
<tr><td>Bit 5</td><td>0</td><td>Reserved</td><td>Aspect ratio
16:9 (1), unknown (0)</td><td>Reserved</td></tr>
<tr><td>Bit 4</td><td>0</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>Bit 3</td><td>1</td><td rowspan="4">Picture rates
50 Hz (9h), 60 Hz (Bh)
60/1.001 Hz (Ah)</td><td rowspan="4">Sampling structure
4:2:2 (0h), Y, C_B, C_R</td><td>Reserved</td></tr>
<tr><td>Bit 2</td><td>0</td><td>Reserved</td></tr>
<tr><td>Bit 1</td><td>1</td><td rowspan="2">Bit depth
8-bit (0h), 10-bit (1h)
Reserved (2h, 3h)</td></tr>
<tr><td>Bit 0</td><td>0</td></tr>
</table>

Byte 1 Shall have a value of (8Ah)

Byte 2

The second byte shall be used to identify the picture rate and the picture and transport structure.

Bit b7 shall be used to identify whether the digital interface uses a progressive or interlaced transport structure such that:

b7 = (0) identifies an interlaced transport

b7 = (1) identifies a progressive transport.

Bit b6 shall be used to identify whether the picture has a progressive or interlaced structure such that:

b6 = (0) identifies an interlaced structure

b6 = (1) identifies a progressive structure.

NOTE – PsF video payloads are identified by a progressive scanning of the video payload transported over an interlaced digital interface transport carrying the progressive video payload as a first and second picture segment within the transport frame duration. These first and second picture segments are indicated by the first and second field indicators in the digital interface transport.

Bits b5 to b4 shall be set to (0).

Bits b3 to b0 shall be used to identify the picture rate in Hz and shall be restricted to the frame rates (50 Hz (9h), 60 Hz (Bh) and 60/1.001 Hz (Ah)) as defined in Recommendation ITU-R BT.709 Part 2.

Byte 3

The third byte shall be used to identify the aspect ratio and sampling structure of the video payload.

Bit b6 shall be used to identify horizontal pixel count:

(0) 1 920 pixels

(1) reserved.

Bit b5 shall be used to identify the image aspect ratio:

(0) aspect ratio unknown

(1) 16:9 image.

Bits b3 to b0 of byte 3 shall be used to identify the sampling structure. This Recommendation is constrained to value (0h).

Bits b7 and b4 shall be reserved and set to (0).

Byte 4

Bits b7 to b2 are reserved and set to (0).

Bits b1 and b0 shall be used to identify the bit depth:

(0) identifies 8 bits per sample

(1) identifies 10 bits per sample.

4.7 Applications of the dual-link bit-serial digital interface

Appendix 1 to Annex 1 shows some HDTV applications of the dual-link high definition bit-serial digital interface for other extended signal formats.

4.8 Applications of a single 3Gbit/s link carrying data formatted on two 1.5 Gbit/s interfaces

Appendix 2 to Annex 1 shows some HDTV applications of a single 3 Gbit/s link high definition bit-serial digital interface for other extended signed formats.

Appendix 1
to Annex 1

Applications of the dual-link high-definition serial digital interface

The dual-link high-definition serial digital interface can also be used to convey HDTV source signal formats listed in Table 19.

TABLE 19

HDTV extended source signal formats

Signal format sampling structure	Pixel bit depth	Frame/field rates
4:4:4 (*RGB*) 4:4:4:4 (*RGB* + *A* or *D*)	10 bit	30, 30/1.001, 25, 24, and 24/1.001 Hz progressive and segmented frame 60, 60/1.001, and 50 Hz fields interlaced
4:4:4 (*RGB*)	12 bit	
4:2:2 (YC_BC_R) 4:2:2:4 (YC_BC_R + *A* or *D*)	12 bit	
4:4:4 (YC_BC_R) 4:4:4:4 (YC_BC_R + *A* or *D*)	10 bit	
4:4:4 (YC_BC_R)	12 bit	

NOTE 1 – The “A” or “D” component is an auxiliary component which is user defined dependent upon the application. The “A” nomenclature refers to a picture channel, whereas the “D” nomenclature refers to a non-picture (i.e. data) channel. In the case of “D” component, the bit depth of the auxiliary signal is constrained to 8 bits maximum.

1 4:4:4 (*RGB*) and 4:4:4:4 (*RGB* + *A* or *D*) 10-bit signals of 30/P, 30/PsF, 60/I, 25/P, 25/PsF, 50/I, 24/P and 24/PsF systems

1.1 Source sample numbering

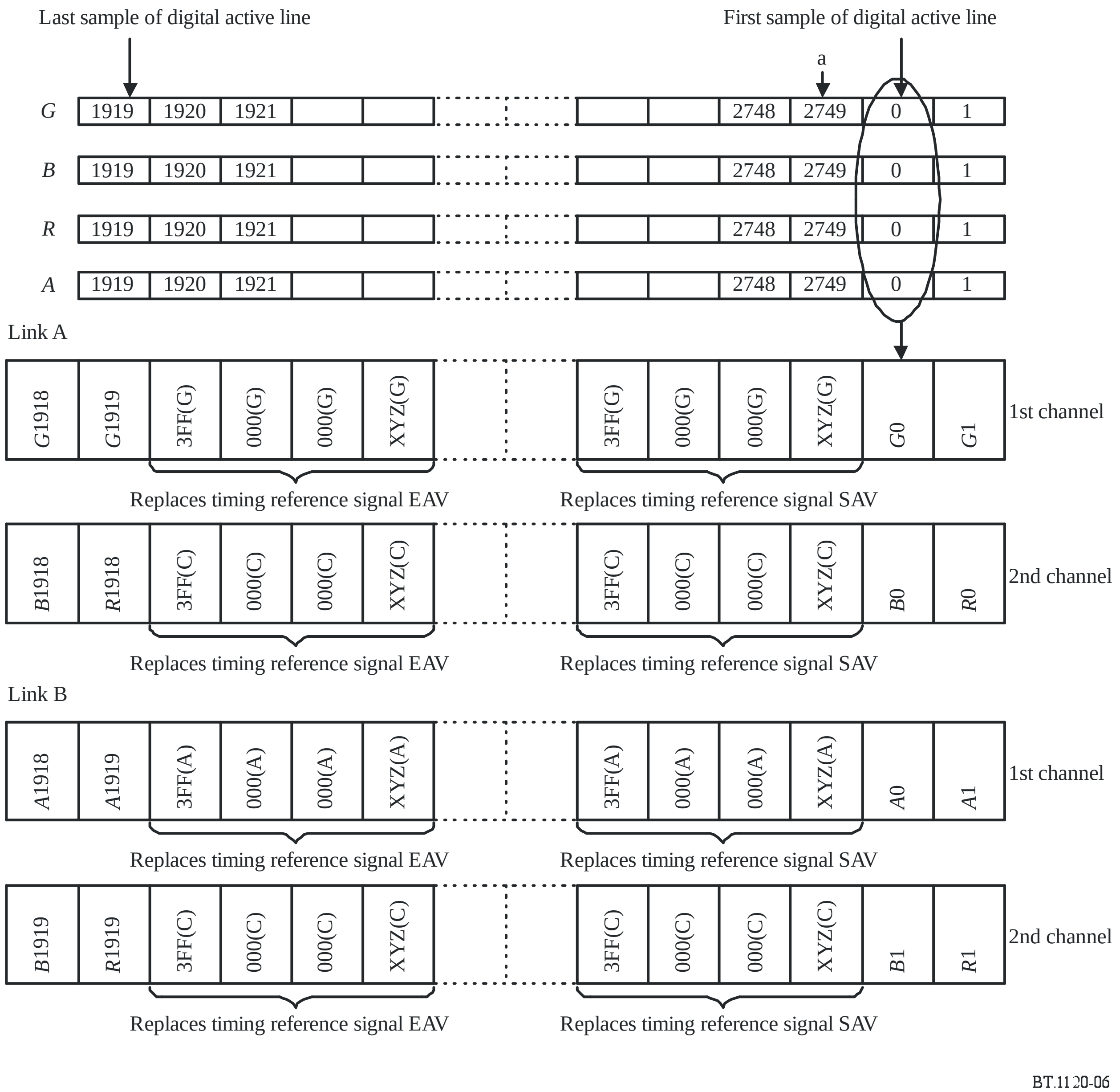
Each line of the *G*, *B*, *R* and *A* or *D* components consists of 2 750, 2 640 or 2 200 total samples as shown in Table 2. The samples are designated 0-2 749, 0-2 639, or 0-2 199 and the individual samples are designated by suffixes such as sample *G*135 or sample *B*429.

1.2 Interface data streams

Link A data stream contains all the *G* component samples plus the even-numbered (0, 2, 4, etc.) samples from the *B* and *R* components. Link B data stream contains the odd-numbered (1, 3, 5, etc.) samples from the *B* and *R* components plus all the *A* or *D* component samples (see Fig. 6).

FIGURE 6

Multiplex structure for 4:4:4 (*RGB*) and 4:4:4:4 (*RGB* + *A*) 10-bit signals



Frame/field rates	Pixel bit depth	Total words per transmission package	Total words of active image data per transmission package	Word number a
60 or 60/1.001 fields, 30 or 30/1.001 frames	10 bit	2 200	1 920	2 199
50 fields, 25 frames	10 bit	2 640	1 920	2 639
24 or 24/1.001 frames	10 bit	2 750	1 920	2 749

1.3 Multiplex structure

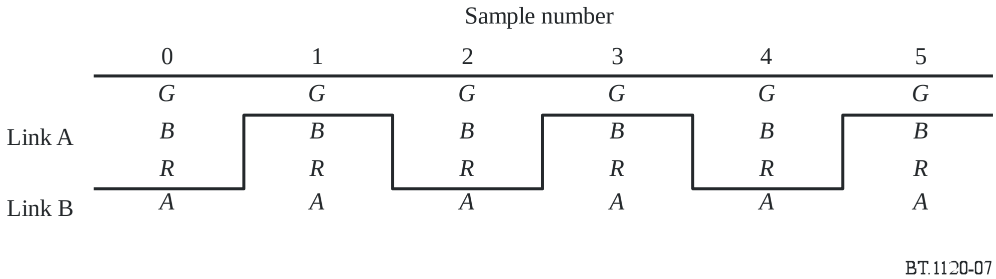
The video data words shall be conveyed in the following order: (see Fig. 7)

Link A data stream: *B*0, *G*0, *R*0, *G*1, *B*2, *G*2, *R*2, *G*3 ...

Link B data stream: *B*1, *A*0, *R*1, *A*1, *B*3, *A*2, *R*3, *A*3 ...

FIGURE 7

Link contents for 4:4:4 (*RGB*) and 4:4:4:4 (*RGB* + *A*) 10-bit signals



1.4 Auxiliary signal

Use of the auxiliary (*A* or *D*) signal is application dependent.

If the auxiliary signal is not present, the default value of the auxiliary component shall be set to $64_{(10)}$. If the auxiliary signal is used for conveying picture information, the raster format and frame/field rate shall be the same as the *G* component carried on the interface. If the auxiliary signal is used for conveying non-picture information, data words of the auxiliary signal shall be 8-bit maximum. As a 10-bit interface, bit b8 shall be the even parity for bits b7 through b0, and bit b9 shall be the complement of bit b8.

Data values $0_{(10)}$ to $3_{(10)}$ and 1 $020_{(10)}$ to 1 $023_{(10)}$ shall not be permitted.

2 4:4:4 (*RGB*) 12-bit signals of 30/P, 30/PsF, 60/I, 25/P, 25/PsF, 50/I, 24/P and 24/PsF systems

2.1 Source sample numbering

Each line of the *G*, *B*, and *R* components consists of 2 750, 2 640 or 2 200 total samples as shown in Table 2. The samples are designated 0-2 749, 0-2 639 or 0-2 199 and the individual samples are designated by suffixes such as sample *G*135 or sample *B*429. The samples are 12-bit quantized according to the digital encoding equations defined below:

$$D'_R = \mathrm{INT}\left[\left(219\, E'_R + 16\right) \cdot 2^{n-8}\right]$$

$$D'_G = \mathrm{INT}\left[\left(219\, E'_G + 16\right) \cdot 2^{n-8}\right]$$

$$D'_B = \mathrm{INT}\left[\left(219\, E'_B + 16\right) \cdot 2^{n-8}\right]$$

"*n*" denotes the number of the bit length of the quantized signal, namely $n = 12$.

The operator INT returns the value of 0 for fractional parts in the range of 0 to 0.4999... and +1 for fractional parts in the range of 0.5 to 0.9999..., i.e. it rounds up fractions above 0.5.

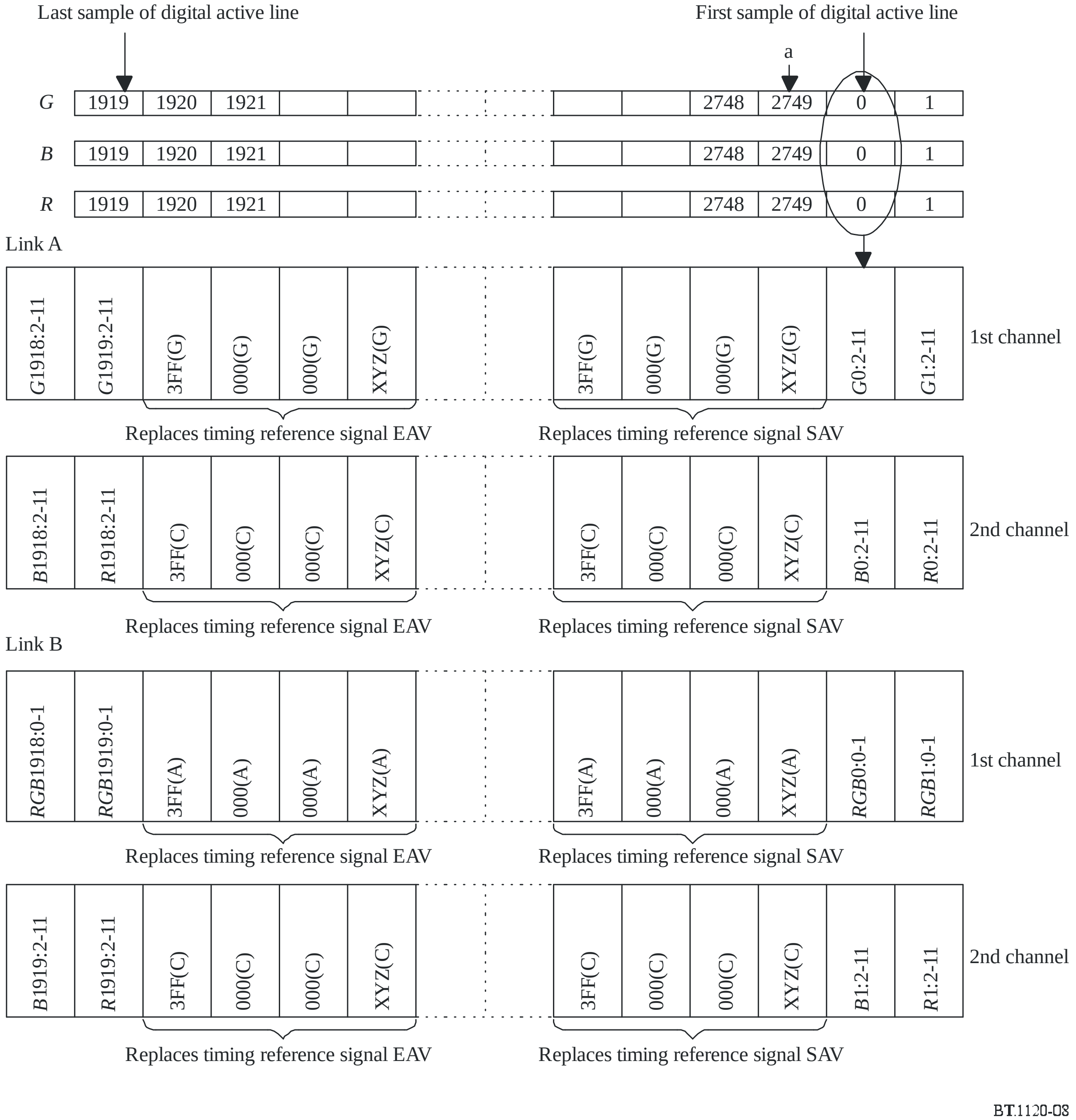
The most significant 10 bits of the 12-bit samples are designated by suffixes such as sample *G*135:2-11 or sample *B*429:2-11, and the least significant 2 bits of 12-bit samples are designated by suffixes such as sample *G*135:0-1 or sample *B*429:0-1. The least significant 2 bits of the *R*, *G* and *B* signals are mapped to the 1st channel of link B, and are designated by suffixes such as *RGB*135:0-1. The *n*-th bit of *R*, *G* and *B* signals is designated by a suffix such as *G*:*n*. The *RGB*:0-1 data structure is defined in § 2.3.

2.2 Interface data streams

Link A data stream contains the most significant 10 bits of all the *G* component samples, plus the most significant 10 bits of the even-numbered (0, 2, 4, etc.) samples in the *B* and *R* components. Link B data stream contains the most significant 10 bits of odd-numbered (1, 3, 5, etc.) samples in the *B* and *R* components, plus the least significant 2 bits from all the samples in the *R*, *G* and *B* components (see Fig. 8).

FIGURE 8

Multiplex structure for 4:4:4 (*RGB*) 12-bit signals



Frame/field rate	Pixel bit depth	Total words per transmission package	Total words of active image data per transmission package	Word number a
60 or 60/1.001 fields, 30 or 30/1.001 frames	12 bits	2 200	1 920	2 199
50 fields, 25 frames	12 bits	2 640	1 920	2 639
24 or 24/1.001 frames	12 bits	2 750	1 920	2 749

2.3 *RGB*:0-1 onto first channel of link B data mapping

Mapping of the least significant 2 bits from *R*, *G* and *B* onto the first channel of link B is shown in Table 20.

TABLE 20

RGB:0-1 onto first channel of link B mapping structure

Word	Bit number 9 (MSB)	 8	 7	 6	 5	 4	 3	 2	 1	 0 (LSB)
	$\overline{\text{B8}}$	EP	*G*:1	*G*:0	*B*:1	*B*:0	*R*:1	*R*:0	Res	Res

MSB: most significant bit.

LSB: least significant bit.

Bit b8 is the even parity for Bits b7 through b0.

Bit b9 is the complement of Bit b8.

Bits b0 and b1 are the reserved bits (reserved bits shall be set to 0 until defined).

2.4 Multiplex structure

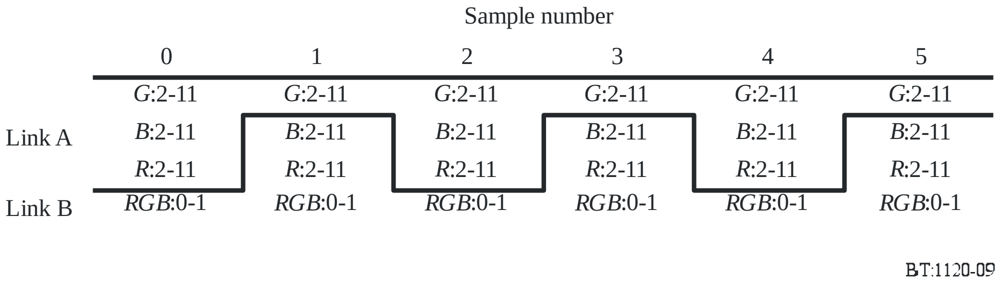
The picture data words shall be conveyed in the following order: (see Fig. 9)

Link A data stream: *B*0:2-11, *G*0:2-11, *R*0:2-11, *G*1:2-11, *B*2:2-11, *G*2:2-11, *R*2:2-11, *G*3:2-11 ...

Link B data stream: *B*1:2-11, *RGB*0:0-1, *R*1:2-11, *RGB*1:0-1, *B*3:2-11, *RGB*2:0-1, *R*3:2-11, *RGB*3:0-1 ...

FIGURE 9

Link contents for 4:4:4 (_RGB_) 12-bit signals



3 4:2:2 (YC_BC_R) 12-bit signals of 30/P, 30/PsF, 60/I, 25/P, 25/PsF, 50/I, 24/P and 24/PsF systems

3.1 Source sample numbering

Each line of the Y component consists of 2 750, 2 640 or 2 200 total samples and each line of the C_B and C_R components consists of 1 375, 1 320, or 1 100 total samples, as shown in Table 2. The samples are designated 0-2 749, 0-2 639 or 0-2 199 for Y component and 0-1 374, 0-1 319 or 0-1 099 for C_B and C_R components, and the individual samples are designated by suffixes such as sample $Y$135 or sample C_B429. The samples are 12-bit quantized according to the digital encoding equations defined below:

$$D'_Y = \mathrm{INT}\left[\left(219\ E'_Y + 16\right) \cdot 2^{n-8}\right]$$

$$D'_{CB} = \mathrm{INT}\left[\left(224\ E'_{CB} + 128\right) \cdot 2^{n-8}\right]$$

$$D'_{CR} = \mathrm{INT}\left[\left(224\ E'_{CR} + 128\right) \cdot 2^{n-8}\right]$$

"n" denotes the number of the bit length of the quantized signal, namely $n = 12$.

The operator INT returns the value of 0 for fractional parts in the range of 0 to 0.4999... and +1 for fractional parts in the range of 0.5 to 0.9999..., i.e. it rounds up fractions above 0.5.

The most significant 10 bits of the 12-bit samples are designated by suffixes such as sample $Y$135:2-11 or sample C_B429:2-11, and the least significant 2 bits of 12-bit samples are designated by suffixes such as sample $Y$135:0-1 or sample C_B429:0-1. The least significant 2 bits of the Y, C_B and C_R signals are mapped to the first channel of link B, and are designated by suffixes such as YC_BC_R135:0-1 and $Y$136:0-1. The n-th bit of Y, C_B and C_R signals is designated by a suffix such as Y:n. The YC_BC_R:0-1 and Y:0-1 data structure is defined in § 3.3.

3.2 Interface data streams

Link A data stream contains the most significant 10 bits of all the Y component samples plus the most significant 10 bits of all the even-numbered C_B, C_R components samples. Link B data stream contains the least significant 2 bits of Y, C_B, C_R components samples at even-numbered sample points, and the least significant 2 bits of Y (only) at odd-numbered sample points, plus the A or D component (see Fig. 10).

3.3 YC_BC_R:0-1 and Y:0-1 onto first channel of link B data mapping

Mapping of the least significant 2 bits from the even-numbered samples of Y, C_B and C_R, and the least significant 2 bits from the odd-numbered samples of Y (only), onto the first channel of link B, is shown in Tables 21 and 22 and Fig. 11.

TABLE 21

YC_BC_R:0-1 onto 1st channel of link B mapping structure

Word	Bit number 9 (MSB)	8	7	6	5	4	3	2	1	0 (LSB)
	$\overline{\text{Bit8}}$	EP	Y:1	Y:0	C_B:1	C_B:0	C_R:1	C_R:0	Res	Res

MSB: most significant bit.

LSB: least significant bit.

Bit b8 is the even parity for Bits b7 through b0.

Bit b9 is the complement of Bit b8.

Bits b0 and b1 are the reserved bits (reserved bits shall be set to 0 until defined).

TABLE 22

Y:0-1 onto 1st channel of link B mapping structure

Word	Bit number 9 (MSB)	8	7	6	5	4	3	2	1	0 (LSB)
	$\overline{\text{Bit8}}$	EP	Y:1	Y:0	Res	Res	Res	Res	Res	Res

MSB: most significant bit.

LSB: least significant bit.

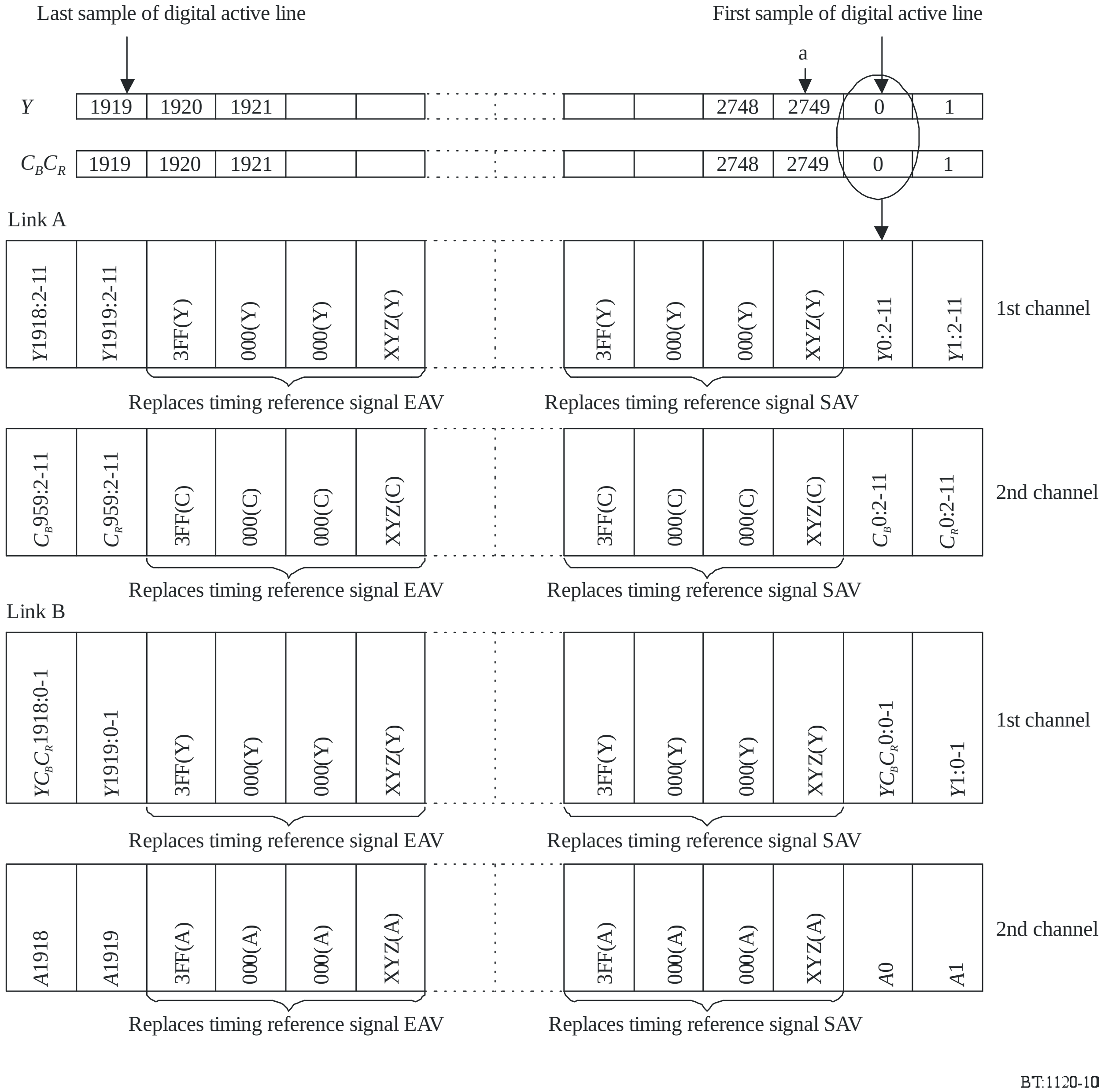
Bit b8 is the even parity for Bits b7 through b0.

Bit b9 is the complement of Bit b8.

Bits b0 through b5 are the reserved bits (reserved bits shall be set to 0 until defined).

FIGURE 10

Multiplex structure for 4:2:2 (YC_BB_R) 12-bit signals



Frame/field rate	Pixel bit depth	Total words per transmission package	Total words of active image data per transmission package	Word number a
60 or 60/1.001 fields, 30 or 30/1.001 frames	12 bit	2 200	1 920	2 199
50 fields, 25 frames	12 bit	2 640	1 920	2 639
24 or 24/1.001 frames	12 bit	2 750	1 920	2 749

3.4 Multiplex structure

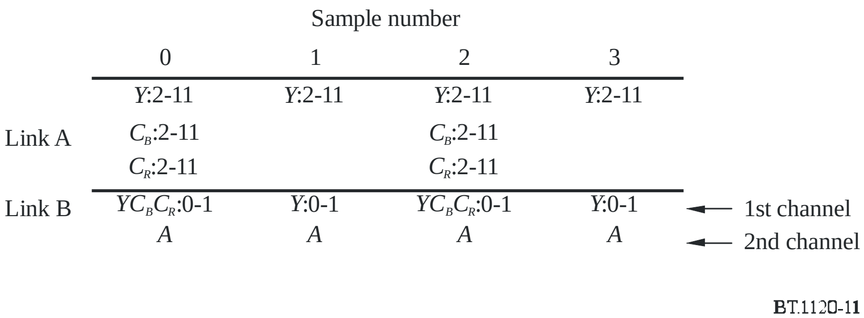
The picture data words shall be conveyed in the following order: (see Fig. 11)

Link A data stream: C_B0:2-11, Y0:2-11, C_R0:2-11, $Y$1:2-11, C_B2:2-11, $Y$2:2-11, C_R2:2-11, $Y$3:2-11 ...

Link B data stream: A0, YC_BC_R0:0-1, $A$1, $Y$1:0-1, $A$2, YC_BC_R2:0-1, $A$3, $Y$3:0-1 ...

FIGURE 11

Link contents for 4:2:2 (YC_BB_R) 12-bit signals



3.5 Auxiliary signal

See § 1.4.

4 4:4:4 (YC_BC_R), 4:4:4:4 (YC_BC_R + A or D) 10-bit signals of 30/P, 30/PsF, 60/I, 25/P, 25/PsF, 50/I, 24/P and 24/PsF systems

4.1 Source sample numbering

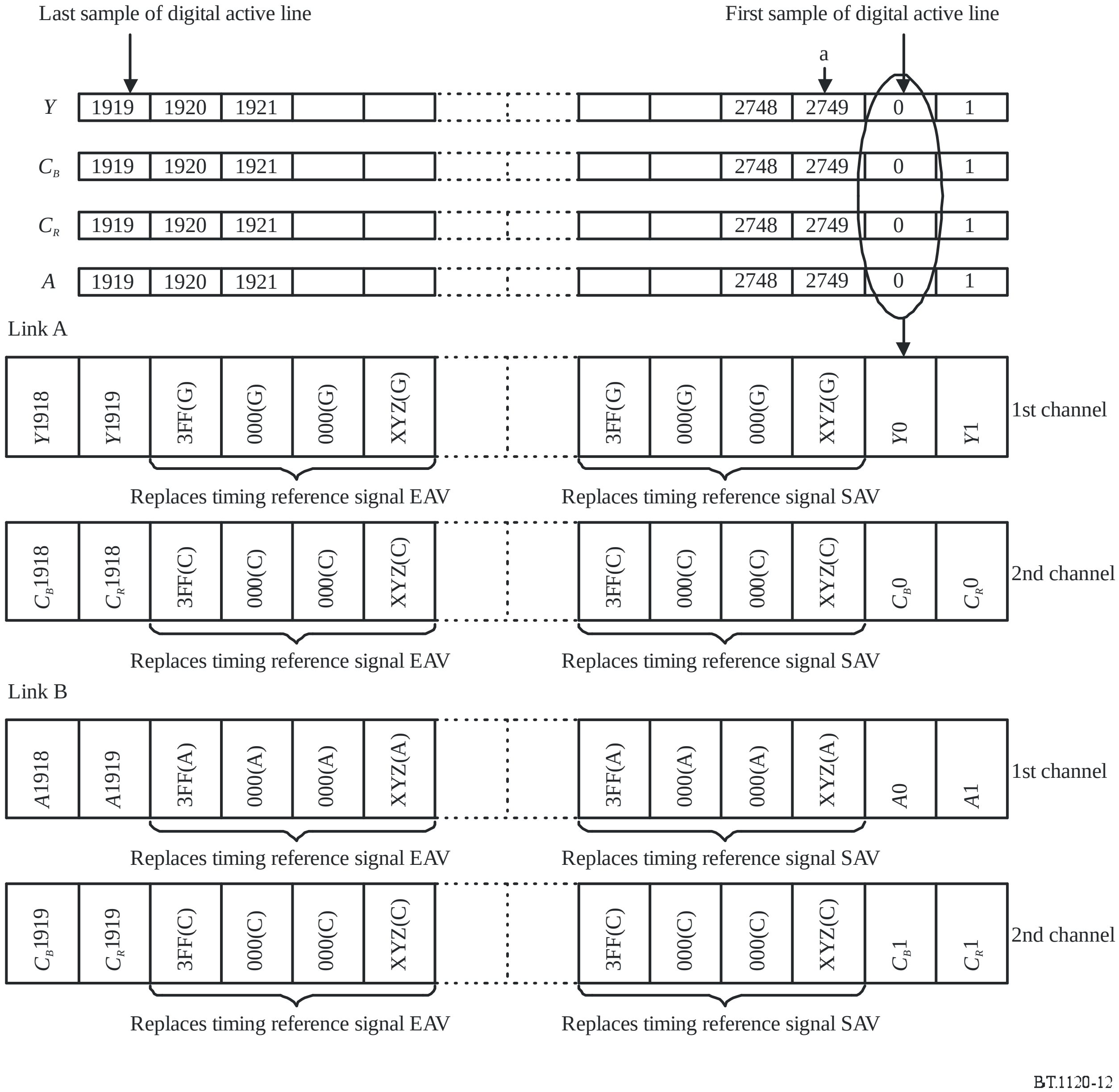
Each line of the Y, C_B, C_R and A or D component consists of 2 750, 2 640 or 2 200 total samples. The samples are designated 0-2 749, 0-2 639, or 0-2199 and the individual samples are designated by suffixes such as sample $Y$135 or sample C_B429.

4.2 Interface data streams

Link A data stream contains all the Y component samples plus the even-numbered (0, 2, 4, etc.) samples from the C_B and C_R components. Link B data stream contains the odd-numbered (1, 3, 5, etc.) samples from the C_B and C_R components plus all the A or D component samples (see Fig. 12).

FIGURE 12

Multiplex structure for 4:4:4 (YC_BC_R) and 4:4:4:4 ($YC_BC_R + A$) 10-bit signals



Frame/field rates	Pixel bit depth	Total words per transmission package	Total words of active image data per transmission package	Word number a
60 or 60/1.001 fields, 30 or 30/1.001 frames	10 bit	2 200	1 920	2 199
50 fields, 25 frames	10 bit	2 640	1 920	2 639
24 or 24/1.001 frames	10 bit	2 750	1 920	2 749

4.3 Multiplex structure

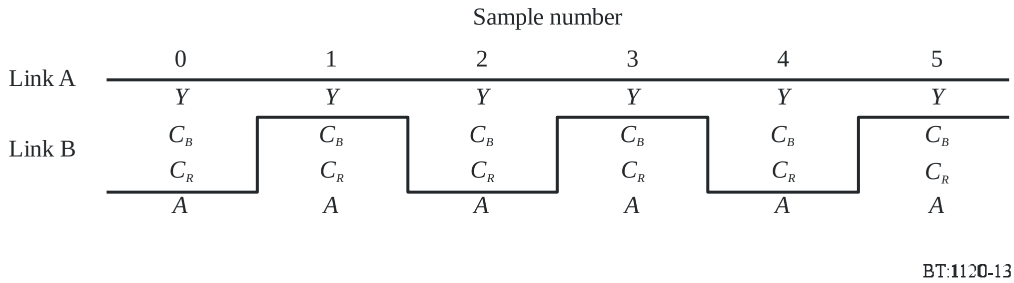
The picture data words shall be conveyed in the following order: (see Fig. 13)

Link A data stream: C_B0, $Y0$, C_R0, $Y1$, C_B2, $Y2$, C_R2, $Y3$ ...

Link B data stream: C_B1, $A0$, C_R1, $A1$, C_B3, $A2$, C_R3, $A3$ ...

FIGURE 13

Link contents for 4:4:4 (YC_BC_R) and 4:4:4:4 (YC_BC_R+A) 10-bit signals



4.4 Auxiliary signal

See § 1.4.

5 4:4:4 (YC_BC_R) 12-bit signals of 30/P, 30/PsF, 60/I, 25/P, 25/PsF, 50/I, 24/P and 24/PsF systems

5.1 Source sample numbering

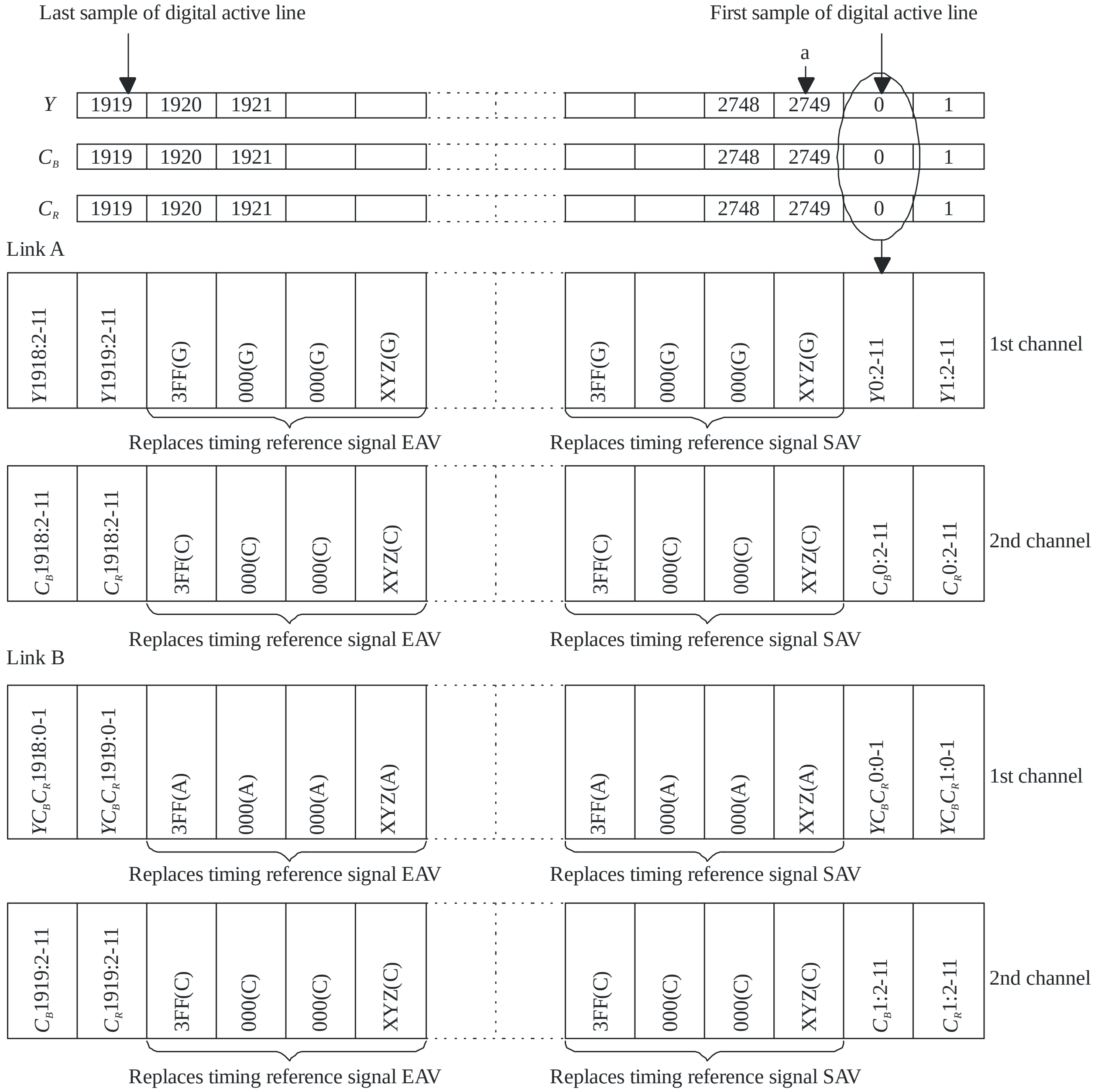
Each line of the Y, C_B, and C_R components consists of 2 750, 2 640 or 2 200 total samples. The samples are designated 0-2 749, 0-2 639 or 0-2 199 and the individual samples are designated by suffixes such as sample $Y135$ or sample C_B429. The samples are 12-bit quantized according to the digital encoding equations in § 3.1. The most significant 10 bits of the 12-bit samples are designated by suffixes such as sample $Y135$:2-11 or sample C_B429:2-11, and the least significant 2 bits of 12-bit samples are designated by suffixes such as sample $Y135$:0-1 or sample C_B429:0-1. The least significant 2 bits of the Y, C_B and C_R signals are mapped to the 1st channel of link B, and are designated by suffixes such as Y, $\mathrm{C_B}$, $\mathrm{C_R}$135:0-1. The n-th bit of Y, C_B and C_R signals is designated by a suffix such as Y:n. The Y, C_B, C_R:0-1 data structure is defined as per § 3.3.

5.2 Interface data streams

Link A data stream contains the most significant 10 bits of all the Y component samples, plus the most significant 10 bits of the even-numbered (0, 2, 4, etc.) samples in the C_B and C_R components. Link B data stream contains the most significant 10 bits of odd-numbered (1, 3, 5, etc.) samples in the C_B and C_R components, plus the least significant 2 bits from all the samples in the Y, C_B and C_R components (see Fig. 14).

FIGURE 14

Multiplex structure for 4:4:4 (YC_BC_R) 12-bit signals



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Frame/field rate	Pixel bit depth	Total words per transmission package	Total words of active image data per transmission package	Word number a
60 or 60/1.001 fields, 30 or 30/1.001 frames	12 bit	2 200	1 920	2 199
50 fields, 25 frames	12 bit	2 640	1 920	2 639
24 or 24/1.001 frames	12 bit	2 750	1 920	2 749

5.3 Multiplex structure

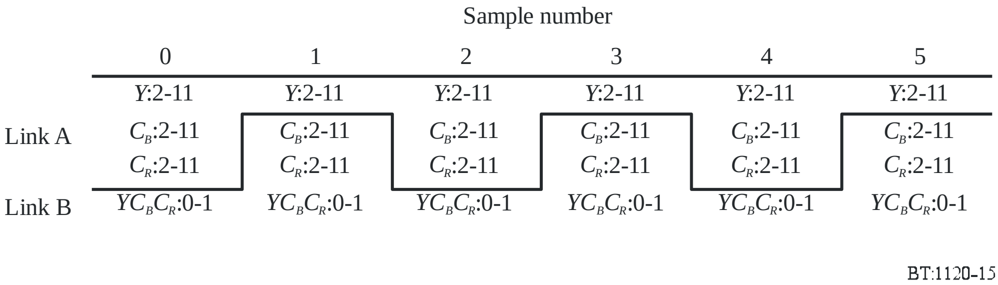
The video data words shall be conveyed in the following order: (see Fig. 15)

Link A data stream: C_B0:2-11, Y0:2-11, C_R0:2-11, $Y$1:2-11, C_B2:2-11, $Y$2:2-11, C_R2:2-11, $Y$3:2-11 ...

Link B data stream: C_B1:2-11, YC_BC_R0:0-1, C_R1:2-11, YC_BC_R1:0-1, C_B3:2-11, YC_BC_R2:0-1, C_R3:2-11, YC_BC_R3:0-1 ...

FIGURE 15

Link contents for 4:4:4 (YC_BC_R) 12-bit signals



5.4 Extended picture payload values

TABLE 23

Extended picture payload identifier definitions for 1 920 × 1 080 video payloads on dual link high definition digital interfaces

Bits	Byte 1	Byte 2	Byte 3	Byte 4
Bit 7	1	Interlaced (0) or progressive (1) transport	Reserved	Reserved
Bit 6	0	Interlaced (0) or progressive (1) picture	Horizontal active sample count 1 920 (0) or reserved (1)	Channel assignment of dual link Link A (0) or Link B (1)
Bit 5	0	Reserved	Aspect ratio 16:9 (1) or unknown (0)	Reserved
Bit 4	0	Reserved	Reserved	Reserved
Bit 3	0	Picture rates 24 Hz (3h), 24/1.001 Hz (2h), 25 Hz (5h), 30 Hz (7h) 30/1.001 Hz (6h)	Sampling structure 4:4:4 *RGB*(2h), 4:4:4:4 *RGB+A* (6h) 4:4:4:4 *RGB+D* (Ah) 4:4:4 Y, C_B,C_R (1h) 4:2:2 Y, C_B, C_R (0h) 4:2:2:4 Y, C_B,C_R+A(4h) 4:2:2:4 Y, C_B,C_R+D (8h)	Reserved
Bit 2	1			Reserved
Bit 1	1			Bit depth 8-bit (0h), 10-bit (1h) 12 bit (2h) reserved (3h)
Bit 0	1			

NOTE 1 – The term 4:4:4 identifies the ratio of component sampling independently of the resolution.

Link A and Link B shall be identified by the payload identifier with a byte 1 value of 87h.

A payload identifier shall be present for this application and shall be mapped into the horizontal ancillary data space immediately following an EAV-LN-CRC word sequence on the Y-channel of both Link A and Link B.

The recommended location of the ancillary data packets, if ancillary data space is available, shall be on the following lines:

1 125I (field 1): Line 10

1 125I (field 2): Line 572.

Appendix 2
to Annex 1

Applications of the single link 3 Gbit/s high definition serial digital interface 1.5 Gbit/s dual link to single link 3 Gbit/s mapping

The single link 3 Gbit/s high definition serial digital interface can also be used to convey HDTV source signal formats listed in Table 19 in Appendix 1 to Annex 1.

1 Dual-link source

Two parallel 10-bit interfaces of the same line and frame structure, having bit synchronization and constructed in conformance with this Recommendation, shall be mapped into a 20-bit virtual interface consisting of two data streams – data stream one and data stream two.

Data-stream one shall contain all of the 10-bit data words of the Link A interface and data stream two shall contain all of the data words of the Link B interface as shown in Fig. 16.

The detail of the mapping of Link A and Link B is described in § 1 to § 5 in Appendix 1 to Annex 1 of this Recommendation.

The 10-bit interfaces so constructed shall contain timing reference code words (SAV/EAV, line numbers and line based CRCs as defined in this Recommendation.

Each parallel 10-bit interface shall be line- and word-aligned, having an interface frequency of 148.5 MHz or 148.5/1.001 MHz.

The extended source formats listed in Table 19 are covered by this Appendix.

1.1 Data mapping

The dual link data is mapped into a single data stream as shown in Figs 16A and 16B.

Figure 16 A is a generic mapping. Figure 16B mapping is the *R*, *G*, *B*+A mapping.

Link A corresponds to data stream 1, Link B corresponds to data stream 2.

1.2 Payload identifier

A payload identifier (see Table 25) shall be present for this application and shall be inserted into the horizontal ancillary data space of the Y channel of both Link A and Link B.

This payload identifier shall be in conformance with the payload identifier data format defined in Recommendation ITU-R BT.1614. The 4-byte payload identifier shall be mapped into the horizontal blanking area of the interface immediately following an EAV-LN-CRC word sequence.

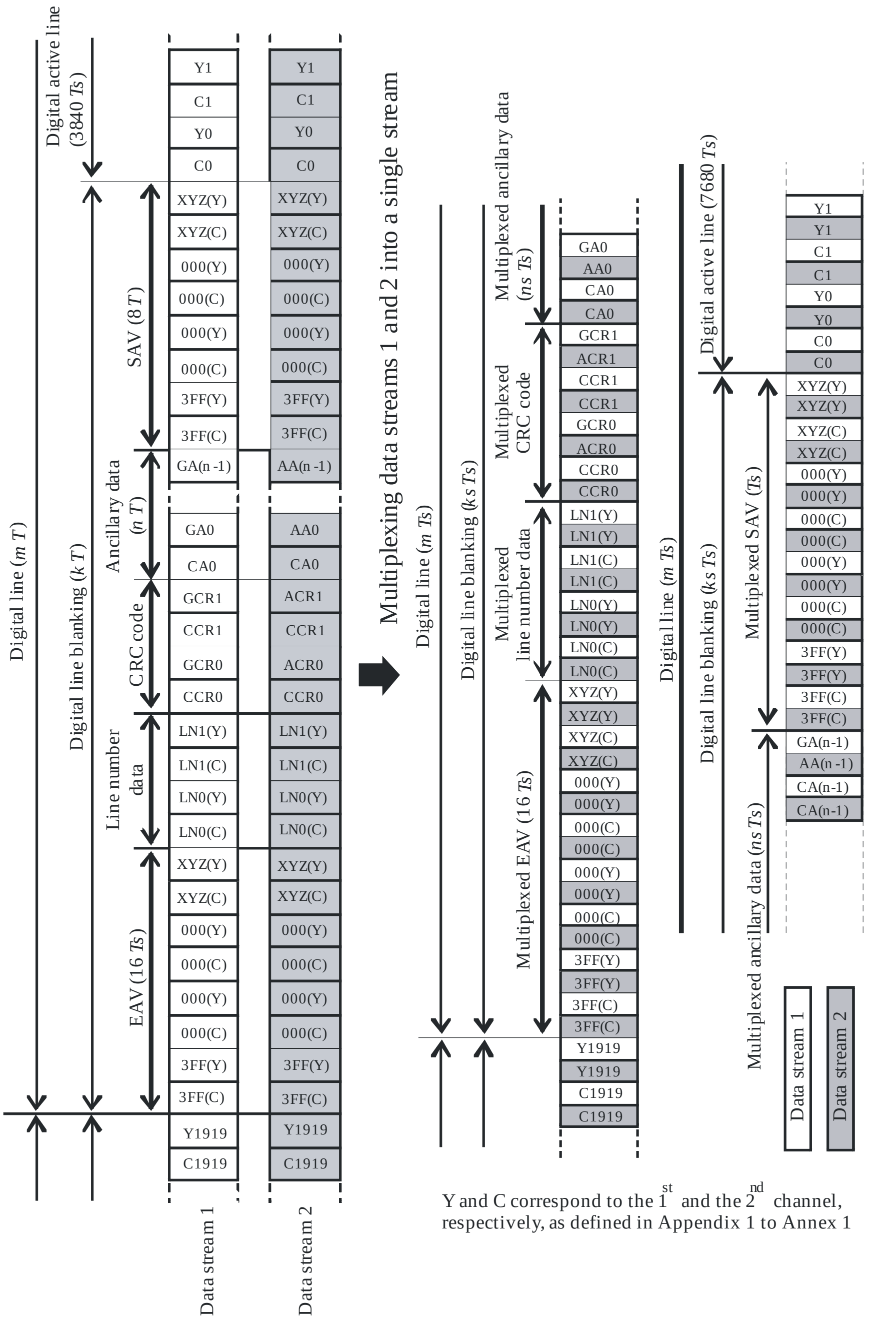
The recommended location of the ancillary data packets, if ancillary data space is available, shall be on the following lines:

1 125I (field 1): Line 10

1 125I (field 2): Line 572.

FIGURE 16A

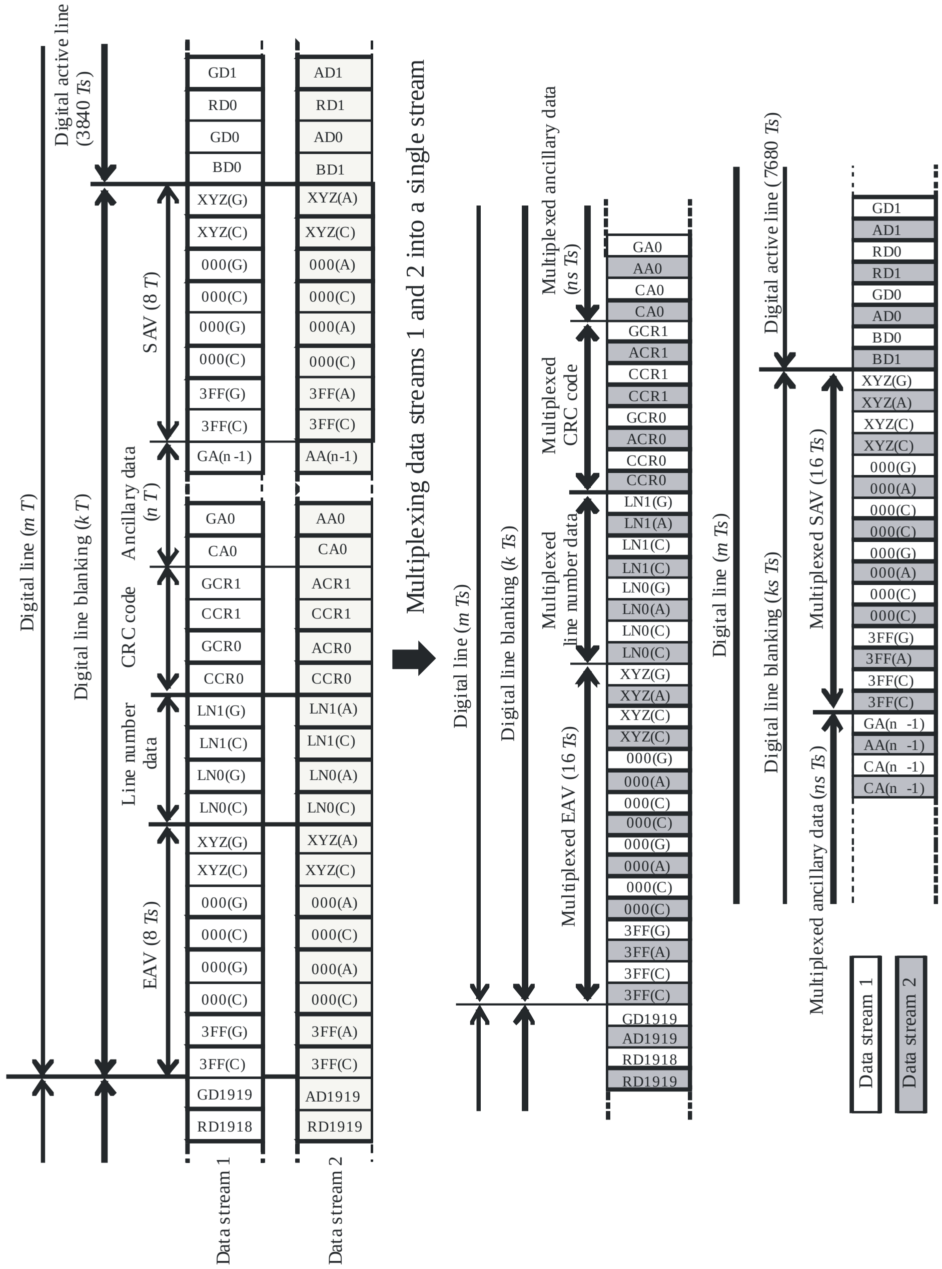
3 Gbit/s single-link data mapping – generic



BT:1120-16a

FIGURE 16B

3 Gbit/s single-link data mapping – informative example R, G, B+A



RD0 - RD1919: Red Data
GD0 - GD1919: Green Data
BD0 - BD1919: Blue Data
AD0 -AD1919: Alpha channel

BT:1120-16b

TABLE 24

Data stream timing specifications (see Fig. 16B)

Symbol	Parameter	Value	
		60I	50I
T	Parallel clock period (ns)	1 000/148.5 (1 001/148.5)	1 000/148.5
T_s	Multiplexed parallel data clock period	T/2	
m	Digital line in parallel data stream	4 400	5 280
k	Digital line blanking in parallel data stream	560	1 440
n	Ancillary data or blanking data in parallel data stream	536	1 416
m_s	Digital line in multiplexed parallel data stream	8 800	10 560
k_s	Digital line blanking in multiplexed parallel data stream	1 120	2 880
n_s	Ancillary data or blanking data in multiplexed parallel data stream	1 072	2 832

TABLE 25

Extended picture payload identifier for 3 Gbit/s single link

<table>
<tr><th>Bits</th><th>Byte 1</th><th>Byte 2</th><th>Byte 3</th><th>Byte 4</th></tr>
<tr><td>Bit 7</td><td>1</td><td>Interlaced (0) or progressive (1) transport</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>Bit 6</td><td>0</td><td>Interlaced (0) or progressive (1) picture</td><td>Horizontal active sample count
1 920 (0) or reserved (1)</td><td>Channel assignment of dual link
Link A (0) or Link B (1)</td></tr>
<tr><td>Bit 5</td><td>0</td><td>Reserved</td><td>Aspect ratio
16:9 (1) or unknown (0)</td><td>Reserved</td></tr>
<tr><td>Bit 4</td><td>0</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>Bit 3</td><td>1</td><td rowspan="4">Picture rates
24 Hz (3h), 24/1.001 Hz (2h),
25 Hz (5h), 30 Hz (7h)
30/1.001 Hz (6h)</td><td rowspan="4">Sampling structure
4:4:4 RGB (2h),
4:4:4:4 RGB+A (6h)
4:4:4:4 RGB+D (Ah)
4:4:4 Y, C_B, C_R (1h)
4:2:2 Y, C_B, C_R (0h)
4:2:2:4 Y, C_B, C_R+A (4h)
4:2:2:4 Y, C_B, C_R+D (8h)</td><td>Reserved</td></tr>
<tr><td>Bit 2</td><td>0</td><td>Reserved</td></tr>
<tr><td>Bit 1</td><td>1</td><td rowspan="2">Bit depth
8-bit (0h), 10-bit (1h)
12 bit (2h) reserved (3h)</td></tr>
<tr><td>Bit 0</td><td>0</td></tr>
</table>

Byte 1 Shall have a value of (8Ah)

Byte 2

The second byte shall be used to identify the picture rate and the picture and transport structure.

Bit b7 shall be used to identify whether the digital interface uses a progressive or interlaced transport structure such that:

b7 = (0) identifies an interlaced transport

b7 = (1) identifies a progressive transport.

Bit b6 shall be used to identify whether the picture has a progressive or interlaced structure such that:

b6 = (0) identifies an interlaced structure

b6 = (1) identifies a progressive structure.

Bits b5 to b4 shall be set to (0).

Bits b3 to b0 shall be used to identify the picture rate in Hz.

(2h) shall identify 24/1.001 Hz

(3h) shall identify 24 Hz

(5h) shall identify 25 Hz

(6h) shall identify 30/1.001 Hz

(7h) shall identify 30 Hz.

Byte 3

The third byte shall be used to identify the aspect ratio and sampling structure of the video payload.

Bit b6 shall be used to identify horizontal pixel count:

(0) 1 920 pixels

(1) reserved.

Bit b5 shall be used to identify the image aspect ratio:

(0) image aspect ratio unknown

(1) 16:9 image aspect ratio

Bits b3 to b0 of byte 3 shall be used to identify the sampling structure.

(2h) shall identify4:4:4 *RGB*

(6h) shall identify 4:4:4:4 *RGB+A*

(Ah) shall identify 4:4:4:4 *RGB+D*

(1h) shall identify 4:4:4 Y, C_B, C_R

(0h) shall identify 4:2:2 Y, C_B, C_R

(4h) shall identify 4:2:2:4 Y, C_B, C_R+A

(8h) shall identify 4:2:2:4 Y, C_B, C_R+D.

Bits b7 and b4 shall be reserved and set to (0).

Byte 4

Bits b7 to b2 are reserved and set to (0).

Bits b1 and b0 shall be used to identify the bit depth:

(0h) shall identify 8 bits per sample

(1h) shall identify 10 bits per sample

(2h) shall identify 12 bits per sample.

Appendix 3
to Annex 1
(Informative)

Mapping of Recommendation ITU-R BT.709 Part 1 1 920 × 1 035 image format

In order to map legacy 1 035 active line active images onto the digital interface conforming to Recommendation ITU-R BT.1120 and maintain the centre of the picture to be consistent with 1 080 active line images the following mapping should be followed:

– Field 1 active lines should be mapped to interface line numbers 32-548;

– Field 2 active lines should be mapped to interface line numbers 596-1 113.

Annex 2

Bit-serial digital checkfield for use in the HDTV digital interfaces

1 Scope

This Annex specifies digital test signals suitable for evaluating the low-frequency response of equipment handling HDTV serial digital video signals. Although a range of signals will produce the desired low-frequency effects, two specific signals are defined to test cable equalization and PLL lock-in, respectively. In the past, these two signals have been colloquially called “pathological signals.”

2 General considerations

Stressing of the automatic equalizer is accomplished by using a signal with the maximum number of ones or zeros, with infrequent single clock period pulses to the opposite level. Stressing of the PLL is accomplished by using a signal with a maximum low-frequency content; that is, with a maximum time between level transitions.

2.1 Channel coding of the serial digital signal defined in this Recommendation utilizes scrambling and encoding into NRZI accomplished by a concatenation of the two following functions:

$$G1\,(x) = x^9 + x^4 + 1 \qquad\qquad G2\,(x) = x + 1$$

As a result of the channel coding, long runs of zeros in the *G*2 (*x*) output data can be obtained when the scrambler, *G*1 (*x*), is in a certain state at the time when the specific words arrive. That certain state will be present on a regular basis; therefore, continuous application of the specific data words will regularly produce the low-frequency effects.

2.2 Although the longest run of parallel data zeros (40 consecutive zeros) will occur during the EAV/SAV timing reference sequence (TRS) words, the frequency with which the scrambling of the TRS words coincide with the required scrambler state to permit either stressing condition is low. In the instances where this coincidence occurs, the generation of the stressing condition is so time limited that equalizers and PLLs are not maximally stressed.

2.3 In the data portions of digital video signals (excluding TRS words in EAVs or SAVs, and ANC data flag words), the sample values are restricted to exclude data levels $0_{(10)}$ to $3_{(10)}$ and $1\ 020_{(10)}$ to $1\ 023_{(10)}$ (000_h to 003_h and $3FC_h$ to $3FF_h$ in 10-bit hexadecimal representation, see Note 1). The result of this restriction is that the longest run of zeros, at the scrambler input, is 16 (bits), occurring when a sample value of $512_{(10)}$ (200_h) is followed by a value between $4_{(10)}$ (004_h) and $7_{(10)}$ (007_h). This situation can produce up to 26 consecutive zeros at the NRZI output, which is also not a maximally stressed case.

NOTE 1 – Within this Annex, the contents of 10-bit digital word are expressed in both decimal and hexadecimal form. For example, the bit pattern 1001000101 would be expressed as $581_{(10)}$ or 245_h.

2.4 Other specific data words in combination with specific scrambler states can produce a repetitive low-frequency serial output signal until the next EAV or SAV affects the scrambler state. It is these combinations of data words that form the basis of the test signals defined by this Annex.

2.5 Because of the *Y*/*C* interleaved nature of the component digital signal, it is possible to obtain nearly any permutation of word pair data values over the entire active picture area by defining a particular flat colour field in a noise-free environment. Certain of these permutations of word pair data values will produce the desired low-frequency effects.

3 Checkfield data

3.1 Receiver equalizer testing is accomplished by producing a serial digital signal with maximum d.c. content. Applying the sequence $768_{(10)}$ (300_h), $408_{(10)}$ (198_h) continuously to the *C* and *Y* samples (respectively) during the active line will produce a signal of 19 consecutive high (low) states followed by one low (high) state in a repetitive manner, once the scrambler attains the required starting condition. Either polarity of the signal can be realized, indicated by the level of the 19 consecutive states. By producing approximately half of a field of continuous lines containing this sequence, the required scrambler starting condition will be realized on several lines, and this will result in the generation of the desired equalizer testing condition.

3.2 Receiver PLL testing is accomplished by producing a serial digital signal with maximum low-frequency content and minimum high-frequency content (i.e., lowest frequency of level transitions). Applying the sequence $512_{(10)}$ (200_h), $272_{(10)}$ (110_h) continuously to the *C* and *Y* samples (respectively) during the active line will produce a signal of 20 consecutive high (low) states followed by 20 low (high) states in a repetitive manner, once the scrambler attains the required starting condition. By producing approximately half of a field of continuous lines containing this sequence, the required scrambler starting condition will be realized on several lines, and this will result in the generation of the desired PLL testing condition.

3.3 Because the equalizer test works by producing a serial digital signal with a bias, steps must be taken to ensure that both polarities of bias are realized. To change the polarity of the bias from one frame to the next, the sum total of all the bits in all the data words in all the lines in a video field must be odd.

To ensure that the polarity of the bias can change often, a single *Y* sample data word in the signal is changed from $480_{(10)}$ (198_h) to $400_{(10)}$ (190_h) (a net change of 1 data bit), once every other frame. This causes the bias polarity to alternate at a frame rate regardless of whether the original frame bit sum is even or odd. The data word in which the value substitution is made is the first *Y* sample in the first active picture line of every other frame. The specific word and line for each signal format is listed in Table 24 as the polarity control word.

3.4 The sequence $768_{(10)}$ (300_h), $408_{(10)}$ (198_h) and $512_{(10)}$ (200_h), $272_{(10)}$ (110_h) applied to *C* and *Y* samples results in shades of purple and gray, respectively. Reversing the *C* and *Y* ordering for each of these two sequences results in lighter and darker shades of green, respectively. Table 26 illustrates one ordering of each of the two sequences, but either ordering of the data values for each sequence is permitted by this Annex.

If the ordering described in § 3.1 is reversed, then the polarity control word described in § 3.3 is changed to $512_{(10)}$ (200_h). The polarity control word in either case is located at the first *Y* sample in the first active picture line in the field(s) specified in § 3.3.

4 Serial digital interface (SDI) checkfield

Distribution of data in the SDI checkfield is shown in Fig. 16 for the signal standards. Specific distributions of sample values are shown in Table 26 In each field, the line where the signal transitions from the equalizer test signal data pattern to the PLL test signal data pattern is specified, is given as a range of lines, rather than as a single specific line. Although the specific line selected within the specified range is not technically significant, the transition point should be consistent from frame-to-frame and from field-to-field (in the case of interlaced signal formats).

TABLE 26

SDI checkfield sample values

<table>
<tr><th colspan="2">System</th><th>60/I, 30/PsF, 50/I, 25/PsF, 24/PsF</th><th>60/P, 30/P, 50/P, 25/P, 24/P</th></tr>
<tr><td colspan="2">Number of active Y samples per line</td><td colspan="2">1 920</td></tr>
<tr><td colspan="2">Number of active lines</td><td colspan="2">1 080</td></tr>
<tr><td rowspan="11">Equalizer test signal</td><td rowspan="2">First line</td><td>21 (field/segment 1)</td><td rowspan="2">42</td></tr>
<tr><td>584 (field/segment 2)</td></tr>
<tr><td rowspan="2">Last line (range)</td><td>287-293 (field/segment 1)</td><td rowspan="2">578-585</td></tr>
<tr><td>850-856 (field/segment 2)</td></tr>
<tr><td>Data values[(1)]</td><td colspan="2">Samples</td></tr>
<tr><td>$768_{(10)}$ C_B</td><td colspan="2">0 ... 3 836</td></tr>
<tr><td>$408_{(10)}$ Y</td><td colspan="2">1 ... 3 837</td></tr>
<tr><td>$768_{(10)}$ C_R</td><td colspan="2">2 ... 3 838</td></tr>
<tr><td>$408_{(10)}$ Y</td><td colspan="2">3 ... 3 839</td></tr>
<tr><td>Polarity control word</td><td colspan="2">(Every other frame)</td></tr>
</table>

	Data value[1],[2] $400_{(10)}\ Y$	Line 21 Sample 1	Line 42 Sample 1

TABLE 26 (*end*)

System		**60/I, 30/PsF, 50/I, 25/PsF, 24/PsF**	**60/P, 30/P, 50/P, 25/P, 24/P**
PLL test signal	First line (range)[3]	288-294 (field/segment 1)	579-586
		851-857 (field/segment 2)	
	Last line	560 (field/segment 1)	1121
		1 123 (field/segment 2)	
	Data values[1]	Samples	
	$512_{(10)}\ C_B$	0 ... 3 836	
	$272_{(10)}\ Y$	1 ... 3 837	
	$512_{(10)}\ C_R$	2 ... 3 838	
	$272_{(10)}\ Y$	3 ... 3 839	

(1) The ordering of data values for each of the pairs of sample values may be reversed. If the ordering of the samples is reversed from the ordering in this Table, then the polarity control word value is ($512_{(10)}\ Y$) (see § 3.4).

(2) The polarity change word is a substitution of the first active picture area *Y* sample, made in the first active picture line of every other frame (see § 3.3).

(3) A range of line numbers for transitioning between the two test patterns is provided. The transition point within these ranges must be consistent across all fields (see § 4).

FIGURE 17

SDI checkfield

	Vertical blanking interval
EAV SAV	First line of active picture 1st half of active field $768_{(10)}$, $408_{(10)}$ for equalizer testing [1]
Horizontal blanking interval	2nd half of active field $512_{(10)}$, $272_{(10)}$ for PLL testing [1] Last line of active picture

(1) The ordering of data values for each of the pairs of sample values may be reversed (see § 3.4)