RECOMMENDATION ITU-R BT.1303*

Interfaces for digital component video signals in 525-line and 625-line television systems operating at the 4:4:4 level of Recommendation ITU-R BT.601 (Part B)

(Question ITU-R 42/6)

(1997)

The ITU Radiocommunication Assembly,

considering

a) that there are clear advantages for television broadcasting organizations and programme producers in digital studio standards which have the greatest number of significant parameter values common to 525-line and 625-line systems;

b) that the worldwide compatible digital approach will permit the development of equipment with many common features, permit operating economies and facilitate the international exchange of programmes;

c) that in implementing the above objectives, agreement has been reached on the fundamental encoding parameters of digital television for studios in the form of Recommendation ITU-R BT.601 (Part B);

d) that the practical implementation of Recommendation ITU-R BT.601 (Part B) for complex digital studio processes requires definition of details of interfaces at the 4:4:4 level and the data streams traversing them;

e) that such interfaces should have a maximum of commonality between 525-line and 625-line versions;

f) that it is desirable that interfaces be defined in both serial and parallel forms,

recommends

that where interfaces for the 4:4:4 level are required for component-coded digital video signals conforming to Recommendation ITU-R BT.601 (Part B) in television studios, the interfaces and the data streams that will traverse them should be in accordance with the following description, defining both bit-parallel and bit-serial implementations.

1 Introduction

This Recommendation describes the means of interconnecting digital television equipment operating on the 525-line or 625-line standards and complying with the 4:4:4 encoding parameters as defined in Recommendation ITU-R BT.601 (Part B).

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* Radiocommunication Study Group 6 made editorial amendments to this Recommendation in 2003 in accordance with Resolution ITU-R 44.

Part 1 describes the signal format common to both interfaces.

Part 2 describes the particular characteristics of the bit-parallel interface.

Part 3 describes the particular characteristics of the bit-serial interface.

Supplementary information is to be found in Annex 1.

The interfaces for the 4:4:4 level are based on the use of parallel and serial interfaces developed for use at the 4:2:2 level and described in Recommendation ITU-R BT.1302. Whereas at the 4:2:2 level a single interface carries a multiplex of a wideband luminance and two lower-bandwidth colour-difference video signals, at the 4:4:4 level a pair of interfaces is used, each carrying a multiplex of two wideband video signals; this gives capacity for carrying the green, blue and red primary signals or, alternatively, the luminance and two colour-difference signals, together with a fourth wideband signal such as an associated key signal. In this case the signal is at the 4:4:4:4 level.

The interfaces for the 4:4:4 level have been specified for 10-bit data words (see Note 1): thus they will carry not only 8-bit signals encoded according to Recommendation ITU-R BT.601 (Part B) but also 10-bit signals where additional bits may have been generated during signal processing.

Only two devices will be connected together at one time through one interface.

NOTE 1 – Within this Recommendation, the contents of digital words are expressed in both decimal and hexadecimal form. To avoid confusion between 8-bit and 10-bit representations, the 8 most significant bits (MSBs) are considered to be an integer part while the 2 additional bits, if present, are considered to be fractional parts.

For example, the bit pattern 10010001 would be expressed as 145_d or 91_h, whereas the pattern 1001000101 is expressed as 145.25_d or 91.4_h.

Where no fractional part is shown, it should be assumed to have the binary value 00.

PART 1

Common signal format of the interfaces

1 Introduction

The interface consists of two unidirectional interconnections between one device and another. The interconnections carry the data corresponding to the television signal and associated data.

The two interconnections are referred to as: link A and link B.

The data signals are carried in the form of binary information coded in ten-bit words. These signals are:

– the video signals themselves,

– digital blanking data,

– timing reference signals,

– ancillary data signals.

These signals are time-multiplexed.

2 Video data signals

2.1 Coding characteristics

The video data signals are derived by coding of the analogue video signal components in accordance with the 4:4:4 level of Recommendation ITU-R BT.601 (Part B), with the field-blanking definition shown in Table 1.

2.2 Video data format

Eight-bit data words resulting from sampling according to Recommendation ITU-R BT.601 (Part B) are carried in the 8 MSBs of the 10-bit interface signal. In this case the remaining least significant bits (LSBs) should be set to zero.

Words in which the 8 MSBs are all set to 1 or are all set to 0 (i.e. 1111 1111 xx or 0000 0000 xx, where xx represents bits which are either absent – the 8-bit case – or can have any value) are reserved for identification purposes. The corresponding data values are excluded from the data coding range.

2.3 Multiplex structure

The video data words are conveyed in two separate 36 Mword/s data-streams.

The multiplex sequence is:

– for links carrying colour primaries

link A: $..B_0\ G_0\ R_0\ G_1\ B_2\ G_2\ R_2\ G_3\ B_4...$

link B: $..B_1\ K_0\ R_1\ K_1\ B_3\ K_2\ R_3\ K_3\ B_5...$

where R, G, B and K represent the red, green and blue signal data words, and K represents the key signal data words, if present. The first sample of the digital active line shall be B_0 for link A and B_1 for link B.

The distribution of the red, green, blue and key signals between link A and link B is shown in Fig. 1a).

– for links carrying luminance and colour-difference signals

link A: $..C_B0\ Y_0\ C_R0\ Y_1\ C_B2\ Y_2\ C_R2...$

link B: $..C_B1\ K_0\ C_R1\ K_1\ C_B3\ K_2\ C_R3...$

where Y, C_B and C_R represent the luminance and colour-difference signals respectively, and K represents the key signal data words, if present. The first sample of the digital active line shall be C_B0 for link A and C_B1 for link B. The distribution of the luminance, colour-difference and key signals between link A and link B is shown in Fig 1b).

TABLE 1

Field interval definitions

		625	525
V – digital field blanking			
Field 1	Start (V = 1)	Line 624	Line 1
	Finish (V = 0)	Line 23	Line 20
Field 2	Start (V = 1)	Line 311	Line 264
	Finish (V = 0)	Line 336	Line 283
F – digital field identification			
Field 1	F = 0	Line 1	Line 4
Field 2	F = 1	Line 313	Line 266

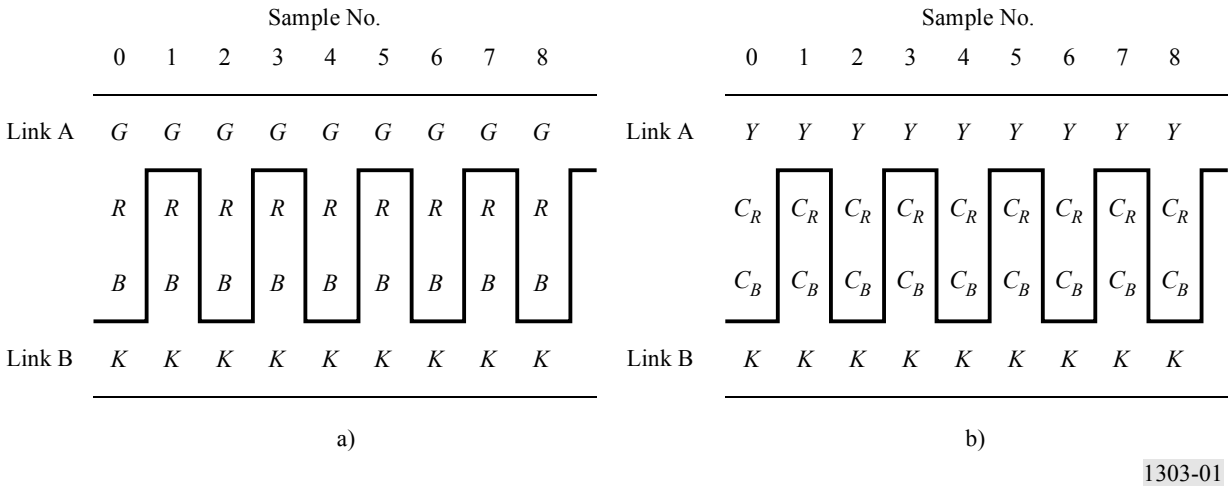
NOTE 1 – Signals F and V change state synchronously with the end of active video timing reference code at the beginning of the digital line.

NOTE 2 – Definition of line numbers is to be found in Recommendation ITU-R BT.470. Note that digital line number changes state prior to O_H as described in Recommendation ITU-R BT.601 (Part B).

NOTE 3 – Designers should be aware that the "1" to "0" transition of the V-bit may not necessarily occur on line 20 (283) in some equipment conforming to previous versions of the Recommendation ITU-R BT.656 for 525 line signals.

FIGURE 1

Link contents when used for *R, G, B, K* and *Y*, C_R, C_B, *K* signals



2.4 Interface signal structure

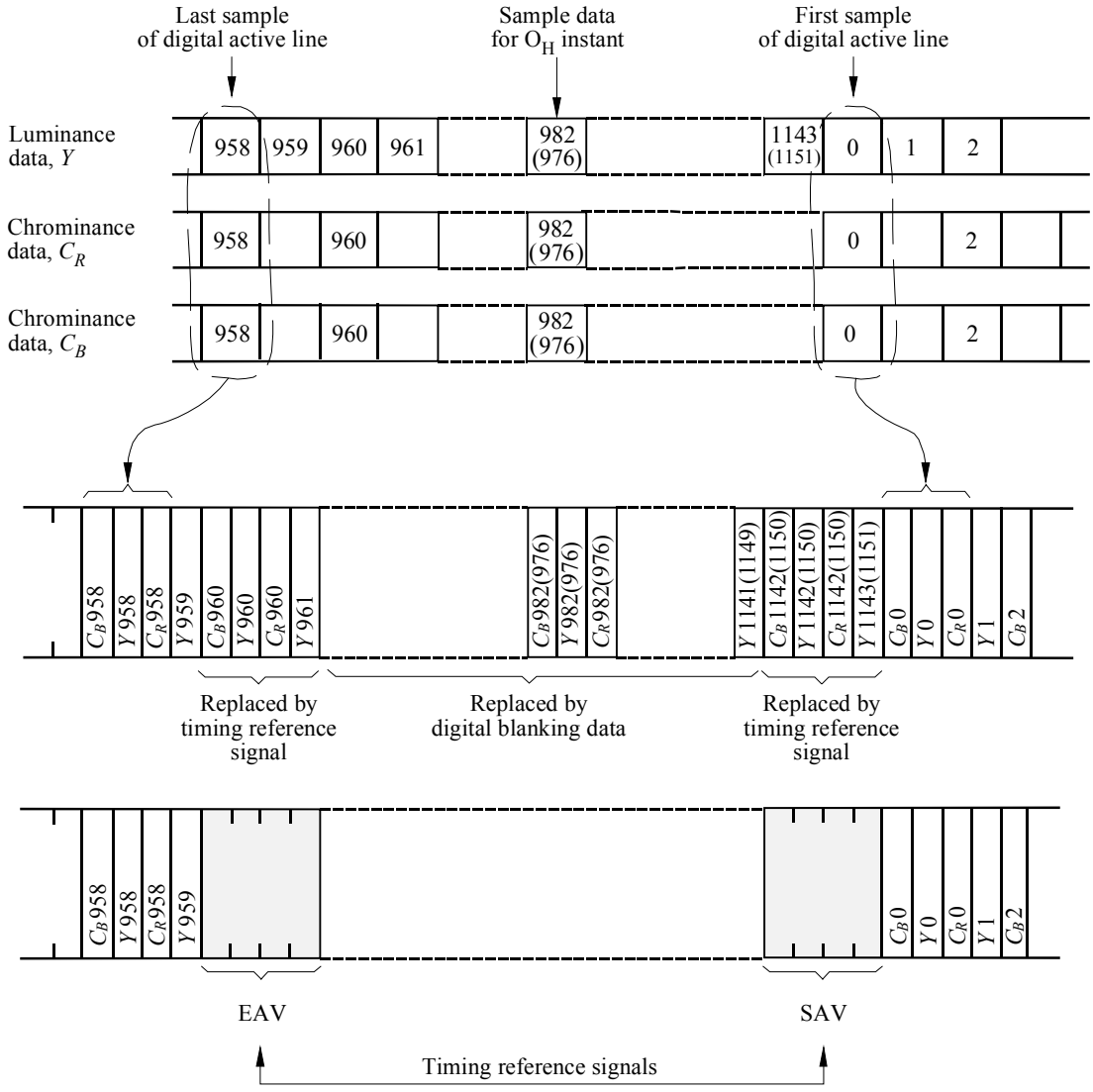
Figure 2 shows the ways in which the video sample data is incorporated in the interface data stream. Sample identification in Fig. 2 is in accordance with the identification in Recommendation ITU-R BT.601 (Part B).

2.5 Video timing reference signals (SAV, EAV)

There are two timing reference signals, one at the beginning of each video data block (start of active video, SAV) and one at the end of each video data block (end of active video, EAV) as shown in Fig 2.

FIGURE 2

Composition of the data multiplex and position of the timing reference signals, EAV and SAV (shown here for link A carrying *Y*, C_R, C_B as an example)



Note 1 – Sample identification numbers in parentheses are for 625-line systems where these differ from those for 525-line systems. (See also Recommendation ITU-R BT.803.)

1303-02

Each timing reference signal consists of a four word sequence in the following format: FF 00 00 XY. (Values are expressed in hexadecimal notation. Words FF 00 are reserved for use in timing reference signals.) The first three words are a fixed preamble. The fourth word contains information defined field 2 identification, the state of field blanking, and the state of line blanking. The assignment of bits within the timing reference signal is shown below in Table 2.

TABLE 2

Video timing reference signal

Data bit number	First word (FF)	Second word (00)	Third word (00)	Fourth word (XY)
9 (MSB)	1	0	0	1
8	1	0	0	F
7	1	0	0	V
6	1	0	0	H
5	1	0	0	P_3
4	1	0	0	P_2
3	1	0	0	P_1
2	1	0	0	P_0
1 (Note 2)	1	0	0	0
0	1	0	0	0

NOTE 1 – The values shown are those recommended for 10-bit interfaces.

NOTE 2 – For compatibility with existing 8-bit interfaces, the values of bits D_1 and D_0 are not defined.

F = 0 during field 1
1 during field 2

V = 0 elsewhere
1 during field blanking 2

H = 0 in SAV
1 in EAV

P_0, P_1, P_2, P_3: protection bits (see Table 3).

Table 1 defines the state of the V and F bits.

Bits P_0, P_1, P_2, P_3, have states dependent on the states of the bits F, V and H as shown in Table 3. At the receiver this arrangement permits one-bit errors to be corrected and 2-bit errors to be detected.

TABLE 3

Protection bits in the timing reference signal

F	V	H	P_3	P_2	P_1	P_0
0	0	0	0	0	0	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	1	0
1	1	0	1	1	0	0
1	1	1	0	0	0	1

2.6 Ancillary data

The ancillary signals should comply with Recommendation ITU-R BT.1364.

2.7 Data words during blanking

During digital blanking the luminance or *R*, *G*, *B* sample values should be set to black, level 10.0_h, and the colour-difference samples set to zero, level 80.0_h. The key samples should be set to peak white, level $EB.0_h$, when not carrying a key signal.

PART 2

Bit-parallel interface

1 General

The 10-bit video data for each link is transferred across the interfaces on ten parallel data pairs together with a clock signal on an eleventh pair.

The signals on the interface are transmitted using balanced conductor pairs. Cable lengths of up to 40 m (≃130 feet) without equalization and up to 160 m (≃520 feet) with appropriate equalization may be employed.

Each interconnection employs a twenty-five pin D-subminiature connector equipped with a locking mechanism (see § 5).

Video data is transmitted in NRZ form in real time (unbuffered) in blocks, each comprising one active television line.

2 Data signal format

The interface carries data in the form of 10 parallel data bits and a separate synchronous clock. Data is coded in NRZ form. The recommended data format is described in Part 1.

3 Link-to-link timing relationship (see Note 1)

The clock transitions for the two links shall lie within 10 ns of each other at the receiver.

NOTE 1 – Where the data receiver incorporates buffering to achieve synchronism between incoming data and an internal reference or between sets of incoming data, this tolerance can be relaxed. However, it is anticipated that a common clock will be used in the sending equipment for both links, so that achieving this tolerance should present little difficulty.

4 Clock signal

4.1 General

The clock signal is a 36 MHz square wave where the 0-1 transition represents the data transfer time. This signal has the following characteristics:

Width: 13.9 ± 2 ns

Jitter: less than 2 ns from the average period over one field.

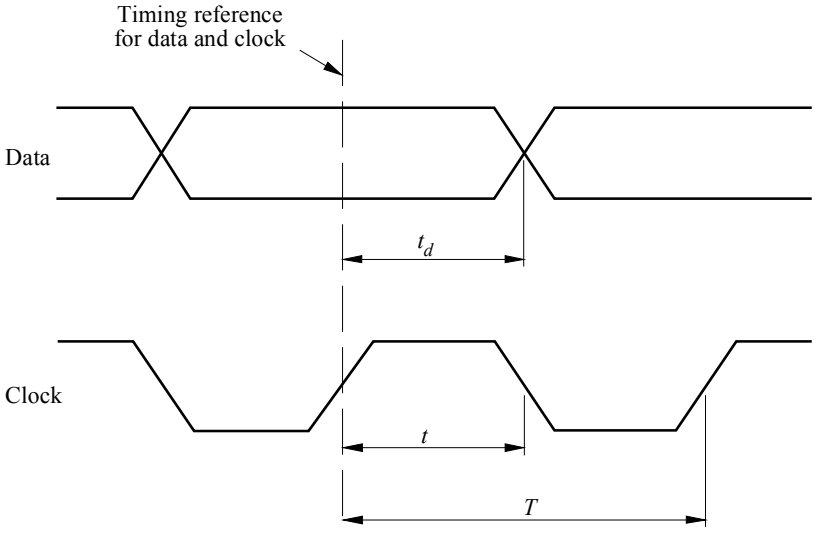
NOTE 1 – This jitter specification, while appropriate for an effective parallel interface, is not suitable for clocking digital to analogue conversion or parallel to serial conversion.

4.2 Clock-to-data timing relationship

The positive transition of the clock shall occur midway between data transitions as shown in Fig. 3.

FIGURE 3

Clock-to-data timing (at source)



Clock period (625): $T = \frac{1}{2\,304 f_H} = 27.8$ ns

Clock period (525): $T = \frac{1}{2\,288 f_H} = 27.8$ ns

Clock pulse width: $t = 13.9 \pm 2$ ns

Data timing – sending end: $t_d = 13.9 \pm 2$ ns

f_H: line frequency

1303-03

5 Electrical characteristics of the interface

5.1 General

Each line driver (source) has a balanced output and the corresponding line receiver (destination) a balanced input (see Fig. 4).

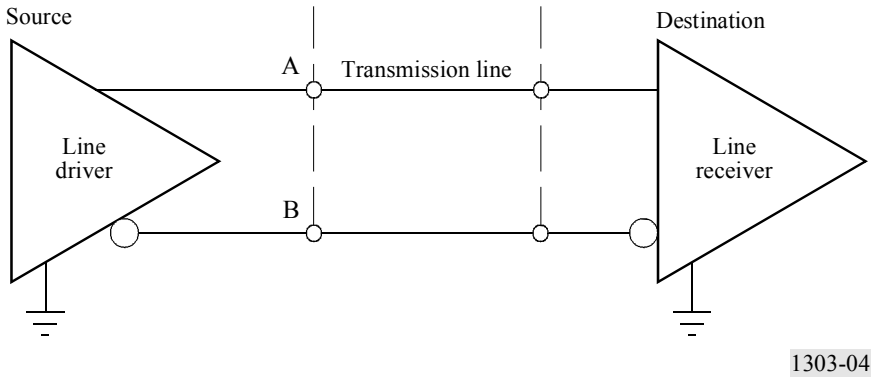
Although the use of an emitter-coupled logic (ECL) technology is not specified, the line driver and receiver must be ECL-compatible, i.e. they must permit the use of ECL for either drivers or receivers.

All digital signal time intervals are measured between the half-amplitude points.

5.2 Logic convention

The A terminal of the line driver is positive with respect to the B terminal for a binary 1 and negative for a binary 0 (see Fig. 4).

FIGURE 4
Line driver and line receiver interconnection



5.3 Line driver characteristics (source)

5.3.1 Output impedance: 110 Ω maximum.

5.3.2 Common mode voltage: −1.29 V ± 15% (both terminals relative to ground).

5.3.3 Signal amplitude: 0.8 to 2.0 V peak-to-peak, measured across a 110 Ω resistive load.

5.3.4 Rise and fall times: less than 5 ns, measured between the 20% and 80% amplitude points, with a 110 Ω resistive load. The difference between rise and fall times must not exceed 2 ns.

5.4 Line receiver characteristics (destination)

5.4.1 Input impedance: 110 Ω ± 10 Ω.

5.4.2 Maximum input signal: 2.0 V peak-to-peak.

5.4.3 Minimum input signal: 185 mV peak-to-peak.

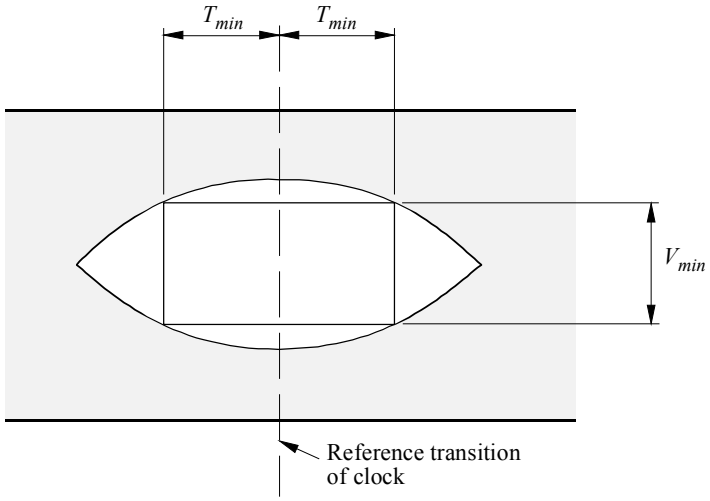
However, the line receiver must sense correctly the binary data when a random data signal produces the conditions represented by the eye diagram in Fig. 5 at the data detection point.

5.4.4 Maximum common mode signal: ±0.5 V, comprising interference in the range 0 to 15 kHz (both terminals to ground).

5.4.5 Differential delay: Data must be correctly sensed when the clock-to-data differential delay is in the range between ± 7 ns (see Fig. 5).

FIGURE 5

Idealized eye diagram corresponding to the minimum input signal level



T_{min} = 7 ns
V_{min} = 100 mV

Note 1 – The width of the window in the eye diagram, within which data must be correctly detected comprises ± 2 ns clock jitter, ± 2 ns data timing (see § 4.2), ± 4 ns available for differences in delay between pairs of the cable. (See also Recommendation ITU-R BT.803.)

1303-05

6 Mechanical details of the connectors

The interface uses the 25 contact type D subminiature connector specified in the International Organization for Standardization (ISO) Doc. 2110-1980, with the contact assignment shown in Table 4.

Connectors are locked together by two UNC 4-40 screws on the cable connectors, which go in female screw locks mounted on the equipment connector.

Cable connectors employ pin contacts and equipment connectors employ socket contacts. Shielding of the interconnecting cable and its connectors must be employed.

TABLE 4

Contact assignments

Contact	Signal line
1	Clock
2	System ground A
3	Data 9 (MSB)
4	Data 8
5	Data 7
6	Data 6
7	Data 5
8	Data 4
9	Data 3
10	Data 2
11	Data 1
12	Data 0
13	Cable shield
14	Clock return
15	System ground B
16	Data 9 return
17	Data 8 return
18	Data 7 return
19	Data 6 return
20	Data 5 return
21	Data 4 return
22	Data 3 return
23	Data 2 return
24	Data 1 return
25	Data 0 return

NOTE 1 – The cable shield (contact 13) is for the purpose of controlling electromagnetic radiation from the cable. It is recommended that contact 13 should provide high-frequency continuity to the chassis ground at both ends and, in addition, provide d.c. continuity to the chassis ground at the sending end (see also Recommendation ITU-R BT.803).

PART 3

Bit-serial interface

1 General

The multiplexed data stream of 10-bit words (as described in Part 1) is transmitted over a single channel in bit-serial form. Prior to transmission, additional coding takes place to provide spectral shaping, word synchronization and to facilitate clock recovery.

The 10-bit data for each link is transferred across the interface as a serial data-stream in unbalanced form and at an impedance of 75 Ω.

2 Link-to-link timing relationship (see Note 1)

The interface must operate correctly when the electrical lengths of the two interconnections between line sender and receiver differ by up to 10 ns.

NOTE 1 – Where the data receiver incorporates buffering to achieve synchronism between incoming data and an internal reference or between sets of incoming data, this tolerance can be relaxed. However, it is anticipated that a common clock will be used in the sending equipment for both links, so that achieving this tolerance should present little difficulty.

3 Coding

The uncoded serial bit-stream is scrambled using the generator polynomial $G1(x) \cdot G2(x)$, where:

$G1(x) = x^9 + x^4 + 1$ to produce a scrambled NRZ signal, and

$G2(x) = x + 1$ to produce a polarity-free NRZI sequence.

4 Order of transmission

The LSB of each 10-bit word shall be transmitted first.

5 Logic convention

The signal is transmitted in NRZI form, for which the bit polarity is irrelevant.

6 Transmission medium

The bit-serial data-stream can be conveyed using either a coaxial cable (see § 7) or fibre optic bearer (see § 8).

7 Characteristics of the electrical interface

7.1 Line driver characteristics (source)

7.1.1 Output impedance

The line driver has an unbalanced output with a source impedance of 75 Ω and a return loss of at least 15 dB over a frequency range of 5-360 MHz.

7.1.2 Signal amplitude

The peak-to-peak signal amplitude lies between 800 mV ± 10% measured across a 75 Ω resistive load directly connected to the output terminals without any transmission line.

7.1.3 DC offset

The DC offset with reference to the mid amplitude point of the signal lies between +0.5 and −0.5V.

7.1.4 Rise and fall times

The rise and fall times, determined between the 20% and 80% amplitude points and measured across a 75 Ω resistive load connected directly to the output terminals, shall lie between 0.75 and 1.50 ns and shall not differ by more than 0.50 ns.

7.1.5 Jitter (see Note 1)

The timing of the rising edges of the data signal shall be between ±10% of the clock period, as determined over a period of one line.

NOTE 1 – Parameters defined in § 7.1.5, 7.2.2 and 7.2.3 are target values and may be refined in the future with regard to practical implementations of the system.

7.2 Line receiver characteristics (destination)

7.2.1 Terminating impedance

The cable is terminated by 75 Ω with a return loss of at least 15 dB over a frequency range of 5 to 360 MHz.

7.2.2 Receiver sensitivity (see Note 1, § 7.1.5)

The line receiver must sense correctly random binary data either when connected directly to a line driver operating at the extreme voltage limits permitted by § 7.1.2, or when connected via a cable having a loss of 40 dB at 360 MHz and a loss characteristic of $1/\sqrt{f}$.

7.2.3 Interference rejection (see Note 1, § 7.1.5)

When connected directly to a line driver operating at the lower limit specified in § 7.1.2, the line receiver must correctly sense the binary data in the presence of a superimposed interfering signal at the following levels:

d.c.:	±2.5 V
below 1 kHz:	2.5 V peak-to-peak
1 kHz to 5 MHz:	100 mV peak-to-peak
Above 5 MHz:	40 mV peak-to-peak.

7.3 Cables and connectors

7.3.1 Cable

It is recommended that the cable chosen should meet any relevant national standards on electromagnetic radiation.

7.3.2 Characteristic impedance

The cable used shall have a nominal characteristic impedance of 75 Ω.

7.3.3 Connector characteristics

The connector shall have mechanical characteristics conforming to the standard BNC type (International Electrotechnical Commission (IEC) Publication 169-8 (1978)), and its electrical characteristics should permit it to be used at frequencies up to 850 MHz in 75 Ω circuits.

8 Characteristics of the optical interface

Specifications for the characteristics of the optical interface should comply with the general rules of Recommendation ITU-R BT.1367.

To make use of this Recommendation the following specifications are necessary

Rise and fall times: < 1.5 ns (20% to 80%)

Output jitter (see Note 1): f_1 = 10 Hz

f_3 = 100 kHz

f_4 = 1/10 of the clock rate

A1 = 0.135 UI (UI: unit interval)

A2 = 0.135 UI.

Input jitter needs to be defined. Input jitter is measured with a short cable (2 m).

NOTE 1 – Specification of jitter and jitter measurements methods shall comply with Recommendation ITU-R BT.1363.

Annex 1

Notes concerning interfaces for digital video signals in 525-line and 625-line television systems

1 Introduction

This Annex includes supplementary information on subjects not yet fully specified, and indicates studies in which further work is required.

2 Definitions

Interface is a concept involving the specification of the interconnection between two items of equipment or systems. The specification includes the type, quantity and function of the interconnection circuits and the type and form of the signals to be interchanged by these circuits.

A parallel interface is an interface in which the bits of a data word are sent simultaneously *via* separate channels.

A serial interface is an interface in which the bits of a data word, and successive data words, are sent consecutively *via* a single channel.

3 Parallel interfaces

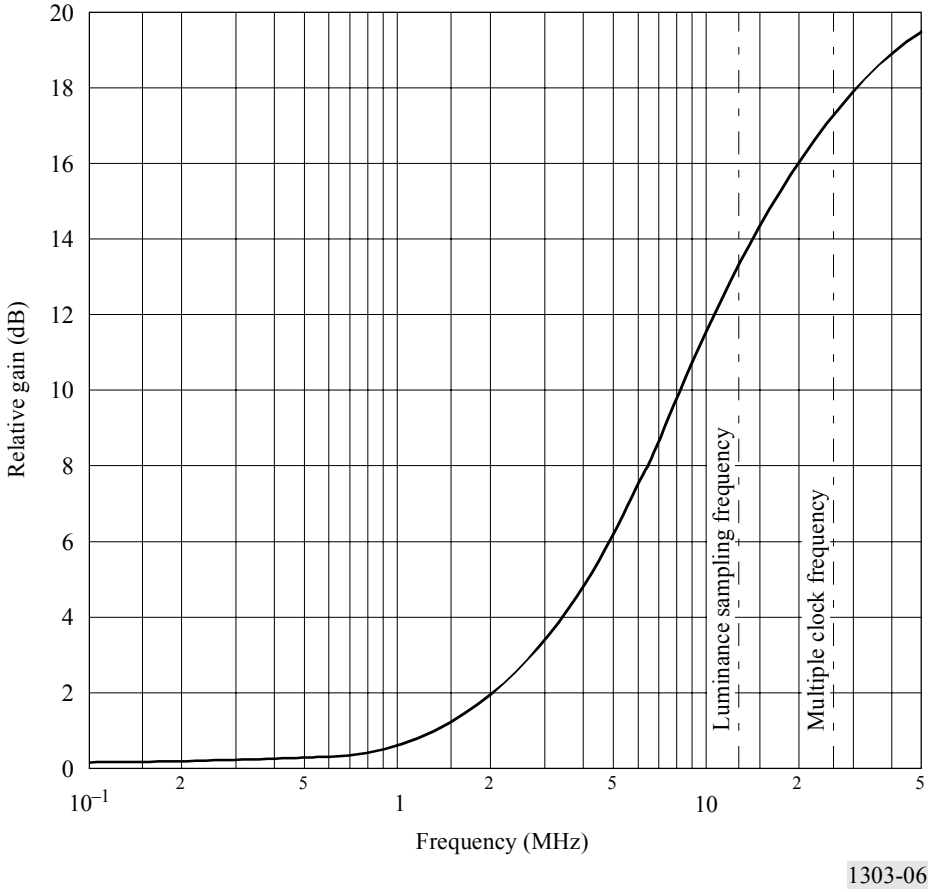
Appropriate coding of the clock signal, such as the use of an alternating parity coding, has been shown to extend the interconnection distance by reducing the effects of cable attenuation.

To permit correct operation with longer interconnection links, the line receiver may incorporate equalization.

When equalization is used, it may conform to the nominal characteristics of Fig. 6. This characteristic permits operation with a range of cable lengths down to zero. The line receiver must satisfy the maximum input signal condition of § 5.4 of Part 2.

FIGURE 6

Line receiver equalization characteristic for small signals



4 Serial interfaces

The transmission of signals can be achieved in both electrical form, using coaxial cable, and in optical form using an optical fibre. Coaxial cables would probably be preferred for connections of medium length, while preference would go to optical fibres for very long connection lengths.

It is possible to implement a system for detection of the occurrence of errors at the receiving end of the connection and thus automatically monitoring its performance.

In a fully integrated digital installation or system it may be useful for all interconnections to be transparent to any appropriate digital stream, irrespective of the message content. Thus, although the interface will be used to transmit a video signal, it should be "transparent" to the message content, i.e. it should not base its operation on the known structure of the message itself.

"Development work is ongoing on the subject of serial interfaces. In the context of the European RACE projects, for example, fibre optic routing systems which can accept a variety of input formats are assembled as part of a pilot installation."

5 Interference with other services

Processing and transmission of digital data, such as digital video signals at high data rates produces a wide spectrum of energy that has the potential to cause cross-talk or interference. In designing cables and interfaces, manufacturers should have due regard for correct shielding and interference minimization practice. Annex 2 of Recommendation ITU-R BT.803 provides general guidance on this subject.

Transmission by optical fibres eliminates radiation generated by the cable and also prevents conducted common-mode radiation, but the performance of coaxial cable can also be made near-perfect. It is believed that the major portion of any radiation would be from the processing logic and high-power drivers common to both methods. Due to the wideband, random nature of the digital signal, little is gained by frequency optimization.

6 Conclusion

Further studies are required on the practical methods required to ensure acceptably low levels of radiated interference from the digital signals.