RECOMMENDATION ITU-R BT.1363

JITTER SPECIFICATIONS AND METHODS FOR JITTER MEASUREMENTS OF BIT-SERIAL SIGNALS CONFORMING TO RECOMMENDATIONS ITU-R BT.656, ITU-R BT.799 AND ITU-R BT.1120

(Question ITU-R 65/11)

(1998)

The ITU Radiocommunication Assembly,

considering

a) that many countries are installing digital television production facilities based on the use of serial digital video components conforming to Recommendations ITU-R BT.656, ITU-R BT.799 or ITU-R BT.1120;

b) that in order to guarantee the operation of such serial digital interfaces specification of jitter parameters and methods to measure jitter is required;

c) that to implement the above objectives, agreement needs to be achieved in specifying and measuring jitter in bit-serial interfaces conforming to Recommendations ITU-R BT.656, ITU-R BT.799 and ITU-R BT.1120;

d) that the implementation of optical interface for the transmission of signals conforming to draft new Recommendation ITU-R BT.1367 requires the specification of jitter parameters and methods to measure jitter,

recommends

that where interfaces conforming to Recommendations ITU-R BT.656, ITU-R BT.799 and ITU-R BT.1120 are implemented, the jitter should be specified and methods of measuring jitter should be in accordance with the provisions included in Annex 1.

NOTE – Additional information on jitter specification and measuring methods can be found in EBU Tech. 3268.

ANNEX 1

Jitter specifications

1 Scope

This Recommendation describes techniques for specifying jitter in self-clocking, bit-serial digital systems. It is applicable to sources, receivers, and regenerators.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this practice. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this practice are encouraged to investigate the possibility of applying the most recent edition of the standards indicated below.

3 Definitions

3.1 **alignment jitter:** The variation in position of a signal's transitions relative to those of a clock extracted from that signal. The bandwidth of the clock extraction process determines the low-frequency limit for alignment jitter.

3.2 **input jitter tolerance**: Peak-to-peak amplitude of sinusoidal jitter that, when applied to an equipment input, causes a specified degradation of error performance.

3.3 **intrinsic jitter:** Jitter at an equipment output in the absence of input jitter.

3.4 **jitter:** The variation of a digital signal's transitions from their ideal positions in time.

3.5 **jitter transfer:** Jitter on the output of equipment resulting from applied input jitter.

3.6 **jitter transfer function:** Ratio of the output jitter to the applied input jitter as a function of frequency.

3.7 **output jitter:** Jitter at the output of equipment that is embedded in a system or network. It consists of intrinsic jitter and the jitter transfer of jitter at the equipment input.

3.8 **timing jitter:** The variation in position of a signal's transitions occurring at a rate greater than a specified frequency, typically 10 Hz or less. Variations occurring below this specified frequency are termed wander and are not addressed by this practice.

3.9 **unit interval (UI):** Abbreviated UI, it is the period of one clock cycle. It corresponds to the nominal minimum time between transitions of the serial signal.

4 Jitter specifications

Equipment jitter specifications fall into three categories: input jitter tolerance, jitter transfer, and intrinsic jitter. A fourth specification, output jitter, is a network specification and may be used to specify jitter limits at equipment interfaces.

4.1 Input jitter tolerance

Input jitter tolerance is the peak-to-peak amplitude of sinusoidal jitter that, when applied to an equipment input, causes a specified degradation of error performance. Input jitter tolerance is applicable to most serial inputs.

4.1.1 Input jitter tolerance requirements are specified with a jitter template that covers a specified sinusoidal amplitude frequency region (see Figure 1). This template represents the minimum amount of jitter that the equipment must accept without causing the specified degradation of error performance. Equipment meeting a jitter tolerance requirement must have an actual jitter tolerance greater than the requirement (see Figure 2).

4.1.2 Input jitter tolerance requirements are specified with the parameters given in Table 1.

4.1.2.1 Frequency band f_1 to f_2 forms the low-frequency jitter tolerance bandpass. At least A_1 UI of peak-to-peak sinusoidal jitter shall be tolerated over this bandpass without exceeding the specified error criterion.

4.1.2.2 Frequency band f_3 to f_4 forms the high-frequency jitter tolerance bandpass. At least A_2 UI of peak-to-peak sinusoidal jitter shall be tolerated over this bandpass without exceeding the specified error criterion.

4.1.2.3 A_1 and A_2 shall be specified in UI.

4.1.2.4 The slope of the jitter tolerance requirement between f_2 and f_3 shall be 20 dB/decade. Frequencies f_2 and f_3 are related as follows: $f_2 = f_3/(A_1/A_2)$.

4.1.2.5 The criterion for reaching the onset of errors shall be specified. Either a BER limit or a maximum number of errored seconds over a specified measurement interval should be used.

4.1.2.6 The test signal used for the measurement (to which sinusoidal jitter is added) shall be specified.

4.1.3 Numerical input jitter tolerance values are provided in the appropriate SMPTE standards which reference this practice. The terminology shall comply with 4.1.2.

4.2 Jitter transfer

Jitter transfer is jitter on the output of equipment resulting from applied input jitter. Jitter transfer is applicable to a device which produces a serial output from a serial input, such as a regenerator.

Jitter transfer can also occur from reference signals applied to equipment, such as analogue black burst. The jitter transfer templates described below are intended for serial input to serial output jitter transfer.

4.2.1 Jitter transfer requirements are specified with a template showing the maximum jitter gain as a function of frequency (see Figure 3). Equipment meeting a jitter transfer requirement will have a jitter transfer function that lies *within* this template (see Figure 4).

TABLE 1

Input jitter tolerance

Parameters	Units	Description
Data rate	bits/s)	(Serial bit rate)
f_1	(Hz)	(Low-frequency specification limit)
f_2	(Hz)	(Upper band edge for A_1, low-frequency jitter tolerance)
f_3	(Hz)	(Lower band edge for A_2, high-frequency jitter tolerance)
f_4	(Hz)	(High-frequency specification limit)
A_1	(UI)	(Low-frequency jitter tolerance, f_1 to f_2)
A_2	(UI)	(High-frequency jitter tolerance, f_3 to f_4)
Error criterion		(Criterion for onset of errors)
Test signal		(Test signal used for measurement)

FIGURE 1

Input jitter tolerance template

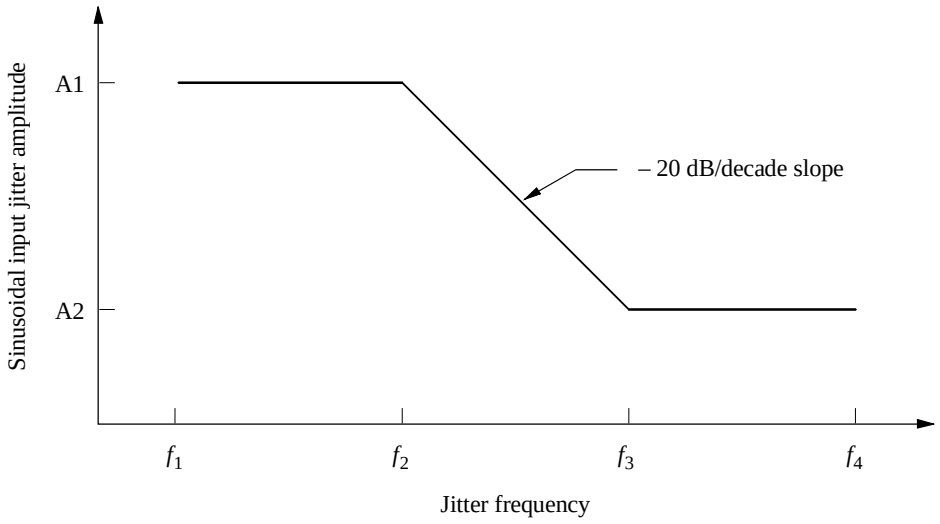


FIGURE 2

Jitter tolerance specification and a compliant jitter tolerance

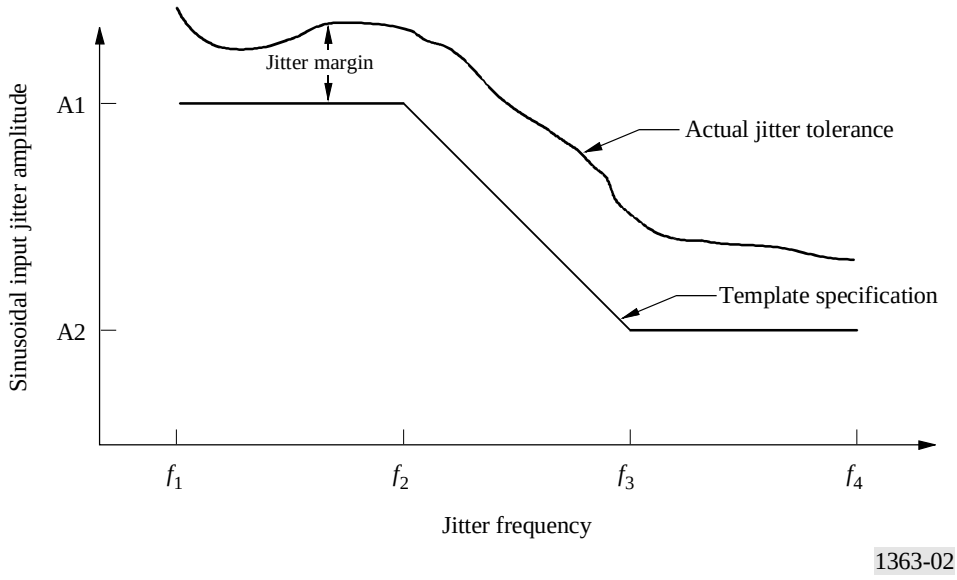


FIGURE 3

Jitter transfer template

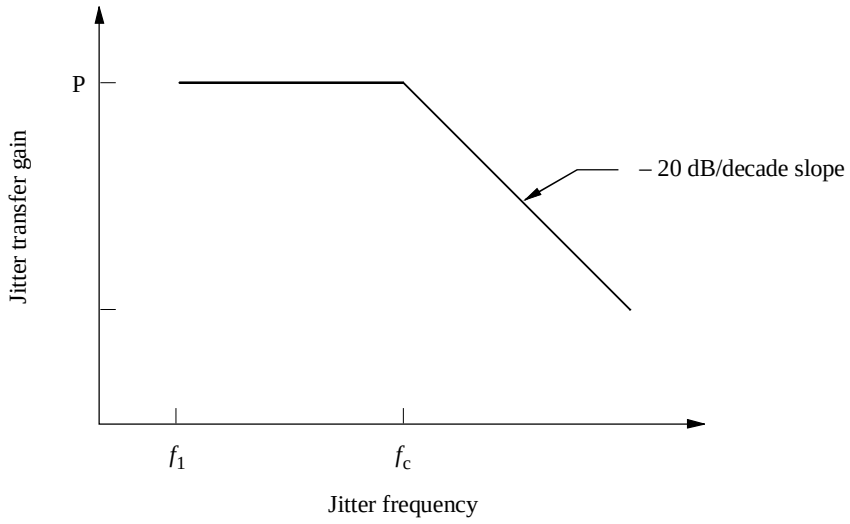
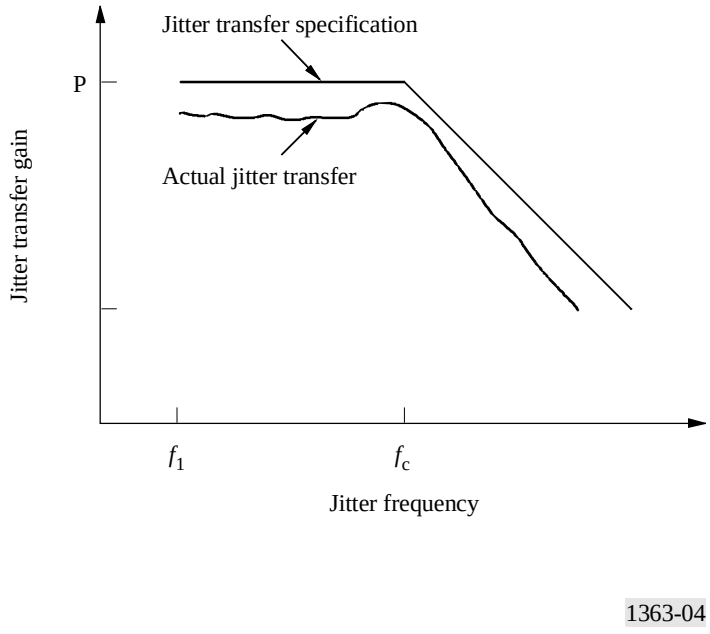


FIGURE 4

Jitter transfer specification and compliant jitter transfer function



4.2.2 Jitter transfer requirements are specified with the parameters given in Table 2.

4.2.2.1 Frequency band f_1 to f_c forms the jitter transfer bandpass. The maximum jitter gain over this bandpass shall be P.

4.2.2.2 From frequency fc to at least 10 (f_c), the jitter transfer template shall decrease at 20 dB/decade.

4.2.2.3 P shall be specified in decibels.

4.2.2.4 The test signal used for the measurement (to which sinusoidal jitter is added) shall be specified.

4.2.3 Numerical jitter transfer values are provided in the appropriate SMPTE standards which reference this practice. The terminology shall comply with 4.2.2.

4.3 Intrinsic jitter and output jitter

Intrinsic jitter and output jitter are both measurements of jitter at an equipment output. They differ in the specification of the input signal to the equipment. Except for this, they are measured identically.

Intrinsic jitter is defined as the amount of jitter at an equipment output when a jitter-free input signal is applied. It is a measure of the amount of jitter generated in the equipment, independent of any jitter transfer. Intrinsic jitter applies to most serial outputs.

Output jitter is the amount of jitter at the output of equipment that is embedded in a system or network. It consists of intrinsic jitter and the jitter transfer of jitter at the equipment input. Output jitter is a network specification, not an equipment specification. Individual equipment should be specified in terms of intrinsic jitter, jitter transfer, and input jitter tolerance. Network interface specifications may use output jitter.

4.3.1 Intrinsic and output jitter shall be specified as peak-to-peak quantities and measured over defined jitter frequency bands. Two measurement bands are specified, one is a subset of the other (see Figure 5).

4.3.2 Intrinsic and output jitter shall be specified with the parameters given in Table 3.

4.3.2.1 The timing jitter measurement bandpass is formed by f_1 to f_4. The maximum peak-to-peak jitter allowed over this bandpass is specified as A_1.

4.3.2.2 The alignment jitter measurement bandpass is formed by f_3 to f_4. The maximum peak-to-peak jitter allowed over this bandpass is specified as A_2.

4.3.2.3 A_1 and A_2 shall be specified in unit intervals.

4.3.2.4 Bandpass slopes shall be at least 20 dB/decade and have a minimum phase response unless otherwise specified. Stop band rejection shall be at least 20 dB. Pass band ripple shall be less than +1 dB.

4.3.2.5 A measurement time (tm) may be specified. If this is omitted, then the measurement time will be determined by the characteristics of the measurement system.

4.3.2.6 The test signal used for the measurement shall be specified. For an intrinsic jitter measurement, the test source jitter shall be negligible compared to the intrinsic jitter specification.

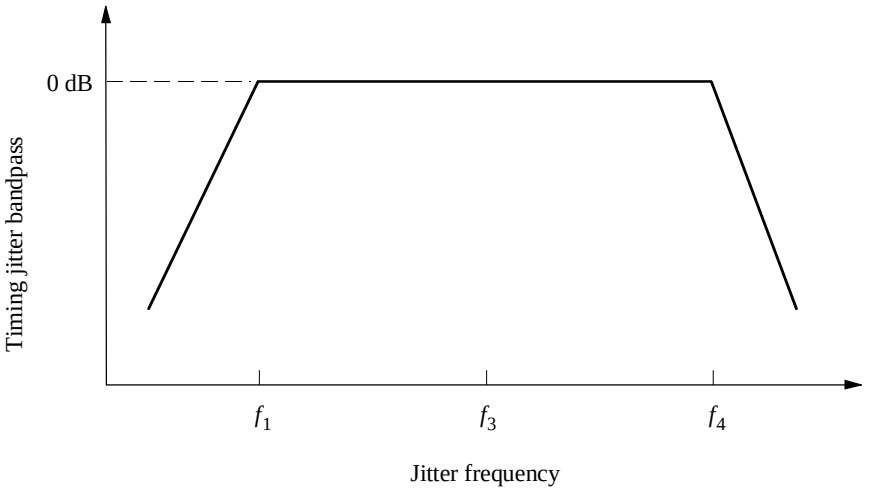
TABLE 2

Jitter transfer requirements

Parameters	Units	Description
Data rate	(bits/s)	(Serial bit rate)
f_l	(Hz)	(Low-frequency specification limit)
f_c	(Hz)	(Upper band edge of jitter transfer bandpass)
P	(dB)	(Maximum jitter gain, f_1 to f_c)
Test signal		(Test signal used for measurement)

FIGURE 5

Intrinsic and output jitter measurement bandpasses



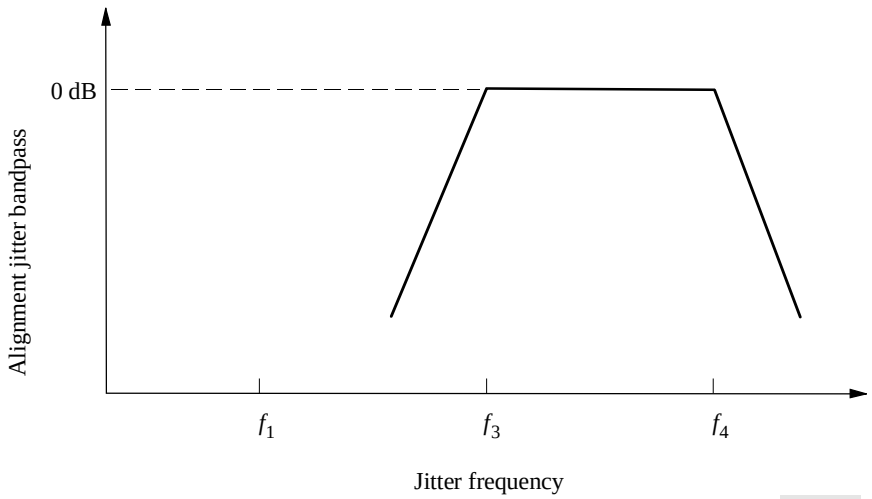


TABLE 3

Intrinsic and output jitter

Parameters	Units	Description
Data rate	(bits/s)	(Serial bit rate)
f_1	(Hz)	(Timing jitter, lower band edge)
f_3	(Hz)	(Alignment jitter, lower band edge)
f_4	(UI)	(Upper band edge)
A_1	(UI)	(Timing jitter)
A_2	(s)	(Alignment jitter)
t_m		(Measurement time)
Test signal		(Test signal used for measurement)
n		(Serial clock divider)

4.3.2.7 The serial clock divider, “n”, used in the clock extractor should be specified (see Appendix 1 for information on the Clock extractor and clock extractor based measurement methods). The ratio of the serial clock frequency to the clock extractor frequency is “n”. It is meaningful for clock extractor jitter measurement methods, but may not be applicable to other measurement techniques.

4.3.3 Numerical intrinsic and output jitter values are provided in the appropriate ITU Recommendations which reference this practice. The terminology shall comply with 4.3.2.

APPENDIX 1

Jitter measurement procedures in bit-serial digital interfaces

1 Scope

This Appendix 1 describes methods for measuring jitter performance in bit-serial digital interfaces.

1.1 Introduction

Jitter is one of the most important parameters in the performance of serial digital transmission systems. It can cause errors in the transmission and recovery of digital data, and may degrade analogue signal performance if the jitter is transferred through the digital-to-analogue conversion process. Characterizing and measuring jitter are important for reliable and predictable serial digital system operation.

2 Informative references

3 Definitions

3.1 **alignment jitter:** Variation in position of a signal’s transitions relative to those of a clock extracted from that signal. The bandwidth of the clock extraction process determines the low-frequency limit for alignment jitter.

3.2 **clock extractor:** A device which is able to extract the serial data clock from a serial data stream, and outputs a clock-related trigger. It may also provide the serial digital data reclocked with the extracted clock.

3.3 **DSO:** Acronym for digital storage oscilloscope.

3.4 **DUT:** Acronym for device under test.

3.5 **error rate tester:** A device that quantifies the error rate of a serial digital signal. Two examples are the classic bit error rate (BER) tester and the field rate CRC method (EDIT) described in SMPTE RP 165.

3.6 **input jitter tolerance:** Peak-to-peak amplitude of sinusoidal jitter that, when applied to an equipment input, causes a specified degradation of error performance.

3.7 **intrinsic jitter:** Jitter at an equipment output in the absence of input jitter.

3.8 **jitter:** Variation of a digital signal's transitions from their ideal positions in time.

3.9 **jitter generator:** A device which produces a serial digital signal containing sinusoidal jitter of adjustable amplitude and frequency.

3.10 **jitter receiver:** Demodulates and allows measurement of the jitter present on a serial signal. It commonly provides an output proportional to the demodulated jitter.

3.11 **jitter transfer:** Jitter on the output of equipment resulting from applied input jitter.

3.12 **jitter transfer function:** Ratio of the output jitter to the applied input jitter as a function of frequency.

3.13 **output jitter:** Jitter at the output of equipment that is embedded in a system network. It consists of intrinsic jitter and the jitter transfer of jitter at the equipment input.

3.14 **phase demodulator:** A device that provides as its output a signal proportional to the phase difference of two input signals.

3.15 **SDI:** Acronym for serial digital interface, typically referring to Recommendation ITU-R BT.656 system.

3.16 **timing jitter:** Variation in position of a signal's transitions occurring at a rate greater than a specified frequency, typically 10 Hz or less. Variations occurring below this specified frequency are termed wander and are not addressed by this practice.

3.17 **unit interval (UI):** The period of one clock cycle. It corresponds to the nominal minimum time between transitions of the serial signal.

4 Jitter specification

Four methods are described: The first uses an available reference clock to trigger an oscilloscope; the second uses a clock extractor with defined characteristics to trigger the oscilloscope; the third and fourth are based on a phase demodulator method jitter receiver.

4.1 Oscilloscope measurement by means of triggering on a reference signal

If a reference signal is available, a basic jitter measurement can be done (see Figure 6). The oscilloscope is directly triggered by the reference signal. This reference signal could also be a serial digital signal with high stability, for example, for a 270 Mbit/s ITU-R BT.656 signal, the 27 MHz parallel clock, the 270 MHz serial clock or an ITU-R BT.656 serial signal. The digital data signal is connected to the suitably terminated vertical channel of the oscilloscope and an eye measurement is done. The jitter is typically measured at the eye crossing.

– Presentation of measurement results: The test signal, the jitter amplitude, the parameters of the oscilloscope (bandwidth, etc.), and the measurement time should be indicated.

– Background information: This measurement procedure provides a coarse survey of jitter in an SDI signal. The measurement result depends on the stability of the reference signal (its jitter sets the measurement floor), the type of oscilloscope, and the measurement time (e.g., when a DSO is used in persistence mode). All of these parameters influence the measurement result and contribute to variability in the result as conditions vary. This method does not allow bandwidth restriction as generally required in jitter specification. This method is not recommended if other jitter measurement methods are available.

4.2 Jitter measurement by means of a clock extractor

The jitter in a signal output can be measured by using a device to extract clock and then trigger an oscilloscope or other indicating device (see Figure 7).

4.2.1 Clock extractor block diagram

The clock extractor typically consists of a wideband clock recovery circuit followed by a second, narrow band PLL (see Figure 8). This second PLL can be set to two different loop bandwidths, so that two different jitter transfer functions are available (see Figure 9). Clock output 2 is used to trigger the indicating device. The clock extractor shall have the following characteristics:

1) It shall be capable of being put in series with the signal output and provide enough signal for the indicating device. It shall not modify the output signal characteristics in ways that obscure or modify the jitter on the signal.

2) To measure timing jitter (A_1), the clock extractor shall have a clock recovery bandwidth of f_1. To measure alignment jitter (A_2), the clock extractor shall have a clock recovery bandwidth of f_3 (see Figure 9).

3) The jitter transfer function of the clock extractor shall roll-off at 20 dB/decade or greater and have a minimum phase response unless otherwise specified. Ripple within the pass band shall be less than + 1 dB (see Figure 9).

4) The extracted clock frequency shall be the serial clock frequency divided by “n”, where “n” is defined in 4.3.2 of the body of this Recommendation.

5) The clock extractor may have an optional clock output 1, which has a clock recovery bandwidth for greater than or equal to f_3. It is preferable that for equal 14.

4.2.2 Indicating device specifications

The indicating device used to observe the jitter shall have the following characteristics:

1) The horizontal and/or trigger bandwidth of the indicating device shall not attenuate the observed jitter. The trigger bandwidth shall be at least f_3.

2) The indicating device shall not create intersymbol interference at the zero-crossing point. This requires a vertical system step response that transitions and settles in less than 1 UI.

3) The indicating device shall acquire sufficient samples so that peak-to-peak jitter can be determined. This requires sampling until the shape of the jitter distribution is known. If the jitter specification includes a measurement time, this shall be the minimum acquisition time. The maximum acquisition time will depend on the device sample rate and the type of jitter distribution. For example, a sinusoidal distribution will typically be determined with fewer samples than will a gaussian-like distribution.

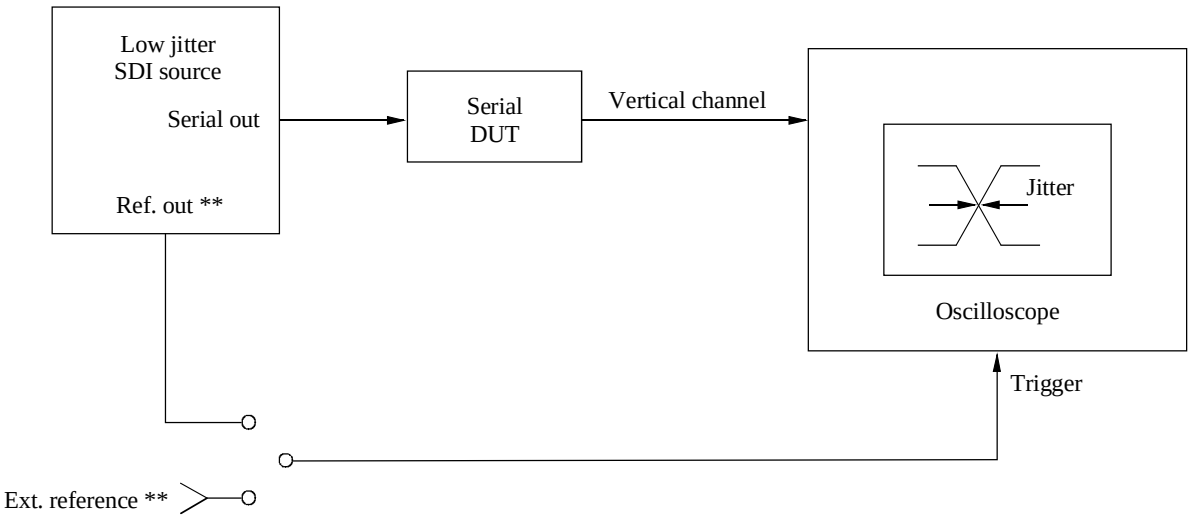
NOTE – The minimum required measurement time depends on how quickly the measurement device collects samples. For digital storage oscilloscopes (DSOs), this is determined by the acquisition rate and the number of samples per acquisition. While the latter term is related to the advertised DSO sample rate, the former is not. DSOs with identical sample rates may take very different amounts of time to build a sufficient sample record to make a measurement.

The minimum measurement for a given oscilloscope may be determined as follows: first, have the scope acquire for a very long time to establish the jitter level. Then, successively shorter measurements are taken until the results start showing unacceptable error or variation. This establishes the minimum measurement time for the scope. Experienced users often have an intuitive feeling for this value based on how the sample distribution is filling in.

4) If the indicating device is an oscilloscope, the jitter measurement is usually made at the eye crossing. A digital storage oscilloscope with infinite persistence is recommended.

FIGURE 6

Oscilloscope jitter measurement by means of a reference signal



** A for a 270 Mb/s ITU-R BT.656 signal, the 27 MHz parallel clock, the 270 MHz serial clock or a ITU-R BT.656 signal.

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FIGURE 7

Jitter measurement less than 1 UI using a clock extractor

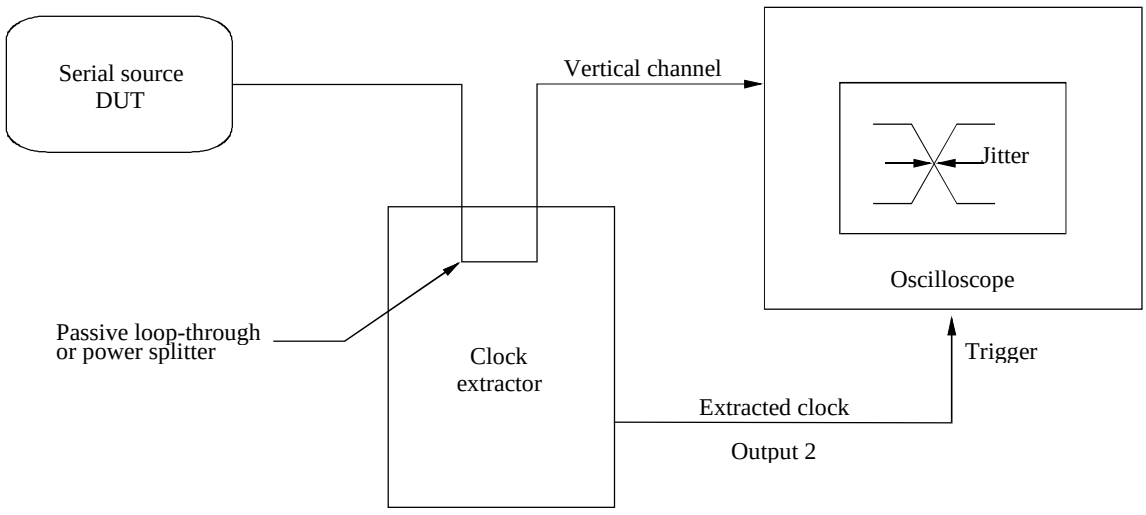

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FIGURE 8

Clock extractor block diagram

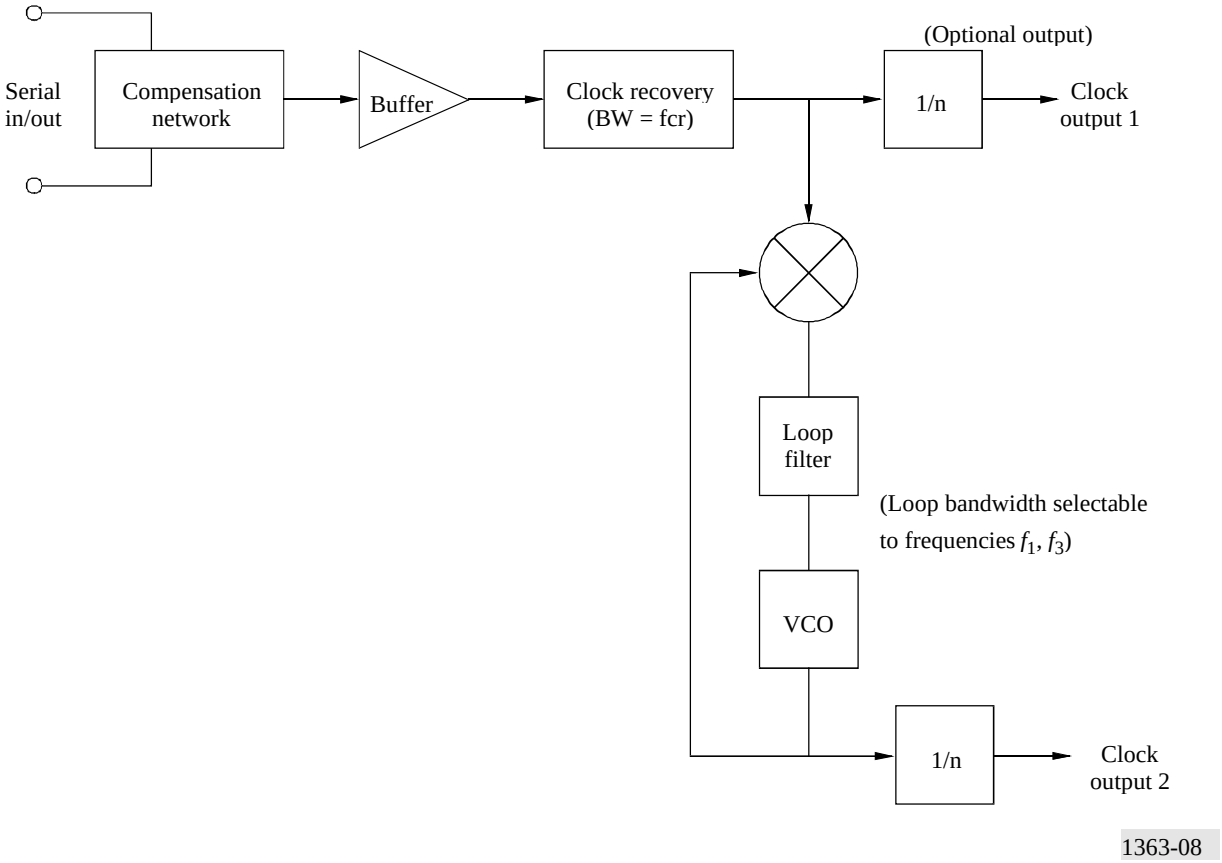
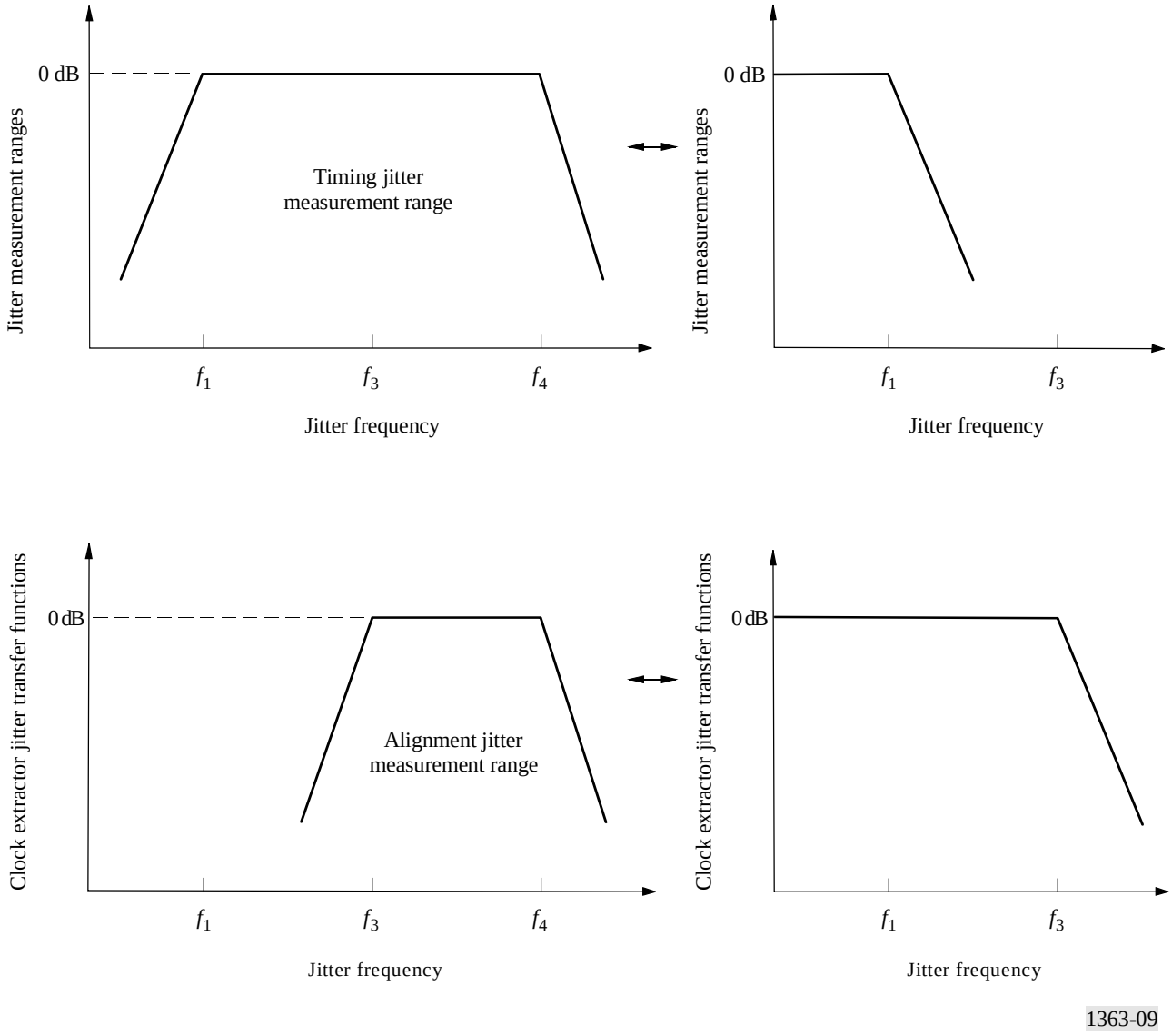


FIGURE 9

Jitter measurement bandwidth and corresponding clock extractor jitter transfer function



4.2.3 Measurement of timing jitter

The clock extractor is set to bandwidth f_1. The clock output 2 is connected to the trigger channel of the oscilloscope. The signal connected to the oscilloscope vertical channel depends on the jitter amplitude being measured. For jitter amplitudes less than 1 UI, the loop-through signal is used (see Figure 7). For jitter amplitudes greater than 1 UI, two different connections are possible:

1) (Preferred) If the clock extractor has a clock 1 output (Figure 8), this signal is applied to the oscilloscope vertical channel (see Figure 10). This connection will ensure jitter between frequencies f_1 and f_c, where for is the bandwidth of the wideband clock recovery circuit.

2) If the clock extractor has simultaneous outputs at bandwidths f_1 and f_3, one output is connected to the vertical channel and the second to the trigger. This connection measures jitter between frequencies f_1 and f_3.

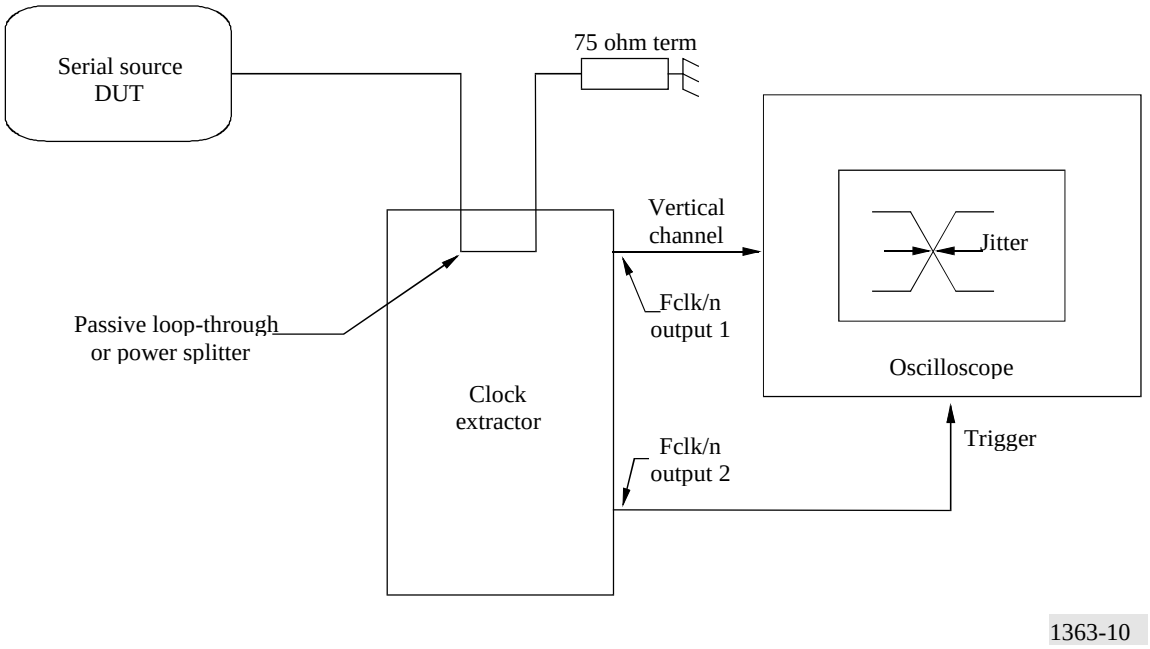
   – Presentation of measurement results: The test signal, the type of oscilloscope, the measurement time, and the jitter amplitude measured at the eye crossing should be documented. A screen plot of the eye pattern is recommended.

4.2.4 Measurement of alignment jitter

The clock extractor is set to bandwidth f_3. The clock output 2 is connected to the trigger channel of the oscilloscope. The loop-through signal is connected to the oscilloscope vertical channel (see Figure 7).

FIGURE 10

Measuring jitter greater 1 UI using a clock extractor and an ocilloscope



– Presentation of measurement results: The test signal, the type of oscilloscope, the measurement time, and the jitter amplitude measured at the eye crossing should be documented. A screen plot of the eye pattern is recommended.

4.2.5 Phase noise measurement by means of a clock extractor

This clause describes a simple method for making a phase noise measurement on the extracted clock using a spectrum analyzer. This technique allows an examination of the side bands of the clock signal, which correspond with the jitter frequencies in the SDI signal (see Figure 11).

The output 1 of the clock extractor is connected to a spectrum analyzer. The spectrum analyzer is switched to phase noise measurement and the phase noise of the clock under test is examined.

– Presentation of measurement results: The test signal, the clock extractor PLL bandwidth, the resolution bandwidth and span of the spectrum analyzer, and a plot of the spectrum should be indicated.

4.3 Jitter measurements using a phase demodulator

Jitter can be conveniently observed and measured if the phase modulation sidebands are heterodyned down to D.C. One popular method is to recover two clocks from the signal, one with a very wide clock recovery bandwidth and the second with a narrow bandwidth, and apply them to a phase demodulator (see Figure 12). The output signal is then applied through selectable bandpass filters to a peak reading voltmeter. The output can also be applied to a spectrum analyzer to observe the jitter frequency terms (see Figure 13). Jitter receivers typically use the phase demodulator method.

4.3.1 A jitter receiver shall be capable of measuring peak-to-peak jitter over the jitter measurement bandpasses described in 4.3.2 of the body of this Recommendation.

4.3.2 The jitter spectrum can be observed by connecting the phase demodulator output to a spectrum analyzer or an oscilloscope with fast Fourier transform (FFT) option (see Figure 13).

Presentation of measurement results: The test signal, measurement time, measured jitter level and measurement bandpass, and a description of the measurement equipment should be documented.

FIGURE 11

Jitter measurement by means of a clock extractor and a spectrum analyser

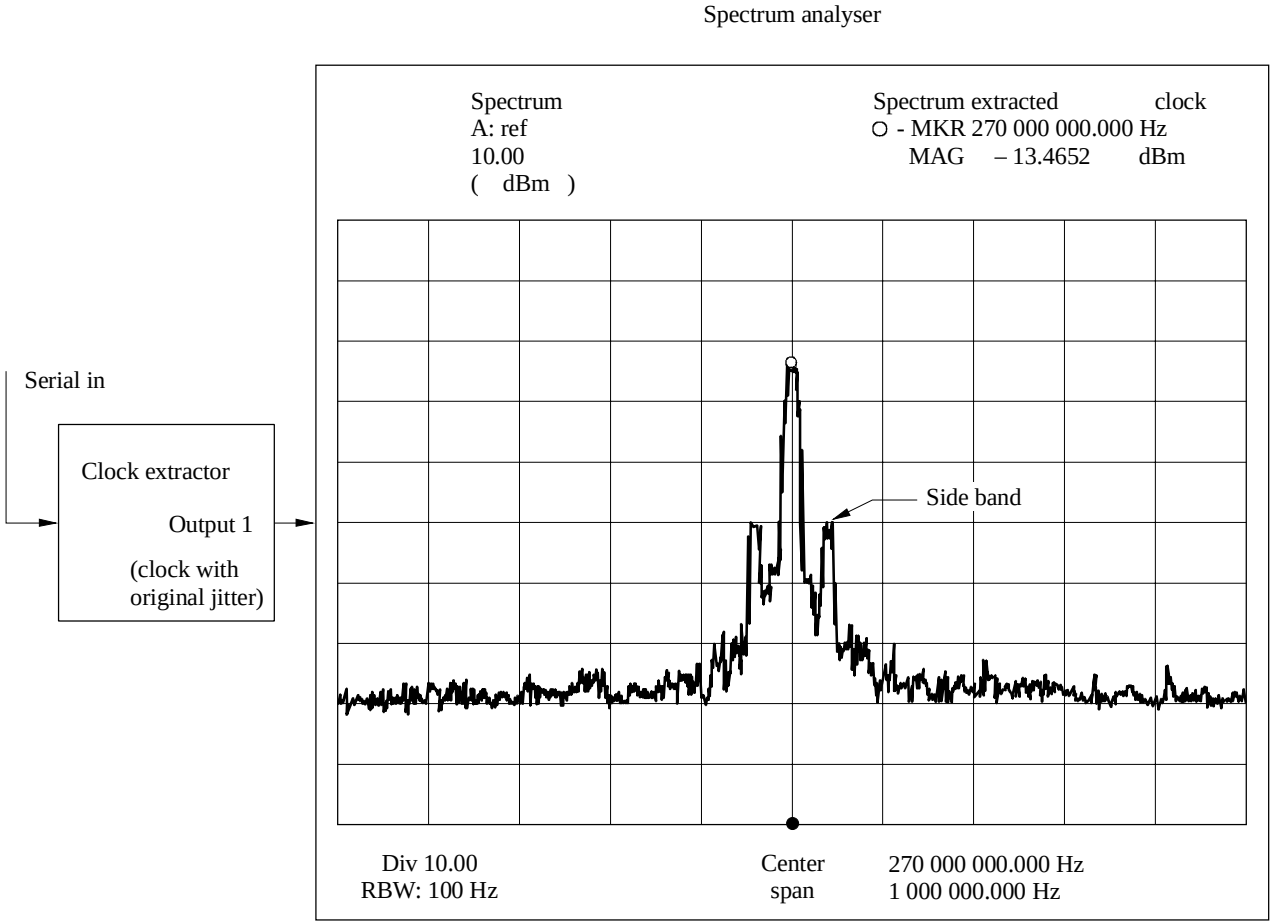


FIGURE 12

Block diagram of a jitter receiver
(clock extractor high-quality PLL, demodulator)

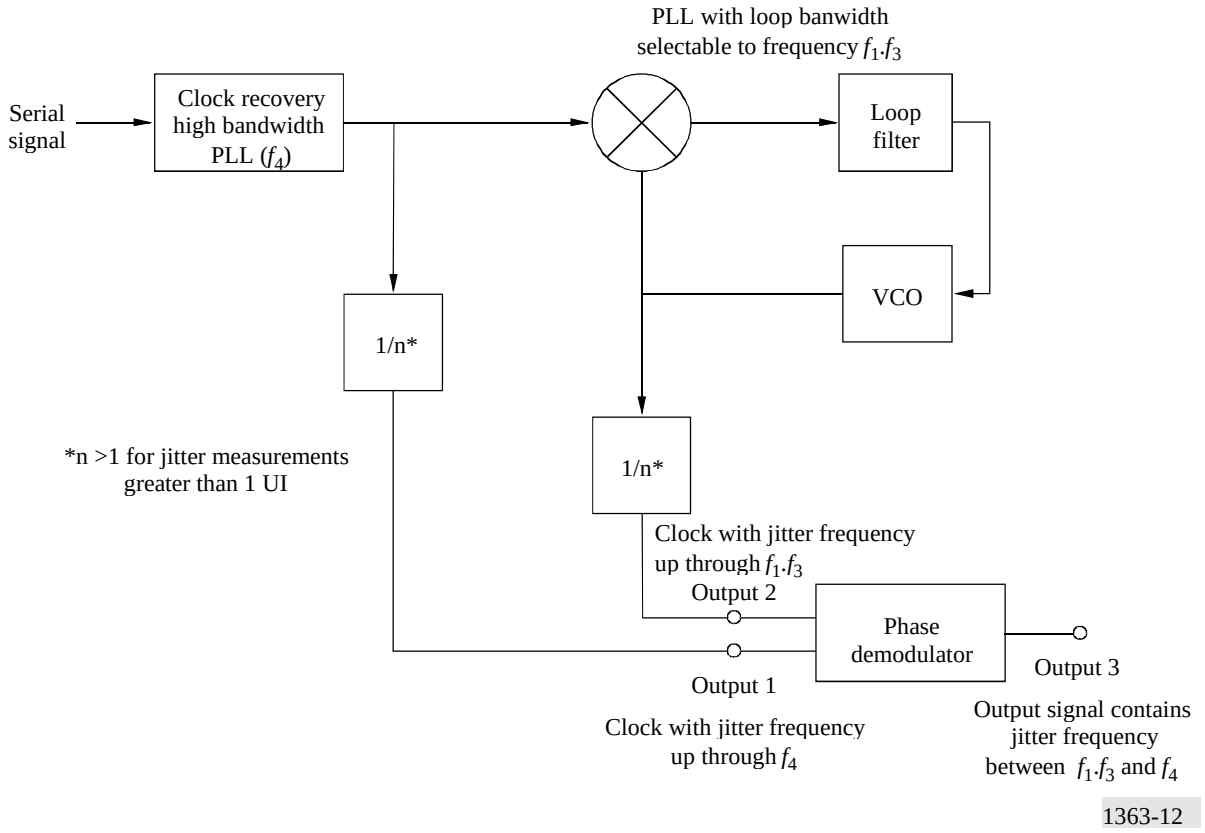
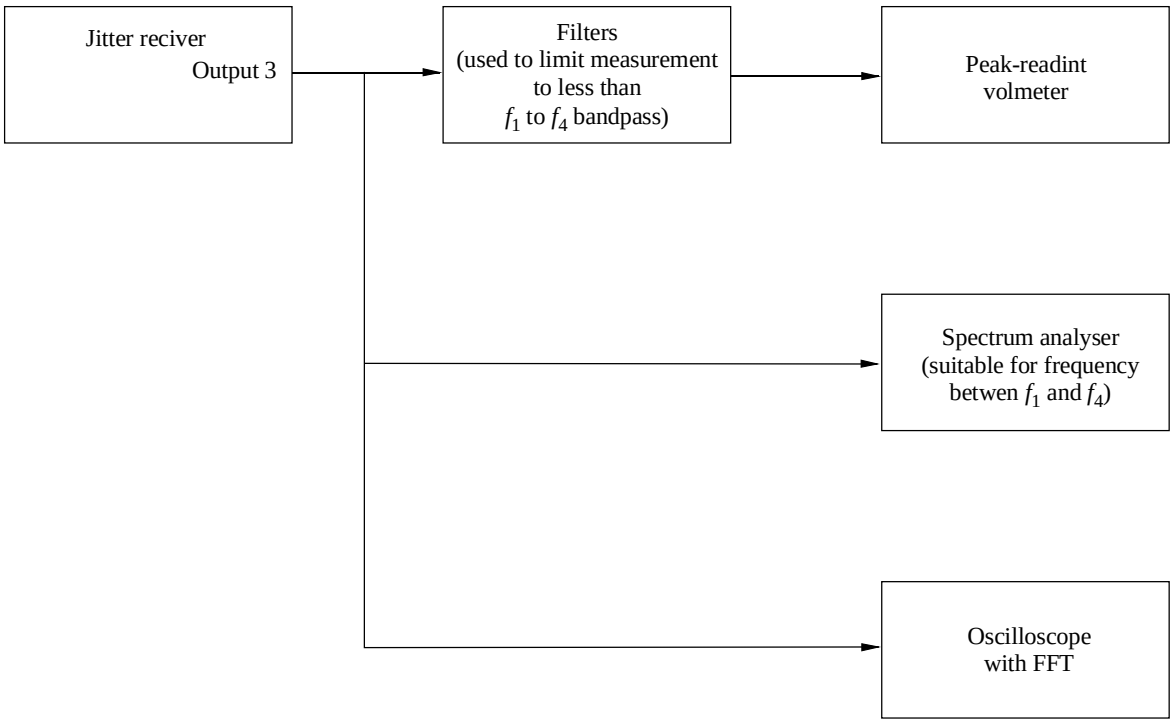


FIGURE 13

Jitter receiver output connections



4.4 Phase demodulator measurement with an available reference signal

If a reference signal is available, then a demodulated jitter measurement may be made using the set-up shown in Figure 14. The reference and data signals are connected to the two inputs of a digital phase demodulator. The output of the demodulator may be processed in several ways. The output may be filtered to establish the lower and upper band edges and then passed to an oscilloscope for display of the jitter results (note that the vertical scale of the oscilloscope now represents the jitter amplitude). Alliteratively, the demodulated jitter waveform may be captured and then digitally filtered to establish the upper and lower band edges. Finally, the jitter spectrum may be obtained either by performing an FFT on a captured waveform, or by connecting the demodulator output to a spectrum analyzer.

– Presentation of measurement results: The test signal type, the upper and lower band edges, the measurement time, and the peak-to-peak jitter amplitude should be recorded.

– Background information: This measurement method is sensitive to any pattern dependent jitter introduced by the phase detector in the jitter demodulator. The phase detector shall be of a type to avoid introducing pattern dependent jitter. The method also requires that the phase demodulator be calibrated so that the vertical indication on the oscilloscope may be related to the jitter amplitude. This may be accomplished by providing a frequency shift between the reference and the data signal and noting the slope of the phase demodulator output. Finally, this technique is only able to resolve jitter less than 1 UI in magnitude in the limit, and in practice less than 1 UI because of nonlinearities in the demodulator transfer function near the limits of its range.

5 Jitter tolerance measurement

Jitter tolerance measurements require a calibrated jitter generator and an error rate measurement device (see Figure 15).

– Procedure

1) Connect the equipment as shown in Figure 15. With the generator jitter amplitude set to 0 UI pp. verify error-free operation.

2) Set the generator jitter frequency as desired, and increase the jitter amplitude until the onset of errors criterion is reached. Note the jitter amplitude and frequency:

3) Repeat step 2) for a sufficient number of frequencies to determine the jitter tolerance curve.

– To verify compliance with a jitter tolerance template:

1) Set the jitter amplitude and frequency to a template point. Verify that the onset of errors criterion is not reached.

2) Repeat step 1) for a sufficient number of template points between frequencies f_1 and f_3. Template form is described in the body of this Recommendation.

NOTE – A calibrated jitter receiver can be used to establish the jitter amplitude of an uncalibrated jitter generator.

6 Jitter transfer measurement

Jitter transfer measurements require a calibrated jitter generator and a calibrated jitter receiver (see Figure 16). An enhanced method requires a jitter generator with an external jitter input, a jitter receiver, and a spectrum analyzer with a tracking oscillator output (see Figure 17).

– Basic technique:

1) Perform a jitter tolerance measurement of the DUT over the desired frequency range.

2) Connect the equipment as shown in Figure 16. Set the jitter generator level so that it is less than the measured jitter tolerance over the band of interest, yet large enough for good measurement accuracy.

3) Note the jitter receiver reading and the jitter frequency.

4) Divide the jitter receiver reading by the jitter generator level to obtain the jitter gain at this frequency.

5) Repeat step 3) for a sufficient number of frequencies to determine the jitter transfer function.

NOTE – If the jitter generator or the jitter receiver frequency response is not flat, connect the generator and receiver directly together to establish a deviation table.

– Enhanced technique:

1) Perform a jitter tolerance measurement of the DUT over the desired frequency range.

2) Connect the equipment as shown in Figure 17, bypassing the DUT. Verify linear, error-free operation of the jitter receiver.

3) Set the tracking generator output amplitude so that the jitter generator level is less than the measured jitter tolerance over the desired frequency range. Select an appropriate resolution bandwidth on the spectrum analyzer. Save the trace on the analyzer.

4) Connect the DUT. Subtract the stored trace from the display trace. The difference is the DUT jitter transfer function.

NOTE – A network analyzer can be used in place of the spectrum analyzer and tracking generator combination. A vector network analyzer permits measurement of both the phase and magnitude of the jitter transfer function.

To verify compliance with a jitter transfer template: Using either the basic or enhanced technique, verify that the jitter transfer is less than the template requirement, from f_1 to $10(f_c)$.

FIGURE 14

Phase demodulator measurement with an available reference signal

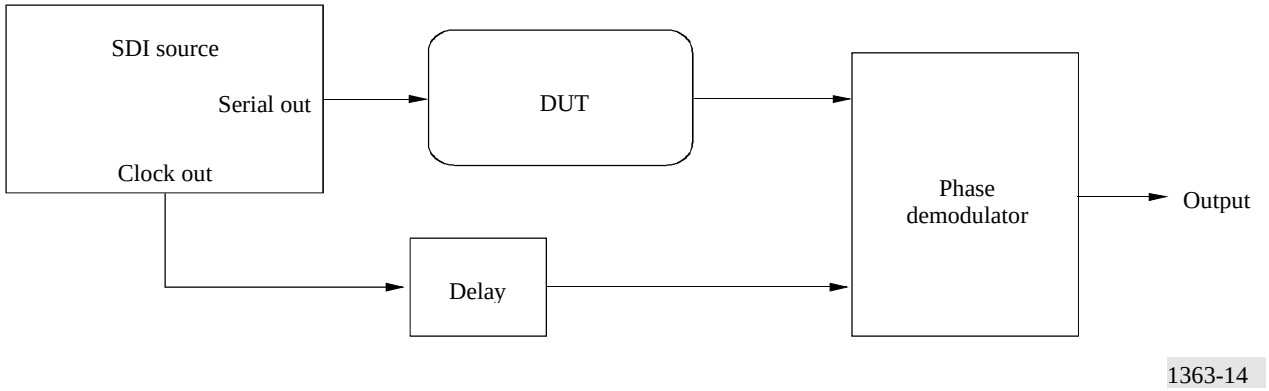


FIGURE 15

Jitter tolerance measurement

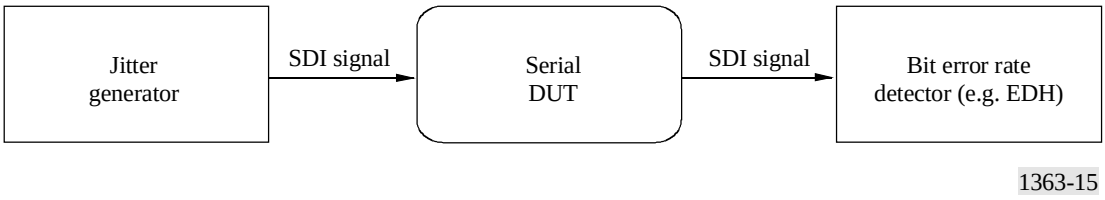


FIGURE 16

Jitter transfer function measurement (basic method)

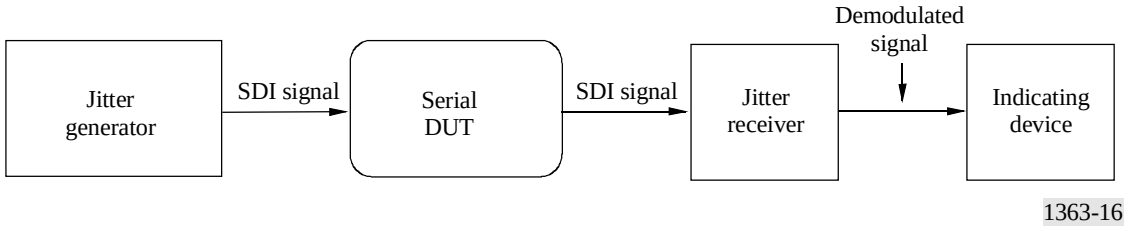


FIGURE 17

Jitter transfer function measurement (enhanced method)