RECOMMANDATION UIT-R BT.1620

Structure de données de type vidéonumérique pour les signaux audio, de données et vidéo comprimés à 100 Mbit/s

(Question UIT-R 12/6)

(2003)

L'Assemblée des radiocommunications de l'UIT,

considérant

a) que l'on a identifié des applications de production et de post-production de télévision professionnelle pour lesquelles la compression vidéo de type vidéonumérique peut présenter des avantages opérationnels et économiques vis-à-vis de l'exploitation fondée sur une interface série numérique;

b) que trois débits de données ont été proposés au sein de la même famille de compression afin d'être utilisés pour différentes applications (25 Mbit/s, 50 Mbit/s et 100 Mbit/s);

c) que les grilles d'échantillonnage sont différentes pour chacune des trois applications;

d) que l'UIT-R préconise l'application de la Recommandation UIT-R BT.709 pour l'échange international de programmes à haute définition;

e) que les composantes audio, de données auxiliaires et de métadonnées font partie intégrante de ces applications;

f) que ces composantes sont multiplexées en un flux de données unique pour le transport et le traitement ultérieur;

g) que la qualité de compression et les caractéristiques fonctionnelles doivent être identiques et reproductibles dans des chaînes de production complexes;

h) qu'à cette fin, tous les détails des paramètres utilisés pour le codage et le multiplexage doivent être définis,

recommande

1 d'utiliser, pour les applications de production et de post-production de télévision professionnelle s'appuyant sur la compression de type vidéonumérique à 100 Mbit/s, les paramètres donnés dans la Norme SMPTE 370M-2002 «Data Structure for DV-Based Audio, Data and Compressed Video at 100 Mb/s – 1 080/60i, 1 080/50i and 720/60p».

NOTE 1 – La Norme SMPTE 370M-2002 fait référence à la norme SMPTE 296M «1280 × 720 Progressive Image Sample Structure – Analog and Digital Representation and Analog Interface». Les formats ci-après, tirés du Tableau 1 de la Norme SMPTE 296M, ne doivent pas être considérés comme faisant partie de la présente Recommandation.

Elément du Tableau 1	Nomenclature du système	Fréquence de trame
3	1280 × 720/50	50
6	1280 × 720/25	25
7	1280 × 720/24	24
8	1280 × 720/23,98	24/1,001

Résumé de la norme SMPTE 370M-2002

Cette norme définit la structure de données de type vidéonumérique à débit d'échantillonnage de 100 Mbit/s applicable à l'interface pour des signaux audio numériques, de données de sous-code et vidéo comprimés présentant les paramètres suivants:

– système 1080/60i: structure d'échantillonnage d'image 1920×1080, fréquence de trame 59,94 Hz, balayage entrelacé;

– système 1080/50i: structure d'échantillonnage d'image 1920×1080, fréquence de trame 50 Hz, balayage entrelacé;

– système 720/60p: structure d'échantillonnage d'image 1280×720, fréquence de trame 59,94 Hz, balayage progressif.

Cette norme ne définit pas la structure de données de type vidéonumérique applicable à l'interface pour des signaux audio numériques, de données de sous-code et vidéo comprimés présentant les paramètres suivants:

– système 720/50p: structure d'échantillonnage d'image 1280×720, fréquence de trame 50 Hz, balayage progressif.

NOTE 1 – Les normes SMPTE 370M-2002 et 296M-2001 sont données dans les Annexes 1 et 2. Les normes SMPTE 370M-2002 et 296M-2001 renvoient uniquement aux versions 2002 et 2001 respectivement qui sont celles qui ont été approuvées, le 03.05.03 en application de la Résolution UIT-R 1-3, par les Administrations des Etats Membres de l'UIT. Comme convenu entre l'UIT et la SMPTE, lesdites versions ont été fournies par la SMPTE qui en a autorisé l'utilisation et l'UIT-R a accepté de les inclure dans la présente Recommandation. Toutes versions ultérieures des normes SMPTE 370M et 296M, qui n'auraient pas été agréées et approuvées par la Commission d'études 6, n'entrent pas dans le cadre de la présente Recommandation. Pour des versions ultérieures de documents SMPTE, le lecteur est prié de consulter le site web de la SMPTE à l'adresse suivante: http://www.smpte.org/.

SMPTE 370M-2002

SMPTE STANDARD

for Television — Data Structure for DV-Based Audio, Data and Compressed Video at 100 Mb/s 1080/60i, 1080/50i, 720/60p

Table of contents

1 Scope

This standard defines the data structure for the interface of DV-based digital audio, subcode data, and compressed video at 100 Mb/s. The standard defines the processes required to decode the DV-based data structure into eight channels of AES-3 digital audio at 48 kHz, subcode data, and high-definition video at 1080/60i, 1080/50i, and 720/60p.

The following high-definition video parameters are used in this standard:

1080/60i system –
Input video format: 1920 x 1080 image sampling structure, 59.94-Hz field rate, interlace format.
Compressed video data rate: 100 Mb/s

1080/50i system –
Input video format: 1920 x 1080 image sampling structure, 50-Hz field rate, interlace format.
Compressed video data rate: 100 Mb/s

720/60p system –
Input video format: 1280 x 720 image sampling structure, 59.94-Hz frame rate, progressive format.
Compressed video data rate: 100 Mb/s

In this standard, the 60-Hz system nomenclature refers to both 1080/60i and 720/60p systems; whereas, the 50-Hz system refers only to the 1080/50i system. The nomenclature 1080-line system refers to both 1080/60i and 1080/50i systems, while, the 720-line system refers only to the 720/60p system.

Approved
June 19, 2002

2 Normative references

The following standards, through reference in this text, constitute provisions of this standard. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below.

AES3-1992, Serial Transmission Format for Two-Channel Linearly Represented Digital Audio Data

ANSI/SMPTE 12M-1999 Television, Audio and Film — Time and Control Code

SMPTE 260M-1999, Television — 1125/60 High-Definition Production System — Digital Representation and Bit-Parallel Interface

SMPTE 274M-1998, Television — 1920 x 1080 Scanning and Analog and Parallel Digital Interfaces for Multiple Picture Rates

SMPTE 296M-1997, Television — 1280x720 Progressive Image Sample Structure — Analog and Digital Representation and Analog Interface

3 Data processing

3.1 General

As shown in figure 1, processed audio, video and subcode data are output for recording on a D-xx recorder. Additionally this data are output in DIF format data for the different application through a digital interface port. Detail of process shown in figure 1 is described in clauses 3 and 4. Dotted lines are related to data flow described in VTR document.

Annex A shows the block diagram of D-xx recorder. Figure A.1 of this document shows the part defined by this compression format document.

3.1.1 Video encoding parameter

The source component signal to be processed shall comply with the video parameters as defined by SMPTE 274M and SMPTE 296M.

3.1.2 Audio encoding parameter

The audio signal is sampled at 48 kHz, with 16-bit quantization defined by AES3.

3.1.3 Subcode data

The time code format in the subcode area complies with SMPTE 12M.

3.1.4 Frame structure

In 1080/60i and 1080/50i systems, video frame data, audio frame data, and subcode data are processed in each frame. The audio frame in this standard is defined as an audio-processing unit. In the 720/60p system, data in two video frames are processed within one frame duration of the 1080/60i system. Consequently, audio data and subcode data are processed in same way as the 1080/60i system.

Each frame of time code shows a frame number that corresponds to each video frame in the 1080-line system, and two video frames each in 720/60p system. Therefore, time codes of the 1080/60i and 720/60p systems are the same.

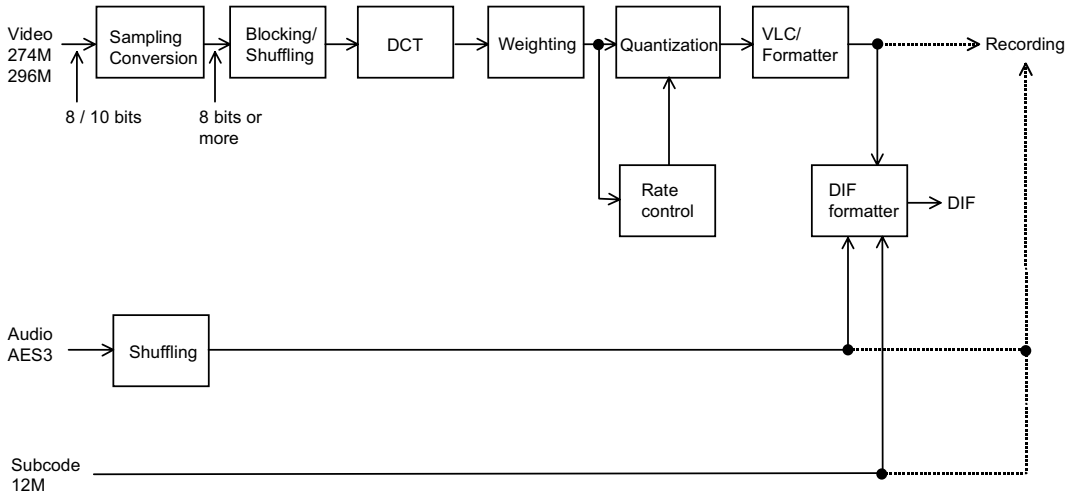


Figure 1 – Data processing block diagram

3.2 Data structure

The data structure of the compressed stream at the digital interface is shown in figure 2. The data of each frame are divided into four DIF channels.

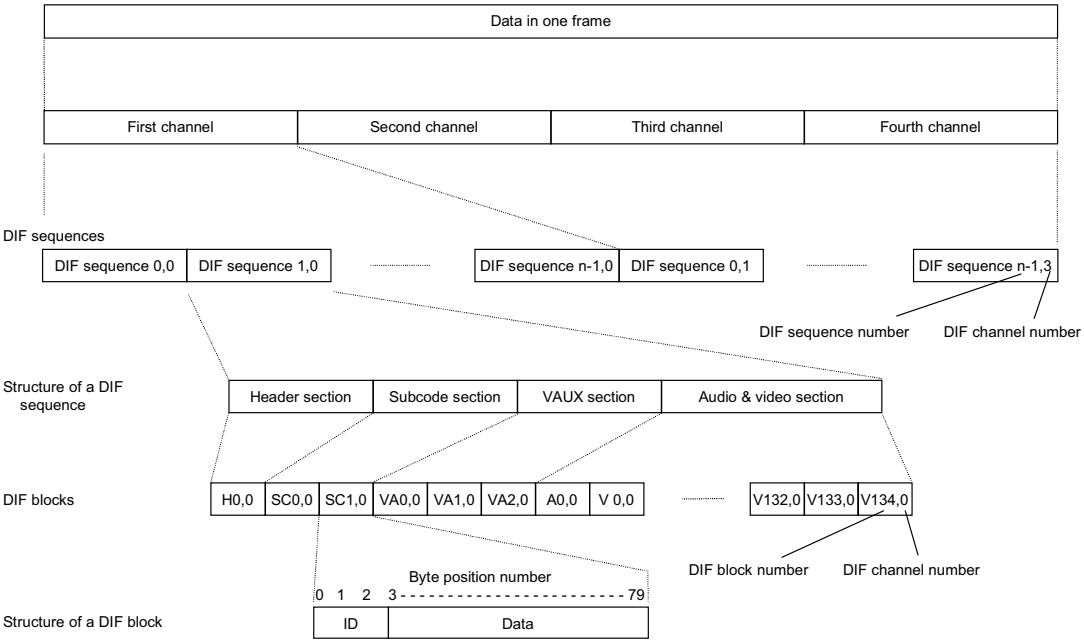
Each DIF channel is divided into 10 DIF sequences for the 60 Hz system and 12 DIF sequences for the 50-Hz system.

Each DIF sequence consists of a header section, subcode section, VAUX section, audio section, and video section with the following DIF blocks respectively;

Header section:	1 DIF block
Subcode section:	2 DIF blocks
VAUX section:	3 DIF blocks
Audio section:	9 DIF blocks
Video section:	135 DIF blocks

As shown in figure 2, each DIF block consists of a 3-byte ID and 77 bytes of data. DIF data bytes are numbered 0 to 79. Figure 3 shows the data structure of a DIF sequence.

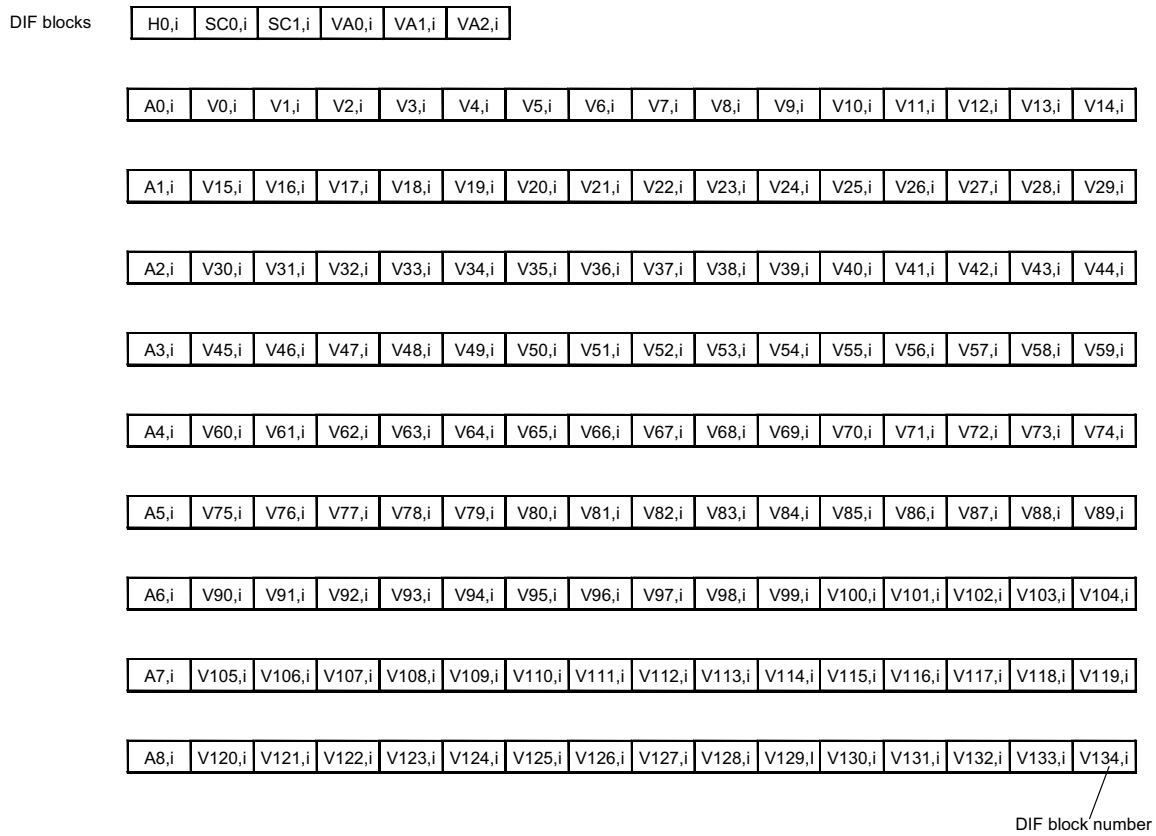
SMPTE 370M-2002



where

n = 10 for 60 Hz system
n = 12 for 50 Hz system

Figure 2 – Data structure



where

i : DIF channel number
i = 0,1,2,3

H0,i : DIF block in header section
SC0,i to SC1,i : DIF blocks in subcode section
VA0,i to VA2,i : DIF blocks in VAUX section
A0,i to A8,i : DIF blocks in audio section
V0,i to V134,i : DIF blocks in video section

Figure 3 – Data structure of a DIF sequence

3.3 Header section

3.3.1 ID

The ID part of each DIF block in the header section, shown in figure 2, consists of 3 bytes (ID0, ID1, ID2). Table 1 shows the ID content of a DIF block.

Table 1 – ID data of a DIF block

	Byte position number		
	0 ID0	1 ID1	2 ID2
MSB	SCT2	Dseq3	DBN7
	SCT1	Dseq2	DBN6
	SCT0	Dseq1	DBN5
	Res	Dseq0	DBN4
	Arb	FSC	DBN3
	Arb	FSP	DBN2
	Arb	Res	DBN1
LSB	Arb	Res	DBN0

The ID contains the followings :

SCT:	Section type (see table 2)
Dseq:	DIF sequence number (see tables 3 and 4)
FSC, FSP:	Channel identification of a DIF block (see table 5) NOTE – FSP bit is reserved in SMPTE 314M
DBN:	DIF block number (see table 6)
Arb:	Arbitrary bit
Res:	Reserved bit for future use Default value shall be set to 1

Table 2 – Section type

Section type bit			Section type
SCT2	SCT1	SCT0	
0	0	0	Header
0	0	1	Subcode
0	1	0	VAUX
0	1	1	Audio
1	0	0	Video
1	0	1	Reserved
1	1	0	
1	1	1	

Table 3 – DIF sequence number for the 60-Hz system

DIF sequence number bit				DIF sequence number
Dseq3	Dseq2	Dseq1	Dseq0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	Not used
1	0	1	1	Not used
1	1	0	0	Not used
1	1	0	1	Not used
1	1	1	0	Not used
1	1	1	1	Not used

Table 4 – DIF sequence number for the 50 Hz system

DIF sequence number bit				DIF sequence number
Dseq3	Dseq2	Dseq1	Dseq0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	Not used
1	1	0	1	Not used
1	1	1	0	Not used
1	1	1	1	Not used

Table 5 – DIF channel number

FSC	FSP	DIF channel number
0	1	0: first channel
1	1	1: second channel
0	0	2: third channel
1	0	3: fourth channel

Table 6 – DIF block number

DIF block number bit								DIF block number
DBN7	DBN6	DBN5	DBN4	DBN3	DBN2	DBN1	DBN0	
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	1	1	3
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	0	0	0	0	1	1	0	134
1	0	0	0	0	1	1	1	Not used
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	Not used

3.3.2 Data

The data part (payload) of each DIF block in the header section is shown in table 7. Bytes 3 to 7 are active and bytes 8 to 79 are reserved.

Table 7 - Data (payload) in the header section

	Byte position number							
	3	4	5	6	7	8	-------	79
MSB	DSF	Res	TF1	TF2	TF3	Res	-------	Res
	0	Res	Res	Res	Res	Res	-------	Res
	Res	Res	Res	Res	Res	Res	-------	Res
	Res	Res	Res	Res	Res	Res	-------	Res
	Res	Res	Res	Res	Res	Res	-------	Res
	Res	APT2	AP12	AP22	AP32	Res	-------	Res
	Res	APT1	AP11	AP21	AP31	Res	-------	Res
LSB	Res	APT0	AP10	AP20	AP30	Res	-------	Res

DSF: DIF sequence flag

0 = 10 DIF sequences included in a DIF channel (60-Hz system)
1 = 12 DIF sequences included in a DIF channel (50-Hz system)

APTn, AP1n, AP2n, and AP3n data shall be identical to the track application IDs (APTn = 001, AP1n = 001, AP2n = 001, AP3n = 001), if the source signal comes from the DV based digital VCR. If the signal source is unknown, all bits for this data shall be set to 1.

T F: Transmitting flag

TF1: Transmitting flag of audio DIF blocks
TF2: Transmitting flag of VAUX and Video DIF blocks
TF3: Transmitting flag of subcode DIF blocks

0 = Valid data
1 = Invalid data.

Res: Reserved bit for future use
Default value shall be set to 1.

3.4 Subcode section

3.4.1 ID

The ID part of each DIF block in the subcode section is the same as described in 3.3.1. The section type shall be 001.

3.4.2 Data

The data part (payload) of each DIF block in the subcode section is shown in figure 4. The subcode data consists of 6 SSYBs, each 48 bytes long, and a reserved area of 29 bytes in each DIF block. SSYBs in a DIF sequence are numbered 0 to 11. Each SSYB is composed of an SSYB ID equal to 2 bytes, an FF_h, and an SSYB data payload of 5 bytes.

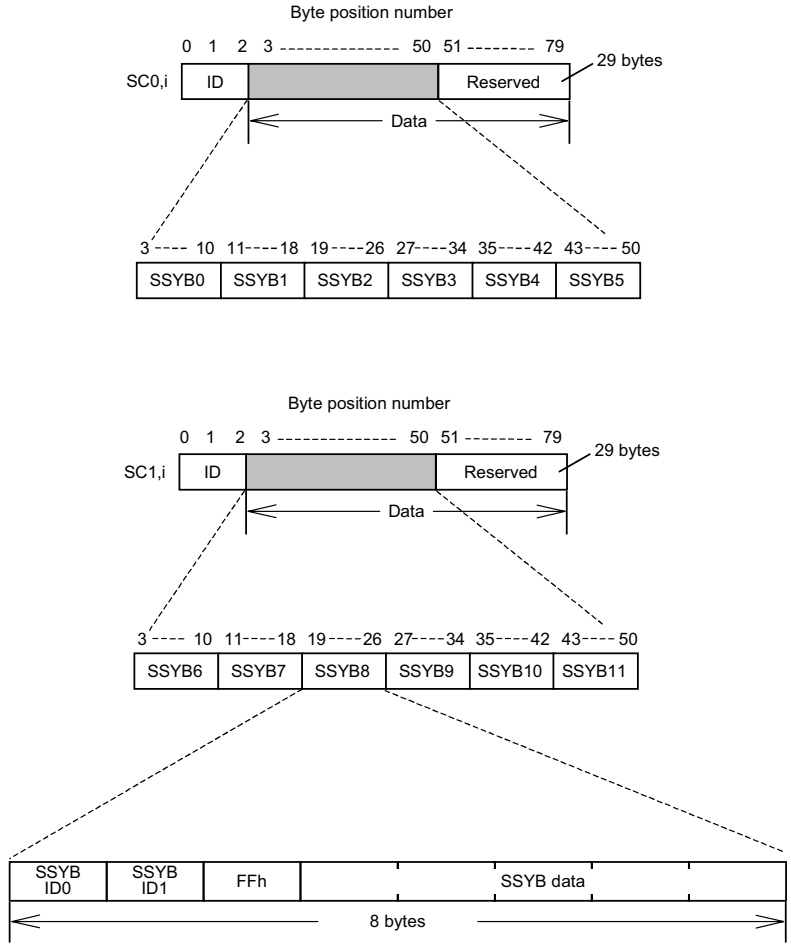


Figure 4 – Data in the subcode section

3.4.2.1 SSYB ID

Table 8 shows the parts of SSYB ID (ID0, ID1). It contains FR ID, application ID ($AP3_2$, $AP3_1$, $AP3_0$), (APT_2, APT_1, APT_0), and SSYB number (Syb_3, Syb_2, Syb_1, Syb_0).

Table 8 – SSYB ID

Bit position	SSYB number 0 and 6		SSYB number 1 to 5 and 7 to		SSYB number 11	
	ID0	ID1	ID0	ID1	ID0	ID1
b7	FR	Arb	FR	Arb	FR	Arb
b6	AP32	Arb	Res	Arb	APT2	Arb
b5	AP31	Arb	Res	Arb	APT1	Arb
b4	AP30	Arb	Res	Arb	APT0	Arb
b3	Arb	Syb3	Arb	Syb3	Arb	Syb3
b2	Arb	Syb2	Arb	Syb2	Arb	Syb2
b1	Arb	Syb1	Arb	Syb1	Arb	Syb1
b0	Arb	Syb0	Arb	Syb0	Arb	Syb0
NOTE – Arb = arbitrary bit						

FR : The identification for the first half or second half of each DIF channel.
1 = the first half of each DIF channel
0 = the second half of each DIF channel

The first half of each DIF channel
DIF sequence number 0, 1, 2, 3, 4 for 60 Hz system
DIF sequence number 0, 1, 2, 3, 4, 5 for 50 Hz system

The second half of each DIF channel
DIF sequence number 5, 6, 7, 8, 9 for 60 Hz system
DIF sequence number 6, 7, 8, 9, 10, 11 for 50 Hz system

If information is not available, all bits shall be set to 1.

3.4.2.2 SSYB data

Each SSYB data payload consists of a pack of 5 bytes as shown in figure 5. Table 9 shows the pack header table (PC0 byte organization). Table 10 shows the pack arrangement in SSYB data for each DIF channel.

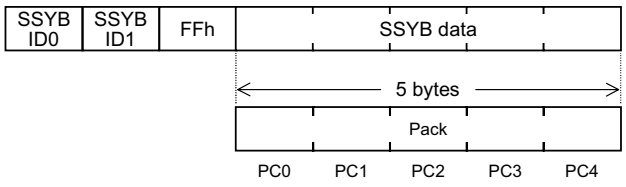


Figure 5 – Pack in SSYB

Table 9 – Pack header table

UPPER / LOWER	0000	0001	0010	0011	0100	0101	0110	0111	—	1111
0000						AUDIO SOURCE	VIDEO SOURCE			
0001						AUDIO SOURCE CONTROL	VIDEO SOURCE CONTROL			
0010										
0011		TIME CODE								
0100		BINARY GROUP								
0101										
⎮										
1111										NO INFO

Table 10 – Mapping of packets in SSYB data

SSYB number	The first half of each DIF channel	The second half of each DIF channel
0	Reserved	Reserved
1	Reserved	Reserved
2	Reserved	Reserved
3	TC	TC
4	BG	Reserved
5	TC	Reserved
6	Reserved	Reserved
7	Reserved	Reserved
8	Reserved	Reserved
9	TC	TC
10	BG	Reserved
11	TC	Reserved

NOTES
1 TC = Time code pack.
2 BG = Binary group pack.
3 Reserved = Default value of all bits shall be set to 1.
4 TC and BG data are the same within each frame.
The time code data are an LCT type

3.4.2.2.1 Time code pack (TC)

Table 11 shows a mapping of the time code pack. Time code data mapped to the time code packs are the same within each frame.

Table 11 – Mapping of time code pack

60 Hz system

	MSB							LSB
PC0	0	0	0	1	0	0	1	1
PC1	CF	DF	TENS of FRAMES		UNITS of FRAMES			
PC2	PC	TENS of SECONDS			UNITS of SECONDS			
PC3	BGF0	TENS of MINUTES			UNITS of MINUTES			
PC4	BGF2	BGF1	TENS of HOURS		UNITS of HOURS			

50 Hz system

	MSB							LSB
PC0	0	0	0	1	0	0	1	1
PC1	CF	Arb	TENS of FRAMES		UNITS of FRAMES			
PC2	BGF0	TENS of SECONDS			UNITS of SECONDS			
PC3	BGF2	TENS of MINUTES			UNITS of MINUTES			
PC4	PC	BGF1	TENS of HOURS		UNITS of HOURS			

NOTE – Detailed information is given in ANSI/SMPTE 12M.

CF: Color frame
0 = unsynchronized mode
1 = synchronized mode

DF: Drop frame flag
0 = Nondrop frame time code
1 = Drop frame time code

PC: Biphase mark polarity correction
0 = Even
1 = Odd

BGF: Binary group flag

Arb: Arbitrary bit

3.4.2.2.2 Binary group pack (BG)

Table 12 shows the mapping of binary group pack. Binary group data mapped to the binary group packs are the same within each frame.

Table 12 – Mapping of binary group pack

	MSB							LSB
PC0	0	0	0	1	0	1	0	0
PC1	BINARY GROUP2				BINARY GROUP1			
PC2	BINARY GROUP4				BINARY GROUP3			
PC3	BINARY GROUP6				BINARY GROUP5			
PC4	BINARY GROUP8				BINARY GROUP7			

3.5 VAUX section

3.5.1 ID

The ID part of each DIF block in the VAUX section is the same as described in 3.3.1. The section type shall be 010.

3.5.2 Data

The data part (payload) of each DIF block in the VAUX section is shown in figure 6. This figure shows the VAUX pack arrangement for each DIF sequence.

There are 15 packs, each 5 bytes long, and two reserved bytes in each VAUX DIF block payload. A default value for the reserved byte is set to FF_h.

Therefore, there are 45 packs in a DIF sequence. VAUX packs of the DIF blocks are sequentially numbered 0 to 44. This number is called a video pack number.

Table 13 shows the mapping of the VAUX packs of the VAUX DIF blocks. A VAUX source pack (VS) and a VAUX source control pack (VSC) must exist in each frame. The remaining VAUX packs of the DIF blocks in a DIF sequence are reserved and the value of all reserved words is set to FF_h.

If VAUX data are not transmitted, a NO INFO pack, which is filled with FF_h, shall be transmitted.

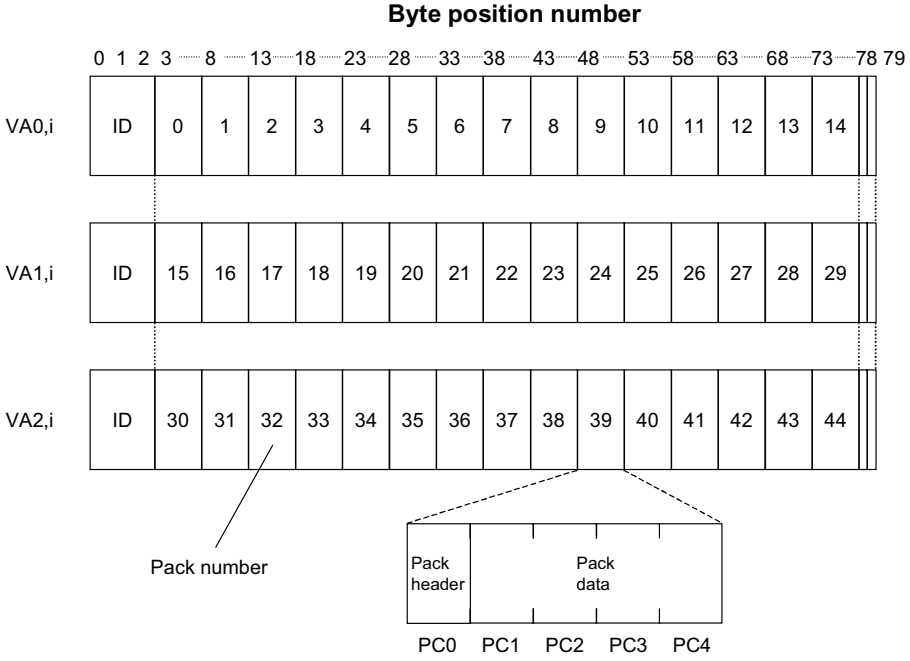


Figure 6 – Data in the VAUX section

Table 13 – Mapping of VAUX pack in a DIF sequence

Pack number		Pack data
Even DIF sequence	Odd DIF sequence	
39	0	VS
40	1	VSC

Even DIF sequence:
DIF sequence number 0, 2, 4, 6, 8 for 60-Hz system
DIF sequence number 0, 2, 4, 6, 8, 10 for 50-Hz system

Odd DIF sequence:
DIF sequence number 1, 3, 5, 7, 9 for 60-Hz system
DIF sequence number 1, 3, 5, 7, 9, 11 for 50-Hz system

3.5.2.1 VAUX source pack (VS)

Table 14 shows the mapping of a VAUX source pack.

Table 14 – Mapping of VAUX source pack

	MSB							LSB
PC0	0	1	1	0	0	0	0	0
PC1	Res	Res	Res	Res	Res	Res	Res	Res
PC2	Res	Res	Res	Res	Res	Res	Res	Res
PC3	Res	Res	50/60	STYPE				
PC4	0	Res	Res	Res	Res	Res	Res	Res

50/60:
0 = 60 Hz system
1 = 50 Hz system

STYPE: Video signal type

For 60 Hz system
1 0 1 0 0 b = 1080/60i - 100 Mb/s compression (active line 1080)
1 0 1 0 1 b = 1080/60i - 100 Mb/s compression (active line 1035)
1 1 0 0 0 b = 720/60p - 100 Mb/s compression
Other = Reserved

For 50 Hz system
1 0 1 0 0 b = 1080/50i - 100 Mb/s compression
Other = Reserved

Res: Reserved bit for future use
Default value shall be set to 1.

3.5.2.2 VAUX source control pack

Table 15 shows mapping of VAUX source control pack.

Table 15 – Mapping of VAUX source control pack

	MSB							LSB
PC0	0	1	1	0	0	0	0	1
PC1	CGMS		Res	Res	Res	Res	Res	Res
PC2	Res	Res	0	0	Res	DISP		
PC3	FF	FS	FC	Res	Res	Res	0	0
PC4	Res	Res	Res	Res	Res	Res	Res	Res

CGMS: Copy generation management system
0 0 b = Copy free
Other = Reserved

DISP: Display select mode
0 1 0 b = 16:9
Other = Reserved

FF: Frame/field flag
For the 1080 line system (See table 16)
FF indicates whether two consecutive fields are delivered, or one field is repeated twice during one video frame period (See table 16)
0 = Only one of the two fields is delivered twice
1 = Both fields are delivered in order.
For the 720 line system (See table 17)
FF indicates whether two consecutive video frames are delivered, or one video frame is repeated twice during the two video frames period.
0 = Only one of the two video frames is delivered twice.
1 = Both video frames are delivered in order.

FS: First/second field flag
For the 1080 line system (See table 16)
FS indicates a field which is delivered during the field one period (See table 16)
0 = Field 2 is delivered
1 = Field 1 is delivered.
For the 720 line system (See table 17)
FS indicates a video frame which is delivered during the video frame one period.
0 = Video frame 2 is delivered.
1 = Video frame 1 is delivered.

Table 16 – FF/FS for the 1080-line system

FF	FS	Output field
1	1	Field 1 and field 2 are output in this order (1,2 sequence).
1	0	Field 2 and field 1 are output in this order (2,1 sequence).
0	1	Field 1 is output twice.
0	0	Field 2 is output twice.

Table 17 – FF/FS for the 720 line system

FF	FS	Output video frame
1	1	Video frame 1 and video frame 2 are output in this order (1,2 sequence).
1	0	Video frame 2 and video frame 1 are output in this order (2,1 sequence).
0	1	Video frame 1 is output twice.
0	0	Video frame 2 is output twice.

FC : Frame change flag

For the 1080 line system

FC indicates whether the picture of the current video frame is repeated based on immediate previous video frame.

0 = Same picture as the previous video frame

1 = Different picture than the previous video frame

For the 720 line system

FC indicates whether the picture of the current two video frames is repeated based on immediate previous two video frames.

0 = Same picture as the previous two video frames

1 = Different picture than the previous two video frames

Res : Reserved bit for future use

Default value shall be set to 1.

3.6 Audio section

3.6.1 ID

The ID part of each DIF block in the audio section is the same as described in 3.3.1. The section type shall be 011.

3.6.2 Data

The data part (payload) of each DIF block in the audio section is shown in figure 7. The data of a DIF block in the audio section are composed of 5 bytes of audio auxiliary data (AAUX) and 72 bytes of audio data which is encoded and shuffled by the process as described in 3.6.2.1 and 3.6.2.2.

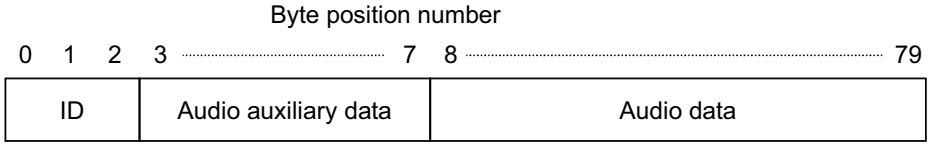


Figure 7 – Data in the audio section

3.6.2.1 Audio encoding

3.6.2.1.1 Source coding

Each audio input signal is sampled at 48kHz, with 16-bit quantization. The system provides eight audio channels. Audio data for each audio channel are located in each respective audio block.

3.6.2.1.2 Emphasis

The audio encoding is carried out with the first order pre-emphasis of 50/15μs. For the analog input recording, emphasis shall be off in the default state.

3.6.2.1.3 Audio error code

In the encoded audio data, 8000_h shall be assigned as an audio error code to indicate an invalid audio sample. This code corresponds to negative full scale value in ordinary twos complement representation. When the encoded data includes 8000_h, it shall be converted to 8001h.

3.6.2.1.4 Relative audio-video timing

1080 line system –

An audio frame begins with an audio sample acquired within the duration of minus 50 samples relative to zero samples from the start of line number 1.

720 line system –

An audio frame begins with an audio sample acquired within the duration of minus 50 samples relative to zero samples from the start of line number 1 of video frame 1.

3.6.2.1.5 Audio frame processing

The audio data is processed in each audio frame. Each audio frame contains 1602 or 1600 audio samples for the 60-Hz system or 1920 audio samples for the 50-Hz system for an audio channel with associated status, user, and validity data. For the 60-Hz system, the number of audio samples per audio frame shall follow the five-frame sequence as shown below:

1600, 1602, 1602, 1602, 1602 samples.

One audio frame shall be capable of 1620 samples for the 60-Hz system or 1944 samples for the 50-Hz system. The unused space at the end of each audio frame is filled with arbitrary values.

3.6.2.2 Audio shuffling

The 16-bit audio data word is divided into two bytes. The upper byte contains MSB, and the lower byte contains LSB, as shown in figure 8. Audio data shall be shuffled over DIF sequences and DIF blocks within an audio frame. The data bytes are defined as D_n (n = 0, 1, 2, ...) which is sampled in the n-th order within an audio frame and shuffled by each D_n unit.

The data shall be shuffled through a process as expressed by the following equations:

60 Hz system –

DIF channel number: i = 0: Audio CH1,CH2
i = 1: Audio CH3,CH4
i = 2: Audio CH5,CH6
i = 3: Audio CH7,CH8

DIF Sequence number: (INT (n/3) + 2 x (n mod 3)) mod 5 for Audio CH1,CH3,CH5,CH7
(INT (n/3) + 2 x (n mod 3)) mod 5 + 5 for Audio CH2,CH4,CH6,CH8

Audio DIF block number: 3 x (n mod 3) + INT ((n mod 45) / 15)

Byte position number: 8 + 2 x INT(n/45) for the most significant byte
9 + 2 x INT(n/45) for the least significant byte

where n = 0 to 1619

50 Hz system –

DIF channel number: i = 0: Audio CH1,CH2
i = 1: Audio CH3,CH4
i = 2: Audio CH5,CH6
i = 3: Audio CH7,CH8

DIF Sequence number: (INT (n/3) + 2 x (n mod 3)) mod 6 for Audio CH1,CH3,CH5,CH7
(INT (n/3) + 2 x (n mod 3)) mod 6 + 6 for Audio CH2,CH4,CH6,CH8

Audio DIF block number: 3 x (n mod 3) + INT ((n mod 54) / 18)

Byte position number: 8 + 2 x INT(n/54) for the most significant byte
9 + 2 x INT(n/54) for the least significant byte

where n = 0 to 1943

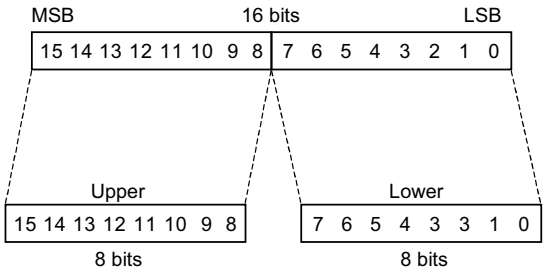


Figure 8 – Conversion of audio sample to audio data bytes

3.6.2.3 Audio auxiliary data (AAUX)

AAUX shall be added to the shuffled audio data as shown in figures 7 and 9. The AAUX pack shall include an AAUX pack header and data (AAUX payload). The length of the AAUX pack shall be 5 bytes as shown in figure 9, which depicts the AAUX pack arrangement. Packs are numbered 0 to 8 as shown in figure 9. This number is called an audio pack number.

Table 18 shows the mapping of an AAUX pack. An AAUX source pack (AS) and an AAUX source control pack (ASC) must be included in the compressed stream.

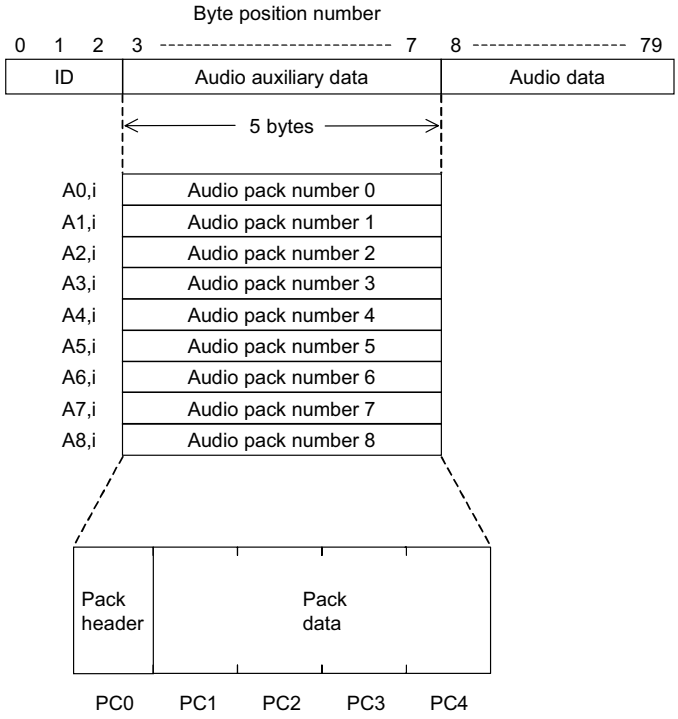


Figure 9 – Arrangement of AAUX packs in audio auxiliary data

Table 18 – Mapping of AAUX pack in a DIF sequence

Audio pack number		
Even DIF sequence	Odd DIF sequence	Pack data
3	0	AS
4	1	ASC

Even DIF sequence :
DIF sequence number 0, 2, 4, 6, 8 for 60-Hz system
DIF sequence number 0, 2, 4, 6, 8, 10 for 50-Hz system

Odd DIF sequence :
DIF sequence number 1, 3, 5, 7, 9 for 60-Hz system
DIF sequence number 1, 3, 5, 7, 9, 11 for 50-Hz system

3.6.2.3.1 AAUX source pack (AS)

The AAUX Source pack is configured as shown in Table 19.

Table 19 – Mapping of AAUX source pack

	MSB							LSB
PC0	0	1	0	1	0	0	0	0
PC1	LF	Res	AF SIZE					
PC2	0	CHN		Res	AUDIO MODE			
PC3	Res	Res	50/60	STYPE				
PC4	Res	Res	SMP		QU			

LF: Locked mode flag
Locking condition of audio sampling frequency with video signal.
0 = Locked mode
1 = Reserved

AF SIZE: The number of audio samples per frame
0 1 0 1 0 0 b = 1600 samples / frame (60-Hz system)
0 1 0 1 1 0 b = 1602 samples / frame (60-Hz system)
0 1 1 0 0 0 b = 1920 samples / frame (50-Hz system)
Other = Reserved

CHN: The number of audio channels within an audio block
0 0 b = One audio channel per an audio block
Other = Reserved
An audio block consists of 45 DIF blocks (9 DIF blocks x 5 DIF sequences) for the 60-Hz system and 54 DIF blocks (9 DIF blocks x 6 DIF sequences) for the 50-Hz system.

AUDIO MODE: The contents of the audio signal on each audio channel
0 0 0 0 b = Audio CH1,CH3,CH5,CH7
0 0 0 1 b = Audio CH2,CH4,CH6,CH8
1 1 1 1 b = Invalid audio data
Other = Reserved

50/60:
0 = 60-Hz system
1 = 50-Hz system

STYPE: Audio blocks for each frame
0 0 0 1 1 b = 8 audio blocks
Other = Reserved

SMP: Sampling frequency
0 0 0 b = 48 kHz
Other = Reserved

QU: Quantization
0 0 0 b = 16 bits linear
Other = Reserved

Res: Reserved bit for future use
Default value shall be set to 1.

3.6.2.3.2 AAUX source control pack (ASC)

The AAUX source control pack is configured as shown in Table 20.

Table 20 – Mapping of AAUX source control pack

	MSB							LSB
PC0	0	1	0	1	0	0	0	1
PC1	CGMS		Res	Res	Res	Res	EFC	
PC2	REC ST	REC END	FADE ST	FADE END	Res	Res	Res	Res
PC3	DRF	SPEED						
PC4	Res	Res	Res	Res	Res	Res	Res	Res

CGMS: Copy generation management system
0 0 b = Copy free
Other = Reserved

EFC: Emphasis audio channel flag
0 0 b = Emphasis off
0 1 b = Emphasis on
Other = Reserved
EFC shall be set for each audio block.

REC ST: Recording start point
0 = Recording start point
1 = Not recording start point
At a recording start frame, REC ST 0 lasts for a duration of one audio block which is equal to 5 or 6 DIF sequences for each audio channel.

REC END: Recording end point
0 = Recording end point
1 = Not recording end point
At a recording end frame, REC END 0 is lasting for a duration of one audio block which is equal to 5 or 6 DIF sequences for each audio channel.

FADE ST: Fading of recording start point
0 = Fading off
1 = Fading on
The FADE ST information is only effective at the recording start frame (REC ST = 0).If FADE ST is 1 at the recording start frame, the output audio signal should be faded in from the first sampling signal of the frame. If FADE ST is 0 at the recording start frame, the output audio signal should not be faded.

FADE END: Fading of recording end point
0 = Fading off
1 = Fading on
The FADE END information is only effective at the recording end frame (REC END = 0). If FADE END is 1 at the recording end frame, the output audio signal should be faded out to the last sampling signal of the frame. If FADE END is 0 at the recording end frame, the output audio signal should not be faded.

DRF: Direction flag
0 = Reverse direction
1 = Forward direction

SPEED: Shuttle speed of VTR (see table 21)

Table 21 – SPEED code definition

Codeword MSB LSB	Shuttle speed of VTR	
	60-Hz system	50-Hz system
0000000	0/120 (=0)	0/100 (=0)
0000001	1/120	1/100
:	:	:
1100100	100/120	100/100 (=1)
:	:	Reserved
1111000	120/120 (=1)	Reserved
:	Reserved	Reserved
1111110	Reserved	Reserved
1111111	Data invalid	Data invalid

Res: Reserved bit for future use
Default value shall be set to 1.

3.7 Video section

3.7.1 ID

The ID part of each DIF block in the video section is the same as described in 3.3.1. The section type shall be 100.

3.7.2 Data

Data part (payload) of each DIF block in Video section consists of 77 bytes of video data which shall be sampled, shuffled and encoded. Video data of every frame is processed as described in clause 4. This 77 byte data are called a compressed macro block.

3.7.2.1 DIF block and compressed macro block

Correspondence between Video DIF blocks and video compressed macro blocks CM h,i,j,k is shown in table 22 for the 60-Hz system and table 23 for the 50-Hz system.

The rule defining the correspondence between video DIF blocks and compressed macro blocks is shown below:

60 Hz system –

```
for(h=0; h<4; h++){
   for(s=0; s<2; s++){
      for(k=0; k<27; k++){
         for(t=0; t<5; t++){
               a = (4h + s + 2t + 2) mod 10;
               b = (4h + s + 2t + 6) mod 10;
               c = (4h + s + 2t + 8) mod 10;
               d = (4h + s + 2t + 0) mod 10;
               e = (4h + s + 2t + 4) mod 10;
               DBNq = (5t + 25k) mod 135;
               DSNp = INT((5t + 25k + 675s) / 135);

               V DBNq, h of DSNp = CM h,a,2,k
               V (DBNq + 1), h of DSNp = CM h,b,1,k
```

```
            V (DBNq + 2), h of DSNp = CM h,c,3,k
            V (DBNq + 3), h of DSNp = CM h,d,0,k
            V (DBNq + 4), h of DSNp = CM h,e,4,k
        }
    }
  }
}
```

where

DBNq: DIF block number
DSNp: DIF sequence number
h: Divided block
s, t: Vertical order of super block
k: Macro block order in super block

50 Hz system –

```
for(h=0; h<4; h++){
  for(k=0; k<27; k++){
    for(i=0; i<11; i++){
            a = (4h + i + 2) mod 11;
            b = (4h + i + 6) mod 11;
            c = (4h + i + 8) mod 11;
            d = (4h + i + 0) mod 11;
            e = (4h + i + 4) mod 11;
            DBNq = (5i + 55k) mod 135;
            DSNp = INT((5i + 55k) / 135);

            V DBNq, h of DSNp = CM h,a,2,k
            V (DBNq + 1), h of DSNp = CM h,b,1,k
            V (DBNq + 2), h of DSNp = CM h,c,3,k
            V (DBNq + 3), h of DSNp = CM h,d,0,k
            V (DBNq + 4), h of DSNp = CM h,e,4,k
    }
  }
}
for(k=0; k<27; k++){
            DBNq = 5k;
            DSNp = 11;

            V DBNq, 0 of DSNp = CM 0,11,0,k
            V (DBNq + 1), 0 of DSNp = CM 0,11,1,k
            V (DBNq + 2), 0 of DSNp = CM 0,11,2,k
            V (DBNq + 3), 0 of DSNp = CM 0,11,3,k
            V (DBNq + 4), 0 of DSNp = CM 0,11,4,k
}
```

where

DBNq: DIF block number
DSNp: DIF sequence number
h: Divided block
i: Vertical order of super block
k: Macro block order in super block

Table 22 – Video DIF blocks and compressed macro blocks for the 60-Hz system

DIF channel number	DIF sequence number	DIF block	Compressed macro block
0	0	V 0,0	CM 0,2,2,0
		V 1,0	CM 0,6,1,0
		V 2,0	CM 0,8,3,0
		V 3,0	CM 0,0,0,0
		V 4,0	CM 0,4,4,0
		:	:
	:	:	:
	9	:	:
		V 134,0	CM 0,3,4,26
1	0	V 0,1	CM 1,6,2,0
		V 1,1	CM 1,0,1,0
		V 2,1	CM 1,2,3,0
		V 3,1	CM 1,4,0,0
		V 4,1	CM 1,8,4,0
		:	:
	:	:	:
	9	:	:
		V 134,1	CM 1,7,4,26
:	:	:	:
3	0	V 0,3	CM 3,4,2,0
		V 1,3	CM 3,8,1,0
		V 2,3	CM 3,0,3,0
		V 3,3	CM 3,2,0,0
		V 4,3	CM 3,6,4,0
		:	:
	:	:	:
	9	:	:
		V 134,3	CM 3,5,4,26

Table 23 – Video DIF blocks and compressed macro blocks for the 50-Hz system

DIF channel number	DIF sequence number	DIF block	Compressed macro block
0	0	V 0,0	CM 0,2,2,0
		V 1,0	CM 0,6,1,0
		V 2,0	CM 0,8,3,0
		V 3,0	CM 0,0,0,0
		V 4,0	CM 0,4,4,0
		:	:
	:	:	:
	10	:	:
		V 134,0	CM 0,3,4,26
	11	V 0,0	CM 0,11,0,0
		V 1,0	CM 0,11,1,0
		:	:
		V 134,0	CM 0,11,4,26
1	0	V 0,1	CM 1,6,2,0
		V 1,1	CM 1,10,1,0
		V 2,1	CM 1,1,3,0
		V 3,1	CM 1,4,0,0
		V 4,1	CM 1,8,4,0
		:	:
	:	:	:
	10	:	:
		V 134,1	CM 1,7,4,26
	11	V 0,1	—
		:	:
		V 134,1	—
:	:	:	:
3	0	V 0,3	CM 3,3,2,0
		V 1,3	CM 3,7,1,0
		V 2,3	CM 3,9,3,0
		V 3,3	CM 3,1,0,0
		V 4,3	CM 3,5,4,0
		:	:
	:	:	:
	10	:	:
		V 134,3	CM 3,4,4,26
	11	V 0,3	—
		:	:
		V 134,3	—

4 Video compression

This clause includes video compression processing for the 1080/60i system, the 1080/50i system, and the 720/60p system.

4.1 Video structure

4.1.1 Video sampling structure

The video sampling structure is defined by SMPTE 274M for the 1080-line system, and SMPTE 296M for the 720-line system. The construction of luminance (Y) and two color-difference signals (CR, C_B) is described in table 24. A sample conversion from 10-bit input video to 8 bits or more is provided by the resampling process (the first processing block of figure 1).

4.1.1.1 Video frame pixel structure

1080/60i system –

The sampling starting point of Y signal shall be 192T from the horizontal sync timing reference;

where $T = 1.001 / (74.25 \times 10^6)$ sec

1920 pixels of luminance and 960 pixels of each color-difference signal per line shall be transmitted as shown in figure 10. The sampling starting point in the active period of C_R and C_B signals shall be the same as the sampling starting point in the active period of the Y signal. Each pixel shall be converted to the code of twos complement (-508 to 507) by inverting the MSB of the input video signal.

1080/50i system –

The sampling starting point of Y signal shall be 192T from the horizontal sync timing reference;

where $T = 1 / (74.25 \times 10^6)$ sec

1920 pixels of luminance and 960 pixels of each color-difference signal per line shall be transmitted as shown in figure 11. The sampling starting point in the active period of C_R and C_B signals shall be the same as the sampling starting point in the active period of the Y signal. Each pixel shall be converted to the code of twos complement (-508 to 507) by inverting the MSB of the input video signal.

720/60p system –

The sampling starting point of Y signal shall be 260T from the horizontal sync timing reference;

where $T = 1.001 / (74.25 \times 10^6)$ sec

1280 pixels of luminance and 640 pixels of each color-difference signal per line shall be transmitted as shown in figure 12. The sampling starting point in the active period of C_R and C_B signals shall be the same as the sampling starting point in the active period of the Y signal. Each pixel shall be converted to the code of twos complement (-508 to 507) by inverting the MSB of the input video signal.

4.1.1.2 Video frame line structure

1080 line system –

540 lines for Y, C_R, and C_B signals from each field shall be transmitted. The transmitted lines in each two fields are described in table 24.

720 line system –

720 lines for Y, C_R and C_B signals from each video frame shall be transmitted. The transmitted lines in each video frame are described in table 24.

4.1.1.3 Horizontal resampling

1080/60i system –

1920 horizontally sampled Y signals shall be resampled to 1280 pixels. The 960 horizontally sampled C_R and C_B signals shall be resampled to 640 pixels. The output signal of the resampler shall have a sample resolution equal to 8 bits or more. (See annex B.)

1080/50i system –

1920 horizontally sampled Y signals shall be resampled to 1440 pixels. The 960 horizontally sampled C_R and C_B signals shall be resampled to 720 pixels. The output signal of the resampler shall have a sample resolution equal to 8 bits or more. (See annex B.)

720/60p system –

The 1280 horizontally sampled Y signals shall be resampled to 960 pixels. The 640 horizontally sampled C_R and C_B signals shall be resampled to 480 pixels. The output signal of the resampler shall have a sample resolution equal to 8 bits or more. (See annex B.)

Table 24 – Construction of input video

		1080/60i system	1080/50i system	720/60p system
Sampling frequency	Y	74.25 / 1.001 MHz	74.25 MHz	74.25 / 1.001 MHz
	CR, CB	37.125 / 1.001 MHz	37.125 MHz	37.125 / 1.001 MHz
Total number of pixels per line	Y	2200		1650
	CR, CB	1100		825
The number of active pixels per line	Y	1920		1280
	CR, CB	960		640
Total number of lines per video frame		1125		750
The number of active lines per video frame		1080		720
The active line numbers		Field 1	21 to 560	26 to 745
		Field 2	584 to 1123	
Quantization		Each sample is linearly quantized to 10 bits for Y, CR and CB.		
The relation between video signal level and quantized level	Scale	4 to 1019		
	Y	Video signal level of white: 940 Video signal level of black: 64		Quantized level 877
	CR, CB	Video signal level of gray: 512		Quantized level 897

SMPTE 370M-2002

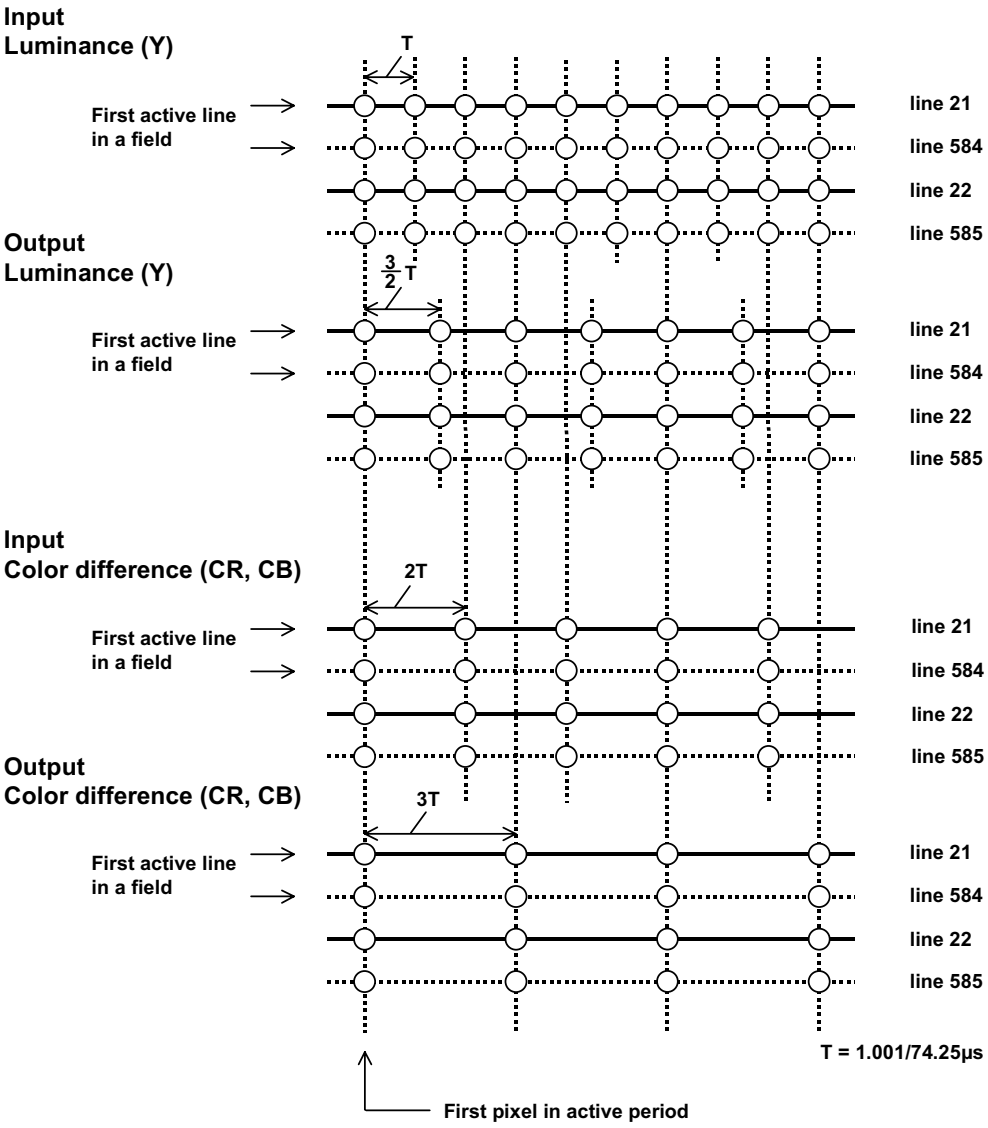


Figure 10 – Sampling structure for the 1080/60i system

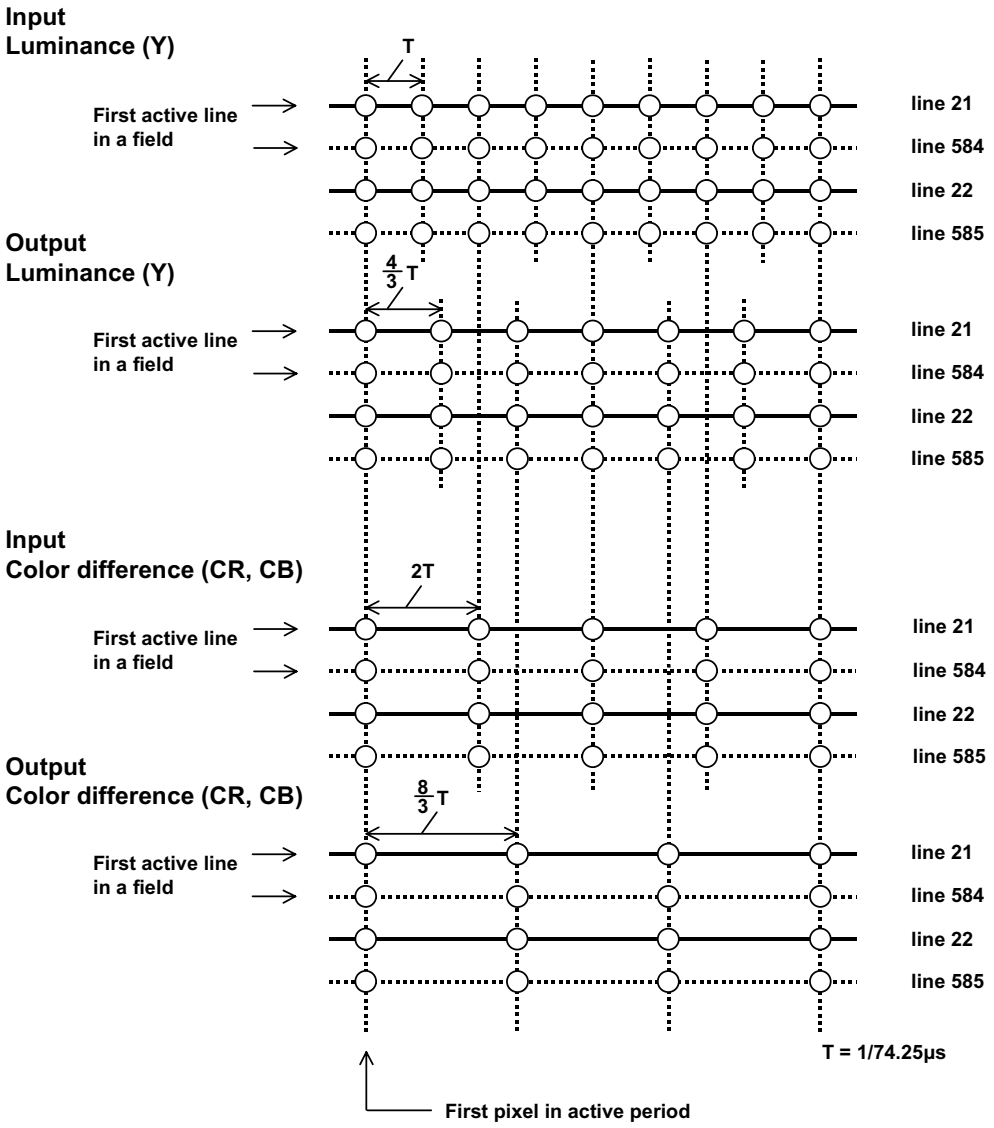


Figure 11 – Sampling structure for the 1080/50i system

SMPTE 370M-2002

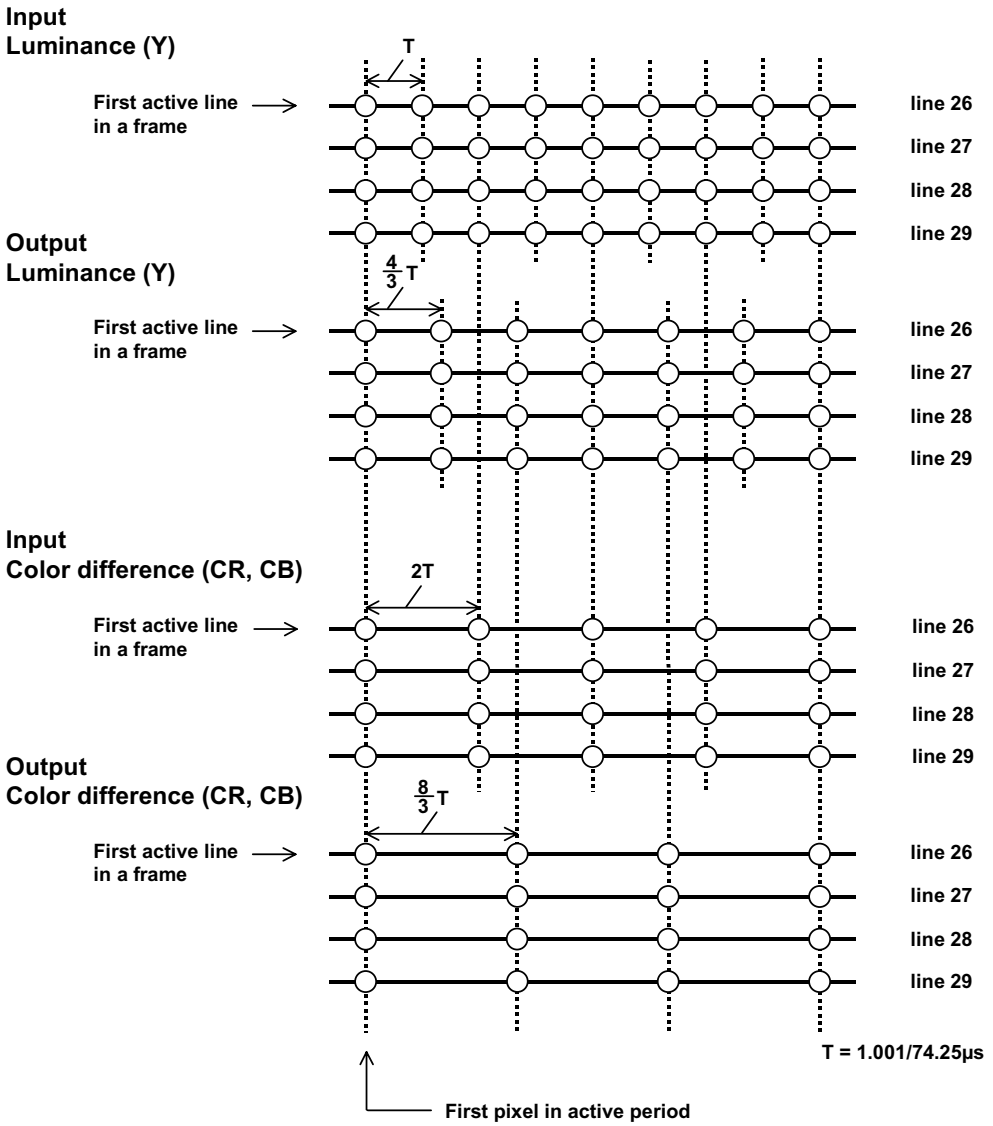


Figure 12 – Sampling structure for the 720/60p system

4.1.2 DCT block

The Y, C_R, and C_B pixels in each video frame shall be divided into DCT blocks as shown in figure 13 for the 1080 line system, and figure 14 for the 720-line system. DCT blocks are structured with a rectangular area of eight vertical pixels and eight horizontal pixels in a video frame. The value of x shows the horizontal coordinate from the left and the value of y shows the vertical coordinate from the top. For the 1080-line system, even lines of y = 0, 2, 4, 6 are the horizontal lines of field one, and odd lines of y = 1, 3, 5, 7 are those of field two.

DCT block arrangement in each video frame

1080/60i system –

The arrangement of horizontal DCT blocks in each video frame is shown in figure 15. The same horizontal arrangement is repeated to 135 DCT blocks in the vertical direction. Pixels in one video frame are divided into 43200 DCT blocks.

Y: 135 Vertical DCT blocks x 160 horizontal DCT blocks = 21600 DCT blocks
C_R: 135 vertical DCT blocks x 80 horizontal DCT blocks = 10800 DCT blocks
C_R: 135 vertical DCT blocks x 80 horizontal DCT blocks = 10800 DCT blocks

1080/50i system –

The arrangement of horizontal DCT blocks in each video frame is shown in figure 16. The same horizontal arrangement is repeated to 135 DCT blocks in the vertical direction. Pixels in one video frame are divided into 48600 DCT blocks.

Y: 135 Vertical DCT blocks x 180 horizontal DCT blocks = 24300 DCT blocks
C_R: 135 vertical DCT blocks x 90 horizontal DCT blocks = 12150 DCT blocks
C_R: 135 vertical DCT blocks x 90 horizontal DCT blocks = 12150 DCT blocks

720/60p system –

The arrangement of horizontal DCT blocks in each video frame is shown in figure 17. The same horizontal arrangement is repeated to 90 DCT blocks in the vertical direction. Pixels in one video frame are divided into 21600 DCT blocks.

Y: 90 vertical DCT blocks x 120 horizontal DCT blocks = 10800 DCT blocks
C_R: 90 vertical DCT blocks x 60 horizontal DCT blocks = 5400 DCT blocks
C_R: 90 vertical DCT blocks x 60 horizontal DCT blocks = 5400 DCT blocks

4.1.3 Macro block

Each macro block consists of eight DCT blocks. Figure 18 for the 1080-line system and figure 19 for the 720-line system show the relationship between macro block and DCT blocks.

4.1.3.1 Arrangement of macro block

1080/60i system –

Macro block arrangement in each video frame has two steps.

Step1: Arranging macro blocks

Pixels in each video frame are divided into 5400 macro blocks as shown in figure 20.

Each macro block except the bottom macro blocks consists of four DCT blocks of Y which are horizontally and vertically adjacent, two vertically adjacent DCT blocks of CR and two vertically adjacent DCT blocks of C_B on a TV screen;

where, 67 vertical macro blocks x 80 horizontal macro blocks = 5360 macro blocks.

Each bottom macro block consists of four horizontally adjacent DCT blocks of Y, two horizontally adjacent DCT blocks of CR and two horizontally adjacent DCT blocks of C_B on a TV screen;

where, 1 vertical macro blocks x 40 horizontal macro blocks = 40 macro blocks.

Step 2: Rearranging macro blocks

Sets consisting of 40 macro blocks which are named A0 to A7 and sets consisting of 30 macro blocks which are named A8 to A15 are arranged as shown in figure 20.

40 macro blocks in A16 are arranged into 4 vertical macro blocks x 10 horizontal macro blocks in B16 respectively as shown in figure 20;

where, 60 vertical macro blocks x 90 horizontal macro blocks = 5400 macro blocks

1080/50i system –

Macro block arrangement in each video frame has two steps.

Step1 : Arranging macro blocks

Pixels in each video frame are divided into 6075 macro blocks as shown in figure 21.

Each macro block except the bottom macro blocks consists of four DCT blocks of Y which are horizontally and vertically adjacent, two vertically adjacent DCT blocks of C_R and two vertically adjacent DCT blocks of C_B on a TV screen;

where, 67 vertical macro blocks x 90 horizontal macro blocks = 6030 macro blocks.

Each bottom macro block consists of four horizontally adjacent DCT blocks of Y, two horizontally adjacent DCT blocks of C_R and two horizontally adjacent DCT blocks of C_B on a TV screen;

where, 1 vertical macro blocks x 45 horizontal macro blocks = 45 macro blocks.

Step 2 : Rearranging macro blocks

Macro blocks are divided into a main unit and an edge unit. The edge unit contains top macro blocks in A0 and bottom macro blocks in A1 as shown in figure 21. The main unit contains the remaining blocks;

where,
main unit: 66 vertical macro blocks x 90 horizontal macro blocks = 5940 macro blocks
edge unit: 1 vertical macro blocks x 135 horizontal macro blocks = 135 macro blocks

720/60p system –

Pixels in each video frame are divided into 2700 macro blocks as shown in figure 22;

where, 45 vertical macro blocks x 60 horizontal macro blocks = 2700 macro blocks

4.1.3.2 Divided blocks

1080/60i system –

Macro blocks in each video frame are divided into halfway blocks as shown in figure 23. Each halfway block H consists of nine macro blocks horizontally and one macro block vertically.

Halfway blocks H are distributed into divided blocks as follows:

Divided blocks: h=0 : H 2m,2n
h=1 : H 2m,2n+1

h=2 : H 2m+1,2n
h=3 : H 2m+1,2n+1
where, m=0,1,2,...,29
n=0,1,2,3,4

As a result, one video frame is divided into four divided blocks. Each divided block consists of 30 vertical macro blocks x 45 horizontal macro blocks.

1080/50i system –

Macro blocks in the main unit are divided into halfway blocks as shown in figure 24. Each halfway block H consists of nine horizontally adjacent macro blocks.

Halfway blocks H are distributed into divided blocks as follows:

Divided blocks: h=0 : H 2m,2n
h=1 : H 2m,2n+1
h=2 : H 2m+1,2n
h=3 : H 2m+1,2n+1
where, m=0,1,2,...,32
n=0,1,2,3,4

As a result, the main unit is divided into four divided blocks. Each divided block is consists of 33 vertical macro blocks x 45 horizontal macro blocks.

720/60p system –

Macro blocks in each video frame are divided into halfway blocks as shown in Figure 25. Each halfway block H consists of six macro blocks horizontally and one macro block vertically.

Halfway blocks H are distributed into divided blocks as follows bellow:

Divided blocks: h=0 : H m, 2n
h=1 : H m, 2n+1
h=2 : H m+45, 2n
h=3 : H m+45, 2n+1
where, m=0,1,2,...,44
n=0,1,2,3,4

As a result, each two video frames are divided into four divided blocks. Each divided block is consists of 45 vertical macro blocks x 30 horizontal macro blocks.

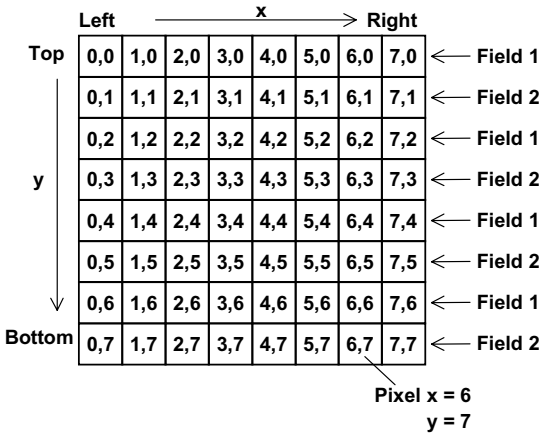


Figure 13 – DCT block and the pixel coordinates for the 1080-line system

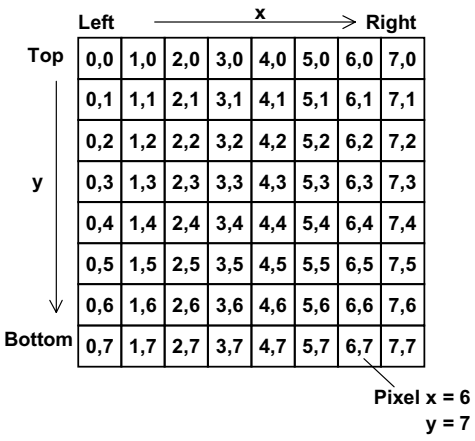


Figure 14 – DCT block and the pixel coordinates for the 720-line system

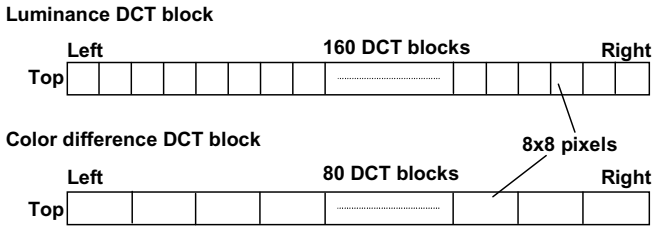


Figure 15 – DCT block arrangement for the 1080/60i system

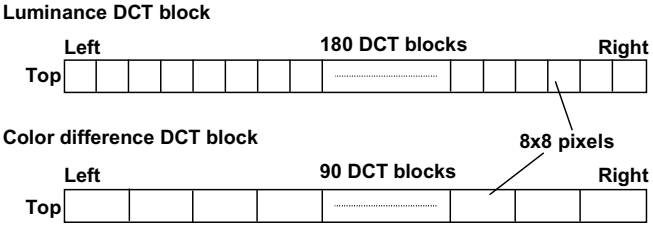


Figure 16 – DCT block arrangement for the 1080/50i system

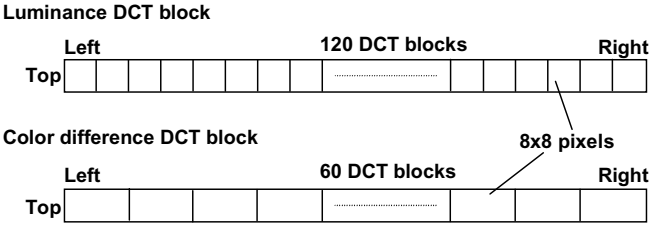


Figure 17 – DCT block arrangement for the 720/60p system

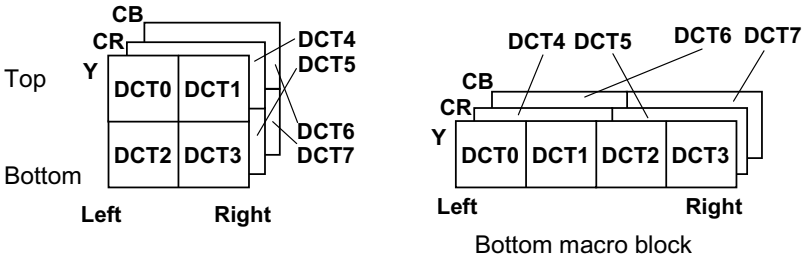


Figure 18 – Macro block and DCT blocks for the 1080-line system

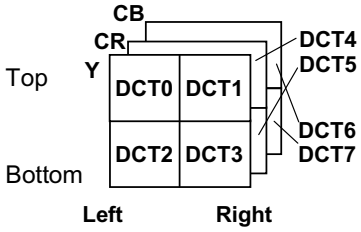


Figure 19 – Macro block and DCT blocks for the 720-line system

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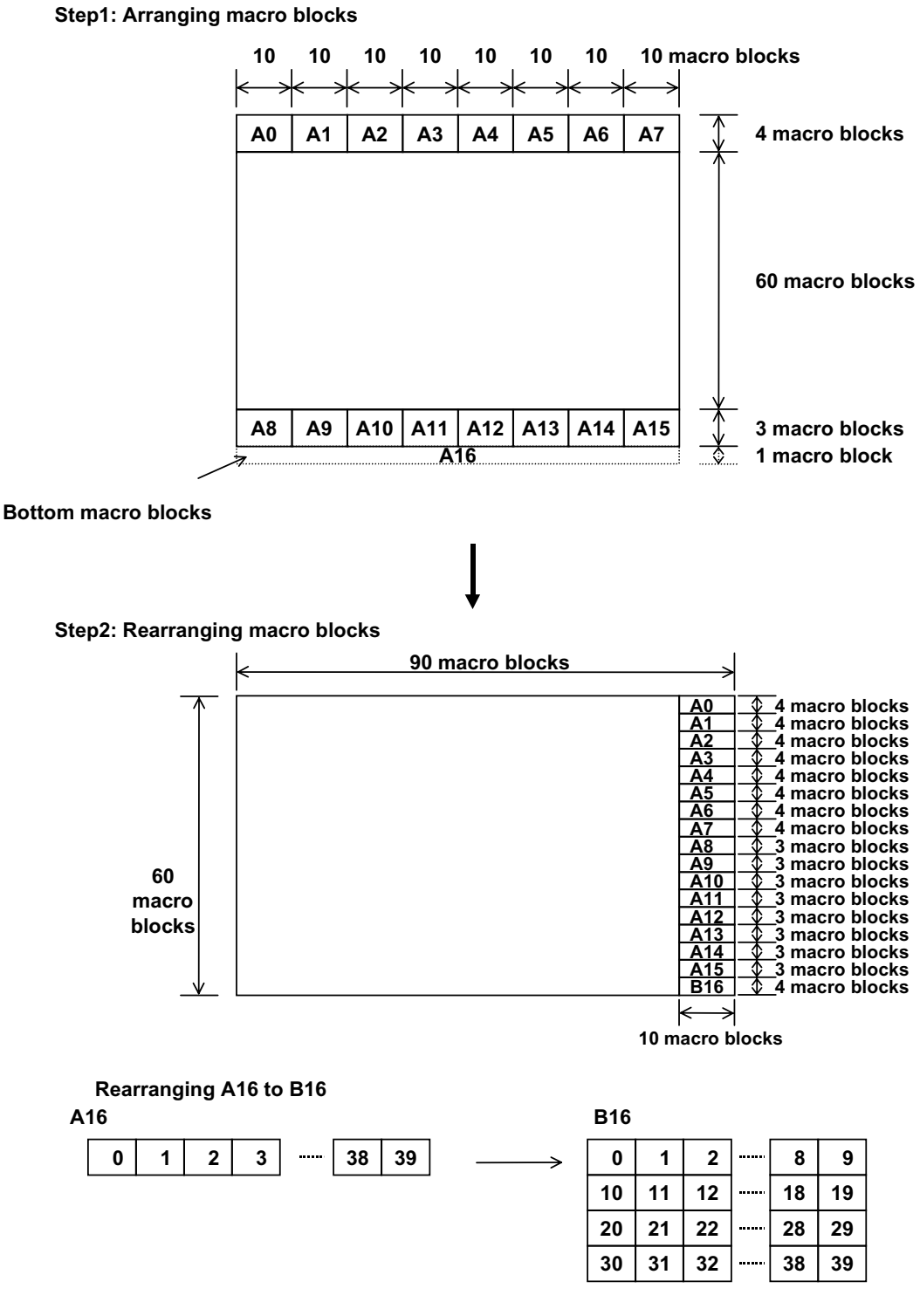

Figure 20 – Arrangement of macro blocks for the 1080/60i system

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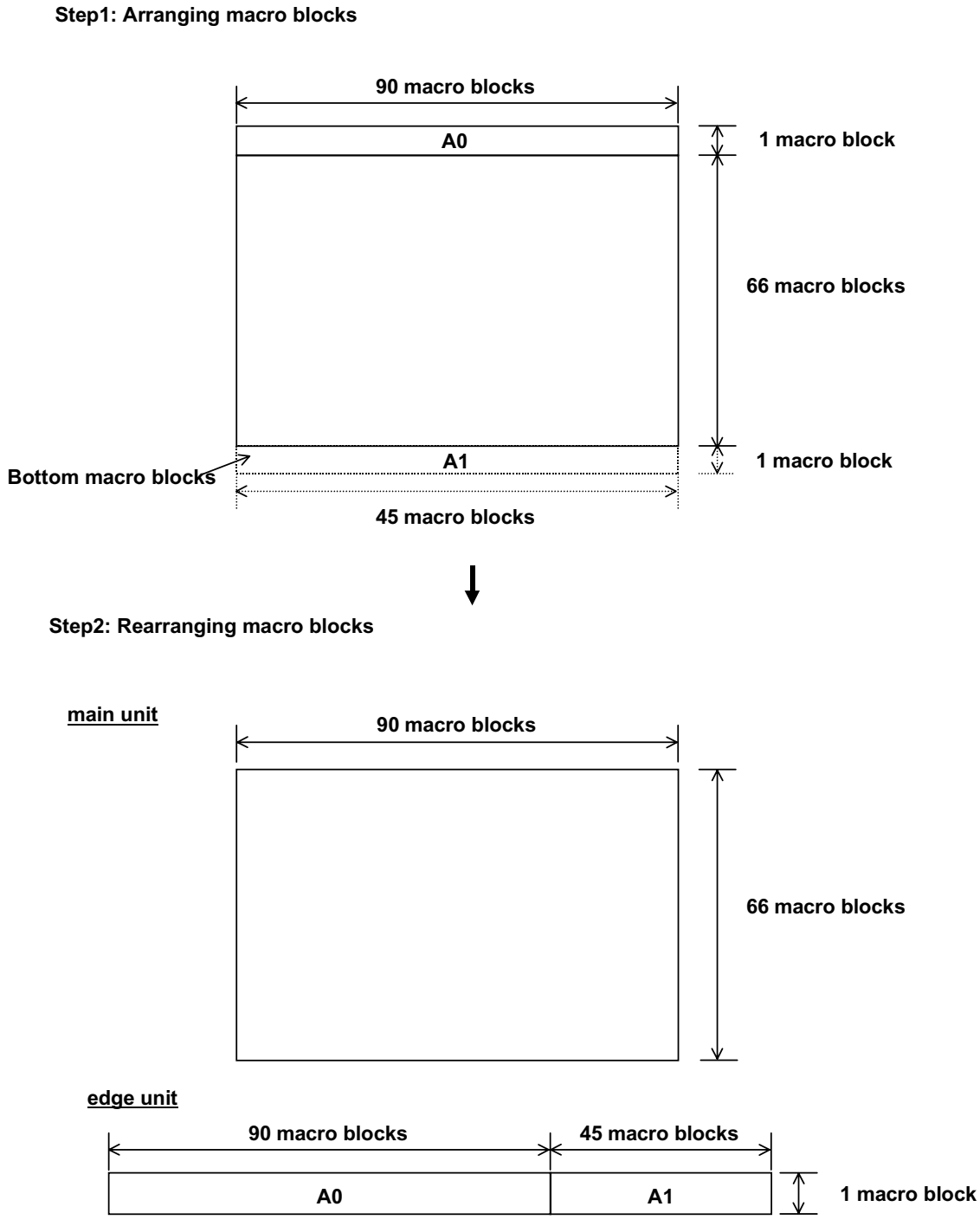

Figure 21 – Arrangement of macro blocks for the 1080/50i system

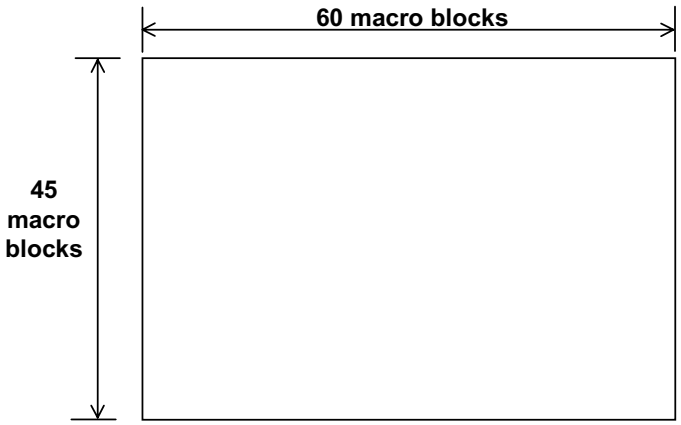

Figure 22 – Arrangement of macro blocks for the 720/60p system

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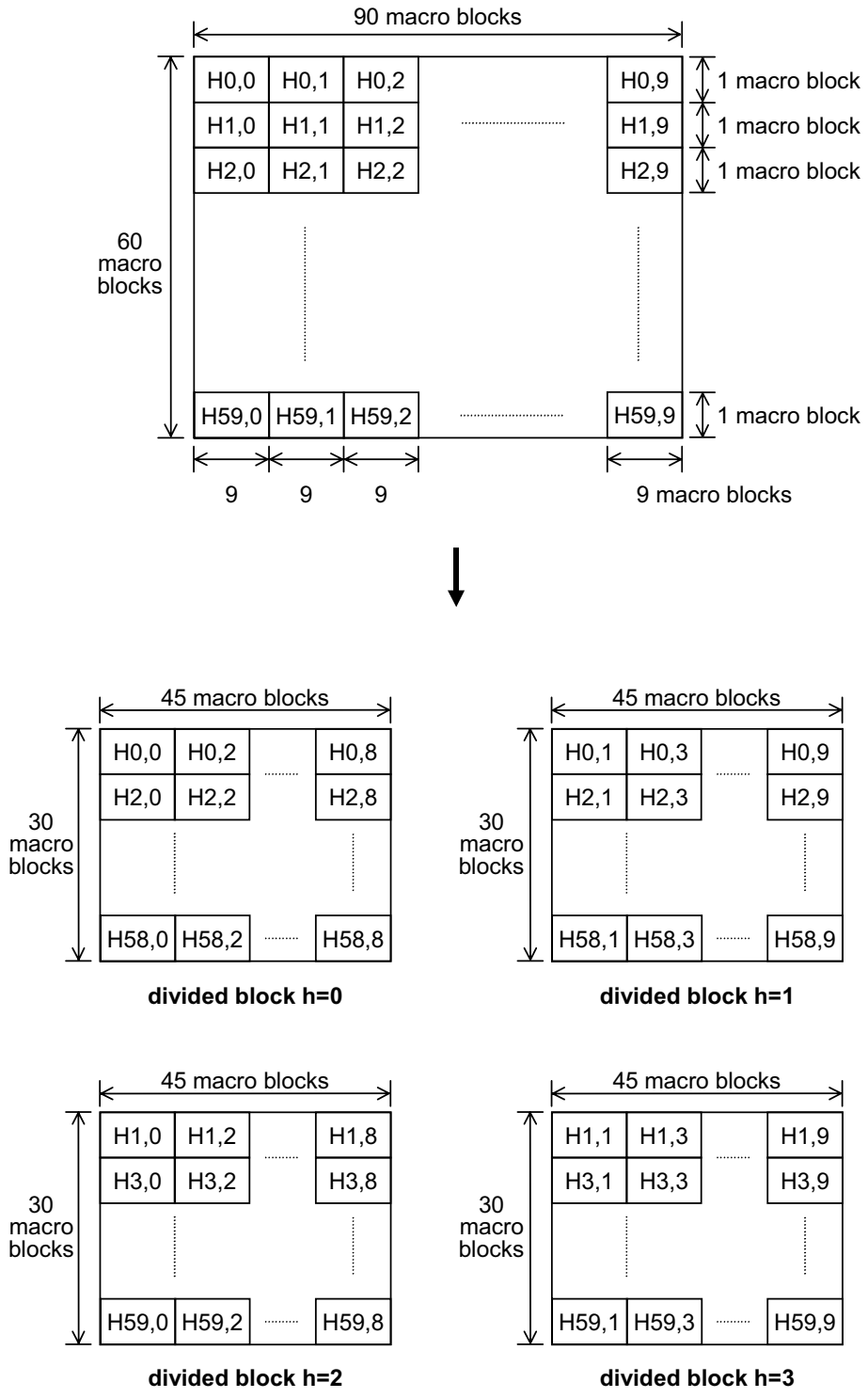

Figure 23 – Divided blocks for the 1080/60i system

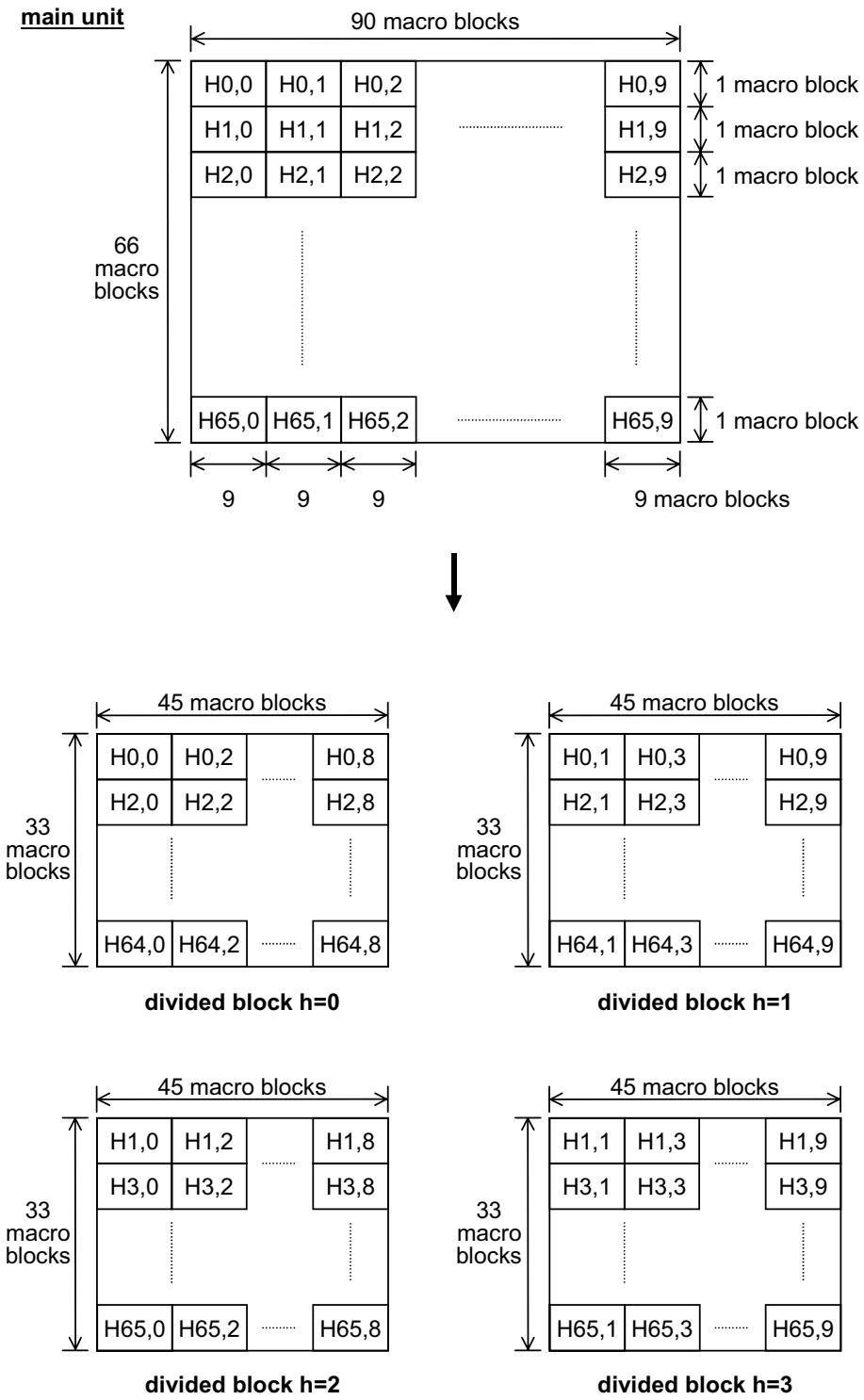

Figure 24 – Divided blocks for the 1080/50i system

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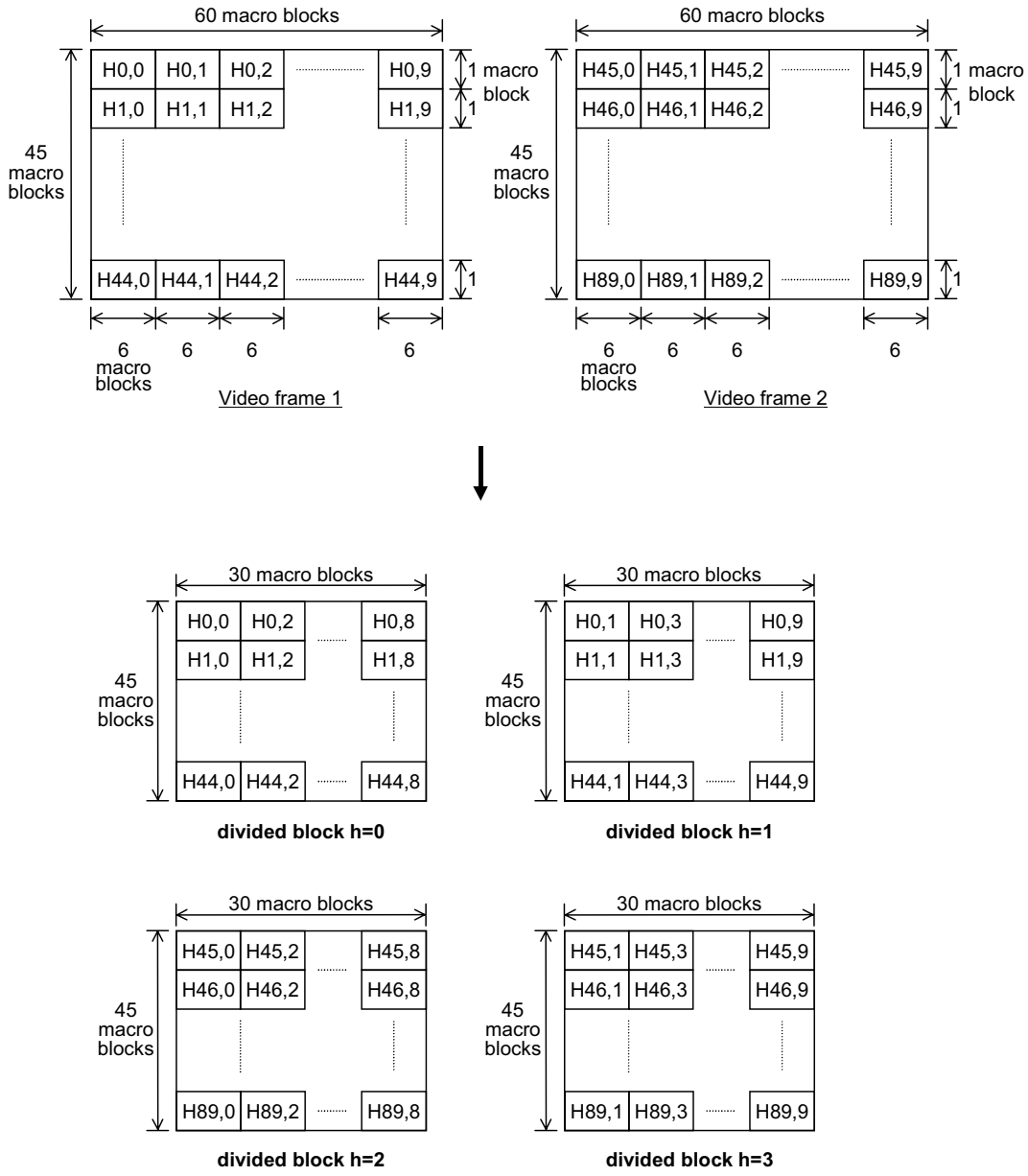

Figure 25 – Divided blocks for the 720/60p system

4.1.4 Super block

Each super block consists of 27 macro blocks.

1080/60i system –

The arrangement of super blocks in a divided block is shown in figure 26. The pixels in a divided block are divided into 50 super blocks.

10 vertical super blocks x 5 horizontal super blocks = 50 super blocks.

1080/50i system –

The arrangement of super blocks in a divided block is shown in figure 28. The pixels in a divided block are divided into 55 super blocks.

11 vertical super blocks x 5 horizontal super blocks = 55 super blocks.

The pixels in the edge unit are divided into 5 super blocks.

1 vertical super blocks x 5 horizontal super blocks = 5 super blocks.

720/60p system –

The arrangement of super blocks in a divided block is shown in figure 30. The pixels in a divided block are divided into 50 super blocks.

10 vertical super blocks x 5 horizontal super blocks = 50 super blocks.

4.1.5 Definition of super block number, macro block number and value of the pixel

Super block number – The super block number is expressed as S h,i,j shown in figures 26, 28, and 30.

S h,i,j where	h: the divided block	h = 0, …, 3	
	i: the vertical order of the super block	i = 0, …, 9	for 60-Hz system
		i = 0, …, 11	for 50-Hz system
	j: the horizontal order of the super block	j = 0, …, 4	

Macro block number – The macro block number is expressed as M h,i,j,k. The symbol k is the macro block order in the super block shown in figure 27 for the 1080/60i system, figure 29 for the 1080/50i system, and figure 31 for the 720/60p system. The small rectangle in these figures shows a macro block, and a number in the small rectangle expresses k.

M h,i,j,k where h,i, j: the super block number
k: the macro block order in the super block k = 0, …,26

Pixel location – The pixel location is expressed as P h,i,j,k,l(x,y). The pixel is indicated as the suffix of h, i, j, k, l (x, y). The symbol l is the DCT block order in a macro block shown in figures 18 and 19. The rectangle in the figure shows a DCT block, and a DCT number in the rectangle expresses l. The symbol x and y are the pixel coordinate in the DCT block as described in 4.1.2.

P h,i,j,k,l(x,y) where h,i, j, k: the macro block number
l: the DCT block order in the macro block
(x, y): the pixel coordinate in the DCT block x = 0, …, 7 y = 0, …, 7

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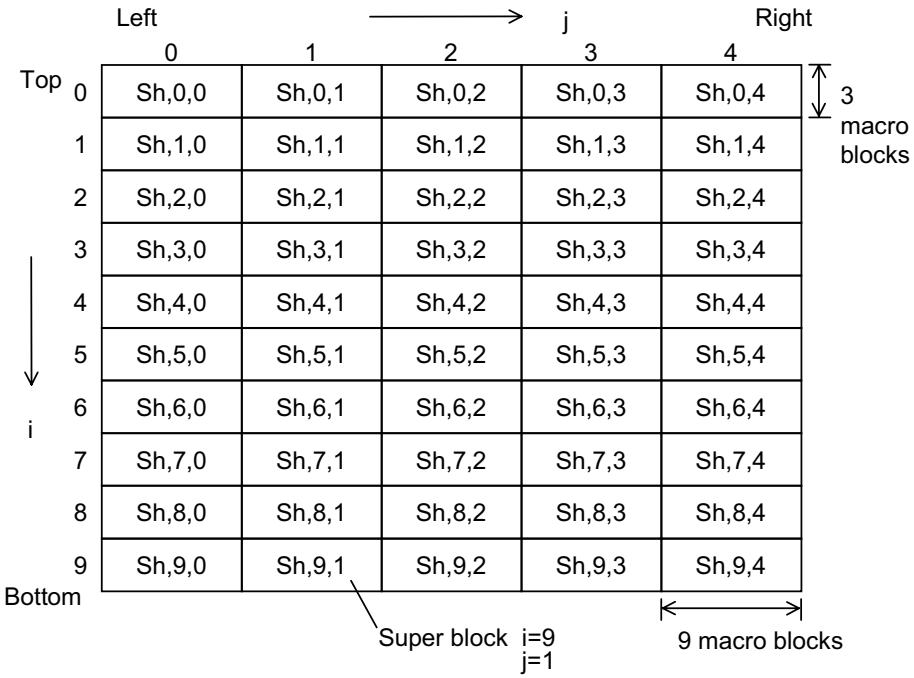

Figure 26 – Super blocks and macro blocks in a divided block for the 1080/60i system

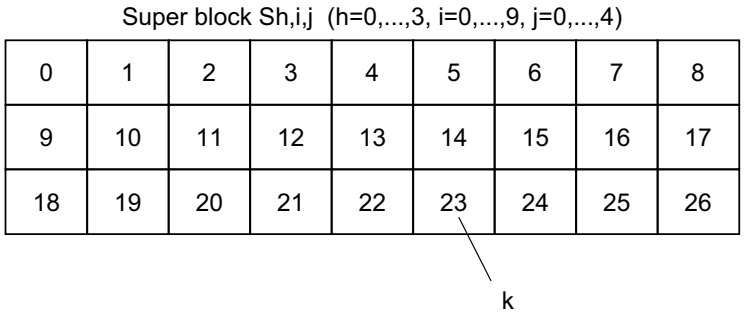

Figure 27 – Macro block order in a super block for the 1080/60i system

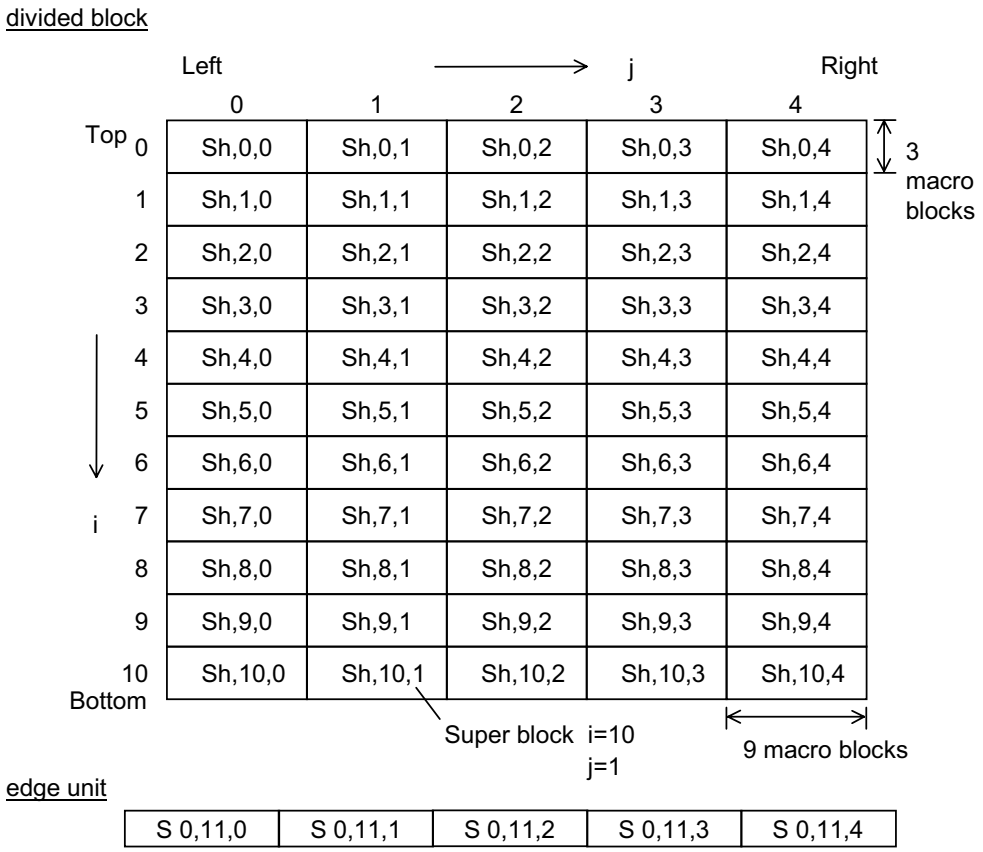

Figure 28 – Super blocks and macro blocks for the 1080/50i system

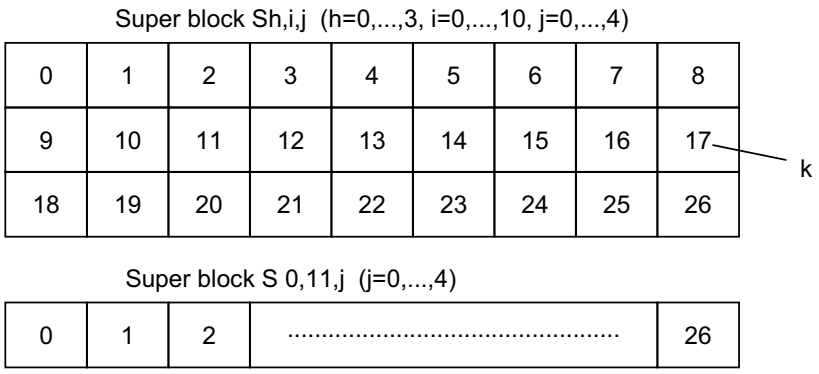

Figure 29 – Macro block order in a super block for the 1080/50i system

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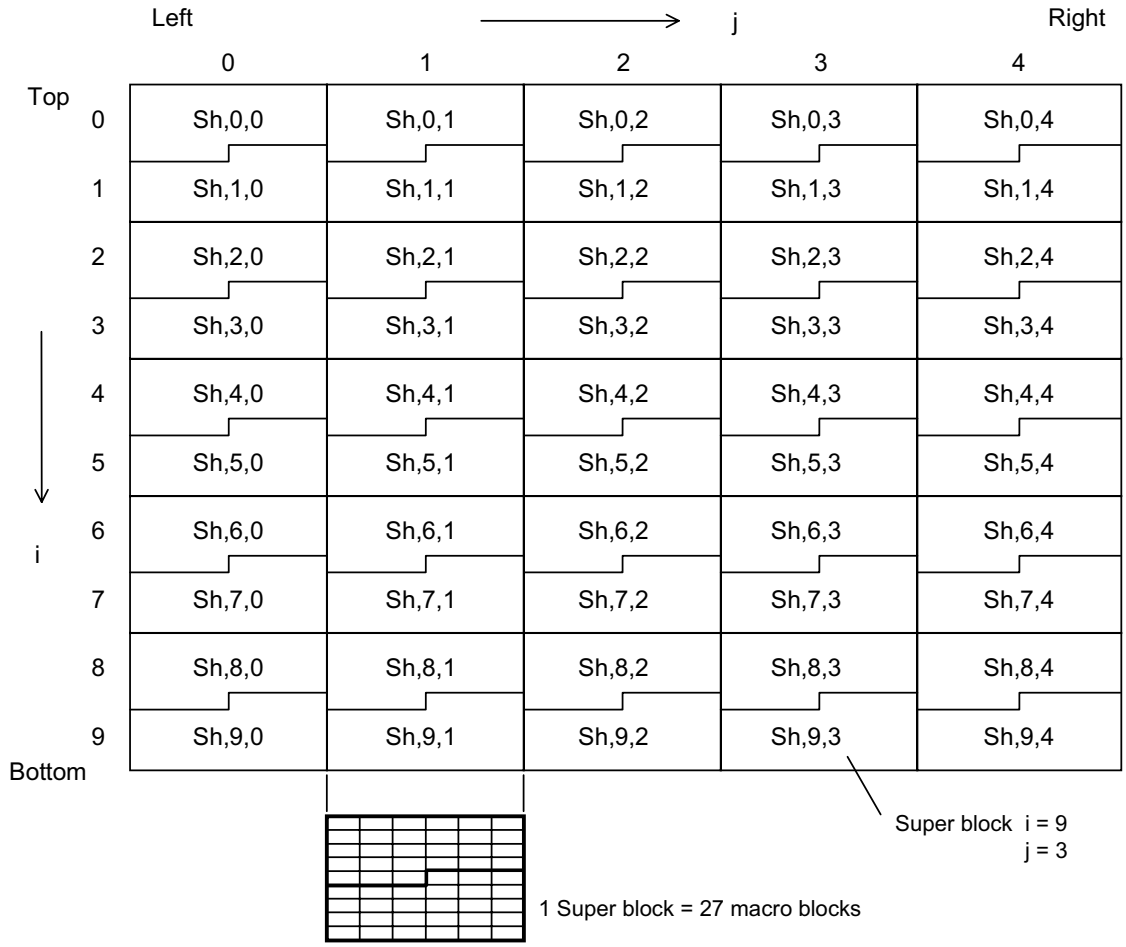

Figure 30 – Super blocks and macro blocks in a divided block for the 720/60p system

Super block Sh,i,j (h=0,...,3, i=0,...,9, j=0,...,4)

0	1	2	3	4	5
6	7	8	9	10	11
12	13	14	15	16	17
18	19	20	21	22	23
24	25	26	0	1	2
3	4	5	6	7	8
9	10	11	12	13	14
15	16	17	18	19	20
21	22	23	24	25	26

k

Figure 31 – Macro block order in a super block for the 720/60p system

4.1.6 Definition of video segment and compressed macro block

A video segment consists of five macro blocks which are assembled from various areas within the video frame.

60-Hz system –

M h,a,p,k where a = (i + 2) mod 10, p = 2
M h,b,q,k where b = (i + 6) mod 10, q = 1
M h,c,r,k where c = (i + 8) mod 10, r = 3
M h,d,s,k where d = (i + 0) mod 10, s = 0
M h,e,t,k where e = (i + 4) mod 10, t = 4

where h: the divided block h = 0, …, 3
i: the vertical order of the super block i = 0, …, 9
k: the macro block order in the super block k = 0, …, 26

50-Hz system –

divided block

M h,a,p,k where a = (i + 2) mod 11, p = 2
M h,b,q,k where b = (i + 6) mod 11, q = 1
M h,c,r,k where c = (i + 8) mod 11, r = 3
M h,d,s,k where d = (i + 0) mod 11, s = 0
M h,e,t,k where e = (i + 4) mod 11, t = 4

where h: the divided block h = 0, …, 3
i: the vertical order of the super block i = 0, …, 10
k: the macro block order in the super block k = 0, …, 26

edge unit

M h,a,p,k where h = 0, a = 11, p = 0
M h,b,q,k where h = 0, b = 11, q = 1
M h,c,r,k where h = 0, c = 11, r = 2
M h,d,s,k where h = 0, d = 11, s = 3
M h,e,t,k where h = 0, e = 11, t = 4

where k: the macro block order in the super block k = 0, …, 26

Each video segment before the bit rate reduction is expressed as V h,i,k which consists of M h,a,p,k; M h,b,q,k; M h,c,r,k; M h,d,s,k; and M h,e,t,k.

The bit-rate reduction process is operated sequentially from M h,a,p,k to M h,e,t,k. The data in a video segment are compressed and transformed to a 385-byte data stream. A set of compressed video data consists of five compressed macro blocks. Each compressed macro block consists of 77 bytes and is expressed as CM. Each video segment after the bit-rate reduction is expressed as CV h,i,k which consists of CM h,a,p,k; CM h,b,q,k; CM h,c,r,k; CM h,d,s,k; and CM h,e,t,k as shown below:

CM h,a,p,k :

This block includes all parts or most parts of the compressed data from macro block M h,a,p,k and may include the compressed data of macro block M h,b,q,k; or M h,c,r,k; or M h,d,s,k; or M h,e,t,k.

CM h,b,q,k :

This block includes all parts or most parts of the compressed data from macro block M h,b,q,k and may include the compressed data of macro block M h,a,p,k; or M h,c,r,k; or M h,d,s,k; or M h,e,t,k.

CM h,c,r,k :

This block includes all parts or most parts of the compressed data from macro block M h,c,r,k and may include the compressed data of macro block M h,a,p,k; or M h,b,q,k; or M h,d,s,k; or M h,e,t,k.

CM h,d,s,k :

This block includes all parts or most parts of the compressed data from macro block M h,d,s,k and may include the compressed data of macro block M h,a,p,k; or M h,b,q,k; or M h,c,r,k; or M h,e,t,k.

CM h,e,t,k :

This block includes all parts or most parts of the compressed data from macro block M h,e,t,k and may include the compressed data of macro block M h,a,p,k; or M h,b,q,k; or M h,c,r,k; or M h,d,s,k.

4.2 DCT processing

Four rows of eight horizontal pixels from each field of a video frame form a DCT block in the 1080-line system. Eight rows of eight horizontal pixels from a video frame form a DCT block in the 720-line system.

The DCT transformation from 64 pixels in a DCT block whose numbers are h, i, j, k, l (x, y) to 64 coefficients whose numbers are h, i, j, k, l (u, v) is described as follows:

P h,i,j,k,l(x,y) is the value of the pixel and C h,i,j,k,l(u,v) is the value of the coefficient.

For u = 0 and v = 0, the coefficient is called DC coefficient.
All other coefficients are called AC coefficients.

4.2.1 DCT mode

For the 1080-line system, there are used two DCT modes for purpose to improve picture quality after bit rate reduction. These modes are called the 8-8-frame-DCT mode and the 8-8-field-DCT mode. The 8-8-frame-DCT mode should be selected when the difference between two fields in a video frame is small. The 8-8-field-DCT mode should be selected when the difference between two fields in a video frame is large.

For the 720-line system, the 8-8-frame-DCT mode should be selected.

The same DCT mode is applied to the DCT blocks in a macro block.

As shown in figure 32, if the 8-8-field-DCT mode is selected, pixels in the two vertical adjacent DCT blocks are rearranged to form re-arranged DCT blocks that contain pixels from the same field.

The following DCT paragraph shows the algorithm that is applied to both DCT modes, the 8-8-frame-DCT and the 8-8-field-DCT modes.

DCT :

$$C_{h,i,j,k,l}(u,v) = C(v)\,C(u) \sum_{y=0}^{7} \sum_{x=0}^{7} \left(P_{h,i,j,k,l}(x,y)\, \cos(\pi v(2y+1)/16)\, \cos(\pi u(2x+1)/16)\right)$$

Inverse DCT:

$$P_{h,i,j,k,l}(x,y) = \sum_{v=0}^{7} \sum_{u=0}^{7} (C(v)\, C(u)\, C_{h,i,j,k,l}(u,v) \cos(\pi v(2y+1)/16) \cos(\pi u(2x+1)/16))$$

where :

$C(u) = 0.5 / \sqrt{2}$ for u = 0
$C(u) = 0.5$ for u = 1 to 7
$C(v) = 0.5 / \sqrt{2}$ for v = 0
$C(v) = 0.5$ for v = 1 to 7

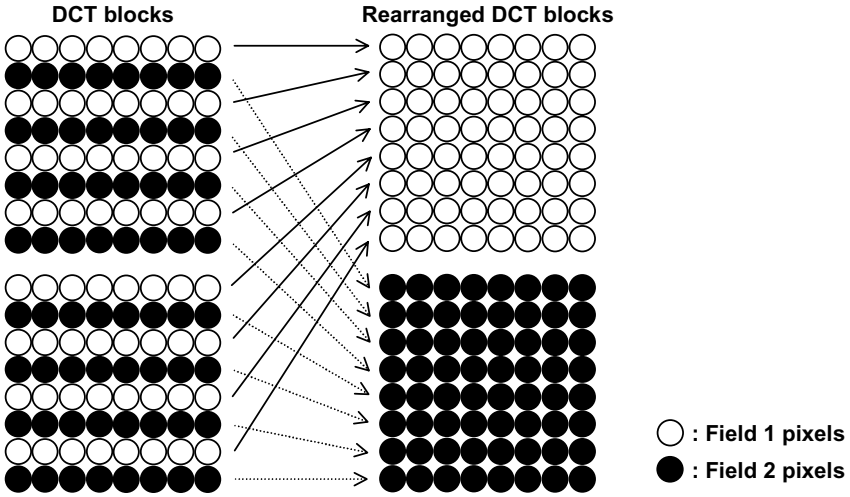

Figure 32 – Rearrangement of pixels in the 8-8-field-DCT mode

4.2.2 Weighting

The DCT coefficients $C_{h,i,j,k,l}(u,v)$ shall be weighted by quantizer matrix. Different quantizer matrices can be set for luminance signals and color difference signals as shown in figure 33 for the 1080/60i system, figure 34 for the 1080/50i system, and figure 35 for the 720/60p system.

4.2.3 Output order

Figure 36 shows the output order of the weighted coefficients.

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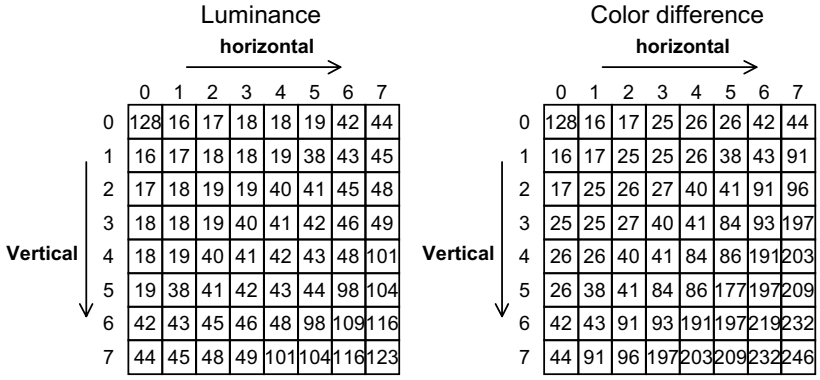
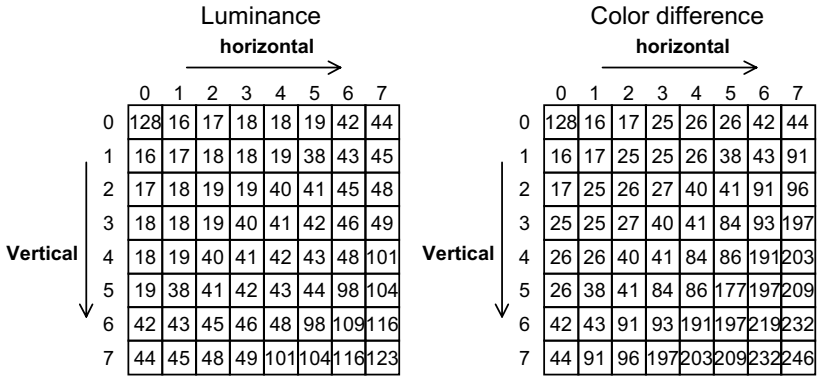


	0	1	2	3	4	5	6	7
0	128	16	17	18	18	19	42	44
1	16	17	18	18	19	38	43	45
2	17	18	19	19	40	41	45	48
3	18	18	19	40	41	42	46	49
4	18	19	40	41	42	43	48	101
5	19	38	41	42	43	44	98	104
6	42	43	45	46	48	98	109	116
7	44	45	48	49	101	104	116	123

	0	1	2	3	4	5	6	7
0	128	16	17	25	26	26	42	44
1	16	17	25	25	26	38	43	91
2	17	25	26	27	40	41	91	96
3	25	25	27	40	41	84	93	197
4	26	26	40	41	84	86	191	203
5	26	38	41	84	86	177	197	209
6	42	43	91	93	191	197	219	232
7	44	91	96	197	203	209	232	246

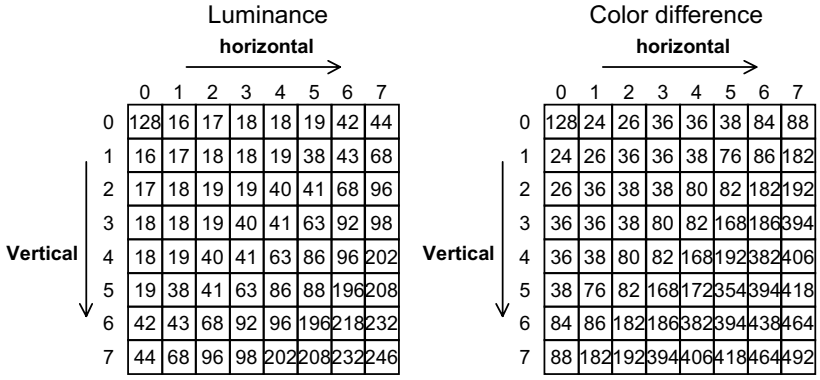
Figure 33 – Quantizer matrix for the 1080/60i system



	0	1	2	3	4	5	6	7
0	128	16	17	18	18	19	42	44
1	16	17	18	18	19	38	43	45
2	17	18	19	19	40	41	45	48
3	18	18	19	40	41	42	46	49
4	18	19	40	41	42	43	48	101
5	19	38	41	42	43	44	98	104
6	42	43	45	46	48	98	109	116
7	44	45	48	49	101	104	116	123

	0	1	2	3	4	5	6	7
0	128	16	17	25	26	26	42	44
1	16	17	25	25	26	38	43	91
2	17	25	26	27	40	41	91	96
3	25	25	27	40	41	84	93	197
4	26	26	40	41	84	86	191	203
5	26	38	41	84	86	177	197	209
6	42	43	91	93	191	197	219	232
7	44	91	96	197	203	209	232	246

Figure 34 – Quantizer matrix for the 1080/50i system



	0	1	2	3	4	5	6	7
0	128	16	17	18	18	19	42	44
1	16	17	18	18	19	38	43	68
2	17	18	19	19	40	41	68	96
3	18	18	19	40	41	63	92	98
4	18	19	40	41	63	86	96	202
5	19	38	41	63	86	88	196	208
6	42	43	68	92	96	196	218	232
7	44	68	96	98	202	208	232	246

	0	1	2	3	4	5	6	7
0	128	24	26	36	36	38	84	88
1	24	26	36	36	38	76	86	182
2	26	36	38	38	80	82	182	192
3	36	36	38	80	82	168	186	394
4	36	38	80	82	168	192	382	406
5	38	76	82	168	172	354	394	418
6	84	86	182	186	382	394	438	464
7	88	182	192	394	406	418	464	492

Figure 35 – Quantizer matrix for the 720/60p system

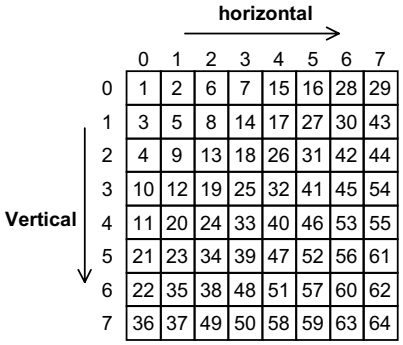


Figure 36 – Output order of a weighted DCT block

4.3 Quantization

4.3.1 Introduction

Weighted DCT coefficients are divided by quantization steps in order to limit the amount of data in one video segment to five compressed macro blocks and transformed 9 bits.

4.3.2 Bit assignment for quantization

Weighted DCT coefficients are represented as follows:

DC coefficient value (9 bits): b8 b7 b6 b5 b4 b3 b2 b1 b0
twos complement (-255 to 255)

AC coefficient value (12 bits): s b10 b9 b8 b7 b6 b5 b4 b3 b2 b1 b0
1 sign bit + 11 bits of absolute value (-2047 to 2047)

4.3.3 Quantization step

The quantization step (Q-step) is selected in order to limit the amount of data in each five compressed macro blocks which are generated from a single video segment. Q-step shall be decided by the quantization number (QNO) and class number as specified in table 25. QNO shall be applied to every macro block. The class number shall be applied to every DCT block.

Data reduction consists of two procedures. First, the AC coefficient is divided by the Q-step. If bit length of the quantized AC coefficient obtained is more than 9, then the second procedure is performed. In the second procedure, the AC coefficient is divided again by larger Q-step according to increasing class numbers in order to make the bit length of the quantized AC coefficient 9 or less.

Table 25 – Quantization step

		Class number			
		0	1	2	3
Quantization number (QNO)	1	1	2	4	8
	2	2	4	8	
	3	3	6	12	
	4	4	8		
	5	5	10		
	6	6	12		
	7	7	14		
	8	8			
	9	16	32	64	
	10	18	36	72	
	11	20	40	80	
	12	22	44	88	
	13	24	48	96	
	14	28	56	112	
	15	52	104		

4.4 Variable length coding (VLC)

Variable length coding is an operation for transforming from quantized AC coefficients to variable length codes. One or more successive AC coefficients within a DCT block are coded into one variable length code according to the order as shown in figure 36. Run length and amplitude are defined as follows:

Run length: The number of successive AC coefficients quantized to 0
(run = 0, …, 61)

Amplitude: Absolute value just after successive AC coefficients quantized to 0
(amp = 0, …, 255)

(run, amp): The pair of run length and amplitude.

Table 26 shows the length of code words corresponding to (run, amp). In the table, sign bit is not included in the length of code words. When the amplitude is not zero, the code length shall be increased by an increment of 1 to express the sign of the amplitude. For empty cells in the table, the code word of the (run, amp) is divided into two words, the (run - 1, 0) and the (0, amp).

Variable length code shall be as shown in table 27. The leftmost bit of code words is MSB and the rightmost bit of code words is LSB in table 4. The MSB of a subsequent code word is next to the LSB of the code word just before. Sign bit “s” shall be as follows.

When the quantized AC coefficient is greater than zero, s = 0

When the quantized AC coefficient is less than zero, s = 1

When the values of all of the remaining quantized coefficients are zero within a DCT block, the coding process is ended by adding the EOB (end of block) code word of 0110b directly after the last code word.

Table 26 – Length of codewords

	Amplitude																								
Run length	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	.....	255
0	11	2	3	4	4	5	5	6	6	7	7	7	8	8	8	8	8	8	9	9	9	9	9	15	.....	15
1	11	4	5	7	7	8	8	8	9	10	10	10	11	11	11	12	12	12								
2	12	5	7	8	9	9	10	12	12	12	12	12														
3	12	6	8	9	10	10	11	12																		
4	12	6	8	9	11	12																				
5	12	7	9	10																						
6	13	7	9	11																						
7	13	8	12	12																						
8	13	8	12	12																						
9	13	8	12																							
10	13	8	12																							
11	13	9																								
12	13	9																								
13	13	9																								
14	13	9																								
15	13																									
⋮	⋮																									
61	13																									

NOTES

1 Sign bit is not included.
2 The length of EOB = 4.

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Table 27 – Codewords of variable length coding

(run, amp)		Codeword	Length
0	1	0 0 s	2+1
0	2	0 1 0 s	3+1
EOB		0 1 1 0	4
1	1	0 1 1 1 s	4+1
0	3	1 0 0 0 s	
0	4	1 0 0 1 s	
2	1	1 0 1 0 0 s	5+1
1	2	1 0 1 0 1 s	
0	5	1 0 1 1 0 s	
0	6	1 0 1 1 1 s	
3	1	1 1 0 0 0 0 s	6+1
4	1	1 1 0 0 0 1 s	
0	7	1 1 0 0 1 0 s	
0	8	1 1 0 0 1 1 s	
5	1	1 1 0 1 0 0 0 s	7+1
6	1	1 1 0 1 0 0 1 s	
2	2	1 1 0 1 0 1 0 s	
1	3	1 1 0 1 0 1 1 s	
1	4	1 1 0 1 1 0 0 s	
0	9	1 1 0 1 1 0 1 s	
0	10	1 1 0 1 1 1 0 s	
0	11	1 1 0 1 1 1 1 s	
7	1	1 1 1 0 0 0 0 0 s	8+1
8	1	1 1 1 0 0 0 0 1 s	
9	1	1 1 1 0 0 0 1 0 s	
10	1	1 1 1 0 0 0 1 1 s	
3	2	1 1 1 0 0 1 0 0 s	
4	2	1 1 1 0 0 1 0 1 s	
2	3	1 1 1 0 0 1 1 0 s	
1	5	1 1 1 0 0 1 1 1 s	
1	6	1 1 1 0 1 0 0 0 s	
1	7	1 1 1 0 1 0 0 1 s	
0	12	1 1 1 0 1 0 1 0 s	
0	13	1 1 1 0 1 0 1 1 s	
0	14	1 1 1 0 1 1 0 0 s	
0	15	1 1 1 0 1 1 0 1 s	
0	16	1 1 1 0 1 1 1 0 s	
0	17	1 1 1 0 1 1 1 1 s	

(run, amp)		Codeword	Length
11	1	1 1 1 1 0 0 0 0 0 s	9+1
12	1	1 1 1 1 0 0 0 0 1 s	
13	1	1 1 1 1 0 0 0 1 0 s	
14	1	1 1 1 1 0 0 0 1 1 s	
5	2	1 1 1 1 0 0 1 0 0 s	
6	2	1 1 1 1 0 0 1 0 1 s	
3	3	1 1 1 1 0 0 1 1 1 s	
4	3	1 1 1 1 0 0 1 1 1 s	
2	4	1 1 1 1 0 1 0 0 0 s	
2	5	1 1 1 1 0 1 0 0 1 s	
1	8	1 1 1 1 0 1 0 1 0 s	
0	18	1 1 1 1 0 1 0 1 1 s	
0	19	1 1 1 1 0 1 1 0 0 s	
0	20	1 1 1 1 0 1 1 0 1 s	
0	21	1 1 1 1 0 1 1 1 0 s	
0	22	1 1 1 1 0 1 1 1 1 s	
5	3	1 1 1 1 1 0 0 0 0 0 s	10+1
3	4	1 1 1 1 1 0 0 0 0 1 s	
3	5	1 1 1 1 1 0 0 0 1 0 s	
2	6	1 1 1 1 1 0 0 0 1 1 s	
1	9	1 1 1 1 1 0 0 1 0 0 s	
1	10	1 1 1 1 1 0 0 1 0 1 s	
1	11	1 1 1 1 1 0 0 1 1 0 s	
0	0	1 1 1 1 1 0 0 1 1 1 0	11
1	0	1 1 1 1 1 0 0 1 1 1 1	
6	3	1 1 1 1 1 0 1 0 0 0 0 s	11+1
4	4	1 1 1 1 1 0 1 0 0 0 1 s	
3	6	1 1 1 1 1 0 1 0 0 1 0 s	
1	12	1 1 1 1 1 0 1 0 0 1 1 s	
1	13	1 1 1 1 1 0 1 0 1 0 0 s	
1	14	1 1 1 1 1 0 1 0 1 0 1 s	
2	0	1 1 1 1 1 0 1 0 1 1 0 0	12
3	0	1 1 1 1 1 0 1 0 1 1 0 1	
4	0	1 1 1 1 1 0 1 0 1 1 1 0	
5	0	1 1 1 1 1 0 1 0 1 1 1 1	

(run, amp)		Codeword	Length
7	2	1 1 1 1 1 0 1 1 0 0 0 0 s	12+1
8	2	1 1 1 1 1 0 1 1 0 0 0 1 s	
9	2	1 1 1 1 1 0 1 1 0 0 1 0 s	
10	2	1 1 1 1 1 0 1 1 0 0 1 1 s	
7	3	1 1 1 1 1 0 1 1 0 1 0 0 s	
8	3	1 1 1 1 1 0 1 1 0 1 0 1 s	
4	5	1 1 1 1 1 0 1 1 0 1 1 0 s	
3	7	1 1 1 1 1 0 1 1 0 1 1 1 s	
2	7	1 1 1 1 1 0 1 1 1 0 0 0 s	
2	8	1 1 1 1 1 0 1 1 1 0 0 1 s	
2	9	1 1 1 1 1 0 1 1 1 0 1 0 s	
2	10	1 1 1 1 1 0 1 1 1 0 1 1 s	
2	11	1 1 1 1 1 0 1 1 1 1 0 0 s	
1	15	1 1 1 1 1 0 1 1 1 1 0 1 s	
1	16	1 1 1 1 1 0 1 1 1 1 1 0 s	
1	17	1 1 1 1 1 0 1 1 1 1 1 1 s	
6	0	1 1 1 1 1 1 1 0 0 0 0 1 1 0	13
7	0	1 1 1 1 1 1 1 0 0 0 0 1 1 1	
R ⋮	0 ⋮	1 1 1 1 1 1 0 Binary notation of R R = 6 to 61	
61	0	1 1 1 1 1 1 0 1 1 1 1 0 1	
0	23	1 1 1 1 1 1 1 1 0 0 0 1 0 1 1 1 s	15+1
0	24	1 1 1 1 1 1 1 1 0 0 0 1 1 0 0 0 s	
0 ⋮	A ⋮	1 1 1 1 1 1 1 Binary notation of A A = 23 to 255 s	
0	255	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 s	

NOTES

1 (R, 0) : 1 1 1 1 1 1 0 r5 r4 r3 r2 r1 r0,
where 32r5 + 16r4 + 8r3 + 4r2 + 2r1 + r0 = R.

2 (0, A) : 1 1 1 1 1 1 1 a7 a6 a5 a4 a3 a2 a1 a0 s,
where 128a7 + 64a6 + 32a5 + 16a4 + 8a3 + 4a2 + 2a1 + a0 = A.

3 S is sign bit. EOB means End of block.

4.5 Arrangement of a compressed macro block

A compressed video segment consists of five compressed macro blocks. Each compressed macro block has 77 bytes of data. The arrangement of the compressed macro block shall be as shown in figure 37.

STA (status of the compressed macro block)

STA expresses the error and concealment of the compressed macro block and consists of four bits: s3, s2, s1, s0. Table 28 shows the definitions of STA.

QNO (quantization number) – QNO is the quantization number applied to the macro block. Code words of the QNO shall be as shown in table 29.

DC –

DCI (where I is the DCT block order in the macro block, I = 0, …, 7) consists of a DC coefficient, the DCT mode, and the class number of the DCT block.

```
        MSB                                          LSB
DCI :   b8  b7  b6  b5  b4  b3  b2  b1  b0  m0  c1  c0
```

where

b8 to b0: DC coefficient value
m0 : DCT mode
for I = 0 0 = 8-8-frame-DCT mode
1 = 8-8-field-DCT mode
for I = 1 to 7 reserved bit for future use
Default value shall be set to 1
c1 c0 : class number

AC –

AC is a generic term for variable length coded AC coefficients within the video segment V h,i,k. The areas of Y_0, Y_1, Y_2, Y_3, CR_0, CR_1, CB_0, and CB_1 are defined as compressed-data areas, each of Y_0, Y_1, Y2, Y_3, CR_0, and CR_1 consists of 80 bits and each CB_0 and CB_1 consists of 64 bits as shown in figure 37. DCI and variable length code for AC coefficients in the DCT block whose DCT block number is h,i,j,k,l are assigned from the beginning of the compressed-data area in the compressed macro block CM h,i,j,k. In figure 37, the variable length code word is located starting from MSB which is shown in the upper left side, and the LSB shown in the lower right side. Therefore, AC data are distributed from the upper left corner to the lower right corner.

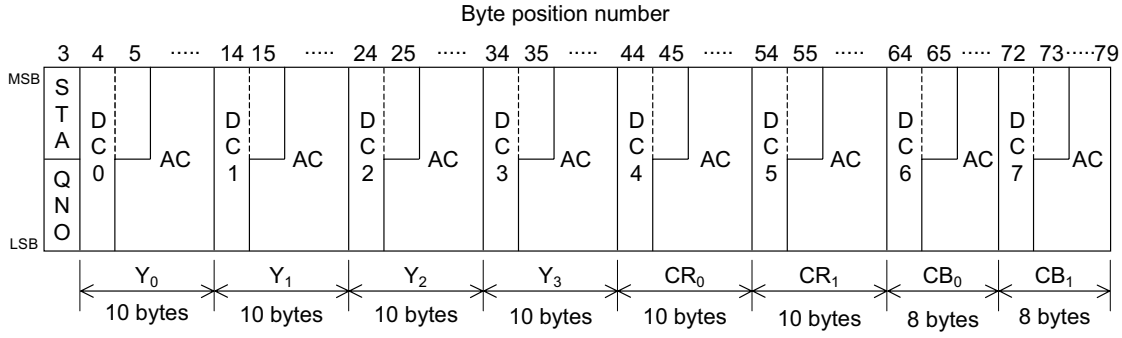

Figure 37 – Arrangement of a compressed macro block

Table 28 – Definition of STA

STA bit				Information of the compressed macro block		
s3	s2	s1	s0	Error	Error concealment	Continuity
0	0	0	0	No error	Not proceeded	———
0	0	1	0		Type A	Type a
0	1	0	0		Type B	
0	1	1	0		Type C	
0	1	1	1	Error exists	———	———
1	0	1	0	No error	Type A	Type b
1	1	0	0		Type B	
1	1	1	0		Type C	
1	1	1	1	Error exists	———	———
other				reserved		

where

Type A: Replaced with a compressed macro block of the same compressed macro block number in the frame immediately previous.
Type B: Replaced with a compressed macro block of the same compressed macro block number in the next immediate frame.
Type C: This compressed macro block is concealed, but the concealment method is not specified.
Type a The continuity of data processing sequence with other compressed macro block whose s0 = 0 and s3 = 0 in the same video segment is guaranteed.
Type b: The continuity of data processing sequence with other compressed macro block is not guaranteed.

NOTES
1 For STA = 0111b, the error code is inserted in the compressed macro block. This is an option.
2 For STA = 1111b, the error position is unidentified.

Table 29 – Codewords of the QNO

Q number bit				QNO
q3	q2	q1	q0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

4.6 Arrangement of a video segment

In this clause, the distribution method of quantized AC coefficients is described. Figure 38 shows the arrangement of a video segment CV h,i,k after bit-rate reduction. The column shows a compressed macro block. Symbol F h,i,j,k,l expresses a compressed data area for a DCT block whose DCT block number is h, i, j, k, l. Bit sequence, defined as B h,i,j,k,l, shall consist of the following concatenated data: DC coefficient, DCT mode information, class number, and AC coefficient code words for DCT blocks numbered h,i,j,k,l. Code words for AC coefficients of B h,i,j,k,l shall be concatenated according to the order as shown in figure 36 and the last code word shall be EOB. The MSB of the subsequent code word shall be next to the LSB of the code word just before it.

The algorithm for the arrangement of a video segment shall be composed of three passes:

Pass 1: The distribution of B h,i,j,k,l to the compressed-data area;

Pass 2: The distribution of the overflow B h,i,j,k,l which remains after the pass 1 operation in the same compressed macro block;

Pass 3: The distribution of the overflow B h,i,j,k,l which remains after the pass 2 operation in the same video segment.

Arrangement algorithm of a video segment

```
for(h = 0;  h < 4;  h ++) {
   if (60 Hz system) n = 10;
   else if (h = 0) n = 12;
   else n = 11;
    for (i = 0;  i < n;  i ++) {
        if (i < 11) {
            a = (i + 2) mod n;
            b = (i + 6) mod n;
            c = (i + 8) mod n;
            d = (i + 0) mod n;
            e = (i + 4) mod n;
            p = 2; q = 1; r = 3; s = 0; t = 4;
        }
        else {
            a = b = c = d = e = 11;
            p = 0; q = 1; r = 2; s = 3; t = 4;
        }
        for (k = 0;  k < 27; k ++) {
            x = a; y = p;
            VR = 0;
            /* VR is the bit sequence for the data                          */
            /*    which are not distributed to video segment CV h,i,k by pass 2. */
    /* pass 1 */
            for (j = 0;  j < 5; j ++) {
                MRy = 0;
               /* MRy is the bit sequence for the data                        */
               /* which are not distributed to macro block M h,x,y,k by pass 1. */
               for (l = 0;  l < 8; l ++) {
                     remain = distribute (B h,x,y,k,l,  F h,x,y,k,l);
                     MRy = connect (MRy,  remain);
               }
                     if (y == p)  {y = q;  x = b;}
               else if (y == q)  {y = r;  x = c;}
```

```
            else if (y == r)  {y = s;  x = d;}
            else if (y == s)  {y = t;  x = e;}
            else if (y == t)  {y = p;  x = a;}
        }
    /* pass 2 */
        for (j = 0;  j < 5; j ++) {
            for (l = 0;  l < 8; l ++) {
                MRy = distribute (MRy,  F h,x,y,k,l);
            }
            VR = connect (VR,  MRy);
                if (y == p)  {y = q;  x = b;}
            else if (y == q)  {y = r;  x = c;}
            else if (y == r)  {y = s;  x = d;}
            else if (y == s)  {y = t;  x = e;}
            else if (y == t)  {y = p;  x = a;}
        }
    /* pass 3 */
        for (j = 0;  j < 5; j ++) {
            for (l = 0;  l < 8; l ++) {
                VR = distribute (VR,  F h,x,y,k,l);
            }
                if (y == p)  {y = q;  x = b;}
            else if (y == q)  {y = r;  x = c;}
            else if (y == r)  {y = s;  x = d;}
            else if (y == s)  {y = t;  x = e;}
            else if (y == t)  {y = p;  x = a;}
        }
    }
}

where
    distribute (data 0, area 0) {       /* Distribute data 0 from MSB into empty area of area 0. */
                                        /* The area 0 is filled starting from the MSB.           */
        remain = (remaining_data);  /* Remaining_data are the data which are not distributed. */
        return (remain);
    }
    connect (data 1, data 2 ) {         /*  Connect the MSB of data 2 with the LSB of data 1.    */
        data 3 = (connecting_data);  /*  Connecting_data are the data which are connected.  */
                                        /*  data 2 with data 1.                                  */
        return (data3);
    }
```

The remaining data which can not be distributed within the unused space of the macro block will be ignored. Therefore, when error concealment is performed for a compressed macro block, some data distributed by pass 3 may not be reproduced.

Video error code processing

If errors are detected in a compressed macro block which is reproduced and processed with error correction, the compressed-data area containing these errors should be replaced with the video error code. This process replaces the first two bytes of data of the compressed-data area with the code as follows:

```
MSB                 LSB
 1000000000000110b
```

The first 9 bits are DC error code, the next 3 bits are the information of DCT mode and class number and the last 4 bits are the EOB as shown in figure 39.

When the compressed macro blocks, after error code processing, are input to the decoder which does not operate with video error code, all data in this compressed macro block should be processed as invalid.

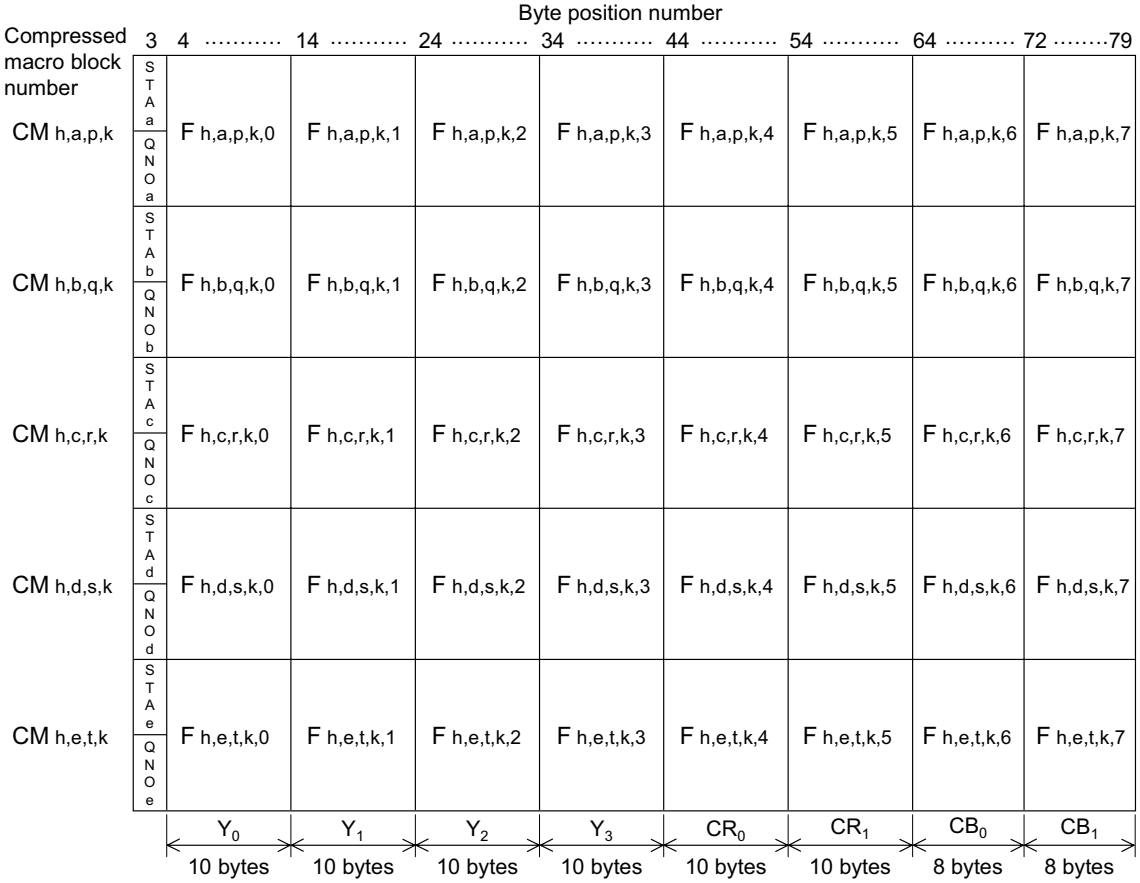

Figure 38 – Arrangement of a video segment after the bit rate reduction

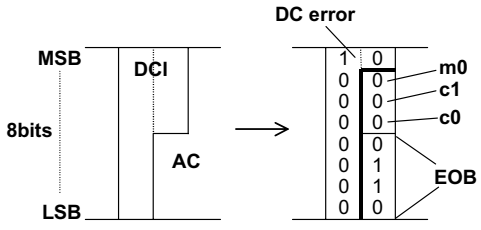

Figure 39 – Video error code

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Annex A (informative)
Relationship between compression format and other documents

Figure A.1 shows the relationship between the compression format (this document) and other documents defining the D-xx recorder.

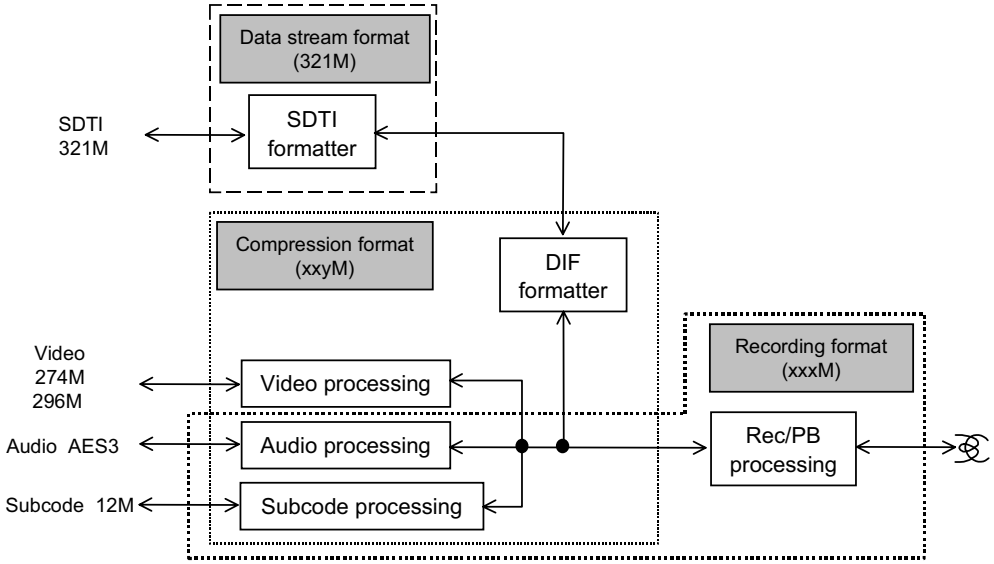


Figure A.1 – Block diagram of D-xx recorder

Annex B (normative)
Digital filter for sampling-rate conversion

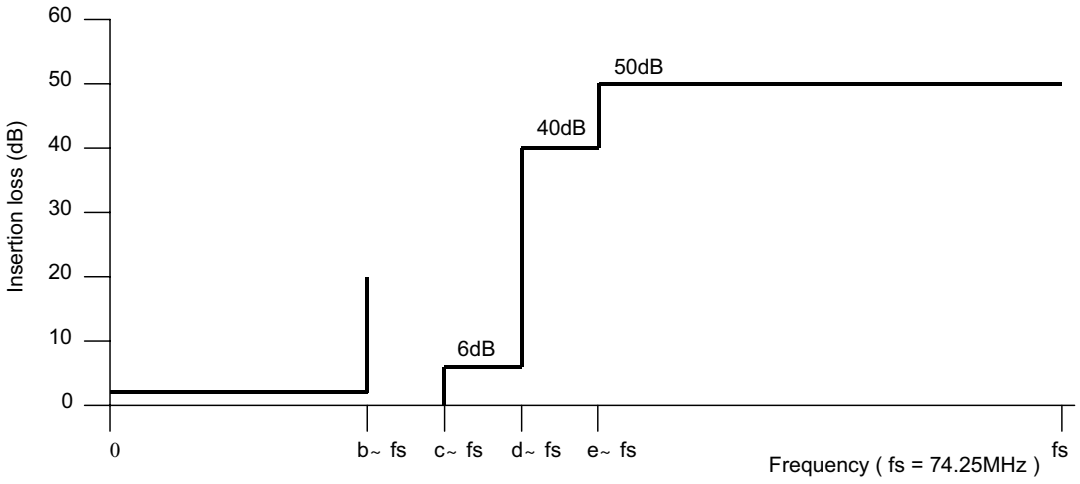


Figure B.1 – Template for insertion loss frequency characteristic

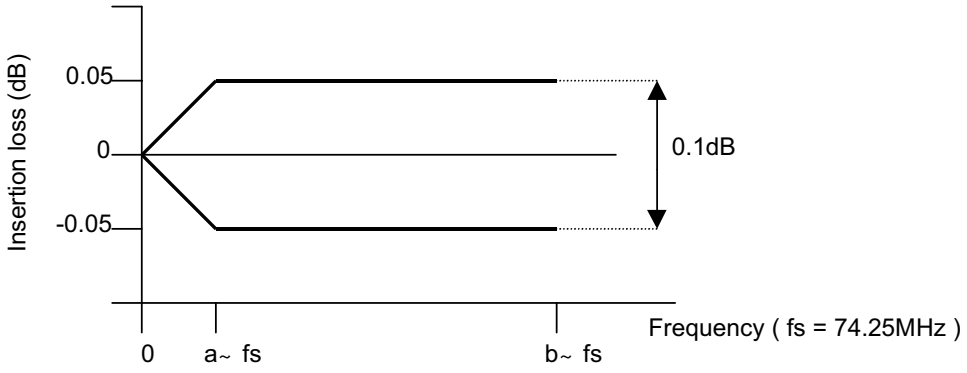


Figure B.2 – Pass band ripple tolerance

Table B.1 – Parameter of digital filter

		a	b	c	d	e
1080/60i	Y	0.05	0.25	0.333	0.45	0.55
	C_B, C_R	0.025	0.125	0.167	0.225	0.275
1080/50i	Y	0.05	0.25	0.375	0.50	0.60
	C_B, C_R	0.025	0.125	0.1875	0.25	0.30
720/60p	Y	0.05	0.25	0.375	0.50	0.60
	C_B, C_R	0.025	0.125	0.1875	0.25	0.30

Annex C (informative)
Compression specification

The compression specification of this standard is different from the IEC 61834-3 HD format for 1125-60 and 1250-50 systems.

Annex D (informative)
Abbreviations and acronyms

AAUX	Audio auxiliary data
AP1	Audio application ID
AP2	Video application ID
AP3	Subcode application ID
APT	Track application ID
Arb	Arbitrary
AS	AAUX source pack
ASC	AAUX source control pack
CGMS	Copy generation management system
CM	Compressed macro block
DBN	DIF block number
DCT	Discrete cosine transform
DIF	Digital interface
DRF	Direction flag
Dseq	DIF sequence number
DSF	DIF sequence flag
EFC	Emphasis audio channel flag
EOB	End of block
LF	Locked mode flag
QNO	Quantization number
QU	Quantization
Res	Reserved for future use
SCT	Section type
SMP	Sampling frequency
SSYB	Subcode sync block
STA	Status of the compressed macro block
STYPE	Signal type
Syb	Subcode sync block number
TF	Transmitting flag
VAUX	Video auxiliary data
VLC	Variable length coding
VS	VAUX source pack
VSC	VAUX source control pack

Annex E (informative)
Bibliography

IEC 61834-2 (1997), Recording — Helical-Scan Digital Video Cassette Recording System Using 6,35 mm Magnetic Tape for Consumer Use (525-60, 625-50, 1125-60 and 1250-50 Systems)
— Part 2: SD Format for 525-60 and 625-50 Systems
— Part 3: HD Format for 1125-60 and 1250-50 Systems

SMPTE STANDARD

SMPTE 296M-2001
Revision of
ANSI/SMPTE 296M-1997

for Television — 1280 × 720 Progressive Image Sample Structure — Analog and Digital Representation and Analog Interface

Contents

1 Scope

1.1 This standard defines a family of progressive image sample systems for the representation of stationary or moving two-dimensional images sampled temporally at a constant frame rate and having an image format of 1280 pixels by 720 lines and an aspect ratio of 16:9 as given in table 1. All systems in the table have the common characteristic that all the samples gathered within a single temporal unit, a frame, shall be spatially contiguous and provide a complete description of that frame (4.2) This standard specifies:

– R′G′B′ color encoding;
– R′G′B′ analog and digital representation;
– $Y'P'_BP'_R$ color encoding, analog representation, and analog interface; and
– $Y'C'_BC'_R$ color encoding and digital representation.

Table 1 – Image sampling systems

	System nomenclature	Luma or R′G′B′ samples per active line (S/AL)	Active lines per frame (AL/F)	Frame rate, Hz	Luma or R′G′B′ sampling frequency (fs), MHz	Luma sample periods per total line (S/TL)	Total lines per frame
1	1280 × 720/60	1280	720	60	74.25	1650	750
2	1280 × 720/59.94	1280	720	60/1.001	74.25/1.001	1650	750
3	1280 × 720/50	1280	720	50	74.25	1980	750
4	1280 × 720/30	1280	720	30	74.25	3300	750
5	1280 × 720/29.97	1280	720	30/1.001	74.25/1.001	3300	750
6	1280 × 720/25	1280	720	25	74.25	3960	750
7	1280 × 720/24	1280	720	24	74.25	4125	750
8	1280 × 720/23.98	1280	720	24/1.001	74.25/1.001	4125	750
NOTE – For systems 4 through 8, analog video interface is not preferred. See clause 12.							

Approved
January 4, 2001

Designers should be aware that serial digital interfaces for formats other than $Y'C'_BC'_R$ have not been defined.

A bit-parallel digital interface is incorporated by reference in clause 10.

NOTE – Throughout this standard, references to signals represented by a single primed letter (e.g., R′, G′, and B′) are equivalent to the nomenclature in earlier documents of the form E_R', E_G', and E_B', which in turn refer to signals to which the transfer characteristics in 5.4 have been applied. Such signals are commonly described as being gamma corrected.

1.2 This standard specifies multiple system formats (table 1). It is not necessary for an implementation to support all formats to be compliant with this standard. However, an implementation must state which of the system formats are supported.

2 Normative references

The following standards contain provisions which, through reference in this text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent edition of the standards listed below.

SMPTE 274M-1998, Television — 1920 × 1080 Scanning and Analog and Parallel Digital Interfaces for Multiple Picture Rates

SMPTE 291M-1998, Television — Ancillary Data Packet and Space Formatting

SMPTE RP 160-1997, Three-Channel Parallel Analog Component High-Definition Video Interface

SMPTE RP 177-1993 (R1997), Derivation of Basic Television Color Equations

CIE Publication 15.2 (1986), Colorimetry, Second Edition

IEC 60169-8 (1978-01), Radio Frequency Connectors, Part 8: R.F. Coaxial Connectors with Inner Diameter of Outer Conductor 6.5 mm (0.256 in) with Bayonet Lock — Characteristic Impedance 50 Ohms (Type BNC) plus amendments IEC 60169-8-am1 (1996-03) and IEC 60169-8-am2 (1997-11)

ITU-R BT.709-4 (09/00), Parameter Values for the HDTV Standards for Production and International Programme Exchange

3 General

3.1 The specification of a system claiming compliance with this standard shall state:

– which of the systems of table 1 are implemented;

– which of the analog $R'G'B'$ or $Y'P'_BP'_R$ and/or which of the digital $R'G'B'$ or $Y'C'_BC'_R$ interfaces are implemented; and

– whether the digital representation employs eight bits or 10 bits per sample in its uniformly quantized (linear) PCM coding.

3.2 Digital codeword values in this standard are expressed as decimal values in the 10-bit representation. An eight-bit system shall either round or truncate to the most significant eight bits as specified in 7.10.

4 Timing

4.1 Timing shall be based on a reference clock of the sampling frequency indicated in table 1, which shall be maintained to a tolerance of ± 10 ppm.

4.2 A frame shall comprise the indicated total lines per frame, each line of equal duration as determined by the sampling frequency (fs) and the samples per total line (S/TL). Samples may be obtained in an optoelectronic conversion process sequentially, simultaneously, or via a combination of both, provided all samples in the frame are contiguous in the image and obtained within the same temporal frame period. The samples within each line shall be uniformly delivered to and collected from the interface in a spatially left-to-right sequence; lines in a frame shall be uniformly delivered to and collected from the interface in a spatially top-to-bottom sequence. Lines are numbered in time sequence according to the raster structure described in clause 6.

4.3 Timing instants in each line shall be defined with respect to a horizontal datum denoted by 0_H which is established by horizontal synchronizing (sync) information in clauses 8 and 11. Each line shall be

divided into a number of reference clock intervals, of equal duration, as specified by the column S/TL in table 1. The time between any two adjacent sample instants is called the reference clock interval T. T = 1/fs.

5 System colorimetry

5.1 Equipment shall be designed in accordance with the colorimetric analysis and optoelectronic transfer function defined in this clause. This corresponds to ITU-R BT.709.

5.2 Picture information shall be linearly represented by red, green, and blue tristimulus values (RGB), lying in the range 0 (reference black) to 1 (reference white), whose colorimetric attributes are based upon reference primaries with the following chromaticity coordinates, in conformance with ITU-R BT.709, and whose white reference conforms to CIE D_{65} as defined by CIE 15.2:

	CIE *x*	CIE *y*
Red primary	0.640	0.330
Green primary	0.300	0.600
Blue primary	0.150	0.060
Reference white	0.3127	0.3290

5.3 From the red, green, and blue tristimulus values, three nonlinear primary components, R′, G′, and B′, shall be computed according to the optoelectronic transfer function of ITU-R BT.709, where L denotes a tristimulus value and V′ denotes a nonlinear primary signal:

$$V' = \begin{cases} 4.5L, & 0 \le L < 0.018 \\ 1.099L^{0.45} - 0.099, & 0.018 \le L \le 1.0 \end{cases}$$

5.4 To ensure the proper interchange of picture information between analog and digital representations, signal levels shall be completely contained in the range specified between reference black and reference white specified in 7.6 and 12.4, except for overshoots and undershoots due to processing.

5.5 The Y′ component shall be computed as a weighted sum of nonlinear R′G′B′ primary components, using coefficients calculated from the reference primaries according to the method of SMPTE RP 177:

$$Y' = 0.2126R' + 0.7152G' + 0.0722B'$$

NOTE – Because the Y′ component is computed from nonlinear R′G′B′ primary components rather than from the linear tristimulus RGB values, it does not represent the true luminance value of the signal, but only an approximation. To distinguish it from luminance, the term luma is used for the Y′ signal. For more information, see e.g. Poynton, *A Technical Introduction to Digital Video*.

5.6 Color-difference component signals P'_B and P'_R, having the same excursion as the Y′ component, shall be computed as follows:

$$P'_B = \frac{0.5}{1 - 0.0722}(B' - Y')$$

$$P'_R = \frac{0.5}{1 - 0.2126}(R' - Y')$$

P'_B and P'_R are filtered and may be coded as C'_B and C'_R components for digital transmission. Example filter templates are given in figure B.2.

6 Raster structure

6.1 For details of vertical timing, see figures 1 and 2.

6.2 In a system according to this standard, each frame shall comprise 750 lines including:

– Vertical blanking: lines 1 through 25 inclusive (including vertical sync, lines 1 through 5 inclusive) and lines 746 through 750 inclusive; and

– Picture: 720 lines, lines 26 through 745 inclusive.

6.3 Ancillary signals, as distinct from ancillary data, may be conveyed during vertical blanking, lines 7 through 25 inclusive. The portion within each of these lines that may be used for ancillary data is defined in 9.3. Ancillary signals shall not convey picture information although they may be employed to convey other related or unrelated signals, coded similarly to picture information. Further specification of ancillary signals is outside the scope of this standard.

6.4 During time intervals not otherwise used, the R′, G′, B′ or Y′, P'_B, C'_B, P'_R, and C'_R components shall have a blanking level corresponding to zero.

6.5 The production aperture defines a region 1280 samples by 720 lines. The horizontal extent of the production aperture shall have the

SMPTE 296M-2001

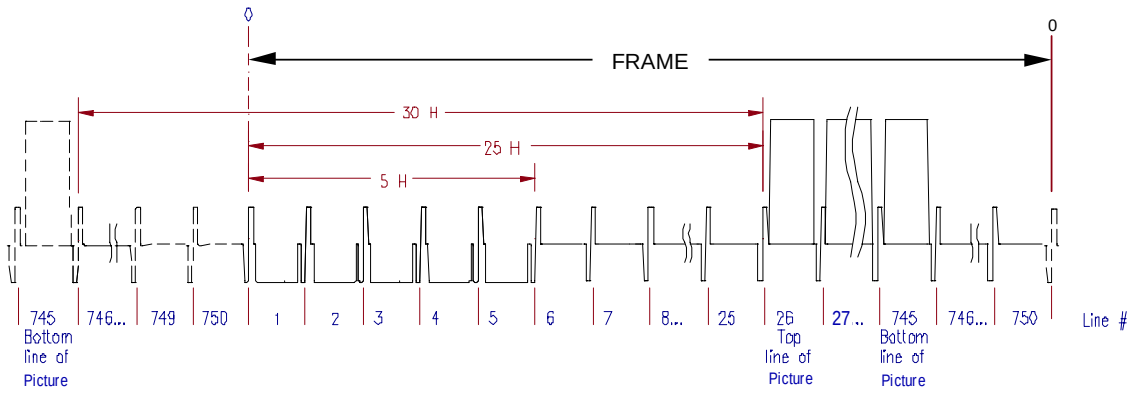


Figure 1 – Vertical timing (analog representation)

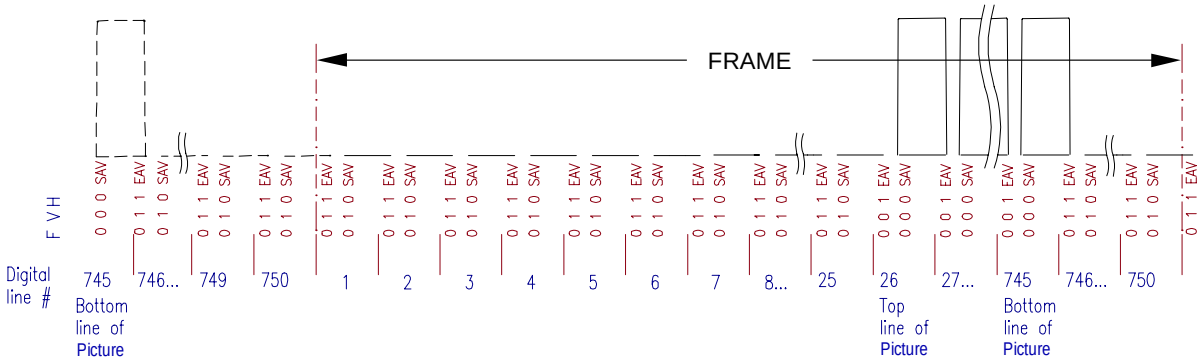


Figure 2 – Vertical timing (digital representation)

50% point of its leading transition at reference luma sample 0 and the 50% point of its trailing transition at luma sample 1279. The production aperture defines the maximum extent of picture information. For further information, consult annex A.

6.6 The aspect ratio of the image represented by the production aperture shall be 16:9. The sample aspect ratio is 1:1 (square pixels).

6.7 The center of the picture shall be located at the center of the production aperture, midway between samples 639 and 640, and midway between lines 385 and 386.

6.8 Each edge of the picture width, measured at the 50% amplitude point, shall lie within six reference clock intervals of the production aperture.

7 Digital representation

7.1 Digital representation shall employ either R′G′B′ or Y′$C'_BC'_R$ components, as defined in clause 5 or clause 6, uniformly sampled.

NOTE – Each component is prepared as an individual channel. Combinations of channels may be presented to an appropriate interface for signal interchange. For example, the Y′ channel and the multiplexed C'_B/C'_R channel data together comprise a source format for the serial interface specified in SMPTE 292M.

7.2 The digital signals described here are assumed to have been filtered to reduce or prevent aliasing upon sampling. For information regarding filtering, consult annex B.

7.3 The characteristics of the digital signals are based on the assumption that the location of any required sin (x)/x correction is at the point where the signal is converted to an analog format.

7.4 R′G′B′ signals and the Y′ signal of the Y′C′$_B$C′$_R$ interface shall be sampled orthogonally, line- and picture-repetitive, at the sampling frequency, f_S. The period of the sampling clock shall be denoted T. R′G′B′ samples shall be cosited with each other.

7.5 A luma sampling number in a line is denoted in this standard by a number from 0 through one less than the total number of samples in a line. Luma sample number zero shall correspond to the first active video sample. The luma sample numbering is shown in figure 3. Note that the distance between 0_H and the start of SAV is 256 samples.

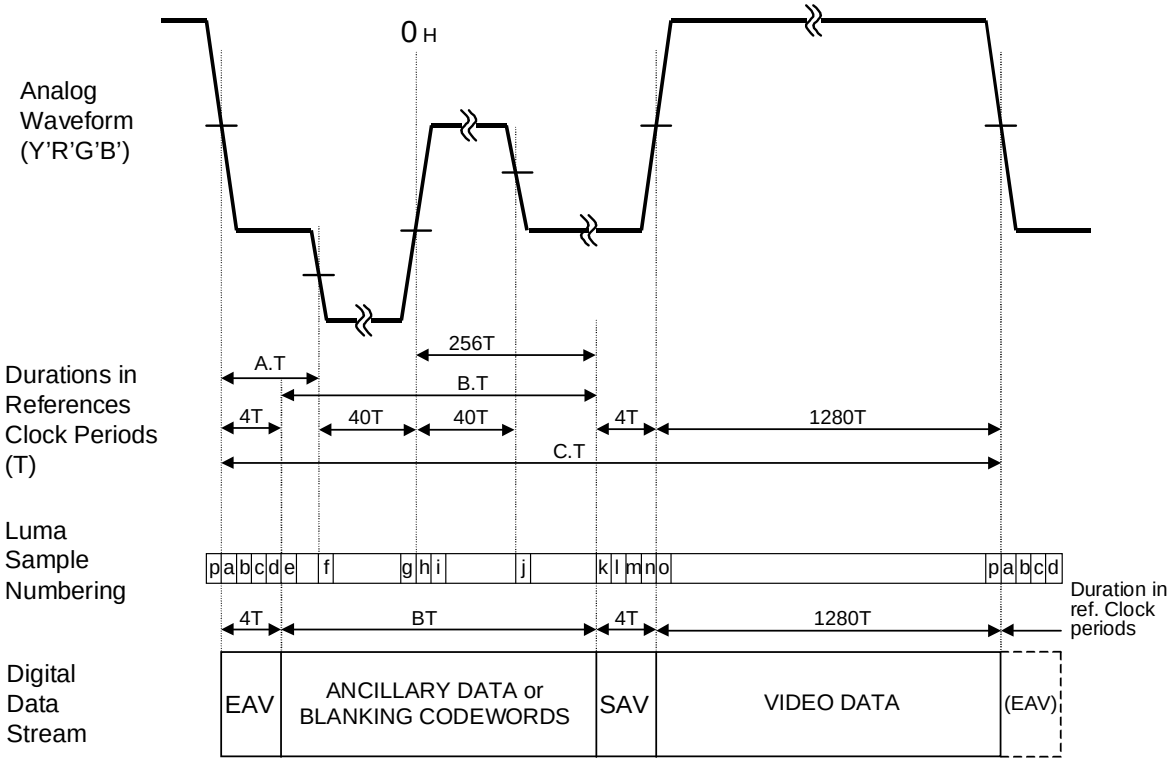
NOTE – The active video digital representation is 1280 clock periods (0-1279) in length.

7.6 Digital R′, G′, B′, and Y′ components shall be computed as follows:

$$L'_D = \text{Floor}\,(219DL' + 16D + 0.5);\ D = 2^{n-8}$$

where L′ is the component value in abstract terms from zero to unity, n takes the value 8 or 10 corresponding to the number of bits to be represented, and L'_D is the resulting digital code. The unary function Floor yields the largest integer not greater than its argument.

NOTE – This scaling places the extrema of R′, G′, B′, and Y′ components at codewords 64 and 940 in a 10-bit representation or codewords 16 and 235 in an eight-bit representation.



NOTES
1 Horizontal axis not to scale.
2 0_H is the analog horizontal timing reference point, and in the analog domain, is regarded as the start of the line.
3 A line of digital video extends from the first word of EAV to the last word of video data.

Figure 3 – Analog and digital timing relationships

7.7 Digital C'_B and C'_R components of the $Y'C'_BC'_R$ set shall be computed as follows:

$$C'_D = \text{Floor}\,(224DC' + 128D + 0.5);\ D = 2^{n-8}$$

where C' is the component value in abstract terms from – 0.5 to + 0.5, and C'_D is the resulting digital code. The unary function Floor yields the largest integer not greater than its argument.

NOTE – This scaling places the extrema of C'_B and C'_R at codewords 64 and 960 in a 10-bit representation or codewords 16 and 240 in an eight-bit representation.

7.8 C'_B and C'_R signals shall be horizontally subsampled by a factor of two with respect to the Y' component. C'_B and C'_R samples shall be cosited with even-numbered Y' samples. The sample number zero of C'_B and C'_R corresponds to the first active video 0 sample. For information regarding filtering, consult annex B.

The subsampled C'_B and C'_R signals shall be time-multiplexed on a sample basis, in the order $C'_BC'_R$. The first data word of an active line shall be a C'_B sample. The multiplexed signal is referred to as C'_B/C'_R.

NOTE – Systems 7 and 8 have 2063 C'_B sample periods and 2062 C'_R sample periods per line. The C'_B/C'_R multiplexer must be reset every line at sample number zero.

7.9 Code values having the eight most significant bits all zero or all one — that is, 10-bit codes 0, 1, 2, 3, 1020, 1021, 1022, and 1023 — are employed for synchronizing purposes and shall be prohibited from video, ancillary signals, and ancillary data.

7.10 A system having an eight-bit interface shall address the conversion of 10-bit video data to eight bits with an appropriate process that minimizes video artifacts such as quantization noise. Ancillary data in 10-bit format shall be converted to eight-bit format by truncating the two least significant bits. In both cases, when converting eight-bit data to 10-bit data, the two least significant bits of the 10-bit word shall be set to 0.

NOTE – SMPTE is addressing rounding for all eight-bit/10-bit digital video standards. SMPTE 291M describes the handling of ancillary data between eight-bit and 10-bit interfaces in annex D.

7.11 For Y', R', G', and B' signals, undershoot and overshoot in video processing may be accommodated by the use of codewords 4 through 63 and codewords 941 through 1019 in a 10-bit system, or codewords 1 through 15 and codewords 236 through 254 in an eight-bit system.

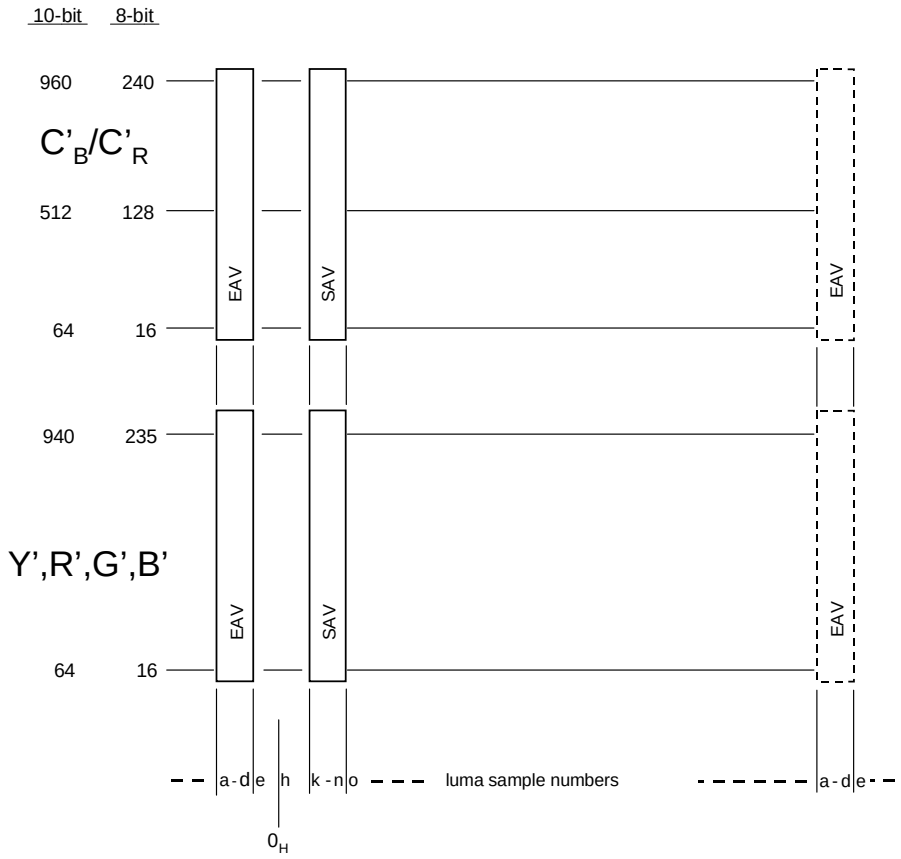
For C'_B and C'_R signals, undershoot and overshoot in video processing may be accommodated by the use of codewords 4 through 63 and codewords 961 through 1019 in a 10-bit system, or codewords 1 through 15 and codewords 241 through 254 in an eight-bit system.

8 Digital timing reference sequences (SAV, EAV)

8.1 SAV (start of active video) and EAV (end of active video) digital synchronizing sequences shall define synchronization across the digital interface. Figures 2, 3, and 4 show the relationship of the SAV and EAV sequences to digital and analog video.

8.2 An SAV or EAV sequence shall comprise four consecutive codewords: a codeword of all ones, a codeword of all zeros, another codeword of all zeros, and a codeword including F (frame), V (vertical), H (horizontal), P3, P2, P1, and P0 (parity) bits. An SAV sequence shall be identified by having H = 0; EAV shall have H = 1 (tables 3 and 4 show details of the coding).

8.3 When digitized, every line shall include a four-sample EAV sequence commencing 110 clocks prior to 0_H (for systems 1 and 2); 440 clocks prior to 0_H (for system 3); 1760 clocks prior to 0_H (for systems 4 and 5); 2420 clocks prior to 0_H (for system 6);and 2585 clocks prior to 0_H (for systems 7 and 8). When digitized, every line shall include a four-sample SAV sequence commencing 256 clocks after 0_H (for all systems [1, 2, 3, 4, 5, 6, 7, and 8]). The EAV sequence immediately preceding the 0_H datum of line 1 shall be considered to be the start of the digital frame as shown in figure 2.



NOTES

1 Figure 3/table 2 show numbering of luma sample numbers for each of the systems covered in this standard.

2 0_H is the analog horizontal timing reference point.

Figure 4 – Digital representation — Horizontal timing details

Table 2 – Values for figures 3 and 4 and table 5 for different systems

Systems	Luma sample numbering															
	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o	p
1,2	1280	1281	1282	1283	1284	1350	1389	1390	1391	1430	1646	1647	1648	1649	0	1279
3	1280	1281	1282	1283	1284	1680	1719	1720	1721	1760	1976	1977	1978	1979	0	1279
4,5	1280	1281	1282	1283	1284	3000	3039	3040	3041	3080	3296	3297	3298	3299	0	1279
6	1280	1281	1282	1283	1284	3660	3699	3700	3701	3740	3956	3957	3958	3959	0	1279
7,8	1280	1281	1282	1283	1284	3825	3864	3865	3866	3905	4121	4122	4123	4124	0	1279

System	Duration in reference clock periods (T)		
	A	B	C
1,2	70	362	1650
3	400	692	1980
4,5	1720	2012	3300
6	2380	2672	3960
7,8	2545	2837	4125

NOTE – Figure 3 and table 2 representations show nominal relationship values between the analog and digital representations. See figure 5 and table 5 for tolerance values for the analog sync including rise and fall tolerances.

Table 3 – Video timing reference codes

Bit number		9 (MSB)	8	7	6	5	4	3	2	1	0 (LSB)
Word	Value										
0	1023	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0	0	0	0
3		1	F	V	H	P3	P2	P1	P0	0	0

Table 4 – Protection bits for SAV and EAV

Bit number		9	8	7	6	5	4	3	2	1	0
Function		1 Fixed	F	V	H	P3	P2	P1	P0	0 Fixed	0 Fixed
Value of (F/V/H)	0	1	0	0	0	0	0	0	0	0	0
	1	1	0	0	1	1	1	0	1	0	0
	2	1	0	1	0	1	0	1	1	0	0
	3	1	0	1	1	0	1	1	0	0	0

8.4 F/V/H flags

– The EAV and SAV of all lines shall have F = 0.

– The EAV and SAV of lines 1 through 25 inclusive and lines 746 through 750 inclusive shall have V = 1.

– The EAV and SAV of lines 26 through 745 inclusive shall have V = 0.

– The EAV of line 1 shall be considered the start of the digital frame.

8.5 A line which in the analog representation is permitted to convey ancillary signals may convey digitized ancillary signals.

9 Ancillary data

9.1 Ancillary data may optionally be included in the blanking intervals of a digital interface according to this standard.

9.2 The interval between the end of EAV and the start of SAV may be employed to convey ancillary data packets. Designers should be aware that when SMPTE 292M serial interface is employed, the first four samples after EAV are reserved for other usage.

9.3 The interval between the end of SAV and the start of EAV of any line that is outside the vertical extent of the picture (as defined in clause 6.2), and that is not employed to convey digitized ancillary signals, may be employed to convey ancillary data packets.

NOTE – Currently SMPTE is defining the switching point(s) for all serial digital video interfaces. The reader is cautioned to be aware that ancillary data should be placed taking into account the switching point.

9.4 Ancillary data packets may be conveyed across each of the three R′, G′, and B′ channels, or across each of the three Y′, C'_B/C'_R channels.

9.5 In the case of 10-bit representation, intervals not used to convey SAV, video data, EAV, ancillary signals, or ancillary data shall convey the codeword 64 (black) in the R′, G′, B′, Y′ channels, or 512 in the C'_B/C'_R channels. They shall be 16 and 128, respectively, in the case of 8-bit representation.

9.6 For specifications of the details of ancillary data, see SMPTE 291M.

10 Bit-parallel interface

The electrical and mechanical parameters of the bit-parallel interface are specified in clauses 10, 11, 12, and 13 of SMPTE 274M, which are incorporated by reference. It is anticipated that in future revisions of SMPTE 274M that auxiliary component A will be eliminated.

11 Analog sync

11.1 Details of analog sync timing are shown in figures 1, 3, and 5 and are summarized in table 5.

11.2 A positive zero-crossing of a trilevel sync pulse shall define the 0_H datum for each line. A negative-going transition precedes this instant by 40 reference clock intervals, and another negative-going transition follows this instant by 40 reference clock intervals.

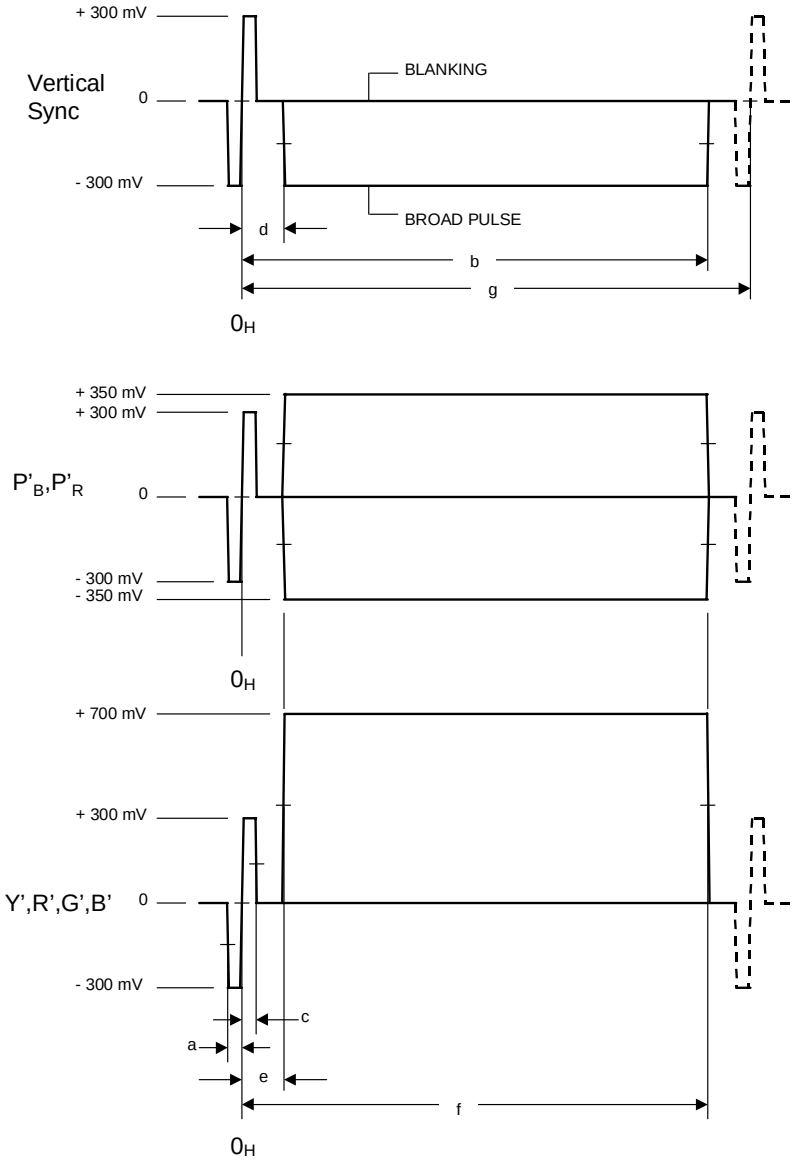


Figure 5 – Analog levels and timing

Table 5 – Analog sync timing (Systems 1 - 8)

		Duration (T)	Tolerance (T)
a	See figure 5	40	± 3
b	See figure 5	1540	– 6 + 0
c	See figure 5	40	± 3
d	See figure 5	260	– 0 + 6
e	See figure 5	260	– 0 + 6
f	See figure 5	1540	– 6 + 0
	Sync rise and fall time	4	± 1.5
g	Total line	Table 2 'C'	
	Active line	1280	– 12 + 0

11.3 Positive transition of a trilevel sync pulse shall be skew-symmetric with a rise time from 10% to 90% of 4 ± 1.5 reference clock periods. The 50% (midpoint) point of each negative transition shall be coincident with its ideal time within a tolerance of ± 3 reference clock periods.

11.4 The trilevel sync pulse shall have structure and timing according to figures 3 and 5. The positive peak of the trilevel sync pulse shall have a level of +300 mV ± 6 mV; its negative peak shall have a level of –300 mV ± 6 mV. The amplitude difference between positive and negative sync peaks shall be less than 6 mV.

11.5 Each line that includes a vertical sync pulse shall maintain blanking level, here denoted zero, except for the interval(s) occupied by sync pulses. During the horizontal blanking interval, areas not occupied by sync shall be maintained at blanking level, here denoted zero.

11.6 Each frame shall commence with five vertical sync lines, each having a broad pulse. The leading 50% point of a broad pulse shall be 260T after the preceding trilevel zero crossing. The trailing 50% point of a broad pulse shall be 1540T after the preceding trilevel zero crossing.

12 Analog interface

NOTE – This clause applies to all frame rates in table 1. However, direct analog interconnection of slow-rate systems (30 Hz and below) is not preferred, except for synchronizing signals.

12.1 An analog interface according to this standard may employ either the R′G′B′ component set or the Y′P′$_B$P′$_R$ component set.

12.2 R′G′B′ and Y′ channels shall have a nominal bandwidth of 30 MHz.

12.3 Each component signal shall be conveyed electrically as a voltage on an unbalanced coaxial cable into a pure resistive impedance of 75 Ω.

12.4 For the Y′, R′, G′, and B′ components, reference black (zero) in the expressions of 5.5 shall correspond to a level of 0 Vdc, and reference white (unity) shall correspond to 700 mV.

12.5 P′$_B$ and P′$_R$ components are analog versions of the C′$_B$ and C′$_R$ components of 5.6, in which zero shall correspond to a level of 0 Vdc and reference peak level (value 0.5 of equations in 5.6) shall correspond to a level of +350 mV.

12.6 Trilevel sync according to clause 11 shall be added to each analog component.

12.7 Each of the electrical signals in an analog interface employs a connector that shall conform to IEC 60169-8, with the exception that the impedance of the connector may be 75 Ω, or to SMPTE RP 160.

Annex A (informative)
Production aperture

A.1 Production aperture

A production aperture for the studio digital signal defines an active picture area of 1280 pixels × 720 lines as produced by signal sources such as cameras, telecines, digital video tape recorders, and computer-generated pictures conforming to this standard.

A.2 Analog blanking tolerance

A.2.1 The duration of the maximum active analog video signal measured at the 50% points is standardized as 1280 clock periods. However, the analog blanking period may differ from equipment to equipment and the digital blanking may not coincide with the analog blanking in actual implementation.

A.2.2 To maximize the active video duration in picture origination sources, it is desirable to have analog blanking match digital blanking. However, recognizing the need for reasonable tolerance in implementation, analog blanking may be wider than digital blanking (see figures 3 and 5).

A.2.3 To accommodate a practical implementation of analog blanking within various studio equipment, a tolerance of six clock periods is provided at the start and end of active video. Accordingly, the analog tolerance to parameters b and e of table 5 are as follows:

Parameter	Definition	Nominal value (T)	Tolerance (T)
b	0_H to end of active video	1540	– 6 + 0
e	0_H to start of active video	260	– 0 + 6

Preferred practice is to provide a full production aperture signal at the output of an analog source prior to first digitization, reserving the tolerance for possible subsequent analog processes.

A.2.4 The relationship of the associated analog representation (inclusive of this tolerance) with the production aperture is shown in figure 5.

A.3 Transient regions

A.3.1 This standard defines a picture aspect ratio of 16:9 with 1280 pixels per active line and 720 active lines per frame. However, digital processing and associated spatial filtering can produce various forms of transient effects at picture blanking edges and within adjacent active video that should be taken into account to allow practical implementation of the studio standard.

A.3.2 Analog transients. The following factors contribute to these effects:

– Bandwidth limitation of component analog signals (most noticeably, the ringing on color-difference signals);

– Analog filter implementation;

– Amplitude clipping of analog signals due to the finite dynamic range imposed by the quantization process;

– Use of digital blanking in repeated analog-digital-analog conversions; and

– Tolerance in analog blanking.

A.4 Clean aperture

A.4.1 The bandwidth limitation of an analog signal (pre- and post-filtering) can introduce transient ringing effects which intrude into the active picture area. Also, multiple digital blanking operations in an analog-digital-analog environment can increase transient ringing effects. Furthermore, cascaded spatial filtering and/or techniques for handling the horizontal and vertical edges of the picture (associated with complex digital processing in post-production) can introduce transient disturbances at the picture boundaries, both horizontally and vertically. It is not possible to impose any bounds on the number of cascaded processes which might be encountered in the practical post-production system. Hence, recognizing the reality of those picture edge transient effects, the definition of a system design guideline is introduced in the form of a subjectively artifact-free area, called clean aperture.

A.4.2 The clean aperture defines an area within which picture information is subjectively uncontaminated by all edge transient distortions. In order to minimize the effects on subsequent compression or transmission processes, the contaminated area should be confined within 16 pixels and 9 lines of the production aperture edges.

A.4.3 The clean aperture of the picture defines a region 1248 samples in width by 702 lines high, symmetrically located in the production aperture. The clean aperture shall be substantially free from transient effects due to blanking and picture processing. An encroachment of 6 samples maximum on each of the left and right edges of the production aperture is allowed for horizonal blanking errors generated by analog processing. Vertical blanking shall be as specified with zero tolerance.

A.4.4 This yields a minimum clean aperture of 1248 horizontal active pixels by 702 active lines whose quality is guaranteed for final release. The clean aperture lies within the production aperture as shown in figure A.1.

A.4.5 It is good practice to minimize variations in analog blanking and to use techniques in digital processing that minimize or prevent transients in the allowed contaminated area as well as inside the clean aperture.

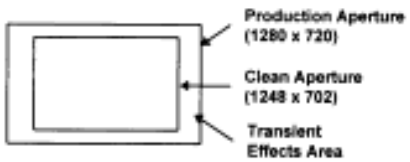


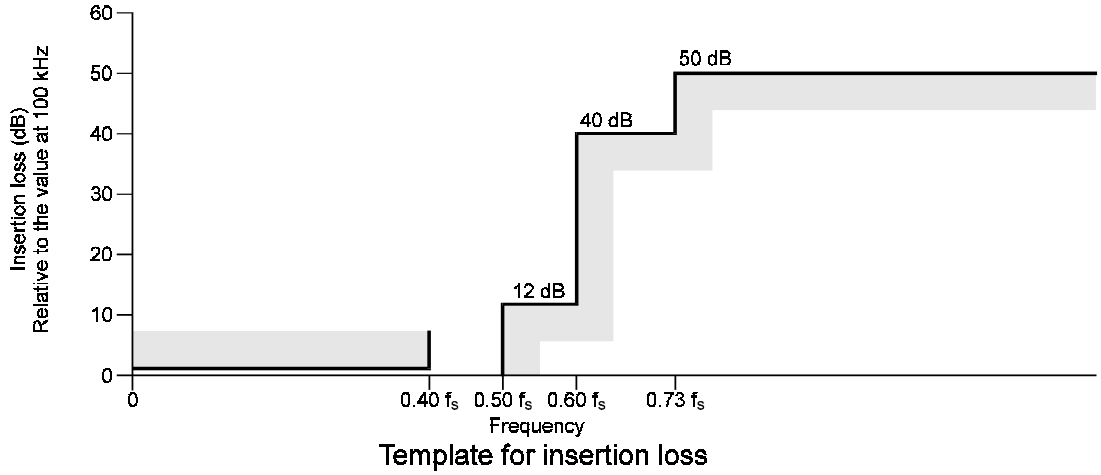
Figure A.1 – Clean aperture

Annex B (informative)
Pre- and post-filtering characteristics

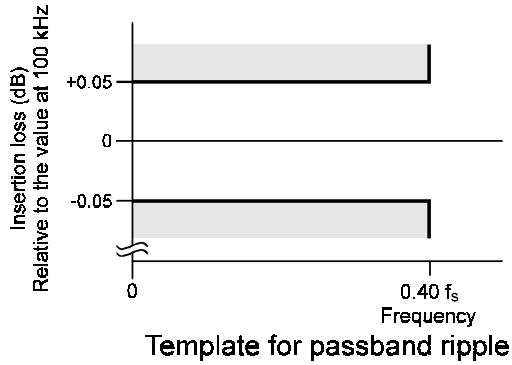
B.1 Figure B.1 depicts example filter characteristics for pre- and post-filtering of Y′, R′, G′, and B′ component signals. Figure B.2 depicts example filter characteristics for pre- and post-filtering of P'_B and P'_R component signals.

B.2 The passband frequency of the component Y′, R′, G′, and B′ signals is nominally 30 MHz.

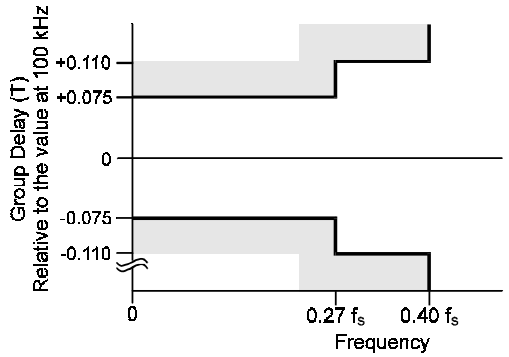
B.3 The value of the amplitude ripple tolerance in the passband is ± 0.05 dB relative to the insertion loss at 100 kHz.



Template for insertion loss



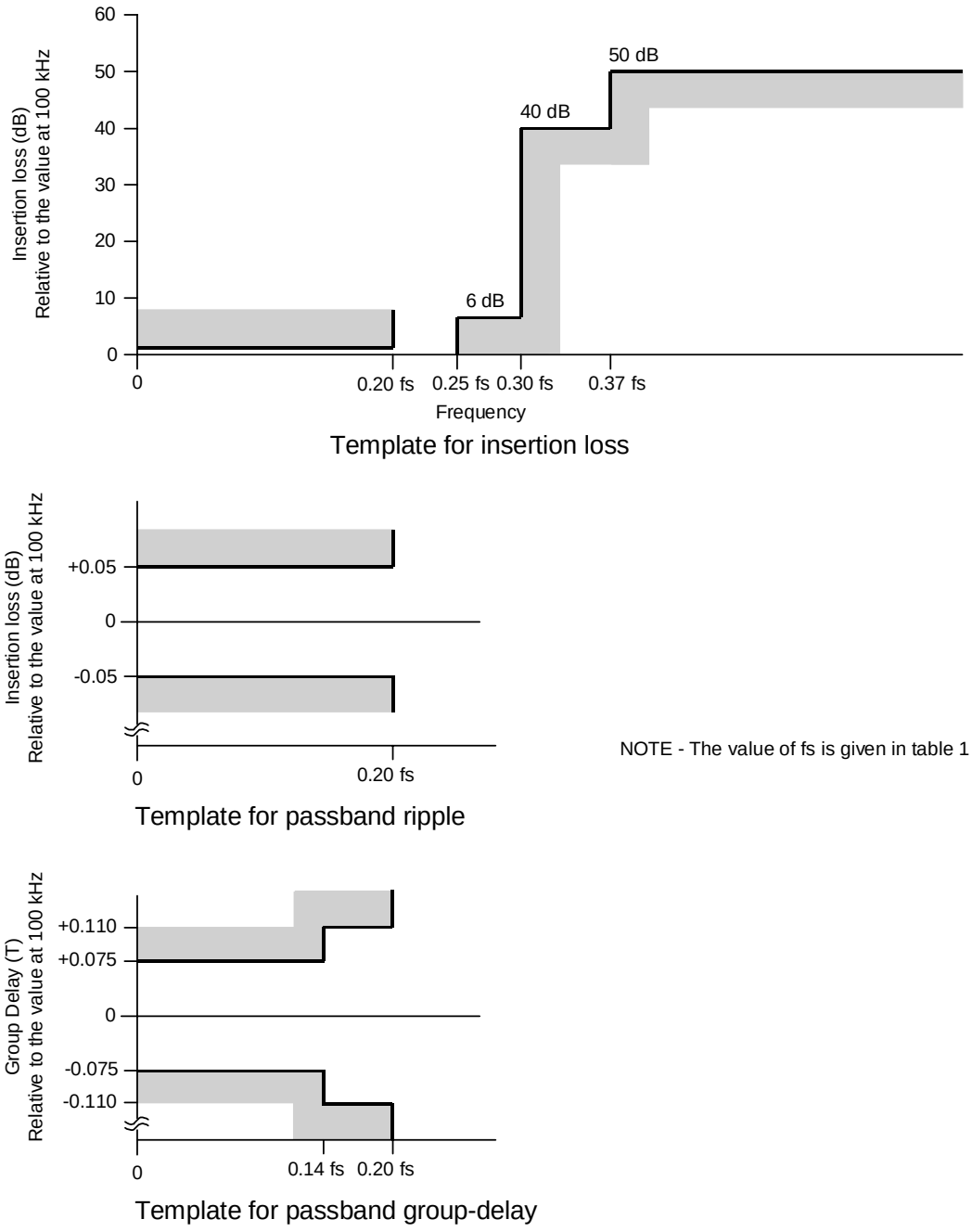
Template for passband ripple



Template for passband group-delay

NOTE - The value of f_s is given in table 1

Figure B.1 – Example filter template for Y′ and R′G′B′ components



NOTE - The value of fs is given in table 1

Figure B.2 – Example filter template for P'_B and P'_R components

B.4 The insertion loss characteristics of the filters are frequency-scaled from the characteristics of ITU-R BT.601. Insertion loss is 12 dB or more at half the sampling frequency of the Y′, R′, G′, and B′ components, and 6 dB or more at half the sampling frequency of the P'_B and P'_R components relative to the insertion loss at 100 kHz.

B.5 The specifications for group-delay in the filters are sufficiently tight to produce good performance while allowing the practical implementation of the filters.

Annex C (informative)
Bibliography

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