

A large, faint, light blue graphic is centered in the background. It features a globe with latitude and longitude lines, overlaid with several curved lines and arrows that suggest motion or a network. The text "Verification of Optical module timing performance" is superimposed on this graphic.

Verification of Optical module timing performance

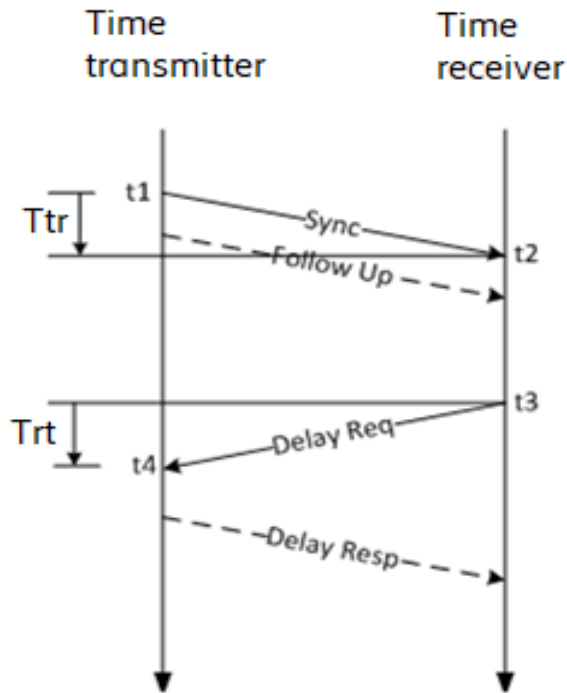
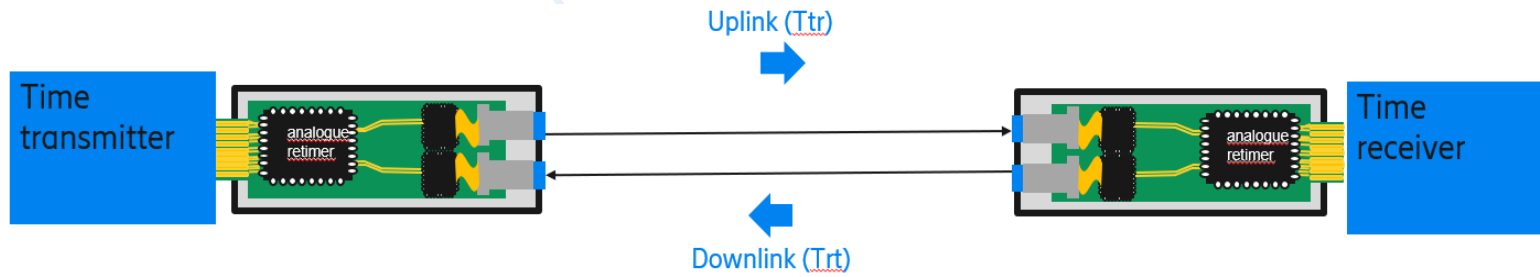
Verification of Optical modules Timing performance

PAM4 optical modules have significant latency (10's of ns) as well as variation in latency

Latency and Latency variation are very important in applications requiring accurate timing (e.g. 5G).

A solution for accurately measuring the Latency of PAM4 optical modules is required.

Time Error in Fiber Optics



$$\text{Delay} = [(t2 - t1) + (t4 - t3)] / 2 = (Ttr + Trt) / 2$$

$$\text{Offset} = t2 - t1 - \text{Delay} = Ttr - \text{Delay}$$

*If Ttr and Trt are different, half the difference becomes **time synchronization error** for the time receiver*

Sources of delay differences in Fiber optics:

- Fiber length (every meter contributes 5 ns)
- Chromatic dispersion
- System Internal optical components
- **Optical transceivers and Digital IC**

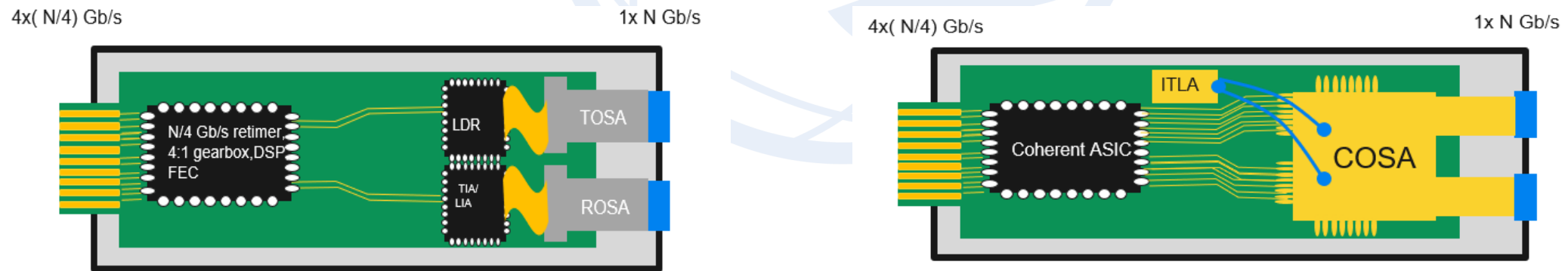
Material from :

[MOPA Technical Paper-v2.0-Final.pdf \(mopa-alliance.org\)](https://mopa-alliance.org/MOPA_Technical_Paper-v2.0-Final.pdf)

MOPA, Mobile Optical Pluggable Alliance is an industry effort publishing technical papers describing all relevant high-level requirements and optical solution "Blueprints" for mobile optical transport

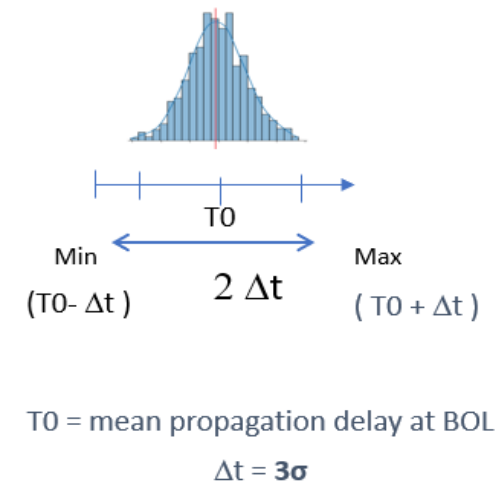
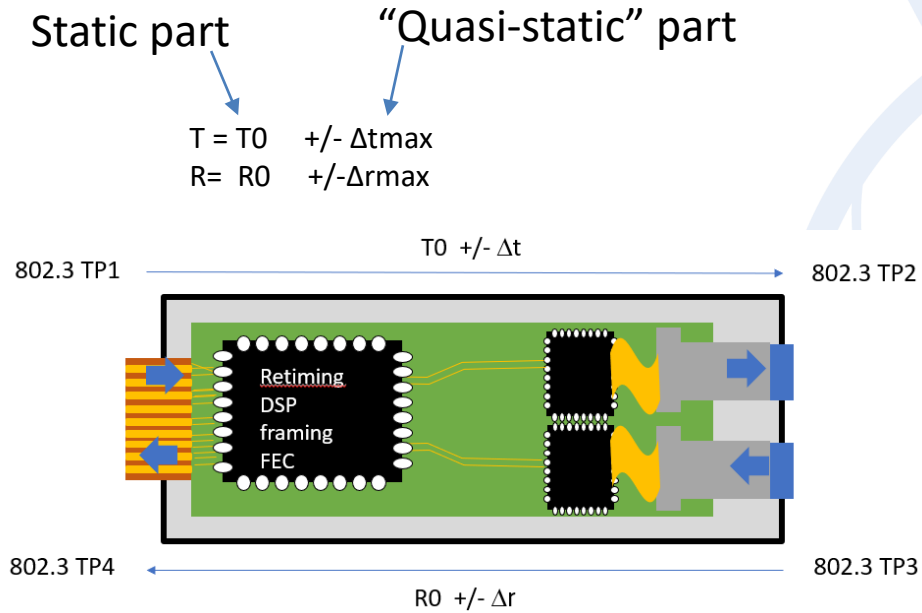
Pluggables with increasing complexity

- **Potential source of time error in complex digital parts of pluggables.**
- Higher bit rates (50 Gb/s and higher) and adoption of advanced modulation formats (PAM-4 or Coherent), require complex digital signal processors (DSPs) in optical pluggables.
 - The presence of DSPs can potentially make T_{tr} and T_{rt} significantly different.
 - more complex digital functions like gear-boxing, framing and FEC (Forward Error Correction) can be implemented in the DSP and they could dominate the contribution of optical pluggables)



Latency compensation

Latency in Optical modules can be compensated for with values stored in the module EEPROM.



These values can be measured during Design Validation Testing (DVT), by grabbing a population of transceivers and measuring Tx and Rx propagation delays at corners and several times after link re-start conditions.

T_0 , R_0 stored in transceiver's EEPROM and compensated for at node level.

Δt_{max} and Δr_{max} contribute to the worst case cTE, which for a **single** pluggable is

$$cTE_{max} = \pm \frac{1}{2} (\Delta t_{max} + \Delta r_{max})$$

Structure of the additional EEPROM data content for propagation delay characterization:

For each supported mode:

- Typical Tx propagation delay (10 ps to 50 μ s).
- Typical Rx propagation delay (10 ps to 50 μ s).
- Quasi-static Tx propagation delay (10 ps to 100 ns)
- Quasi-static Rx propagation delay (10 ps to 100 ns)

MOPA Methodology for Delay Characterization

- Classes of pluggables defined based on achievable accuracy
- Examples:
 - “Class C.2” pluggable : 2% of the cTE budget ITU-T G.8273.2 allocated for Class C nodes.
For very simple pluggable implementations, maintaining an analogue signal chain.
 - “Class A.20” pluggable : 20% of the cTE budget ITU-T G.8273.2 allocated for Class A nodes.
To enable use of complex digital parts inside the pluggable.

	Class A.10	Class A.20	Class B.10	Class B.20	Class C.2	Class C.10
Max constant time error budget allocated to one pluggable	+/- 5ns	+/-10ns	+/- 2ns	+/- 4ns	+/- 0.2ns	+/- 1ns
	$\Delta T_{max} = +/- 5ns$	$\Delta T_{max} = +/- 10ns$	$\Delta T_{max} = +/- 2ns$	$\Delta T_{max} = +/- 5ns$	$\Delta T_{max} = +/- 0.2ns$	$\Delta T_{max} = +/- 1ns$
	$\Delta r_{max} = +/- 5ns$	$\Delta r_{max} = +/- 10ns$	$\Delta r_{max} = +/- 2ns$	$\Delta r_{max} = +/- 5ns$	$\Delta r_{max} = +/- 0.2ns$	$\Delta r_{max} = +/- 1ns$

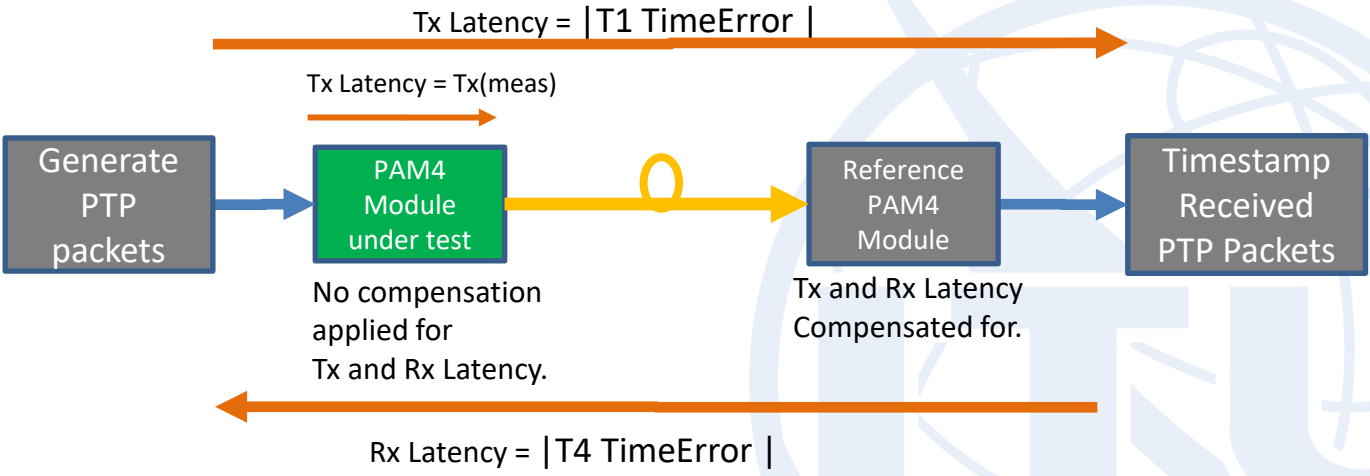
Table APB.2: Proposed optical pluggable classes.



Latency Measurement using PTP

Accurate (ns) evaluation of PAM4 Module Tx and Rx; e.g., for use at **System Verification activities**

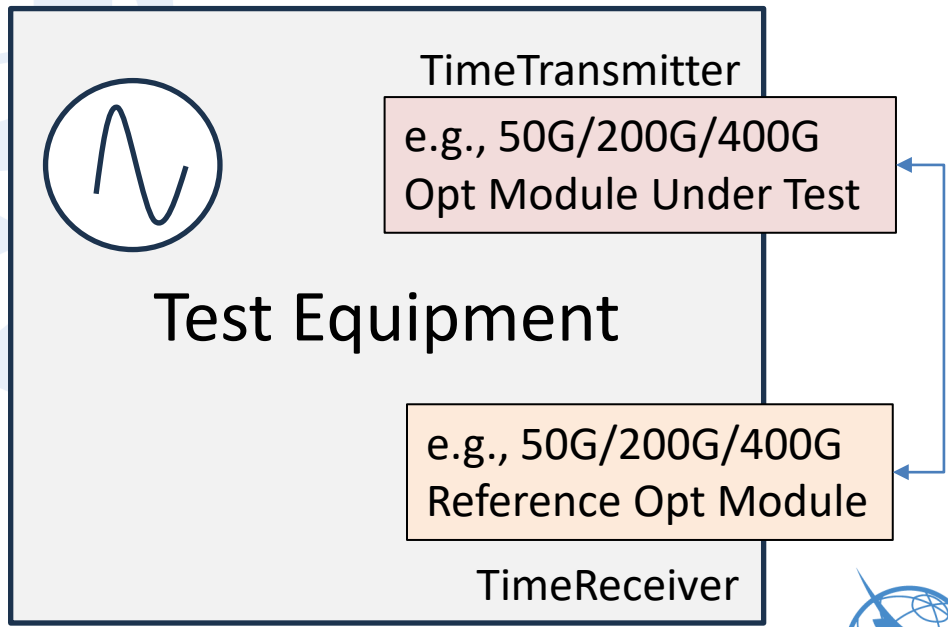
Note: baseline tests with pair of reference PAM4 modules can be done to improve accuracy



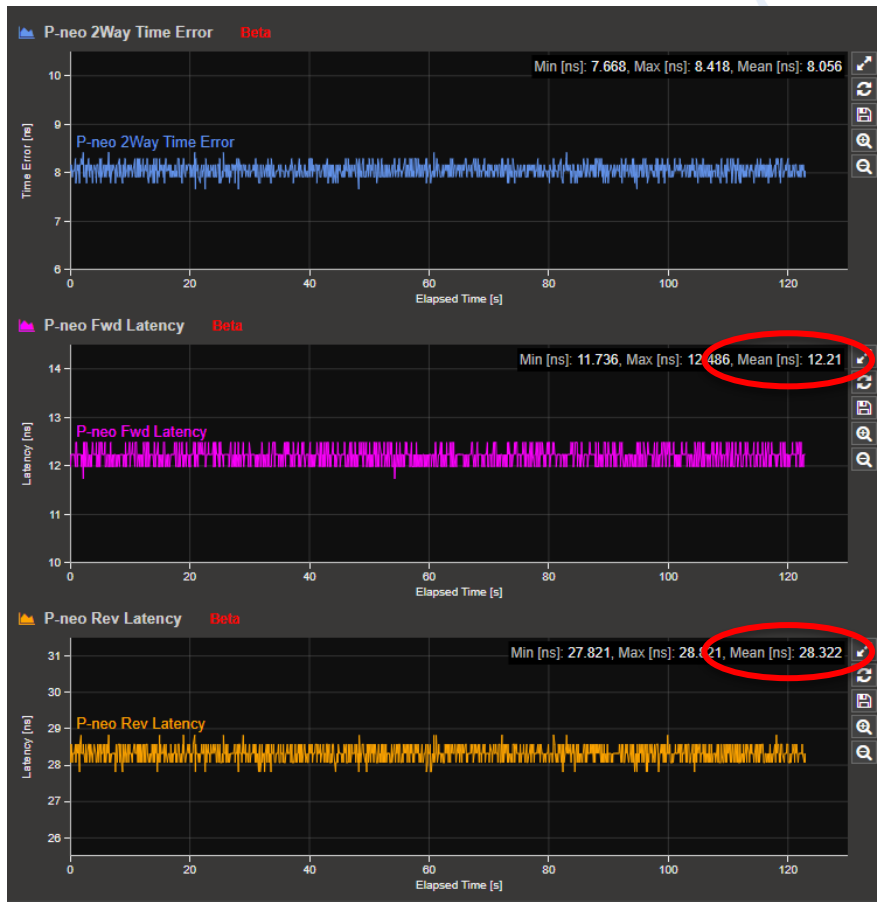
For a PTP Transparent clock measurement, T1 and T4 should equal 0, provided the correct compensation is used for Optical modules and Optical fibre.

- Measured **T1** time error provides the **Tx latency** of the Module
- Measured **T4** time error provides the **Rx latency** of the Module.

Perform multiple runs for reliable statistics (depends on level of accuracy required, typically 200 runs)



PTP test results 1



Latency Measurements above show

- reset to reset variation
- asymmetry between Tx and Rx latency which needs to be compensated for



PTP Test Results 2

Test Case	Vendor	Mean Latency (ns)	Reset-to-reset Variation (ns)	Packet-to-packet Variaton (ns)
50G SR	Vendor A	68.0	2.1	<1
50G SR	Vendor B	60.9	1.5	<1
400G SR8	Vendor A	70.9	3.0	<1
400G LR8	Vendor A	64.8	3.5	<1
400G FR4	Vendor A	73.8	1.2	<1
400G FR4	Vendor C	74.9	1.4	2.5

Table 1: Results for Optical module latency measurement Different Vendors and reset to reset variation

Test Case	Asymmetry	Total Latency (ns)	Tx Latency (ns)	Rx Latency (ns)
400G SR8	Measured asymmetry	70.9	26.0	44.9
400G SR8	Assumed 50/50	70.9	35.45	35.45
400G SR8 Error	-		-9.45	+9.45

Table 2: Error introduced by Optical module asymmetry

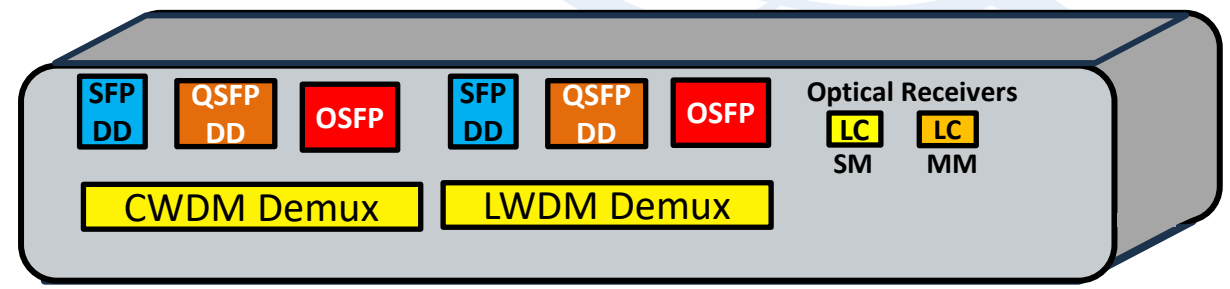
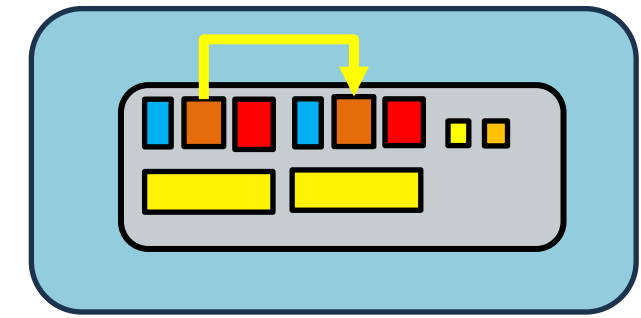
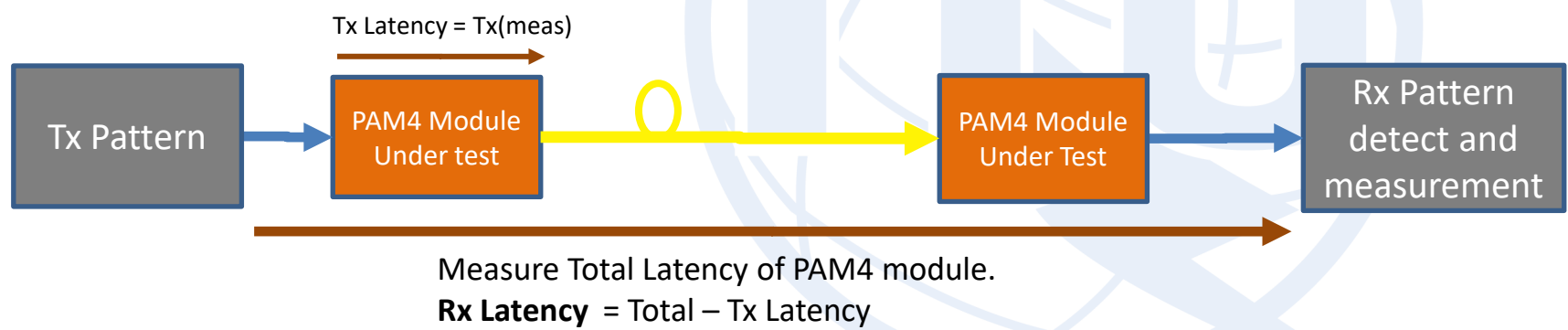
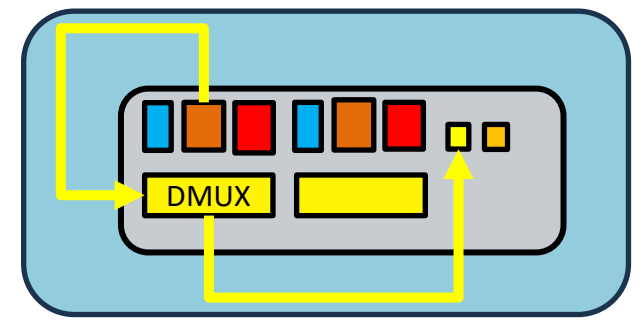
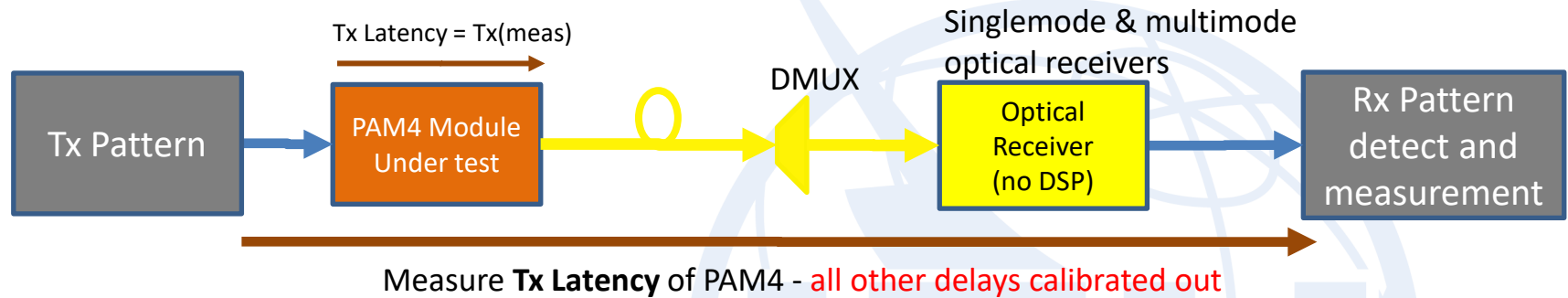
Test Case	Total Latency (ns)	Tx Latency (ns)	Rx Latency (ns)
50G PAM4 SR	68.1	25.0	43.1
50G PAM4 LR	68.1	25.0	43.1
100G PAM4 LR (QSFP28)	334.0	124.1	209.9
100G PAM4 LR (SFPDD)	103.6	38.7	64.9
200G SR4	70.0	26.0	44.0
200G FR4	63.1	24.0	39.1
400G SR8	70.9	26.0	44.9
400G FR8	64.8	24.0	40.8
400G FR4	73.7	28.5	45.3

Table 3: Tx/Rx Latencies for different rates and reaches

Latency Measurement using Reference Optical Receiver



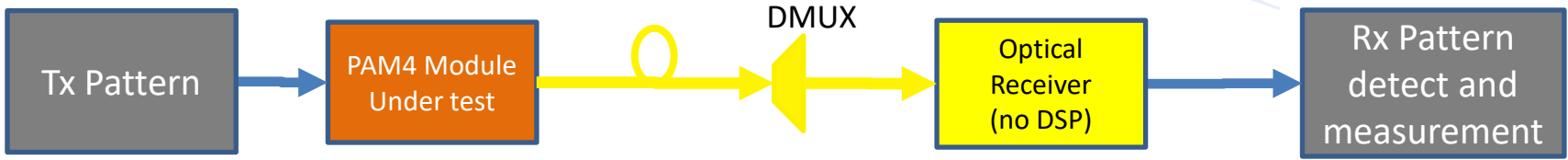
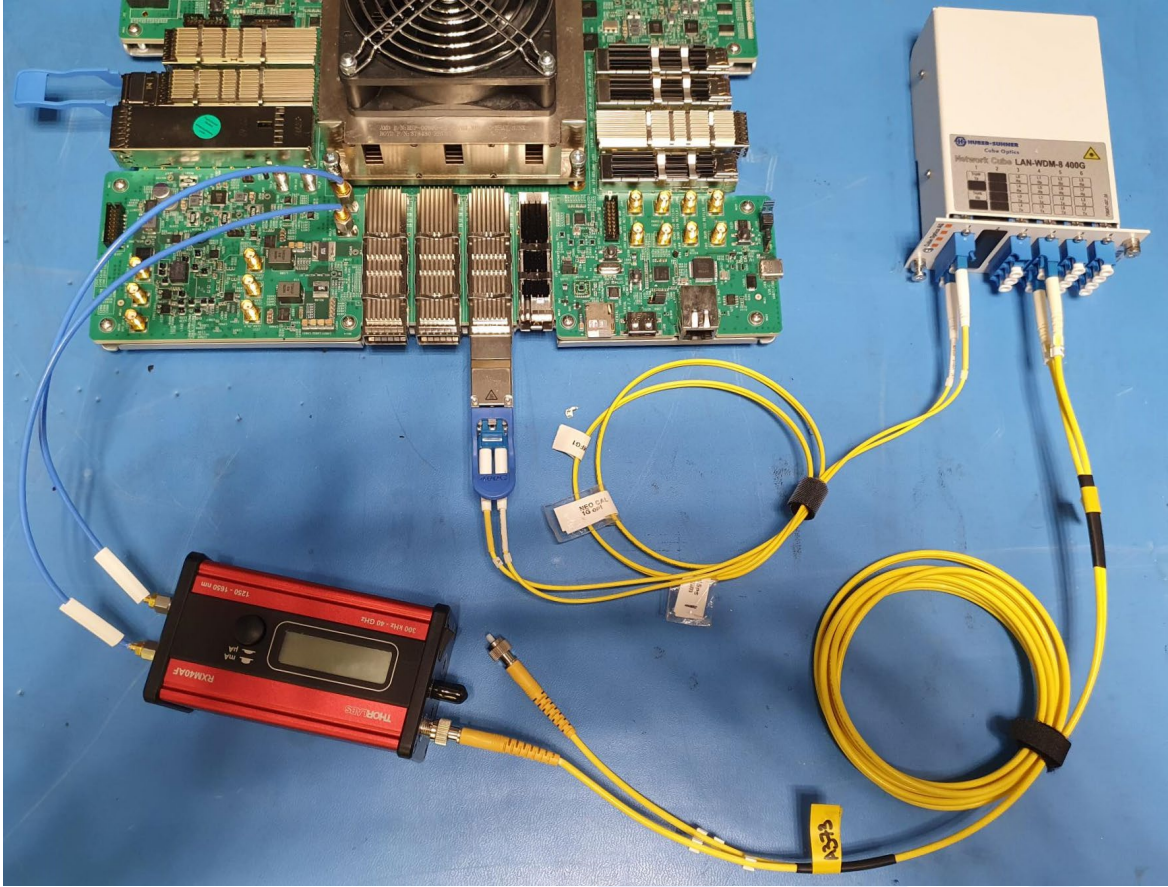
Very Accurate (sub-ns) evaluation of PAM4 Module Tx and Rx;
e.g., for use at **Design Verification Testing**; Used also to build the Reference PAM 4 module in previous set up



Perform multiple runs for reliable statistics (depends on level of accuracy required, typically 100 runs) ¹⁰

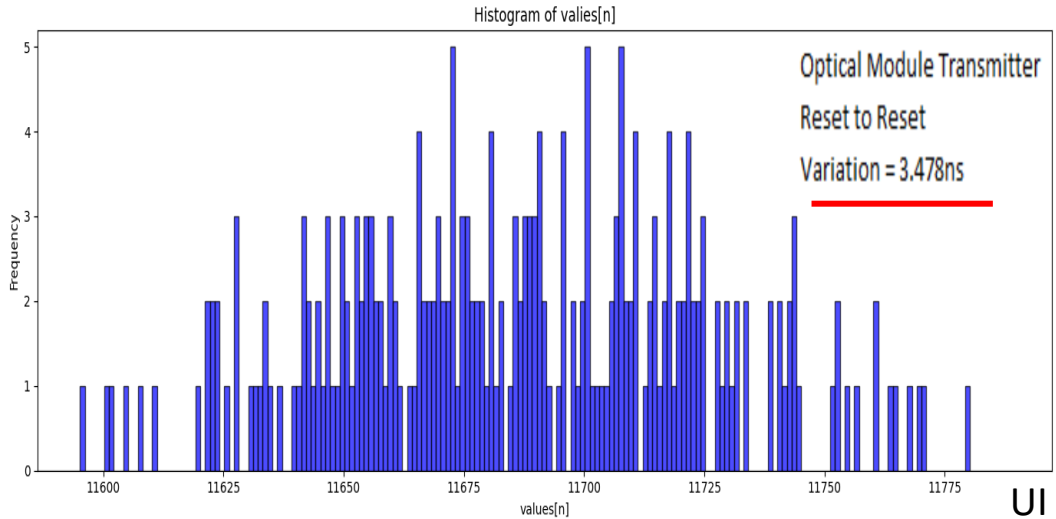
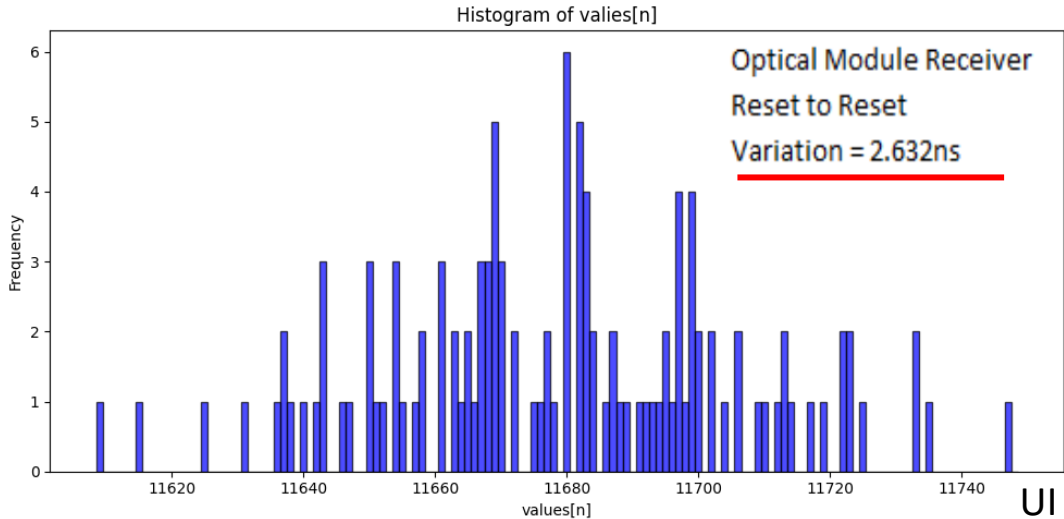


Prototype of Reference Optical Receiver Approach



Optical Receiver Test Results

- 25Gbaud solution working with Measurements done to determine Tx and Rx latency variation independently.



UI = 18.8 ps

- Work ongoing at 50GBaud.



