Digital Multiplexes

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1. Digital Multiplexes

1.1 Introduction

The primary PCM systems are intended for short distance applications. In the medium and long distance network, where high channel capacity is demanded, it is more economical and practical to group together larger number of PCM systems to one common transmission line than to use several primary PCM systems. These higher order systems are also called digital multiplexes.

The basic task of a digital multiplexer is to combine a number of incoming pulse flows, tributaries, into one outgoing pulse flow with a gross digit rate which is somewhat higher than the sum of the tributary rates and vice versa. In a second order system, four primary PCM signals are combined to one common digital signal. The two standardised primary PCM systems originate in two digital multiplexes with different bit rates (see Figure 1). A digital multiplex based on the 30-channel PCM-system has a bit rate of 8448 Kb/S, while the 24-channel PCM-system gives rise to a digital multiplex with a bit rate of 6312 Kb/s.

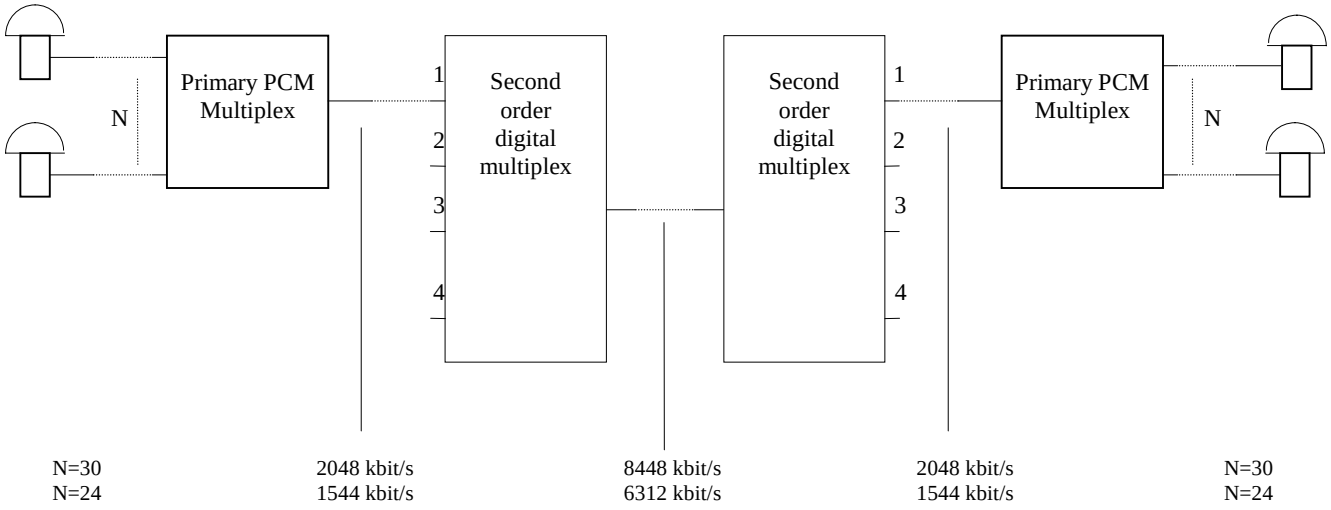

Figure 1

Digital transmission systems can be tied together in a hierarchy, in the same way as the FDM systems. A digital multiplex hierarchy, based on the 30-channel PCM-system, is shown in Figure 2. From the Figure, it can be seen that the transmission facilities can be used not only for pulse code modulated speech, but also for data, visual telephone, FDM groups and TV.

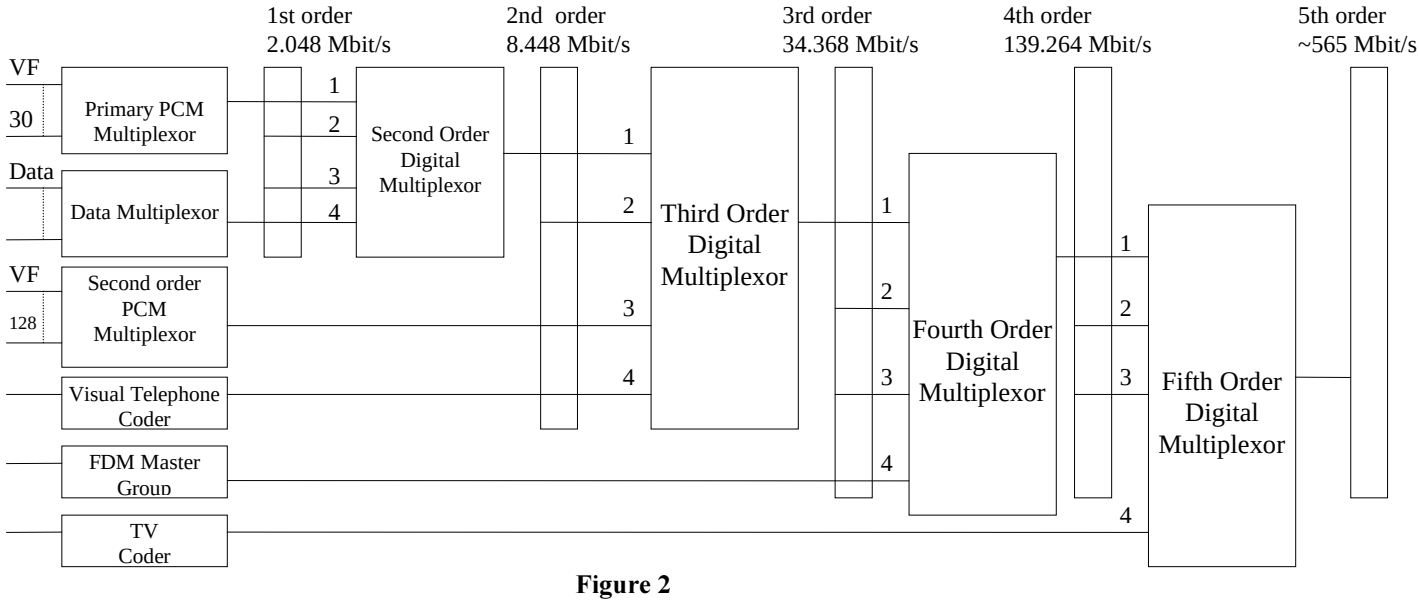

Figure 2

1.2 **The Second Order Digital Multiplex**

The basic principles for digital multiplexing are the same in all hierarchical stages. Multiplexing in the second order multiplexer can therefore serve as a general model. The main principle for digital multiplexing is the bit interleaving process in which the tributaries are combined bit by bit to a common outgoing bit flow (see Figure 3).

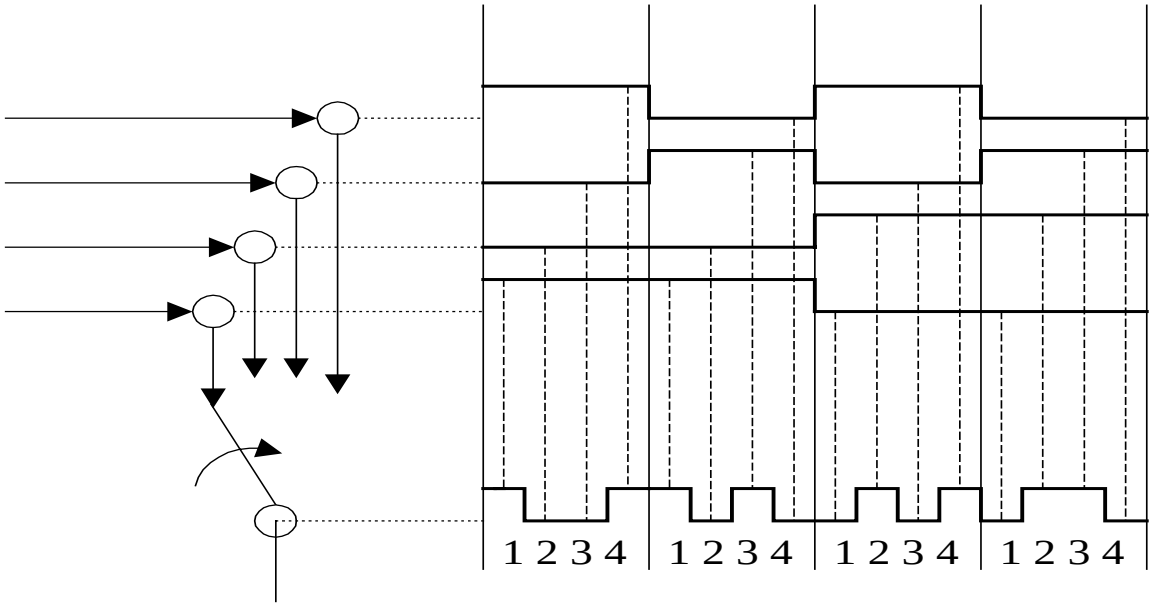

Figure 3 : Bit interleaving

When entering the bit interleaver, the four tributaries have to be synchronised. All primary multiplexes have independently working clocks, thus giving bit flows with slightly different bit rates and hence different phases.

To attain synchronisation between the tributaries, buffer memories are placed between the tributaries and the bit interleaver. This is shown in the block diagram in Figure 4. Synchronisation is now achieved by reading out bits from the buffer memory with a higher bit rate than when writing bits into it. The read out rate is 2112 Kb/s, thus giving a second order bit rate of 4 x 2112 = 8448 Kb/s. The nominal bit rate of a primary flow is 2048 Kb/s. A control unit orders read out from the four buffer memories at the same time. The read out has to be done in showers because of the higher bit rate.

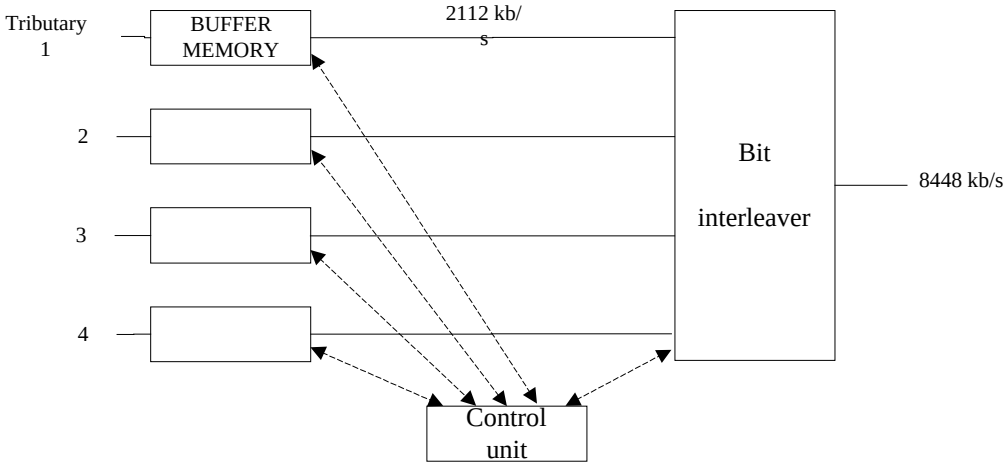

Figure 4

The second order frame structure is decided by the control unit where second order frame alignment word (1111010000), two Service bits and justification control bits are inserted into the available time between the showers (sub-frames) - see Figure 5.

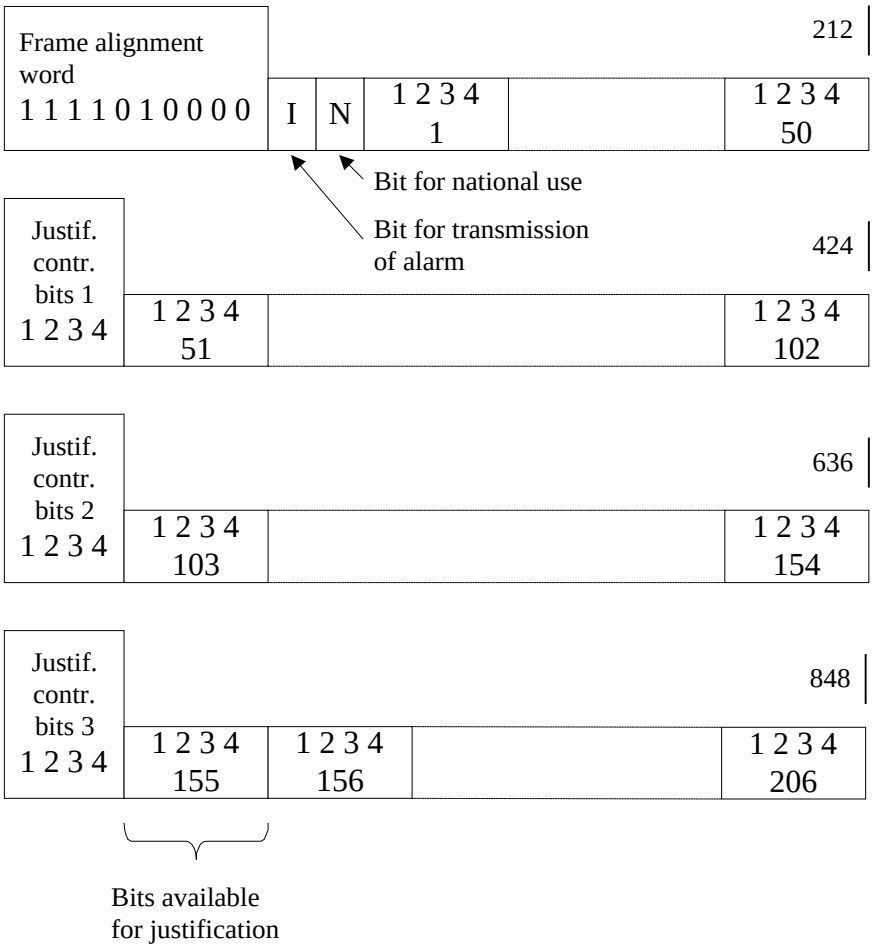

Figure 5

Here, the justification control bits and the four bit word no. 155 call for more detailed explanation. Since the bit rates of the tributaries are allowed to vary somewhat from their nominal value of 2048 Kb/s, while the read out rate from the buffer memories is always constant, there is a risk of exhausting some buffer memories. The risk is eliminated by stopping the read out of that memory during the period of one bit. The four bit word no. 155 (one bit/tributary) is reserved for this purpose. The bit positions contain either information from tributaries or redundant bit depending on the load in the buffer memories.

If one of the bit positions in the bit word no. 155 carries tributary information, the three corresponding justification control bits are set to ONE, otherwise they are set to ZERO. The receiving multiplexer can then make a majority decision by means of the three justification control bits. Consequently, an isolated bit error will not upset the result.

In the receiving direction, the frame alignment word is used as a reference when dividing the incoming digital signal into its components. The status of the justification control bits is noted and unwanted bit words no. 155 are removed. The bits are written into buffer memories in order to smooth variations in the transmission. The read out from the buffer memories takes place at the same bit rate as an average of the original tributary signal.