Interfaces Associated with

a Digital Switch

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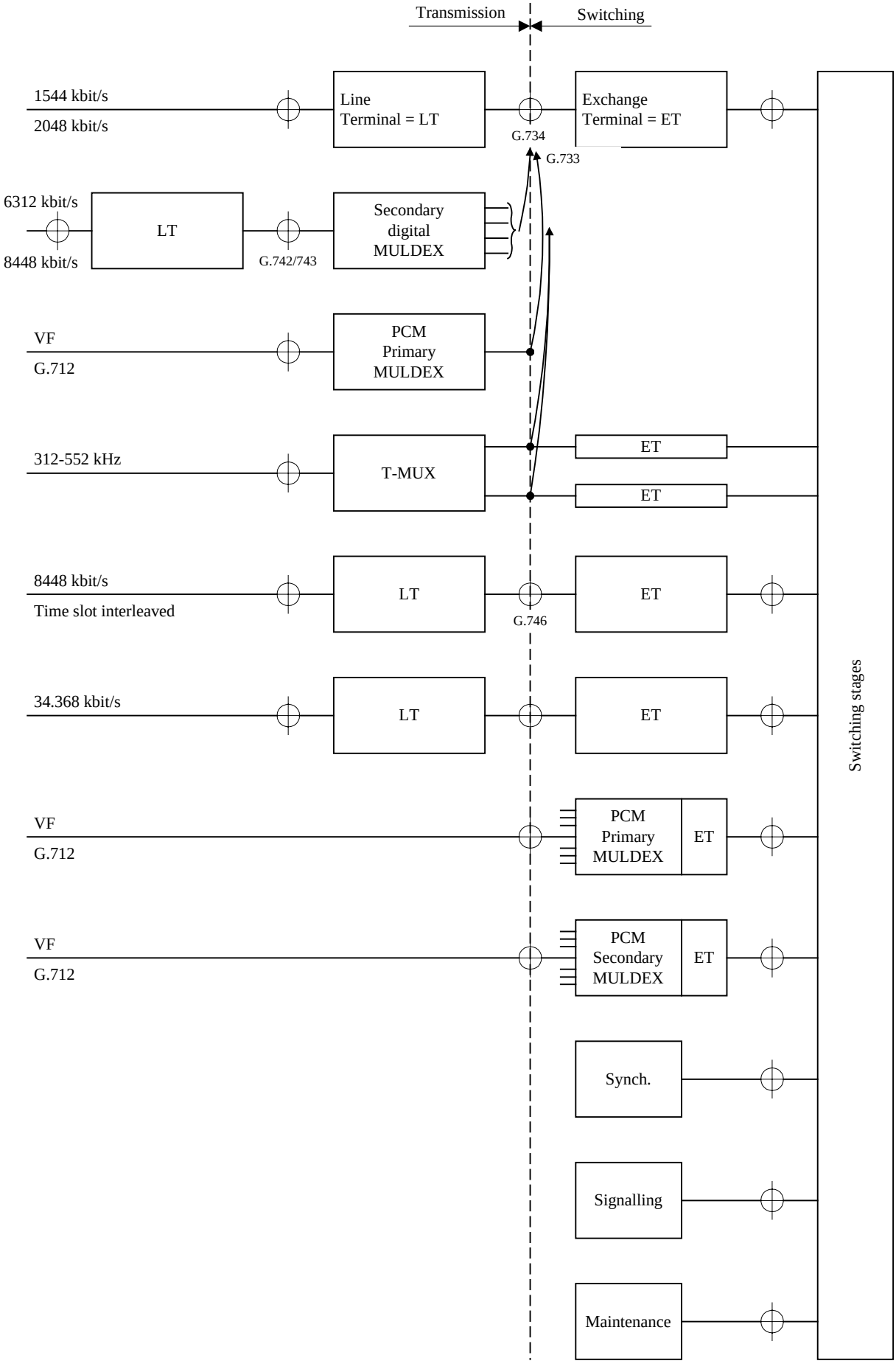
INTERFACES ASSOCIATED WITH A DIGITAL SWITCH



Digital Switching

1. Introduction
2. Block description of a Digital Group Selector
3. The Digital switching network

1. INTRODUCTION

Digital technology is constantly reducing the cost of solutions to telecommunication problems. For economic reasons PCM transmission was widely introduced during the 1960's. Transmission of conversations between exchanges was achieved by putting analogue speech into digital packets or time slots. Conversion back to analogue being necessary for switching purposes. Development has made it possible and economical to switch incoming time slots to the required outgoing time slot, directly. For routing purposes an incoming conversation in a certain time slot of a PCM system, needs to be connected to an outgoing circuit, another certain time slot on another PCM system. The digital switch switches a digital speech sample in an incoming time slot to the chosen outgoing time slot towards the next point in the telephone network. See Fig. 1.

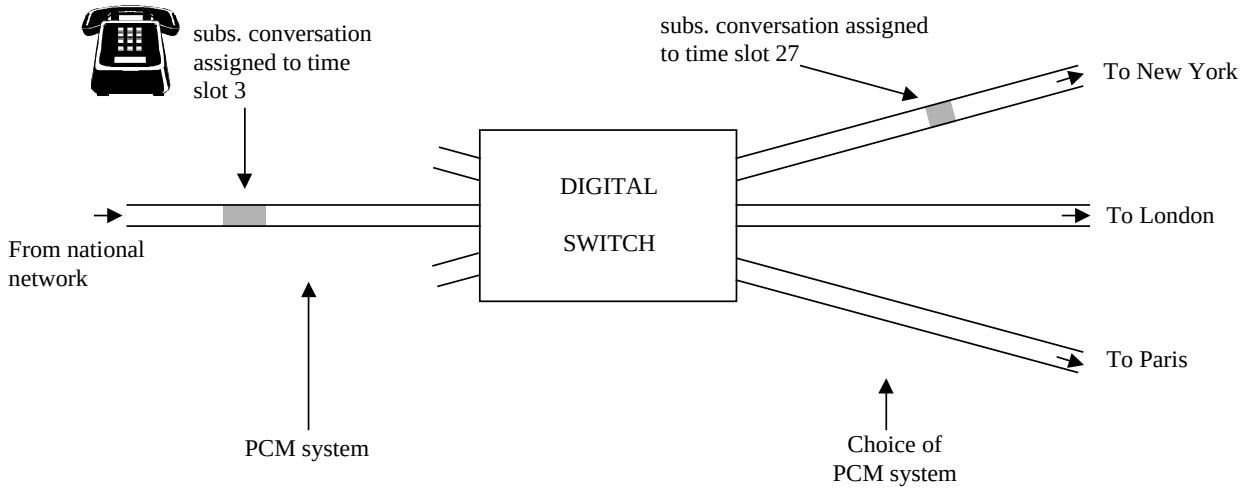


Fig. 1 The subscriber is to be connected to New York, a free time slot has to be selected in the outgoing PCM system to New York (e.g. time slot 27)

2. BLOCK DESCRIPTION OF A DIGITAL GROUP SELECTOR

A DGS must be able to work in a network with a mixture of different transmission principles. It must be possible to connect PCM Links as well as analogue Links with FDM or voice frequency transmission. This will influence the circuits which serve as interfaces between the Lines and the switch. For a start we shall assume that the lines connected to the DGS are all analogue voice frequency lines. The differences which arise when the lines are digital will be discussed later.

Analogue environment

A model of a DGS in an analogue environment is shown in Fig. 2. It consists of the following blocks:

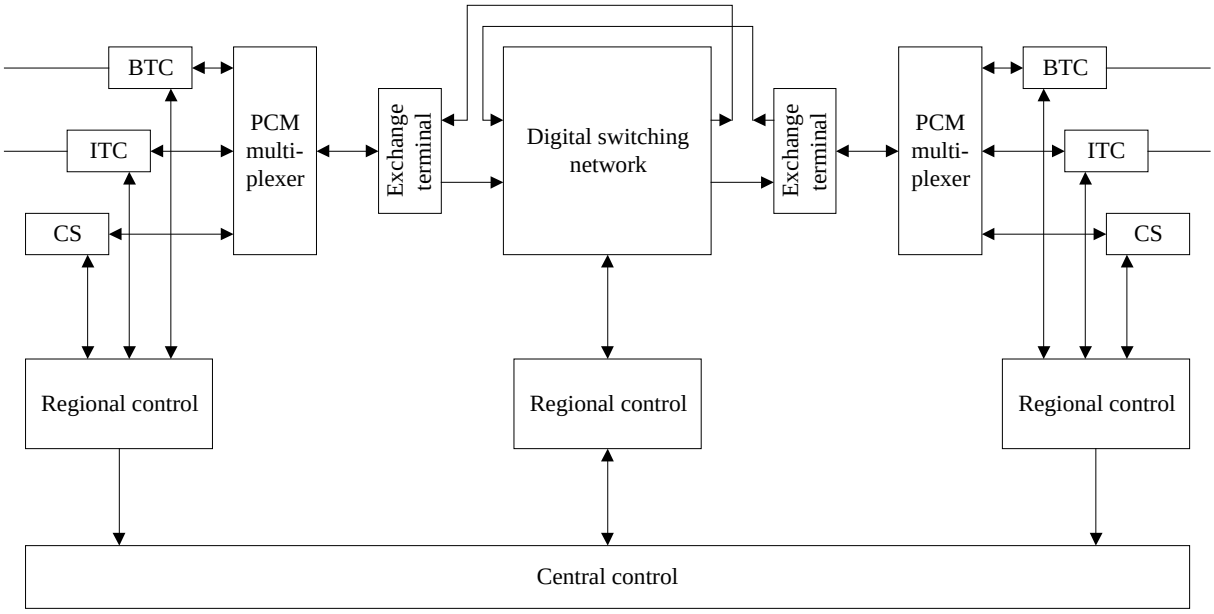


Fig. 2 Block diagram of a digital group selector and associated control in an analogue environment.

Line relay sets

As the Lines are analogue the Line relay sets (Incoming, Outgoing and Bothway Trunk Circuits) are of conventional design. Whether the switching network is analogue or digital is of no importance in this case.

PCM multiplexer

Conversion from analogue signals to PCM transmission is carried out in the PCM multiplexer. In the normal way sampling, quantizing and coding is performed and the output towards the exchange terminal is digital bitstream with, in the CEPT case, 2.048 Mb/s bitrate divided into 32 time slots. This applies to the incoming speech signals; for the outgoing signals the reverse sequence is carried out.

Exchange terminal

The purpose of the exchange terminal is to arrange the time slots, coming from different PCM multiplexers, in phase with the exchange time slots. This is done by buffering and reclocking. In order to optimise the switching network, very often serial/parallel conversion and multiplexing of several PCM-systems are performed. If, for example, eight PCM-ssytems are multiplexed and transmitted in parallel on an eight-wire bus, the original frequency, 2.048 Mb/s, is preserved on each wire.

Digital switching network

The switching network performs switching between the time-multiplexed buses. It consists of digital, electronic components. The time-multiplexed use of these, combined with their moderate price allows practical realisations without any or with extremely low internal blocking. As the digital components are transmissionwise unidirectional, i.e. simplex, two different paths through the network are needed to obtain a bi-directional, duplex, connection.

In part 3 a more detailed treatment of the switching network is given.

Regional and central control.

The control of the group selector is performed with some type of processor system. As the telephony process is the same whether the switching network is digital or analogue the control of a DGS does not differ significantly from the control of a semielectronic group selector. Consequently normal SPC techniques can be utilised, where the regional control takes care of frequent and simple functions whereas the central control handles the more complex functions.

Signalling

The register signalling is handled by code senders (CS) and code receivers (CR) in a conventional way. Signals from other exchanges are extracted from the Line relay sets and multiplexed into the control system, while signals to other exchanges are injected into the Line relay sets by the control. Any signalling system for analogue Lines can be used.

Digital environment

Up till now we have assumed that only analogue Lines are connected to the DGS. If digital Lines, PCM systems, are connected we obtain the situation in Fig. 3.

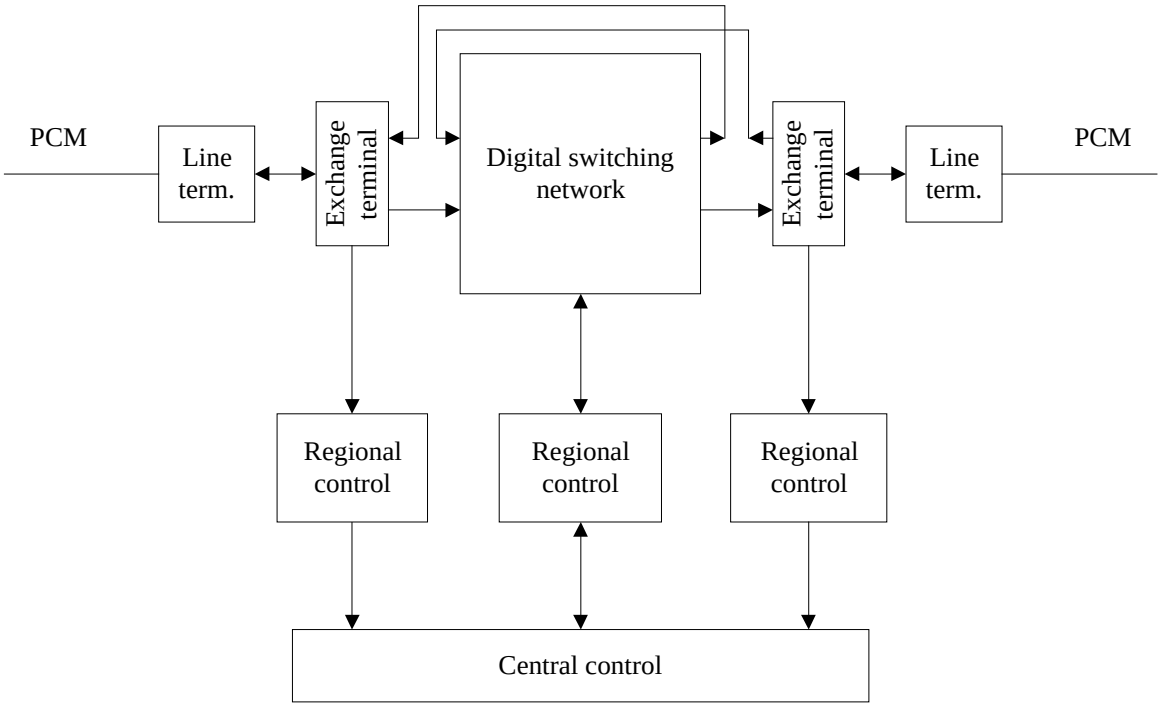


Fig. 3 Block Diagram of a digital group selector and associated control in a digital environment,

The essential differences between this picture and picture 2 are:

Line terminal

As the incoming signals are already digital, no analogue/digital conversion is needed and no complete PCM multiplexers used. Instead simple Line functions such as power feeding and regeneration. Functionally these terminals belong to the PCM transmission system.

Signalling

The most interesting signalling method to be used between digital exchanges is common channel signalling. The information in the signalling channel, channel 16, can either be extracted/injected directly by the exchange terminal before switching, or taken via the switching network.

3. THE DIGITAL SWITCHING NETWORK

Building blocks

The switching network performs switching between time-multiplexed buses. To allow connection between different time slots on different buses both switching in time and switching in space are necessary. Time space switching is performed by crosspoint matrixes.

A connection through the switching network implies exchange of information between an incoming and an outgoing channel. This interchange is achieved by a certain sequence of time and space switching. As a normal call is in progress during many PCM frames (in the order of one million), this sequence has to be repeated once every PCM frame during the whole call. This requires some kind of cyclic control which is achieved by control memories.

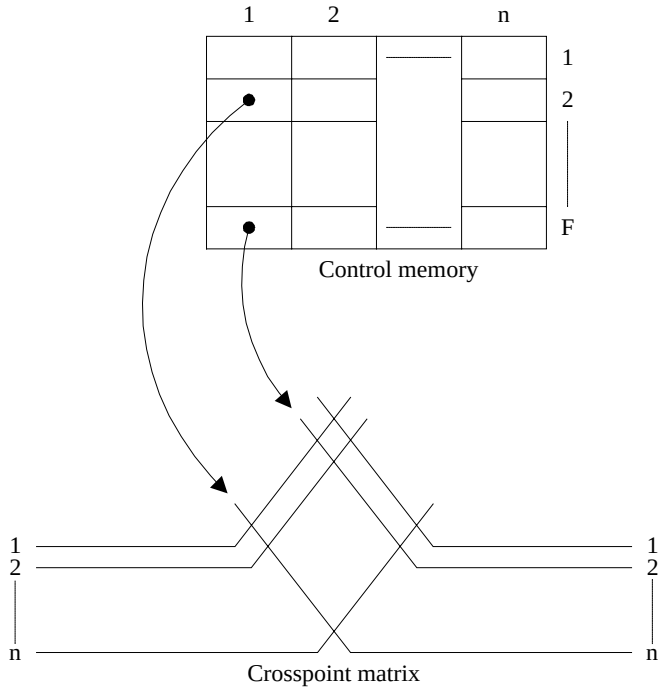


Fig. 4 Space Switch

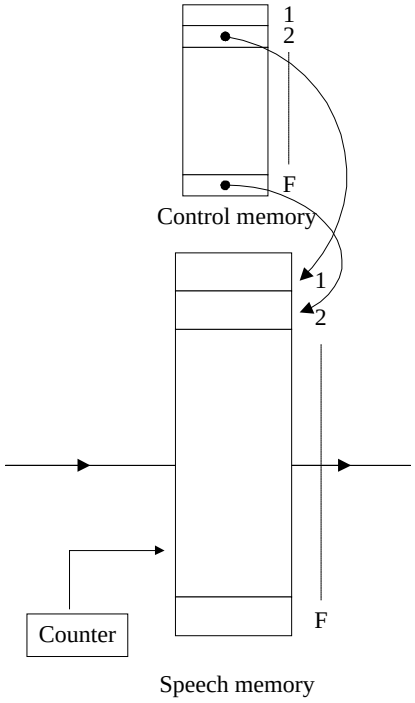


Fig. 5 Time Switch

A space switch and a time switch with their control memories are shown in Fig. 4 and 5. The space switch consists of a crosspoint matrix, n x n, where the individual crosspoints consist of digital, electronic gates. Each crosspoint column is assigned a column of the control memory, which has as many words, F, as there are time slots. Typical figures for F are from 32 up to 1024. During each individual time slot the crosspoint matrix works as a normal, space divided matrix with full availability between incoming and outgoing buses, the crosspoints being controlled by certain cells in the control memory. Just in the shift between two time slots the control memory is advanced one step and during the new time slot a completely different set of crosspoints is activated. This goes on in cycles of F steps. This time-divided behaviour increases the utilisation of crosspoints in the order of 32 to 1024 times as compared to a normal space divided switch.

The time switch (Fig. 5) consists of a speech memory, where the PCM words are delayed an arbitrary number of time slots (less than one frame). The speech memory is controlled by a control memory. The writing of the information of the incoming time slots into the speech memory can be sequential and controlled by a simple counter, time slot No 1 into cell No 1, No 2 into cell No 2 etc., while the reading of the speech memory is controlled by the control memory. This memory has as many cells as there are time slots, and during each time slot it orders the reading of a specific cell in the speech memory. The effective delay, switching in time, is obviously the time difference between the writing into the speech memory and the reading out of the memory.

As long as the information in the control memories is unchanged, the same sequence of space and time switching is performed cyclically, frame after frame. During connection and disconnection of a call this information is changed by the central and regional control.

Different combinations of space switches, S, and time switches, T, give switching-networks with different qualities. We shall here discuss the TST (time-space-time) structure, and a variant of a TS (time-space) structure, here called the memory principle. For very large networks, additional stages may be added, e.g. forming SSTSS or TSST structures.

TST

A model of a TST network is shown in Fig. 6. It has three incoming and three outgoing buses, each containing 32 time slots. In practice the numbers of time slots is higher, e.g. 256 or 512, achieved after multiplexing and serial/parallel conversion in the exchange terminal, but this does not influence the functioning principle of the switch. The higher figures have rather to do with required capacity and cost optimisation of the switch.

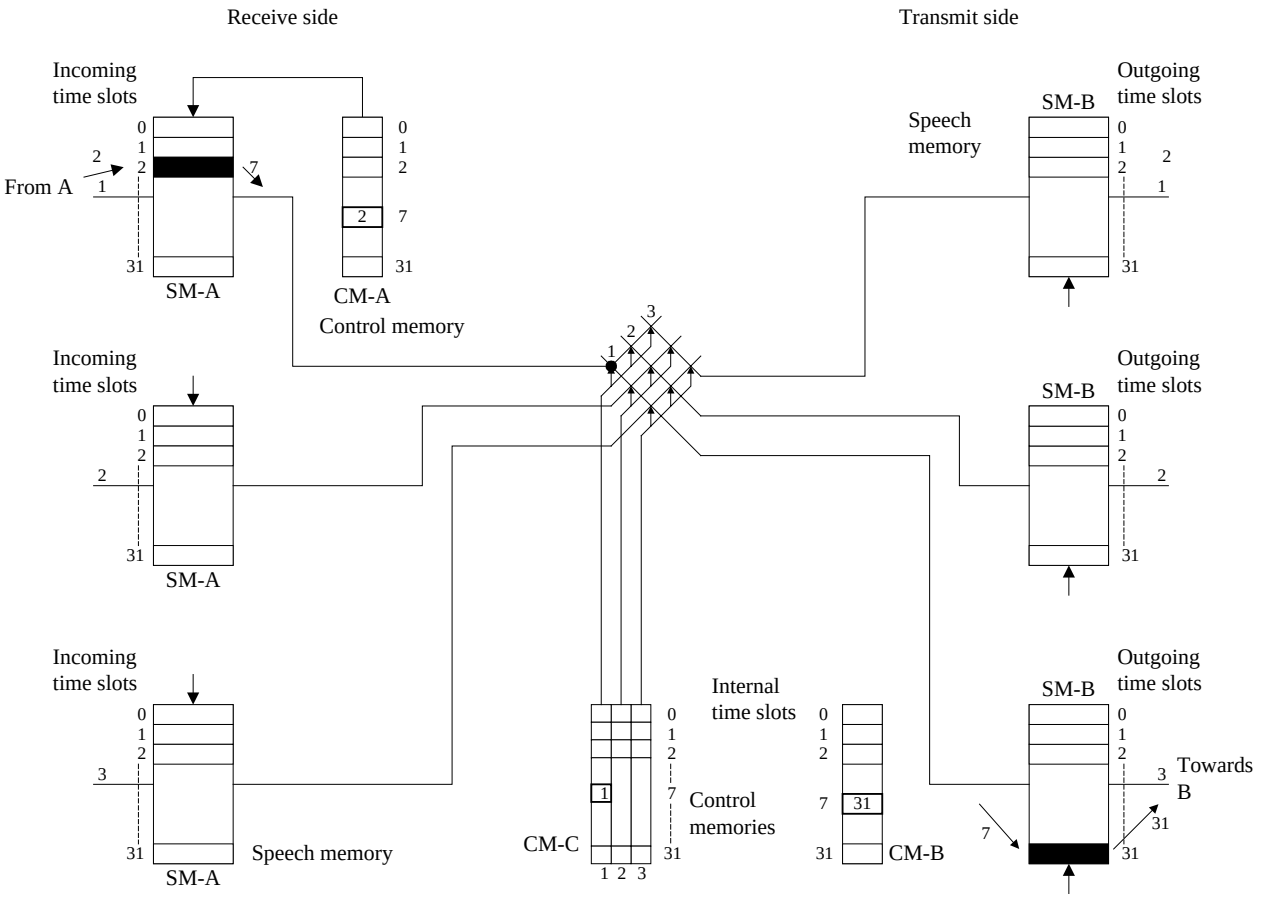


Fig. 6 Digital Switching network, TST structure.

To explain the functioning of the switch we assume, according to the diagram, that the control system orders a connection between inlet A, assigned incoming time slot No 2 on incoming bus No 1, and outlet B, assigned outgoing time slot No 31 on outgoing bus No 3.

To do this, a free path through the network has to be found. This implies the search for an internal time slot which is idle on A's incoming side as well as on B's outgoing side of the space matrix. The search is carried out by the central control. When the first vacant time slot, say No 7, is found this number and the required addresses, (2, 31 and 1), are sent to the control memories CM-A, CM-B and CM-C. The addresses are stored in cell No 7 of these memories

A's PCM word is written into cell No 2 of SM-A during incoming time slot No 2. It is stored here until internal time slot No 7 arrives. As incoming time slot numbers probably will not coincide with internal

time slot numbers, this store time can be anything from 0 to 31 time slots. During internal time slot No 7 the address to cell No 2 is delivered from CM-A and the PCM word is read out towards the space matrix. Simultaneously the address to the appropriate cross-point (No 1) is delivered from CM-C and the PCM word is switched towards the required SM-B. Finally, when outgoing time slot No 31 arrives the PCM word is sent towards B.

This sequence, which is repeated once every frame, creates a path from A to B. There is, however, so far no transmission from B to A, see Fig. 2 and 3. To arrange this, two methods can be used. Either the second path is established completely independent of the first one or the two paths are established in coordination. The first method perhaps gives a more flexible system while the second method makes it possible to save hardware because of the symmetric behaviour of the switch. With the second method the path searching for the two paths is carried out in one search, while the first method requires two separate searches.

A special way of controlling the two paths, the go and the return path, is the anti phase method. If a free path is found from A to B during a certain time slot, the return path is guaranteed half a frame later. Applied to our example we obtain the go path during time slot 7 and consequently the return path during time slot (7 + 32/2) = 23. The method is combined with a reduction of control memory. Fig. 7 gives an explanation of the method.

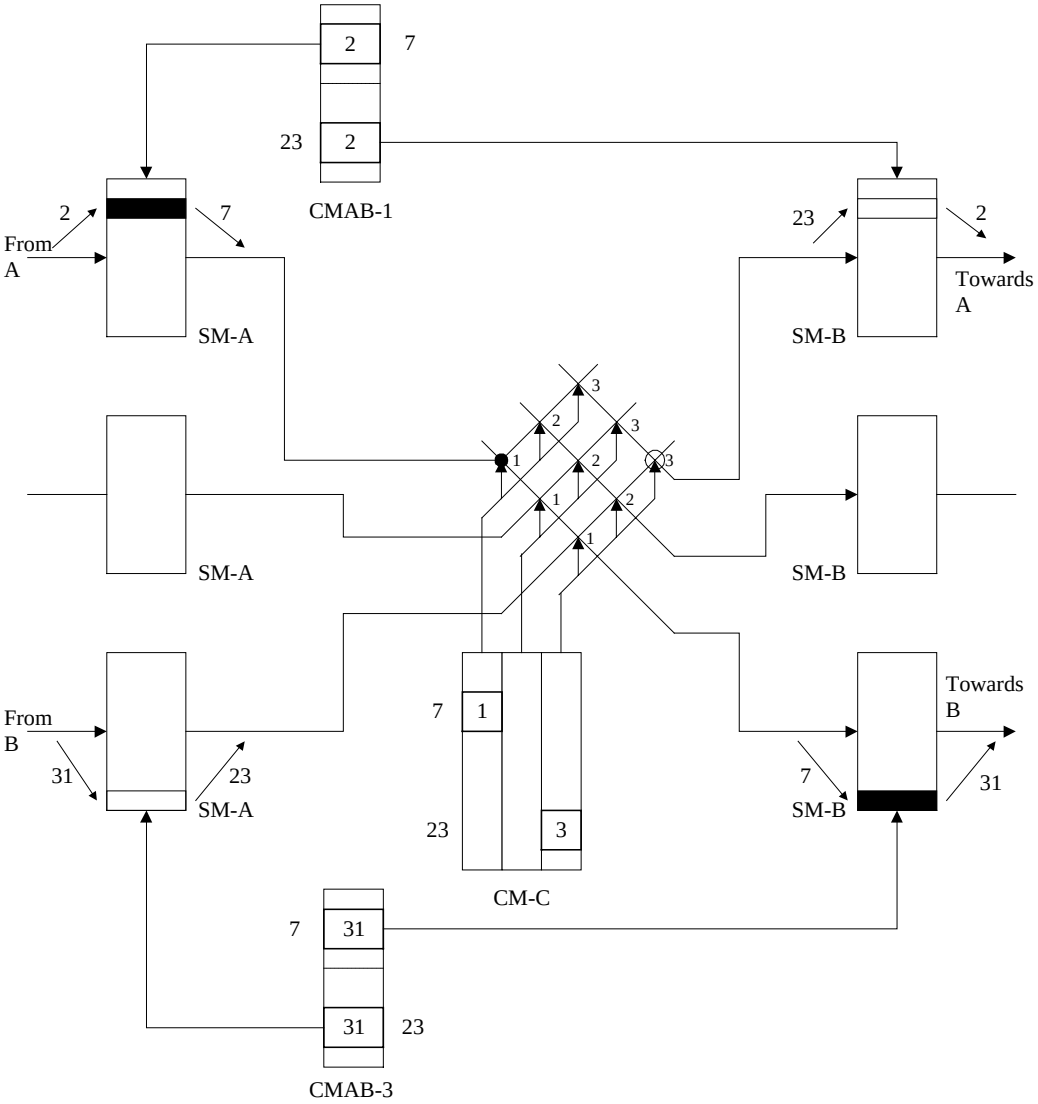
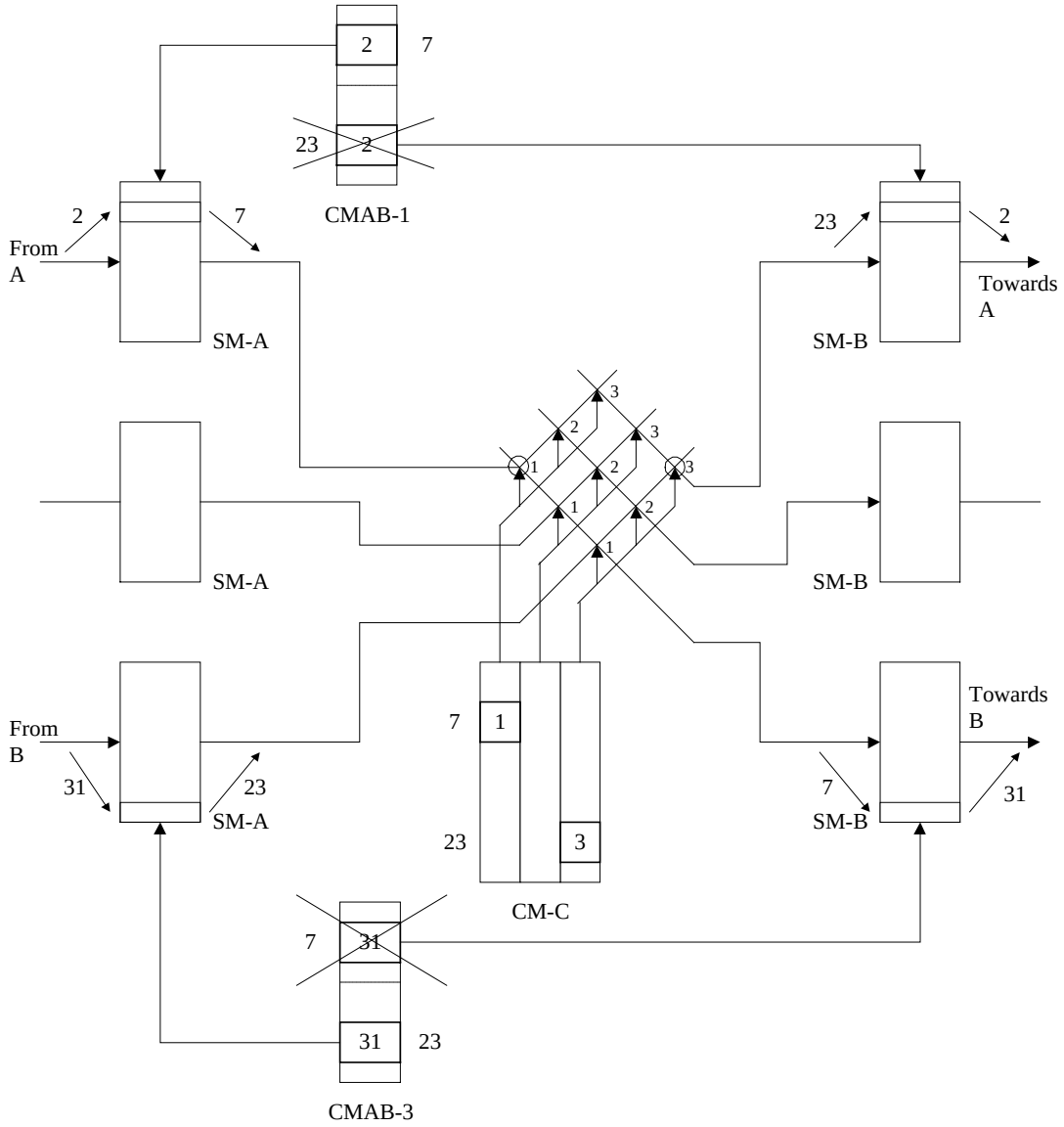


Fig. 7 TST structure with anti-phase method.

In reality the control memory does not have the same information in two separate time slots as in Fig. 7. To save on control memory the anti-phase method takes advantage of the address always being half a frame displaced. See Fig. 8



Direction A → B (during internal TS 7)

CMAB-1	Read from SMA at address given in internal TS 7 (2).
CMAB-3	Write, via space switch, in SMB at address given in internal TS 7 + 16 = 23 (31).

Direction B → A (during internal TS 23)

CMAB-3	Read from SMA at address given in internal TS 23 (31)
CMAB-1	Write, via space switch, in SMB at address given in internal TS 23 +16 = 7 (2)

Fig. 8 TST realisation of anti-phase method.

For disconnection of the call the central control orders the erasing of the appropriate word in the control memories.

The blocking created by the TST network is obviously dependent on whether a pair of vacant time slots can be found for the transmission between the two time switches.

The memory principle (TS)

The basic switch principle is a variant of a TS-structure, here called the memory principle. This name is used, rather than TS, because no space switching in the sense that we have used the phrase above is actually performed. The switch works as shown in Fig. 9.

Assume that the switch consists of 32 incoming/outgoing buses, each containing 32 time slots. The internal bit rate is then chosen in such a way that we get 32 x 32 = 1024 internal time slots. The control memory is chosen to consist of 32 blocks, each containing 32 cells, i.e. a total of 1024 cells. Consequently we have as many internal time slots and control memory cells as there are required connections through the switch.

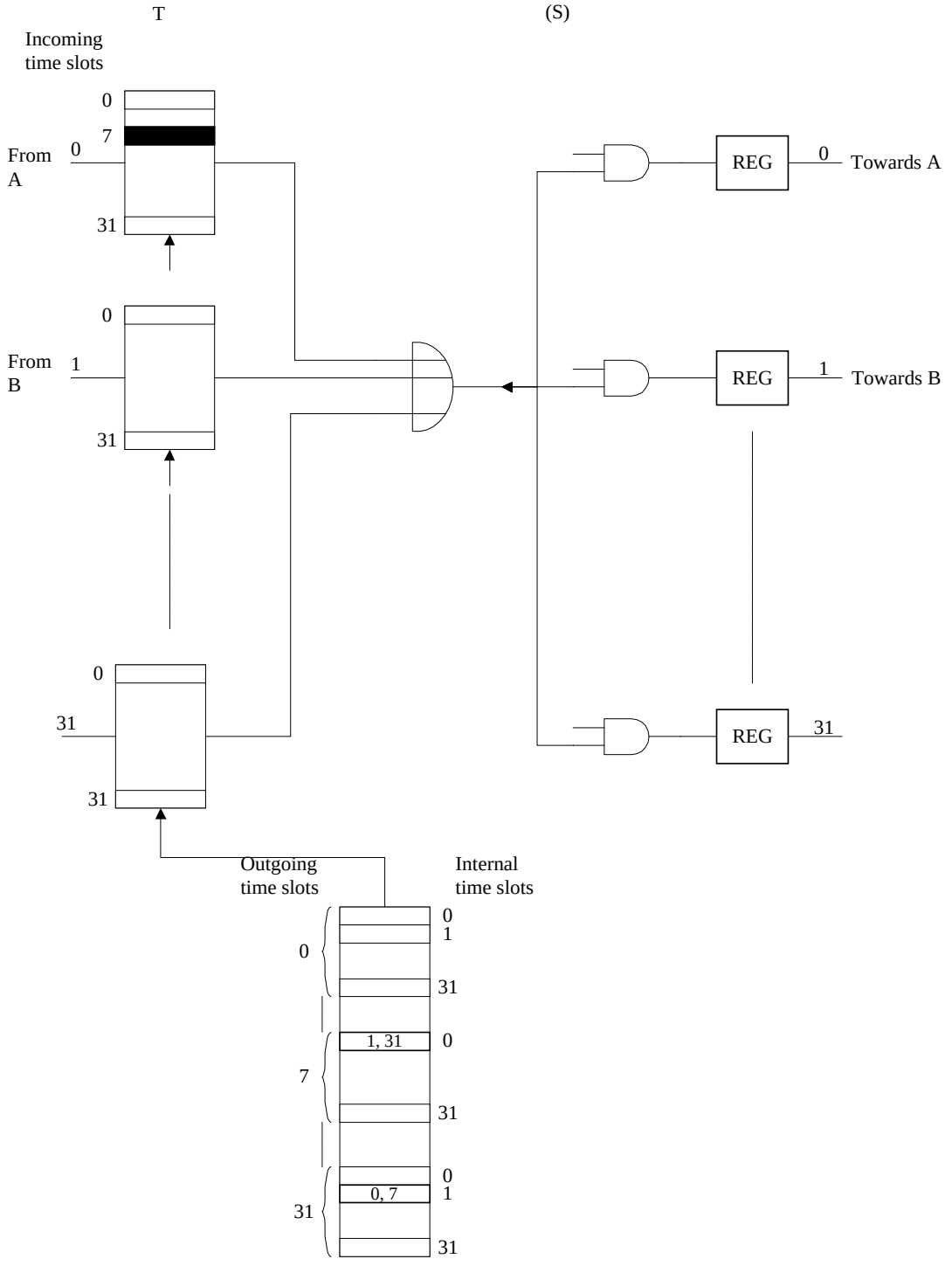


Fig. 9 Digital switching network. Memory (TS) principle.

The functioning of the switch is based on a certain relationship between the cells of the control memory and the outlets. The 32 blocks of cells in the control memory correspond to the 32 outgoing time slots, while the 32 cells per block correspond to the 32 outlets of the switch. The control memory is canned sequentially.

During the first outgoing time slot, No 0, the 32 cells of the first block are scanned in such a way that the PCM word which is going to be switched towards outlet No 0 is connected during internal time slot No 0 controlled by memory cell No 0, the word towards outlet No 1 during internal time slot No 1 being controlled by memory cell No 1 etc. The same procedure is repeated during the second outgoing time slot, only with the difference that the second instead of the first memory block is scanned. This goes on until finally all 32 outgoing (and 1024 internal) time slots have passed and a new sequence begins.

In the figure a connection between an inlet A, assigned incoming time slot No 7, and an outlet B, assigned outgoing time slot No 31, is indicated. A's PCM word is written into cell No 7 of the speech memory during incoming time slot No 7. It is stored here until the internal time slot No 1 of the outgoing time slot No 31 arrives. During this internal time slot the PCM word is passed on to B via an outgoing register, which mainly serves as a re-clocking buffer. The return path, from B to A, is executed during outgoing time slot No 7, internal time slot No 0.

The switch is obviously strictly non-blocking. Given a free outlet, a path through the switch can always be found. It is also found instantaneously because of the fixed relationship that exists between the outlet and the control memory.

There is however, a disadvantage. As we have seen, the internal bit rate is proportional to the capacity of the switch. A large switch implies high internal bit rate, which requires memories with very rapid access times. With present technology this results in a maximum capacity of 1500 - 2000 Erlangs of switched traffic.