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**Amendment 2**  
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SERIES G: TRANSMISSION SYSTEMS AND MEDIA,  
DIGITAL SYSTEMS AND NETWORKS

Digital terminal equipments – General

SERIES Y: GLOBAL INFORMATION  
INFRASTRUCTURE, INTERNET PROTOCOL ASPECTS,  
NEXT-GENERATION NETWORKS, INTERNET OF  
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Internet protocol aspects – Transport

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Interfaces for the optical transport network

**Amendment 2**

Recommendation ITU-T G.709/Y.1331 (2020) –  
Amendment 2

ITU-T G-SERIES RECOMMENDATIONS  
**TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS**

INTERNATIONAL TELEPHONE CONNECTIONS AND CIRCUITS	G.100–G.199
GENERAL CHARACTERISTICS COMMON TO ALL ANALOGUE CARRIER-TRANSMISSION SYSTEMS	G.200–G.299
INDIVIDUAL CHARACTERISTICS OF INTERNATIONAL CARRIER TELEPHONE SYSTEMS ON METALLIC LINES	G.300–G.399
GENERAL CHARACTERISTICS OF INTERNATIONAL CARRIER TELEPHONE SYSTEMS ON RADIO-RELAY OR SATELLITE LINKS AND INTERCONNECTION WITH METALLIC LINES	G.400–G.449
COORDINATION OF RADIOTELEPHONY AND LINE TELEPHONY	G.450–G.499
TRANSMISSION MEDIA AND OPTICAL SYSTEMS CHARACTERISTICS	G.600–G.699
DIGITAL TERMINAL EQUIPMENTS	G.700–G.799
<b>General</b>	<b>G.700–G.709</b>
Coding of voice and audio signals	G.710–G.729
Principal characteristics of primary multiplex equipment	G.730–G.739
Principal characteristics of second order multiplex equipment	G.740–G.749
Principal characteristics of higher order multiplex equipment	G.750–G.759
Principal characteristics of transcoder and digital multiplication equipment	G.760–G.769
Operations, administration and maintenance features of transmission equipment	G.770–G.779
Principal characteristics of multiplexing equipment for the synchronous digital hierarchy	G.780–G.789
Other terminal equipment	G.790–G.799
DIGITAL NETWORKS	G.800–G.899
DIGITAL SECTIONS AND DIGITAL LINE SYSTEM	G.900–G.999
MULTIMEDIA QUALITY OF SERVICE AND PERFORMANCE – GENERIC AND USER-RELATED ASPECTS	G.1000–G.1999
TRANSMISSION MEDIA CHARACTERISTICS	G.6000–G.6999
DATA OVER TRANSPORT – GENERIC ASPECTS	G.7000–G.7999
PACKET OVER TRANSPORT ASPECTS	G.8000–G.8999
ACCESS NETWORKS	G.9000–G.9999

*For further details, please refer to the list of ITU-T Recommendations.*

# **Recommendation ITU-T G.709/Y.1331**

## **Interfaces for the optical transport network**

### **Amendment 2**

#### **Summary**

Recommendation ITU-T G.709/Y.1331 defines the requirements for the optical transport network (OTN) interface signals of the optical transport network, in terms of:

- OTN hierarchy
- functionality of the overhead in support of multi-wavelength optical networks
- frame structures
- bit rates
- formats for mapping client signals.

Edition 6.3 of this Recommendation adds specifications for OTU<sub>k</sub>, k=0, references to specific bit patterns that may appear in Status and Payload Type overhead fields during the presence of the FlexO Squelch text pattern [ITU-T G.709.1], a clarification of the ODU Locked maintenance signal and an enhancement of the introductory text in Annex L.

## History

Edition	Recommendation	Approval	Study Group	Unique ID*
1.0	ITU-T G.709/Y.1331	2001-02-09	15	<a href="http://handle.itu.int/11.1002/1000/5350">11.1002/1000/5350</a>
1.1	ITU-T G.709/Y.1331 (2001) Amd. 1	2001-11-29	15	<a href="http://handle.itu.int/11.1002/1000/5629">11.1002/1000/5629</a>
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2.1	ITU-T G.709/Y.1331 (2003) Amd. 1	2003-12-14	15	<a href="http://handle.itu.int/11.1002/1000/7060">11.1002/1000/7060</a>
2.2	ITU-T G.709/Y.1331 (2003) Cor. 1	2006-12-14	15	<a href="http://handle.itu.int/11.1002/1000/8982">11.1002/1000/8982</a>
2.3	ITU-T G.709/Y.1331 (2003) Amd. 2	2007-11-22	15	<a href="http://handle.itu.int/11.1002/1000/9155">11.1002/1000/9155</a>
2.4	ITU-T G.709/Y.1331 (2003) Cor.2	2009-01-13	15	<a href="http://handle.itu.int/11.1002/1000/9646">11.1002/1000/9646</a>
2.5	ITU-T G.709/Y.1331 (2003) Amd. 3	2009-04-22	15	<a href="http://handle.itu.int/11.1002/1000/9671">11.1002/1000/9671</a>
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3.3	ITU-T G.709/Y.1331 (2009) Amd. 2	2011-04-13	15	<a href="http://handle.itu.int/11.1002/1000/11115">11.1002/1000/11115</a>
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4.5	ITU-T G.709/Y.1331 (2012) Cor. 2	2015-01-13	15	<a href="http://handle.itu.int/11.1002/1000/12365">11.1002/1000/12365</a>
4.6	ITU-T G.709/Y.1331 (2012) Amd. 4	2015-01-13	15	<a href="http://handle.itu.int/11.1002/1000/12364">11.1002/1000/12364</a>
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## Keywords

Client mappings, frame formats, multiplexing, OTN.

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\* To access the Recommendation, type the URL <http://handle.itu.int/> in the address field of your web browser, followed by the Recommendation's unique ID. For example, <http://handle.itu.int/11.1002/1000/11830-en>.

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## Table of Contents

	<b>Page</b>
1	Scope ..... 1
2	References..... 1
3	Definitions ..... 3
3.1	Terms defined elsewhere ..... 3
3.2	Terms defined in this Recommendation ..... 4
4	Abbreviations and acronyms ..... 5
5	Conventions ..... 10
6	Optical transport network interface structure ..... 11
6.1	Basic signal structure..... 11
6.2	Information structure for OTN interfaces..... 14
7	Multiplexing/mapping principles and bit rates ..... 16
7.1	Mapping..... 18
7.2	Wavelength division multiplex..... 19
7.3	Bit rates and capacity..... 19
7.4	ODUk time-division multiplex..... 25
7.5	Interconnection of Ethernet UNI and FlexE Group UNI in two administrative domains in the OTN ..... 35
8	OTN Interfaces ..... 36
8.1	Point-to-point interface, type I ..... 36
8.2	Point-to-point interface, type II ..... 36
8.3	Optical networking interface, type II..... 36
8.4	Optical networking interface, type I..... 37
9	Media Element..... 37
10	OCh and OTSiA ..... 37
10.1	OCh..... 37
10.2	Optical tributary signal assembly (OTSiA)..... 37
11	Optical transport unit (OTU) ..... 37
11.1	OTUk (k=0,1,2,3,4,4-SC) frame structure ..... 38
11.2	Scrambling for OTUk (k=0,1,2,3,4)..... 39
11.3	OTUCn frame structure ..... 39
11.4	OTU25 and OTU50 frame structure..... 40
12	Optical data unit (ODU) ..... 41
12.1	ODU frame structure ..... 41
12.2	ODU bit rates and bit-rate tolerances ..... 41
13	Optical payload unit (OPU) ..... 45
14	Overhead information carried over the OSC and OCC ..... 46
14.1	OSC ..... 46

	<b>Page</b>
14.2	OCC..... 46
15	Overhead description..... 47
15.1	Types of overhead ..... 51
15.2	Trail trace identifier and access point identifier definition ..... 53
15.3	OTS-O description..... 54
15.4	OMS-O description ..... 55
15.5	OCh-O and OTSiG-O description ..... 56
15.6	OTU/ODU frame alignment OH description ..... 57
15.7	OTU OH description ..... 58
15.8	ODU OH description..... 64
15.9	OPU OH description..... 78
16	Maintenance signals..... 81
16.1	OTS maintenance signals ..... 81
16.2	OMS maintenance signals ..... 81
16.3	OCh and OTiSA maintenance signals ..... 81
16.4	OTU maintenance signals..... 82
16.5	ODU maintenance signals ..... 83
16.6	Client maintenance signal..... 85
17	Mapping of client signals ..... 85
17.1	OPU client signal fail (CSF)..... 86
17.2	Mapping of CBR2G5, CBR10G, CBR10G3 and CBR40G signals into OPUk..... 86
17.3	Blank clause..... 90
17.4	Mapping of GFP frames into OPUk (k=0,1,2,3,4,flex)..... 90
17.5	Mapping of test signal into OPU ..... 91
17.6	Mapping of a non-specific client bit stream into OPUk..... 92
17.7	Mapping of other constant bit-rate signals with justification into OPUk..... 93
17.8	Mapping a 1000BASE-X and FC-1200 signal via timing transparent transcoding into OPUk ..... 103
17.9	Mapping a supra-2.488 Gbit/s CBR signal into OPUflex using BMP ..... 105
17.10	Mapping of packet client signals into OPUk..... 108
17.11	Mapping of 64B/66B encoded packet client signals into OPUflex using IMP ..... 109
17.12	Mapping of FlexE aware signals into OPUflex..... 111
17.13	Mapping a 64B/66B PCS coded signal into OPUflex using BMP and 2-bit alignment of 66B code words..... 118
18	Blank clause..... 124
19	Mapping ODUj signals into the ODTU signal and the ODTU into the OPUk tributary slots ..... 124
19.1	OPUk tributary slot definition ..... 124

	<b>Page</b>
19.2	ODTU definition ..... 137
19.3	Multiplexing ODTU signals into the OPUk..... 139
19.4	OPUk multiplex overhead and ODTU justification overhead ..... 149
19.5	Mapping ODUj into ODTUjk ..... 162
19.6	Mapping of ODUj into ODTUk.ts..... 171
20	Mapping ODUk signals into the ODTUCn signal and the ODTUCn into the OPUCn tributary slots ..... 176
20.1	OPUCn tributary slot definition ..... 176
20.2	ODTUCn definition..... 180
20.3	Multiplexing ODTUCn signals into the OPUCn..... 181
20.4	OPUCn multiplex overhead and ODTU justification overhead..... 182
20.5	Mapping ODUk into ODTUCn.ts ..... 186
Annex A	– Forward error correction using 16-byte interleaved RS(255,239) codecs ..... 189
Annex B	– Adapting 64B/66B encoded clients via transcoding into 513B code blocks..... 191
B.1	Transmission order ..... 191
B.2	Client frame recovery ..... 191
B.3	Transcoding from 66B blocks to 513B blocks ..... 192
B.4	Link fault signalling ..... 197
Annex C	– Adaptation of OTU3 and OTU4 over multichannel parallel interfaces ..... 198
Annex D	– Generic mapping procedure principles..... 201
D.1	Basic principle ..... 201
D.2	Applying GMP in OTN ..... 204
D.3	$C_m(t)$ encoding and decoding ..... 208
D.4	$\Sigma C_{nD}(t)$ encoding and decoding..... 214
Annex E	– Adaptation of parallel 64B/66B encoded clients ..... 210
E.1	Introduction ..... 216
E.2	Clients signal format..... 216
E.3	Client frame recovery ..... 216
E.4	Additions to Annex B transcoding for parallel 40GBASE-R clients ..... 219
Annex F	– Improved robustness for mapping of 40GBASE-R into OPU3 using 1027B code blocks ..... 222
F.1	Introduction ..... 222
F.2	513B code block framing and flag bit protection..... 222
F.3	66B block sequence check..... 223
Annex G	– Mapping ODU0 into a low latency OTU0 (OTU0LL) ..... 228
G.1	Introduction ..... 228
G.2	Optical transport unit 0 low latency (OTU0LL)..... 228
Annex H	– OTUCn sub rates (OTUCn-M)..... 231
H.1	Introduction ..... 231



	<b>Page</b>
H.2 OTUCn-M frame format .....	231
Annex I .....	232
Annex J – Recovery of 64B/66B encoded clients from parallel 256B/257B interfaces.....	233
Annex K – Transporting 200GbE and 400GbE am_sf<2:0> information through a single optical link between two Ethernet/OTN transponder entities in the OTN .....	235
K.1 Introduction .....	235
K.2 Client Degrade Indication (CDI) overhead .....	236
Annex L – OTU25u and OTU50u interfaces.....	237
L.1 Introduction .....	237
L.2 Bit rates.....	237
Appendix I – Range of stuff ratios for asynchronous mappings of CBR2G5, CBR10G, and CBR40G clients with $\pm 20$ ppm bit-rate tolerance into OPUk, and for asynchronous multiplexing of ODUj into ODUk ( $k > j$ ).....	241
Appendix II – Examples of functionally standardized OTU frame structures .....	247
Appendix III – Example of ODUk multiplexing .....	250
Appendix IV – Blank appendix .....	252
Appendix V – ODUk multiplex structure identifier (MSI) examples .....	253
Appendix VI – Parallel logic implementation of the CRC-9, CRC-8, CRC-5 and CRC-6.....	256
Appendix VII – OTL4.10 structure.....	259
Appendix VIII – CPRI into ODU mapping .....	260
Appendix IX – Overview of CBR clients into OPU mapping types .....	261
Appendix X – Overview of ODUj into OPUk mapping types .....	263
Appendix XI – Derivation of recommended ODUflex(GFP) bit-rates based on $n \times$ ODUk.ts clock and examples of ODUflex(GFP,n,k) clock generation.....	265
XI.1 Introduction .....	265
XI.2 Tributary slot sizes .....	265
XI.3 Example methods for ODUflex(GFP,n,k) clock generation .....	268
Appendix XII – Terminology changes between ITU-T G.709 Edition 4, Edition 5 and Edition 6 .....	270
Appendix XIII – OTUCn sub rates (OTUCn-M) Applications .....	272
XIII.1 Introduction .....	272
XIII.2 OTUCn-M frame format and rates .....	273
XIII.3 OTUCn-M fault condition.....	273
Appendix XIV – Examples of interconnection of Ethernet UNI and FlexE Group UNI in two administrative domains in the OTN for the case that these UNIs deploy different mapping methods .....	274
Appendix XV – Examples of ODUflex(GFP) and ODUflex(IMP) clock generation methods.....	277
XV.1 Client timing based.....	277

	<b>Page</b>
XV.2 Local clock based .....	277
Appendix XVI –Implications of OTSiG (de)modulator processes and OCh OTSiG overhead trail termination functions being located in adjacent network elements.....	279
XVI.1 Introduction .....	279
XVI.2 Black link deployment without co-location of OTSiG (de)modulator and OTSiG-O_TT/OCh-O_TT function .....	280
XVI.3 Failure correlation for black link deployment without colocation of OTSiG (de)modulator and OTSiG-O_TT/OCh-O_TT function.....	281
Bibliography.....	284

# Recommendation ITU-T G.709/Y.1331

## Interfaces for the optical transport network

### Amendment 2

*Editorial note: This is a complete-text publication. Modifications introduced by this amendment are shown in revision marks relative to Recommendation ITU-T G.709/Y.1331 (2020) plus its Amendment 1 and Corrigendum 1.*

#### 1 Scope

The optical transport network (OTN) supports the operation and management aspects of optical networks of various architectures, e.g., point-to-point, ring and mesh architectures.

This Recommendation defines the interfaces of the OTN to be used within and between subnetworks of the optical network, in terms of:

- OTN hierarchy;
- functionality of the overhead in support of multi-wavelength optical networks;
- frame structures;
- bit rates;
- formats for mapping client signals.

Functions and process flows associated with the defined interfaces are specified in [ITU-T G.798].

The interfaces defined in this Recommendation can be applied at user-to-network interfaces (UNI) and network node interfaces (NNI) of the OTN.

#### 2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

- |                 |  |
|-----------------|--|
| [ITU-T G.652]   | Recommendation ITU-T G.652 (2016), <i>Characteristics of a single-mode optical fibre and cable.</i>  |
| [ITU-T G.693]   | Recommendation ITU-T G.693 (2009), <i>Optical interfaces for intra-office systems.</i>   |
| [ITU-T G.695]   | Recommendation ITU-T G.695 (2018), <i>Optical interfaces for coarse wavelength division multiplexing applications.</i>   |
| [ITU-T G.698.1] | Recommendation ITU-T G.698.1 (2009), <i>Multichannel DWDM applications with single-channel optical interfaces.</i>   |
| [ITU-T G.698.2] | Recommendation ITU-T G.698.2 (2018), <i>Amplified multichannel dense wavelength division multiplexing applications with single channel optical interfaces.</i> |

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[ITU-T G.8260]	Recommendation ITU-T G.8260 (2015 <del>20</del> 20), <i>Definitions and terminology for synchronization in packet networks.</i>
[ITU-T G.8262]	Recommendation ITU-T G.8262/Y.1362 (2018), <i>Timing characteristics of a synchronous equipment slave clock.</i>
[ITU-T G.8264]	Recommendation ITU-T G.8264 (2017), <i>Distribution of timing information through packet networks.</i>
[ITU-T M.1400]	Recommendation ITU-T M.1400 (2001), <i>Designations for interconnections among operators' networks.</i>
[ITU-T M.3100]	Recommendation ITU-T M.3100 (2004), <i>Generic network information model.</i>
[ITU-T O.150]	Recommendation ITU-T O.150 (1996), <i>General requirements for instrumentation for performance measurements on digital transmission equipment.</i>
[ITU-T T.50]	Recommendation ITU-T T.50 (1992), <i>International Reference Alphabet (IRA) (Formerly International Alphabet No. 5 or IA5) – Information technology – 7-bit coded character set for information interchange.</i>
[IEEE 802.3]	IEEE Std. 802.3:2018, <i>Standard for Ethernet.</i>
[IEEE 802.3cd]	IEEE Std 802.3cd-2018, <i>Standard for Ethernet Amendment 3: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation.</i>
[OIF FlexE IA]	OIF, <i>Flex Ethernet 2.0 Implementation Agreement</i> (2018).

### 3 Definitions

#### 3.1 Terms defined elsewhere

This Recommendation uses the following terms defined elsewhere:

##### 3.1.1 Terms defined in [ITU-T G.780]:

- BIP-X
- network node interface

##### 3.1.2 Terms defined in [ITU-T G.805]:

- adapted information (AI)
- characteristic information (CI)
- network
- subnetwork

##### 3.1.4 Terms defined in [ITU-T G.872]:

- optical multiplex section (OMS)
- optical transmission section (OTS)

##### 3.1.5 Terms defined in [ITU-T G.959.1]:

- optical tributary signal (OTSi).

##### 3.1.6 Terms defined in [OIF FlexE IA]:

- FlexE Client

**3.1.7** Terms defined in [ITU-T G.807]:

- optical signal maintenance entity (OSME)

## **3.2 Terms defined in this Recommendation**

This Recommendation defines the following terms:

**3.2.1 ODU<sub>k</sub>.ts:** The ODU<sub>k</sub>.ts is an increment of bandwidth which when multiplied by a number of tributary slots gives the recommended size of an ODUflex(GFP,n,k) optimized to occupy a given number of tributary slots of an OPU<sub>k</sub>.

**3.2.2 OTU0 low latency:** The OTU0 low latency (OTU0LL) is the information structure used for transport of an ODU0 over a multi-vendor optical network interface in one administrative domain at the edge of the optical transport network.

**3.2.3 optical tributary signal assembly (OTSiA):** The OTSiG together with the non-associated overhead (OTSiG-O).

**3.2.4 optical tributary signal group (OTSiG):** The set of OTSi signals that supports an OTU.

**3.2.5 optical tributary signal overhead (OTSiG-O):** The non-associated overhead for an OTSiG.

**3.2.6 connection monitoring end-point (CMEP):** Connection monitoring end-points represent end-points of trails and correspond as such with the trail termination functions. Connection monitoring overhead (CMOH) is inserted and extracted at the CMEPs.

For the ODU and OTU the CMEPs are categorized in three classes:

- OTU section CMEP (OS\_CMEP), which represents the end-points of the OTU<sub>k</sub>/OTUC<sub>n</sub> trail. The SM overhead field contains the related CMOH.
- ODU tandem connection CMEP (TC\_CMEP), which represents the end-points of ODU<sub>k</sub>T/ODUC<sub>n</sub>T trails. The TCM1..6 overhead fields contain the related CMOH.
- ODU path CMEP (P\_CMEP), which represents the end-points of the ODU<sub>k</sub>P/ODUC<sub>n</sub>P trail. The PM overhead field contains the related CMOH.

**3.2.7 non-associated overhead:** Supervisory information transported in an optical supervisory signal, overhead communication channel or other means.

**3.2.8 optical data unit (ODU):** The ODU is an information structure consisting of the information payload (OPU) and ODU related overhead, either as ODU<sub>k</sub> or ODUC<sub>n</sub>.

**3.2.9 optical payload unit (OPU):** The OPU is the information structure used to adapt client information for transport over the OTN, either as an OPU<sub>k</sub> or an OPUC<sub>n</sub>. It comprises client information together with any overhead needed to perform rate adaptation between the client signal rate and the OPU payload rate, and other OPU overheads supporting the client signal transport. The index k or C<sub>n</sub> (see clause 5) is used to identify the approximate bit rate and different versions.

**3.2.10 optical transport unit (OTU):** The OTU is the information structure used for transport of an ODU over an OTSiA or OCh, either as an OTU<sub>k</sub> or an OTUC<sub>n</sub>.

For OCh and OTN point-to-point interface cases, the OTU overhead is used as overhead for the transport over the optical layer, and the OTU must terminate where the OCh and OTN point-to-point interface is terminated. For an OTSiA, the OTU overhead may or may not be terminated where the OTSiA is terminated.

Three versions of the OTU<sub>k</sub> are defined: completely standardized OTU<sub>k</sub> (OTU<sub>k</sub>), functionally standardized OTU<sub>k</sub> (OTU<sub>k</sub>V) and an OTU<sub>k</sub> with completely standardized overhead and functionally standardized FEC (OTU<sub>k</sub>-v). The completely standardized OTU<sub>k</sub> is used on OTN IrDIs and may be used on OTN IaDIs. The other two are used on OTN IaDIs.

**3.2.11 OCh:** The OCh is an information structure consisting of the information payload (OTSiG) with a certain bandwidth and non-associated overhead (OCh-O) for management of the OCh.

**3.2.12 optical transport network:** An optical transport network (OTN) is composed of a set of optical network elements connected by optical fibres, that provide functionality to encapsulate, transport, multiplex, route, manage, supervise and provide survivability of client signals. The information of the client signals is processed in the digital domain and carried across the media, according to the requirements given in [ITU-T G.872].

**3.2.13 optical transport network node interface (ONNI):** The interface at an optical transport network node which is used to interconnect with another optical transport network node.

**3.2.14 ODUflex(GFP):** ODUflex for GFP-F mapped client signals with user configured bit rate.

**3.2.15 ODUflex(GFP,n,k):** ODUflex for GFP-F mapped client signals with user configured bit rate of  $n \times \text{ODUk.ts}$  in which  $n$  = number of 1.25G tributary slots and  $k$  = ODUk.ts representative.

ODUflex(GFP,n,k) is a subset of ODUflex(GFP).

**3.2.16 ODUflex(IMP):** ODUflex for IMP mapped client signals with user configured bit rate.

**3.2.17 ODUflex(IMP,s):** ODUflex for IMP mapped client signals with bit rate of  $s \times 239/238 \times 5\ 156\ 250\ \text{kb/s} \pm 100\ \text{ppm}$  in which  $s = 2, 8, n \times 5$  with  $n \geq 1$ .

ODUflex(IMP,s) is a subset of ODUflex(IMP).

## 4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

16FS	16 columns with Fixed Stuff
3R	Reamplification, Reshaping and Retiming
AI	Adapted Information
AIS	Alarm Indication Signal
AMP	Asynchronous Mapping Procedure
API	Access Point Identifier
APS	Automatic Protection Switching
ASI	Asynchronous Serial Interface for DVB
BDI	Backward Defect Indication
BDI-O	Backward Defect Indication Overhead
BDI-P	Backward Defect Indication Payload
BEI	Backward Error Indication
BI	Backward Indication
BIAE	Backward Incoming Alignment Error
BIP	Bit Interleaved Parity
BMP	Bit-synchronous Mapping Procedure
CAUI	(Chip to) 100 Gb/s Attachment Unit Interface
CB	Control Block
CBR	Constant Bit Rate

CI	Characteristic Information
CM	Connection Monitoring
$C_m$	number of m-bit Client data entities
CMEP	Connection Monitoring End Point
CMGPON_D	Continuous Mode GPON Downstream
CMGPON_U2	Continuous Mode GPON Upstream 2
CMOH	Connection Monitoring Overhead
CMXGPON_D	Continuous Mode XGPON Downstream
CMXGPON_U2	Continuous Mode XGPON Upstream 2
$C_n$	number of n-bit client data entities
$C_{nD}$	difference between $C_n$ and $(m/n \times C_m)$
CPRI	Common Public Radio Interface
CRC	Cyclic Redundancy Check
CS	Client Specific
CSF	Client Signal Fail
CTRL	Control word sent from source to sink
DAPI	Destination Access Point Identifier
DDR	Double Data Rate
DMp	Delay Measurement of ODUk path
DMti	Delay Measurement of TCMi
DNU	Do Not Use
DVB	Digital Video Broadcast
EDC	Error Detection Code
EXC	Electrical cross Connect
EOS	End Of Sequence
ESCON	Enterprise Systems Connection
eSSM	enhanced Synchronization Status Message
EXP	Experimental
ExTI	Expected Trace Identifier
FA	Frame Alignment
FAS	Frame Alignment Signal
FC	Fibre Channel
FC	Flag Continuation
FDI	Forward Defect Indication
FDI-O	Forward Defect Indication Overhead
FDI-P	Forward Defect Indication Payload
FEC	Forward Error Correction



FlexO	Flexible <del>Optical Transport Network</del> information structure
FlexO-x	FlexO interface information structure of order x
FlexO-x-<fec>	FlexO interface signal of order x with a FEC
FlexO-x-<fec>-m	Group of $m \times$ FlexO-x-<fec> interfaces
GCC	General Communication Channel
GID	Group Identification
GMP	Generic Mapping Procedure
GPON	Gigabit-capable Passive Optical Networks
IAE	Incoming Alignment Error
IB	InfiniBand
IMP	Idle Mapping Procedure
IP	Internet Protocol
JC	Justification Control
JOH	Justification Overhead
LF	Local Fault
LLM	Logical Lane Marker
LSB	Least Significant Bit
MFAS	MultiFrame Alignment Signal
MFI	Multiframe Indicator
MPLS	Multi Protocol Label Switching
MPLS-TP	Multi Protocol Label Switching – Transport Profile
MS	Maintenance Signal
MSB	Most Significant Bit
MSI	Multiplex Structure Identifier
NJO	Negative Justification Opportunity
NNI	Network Node Interface
NOS	Not_Operational Sequence
OADM	Optical Add/Drop Multiplexer
OCC	Overhead Communication Channel
OCI	Open Connection Indication
OCN	Overhead Communication Network
ODTUG	Optical Data Tributary Unit Group
ODTUGk/Cn	Optical Data Tributary Unit Group-k/Cn
ODTUjk	Optical Data Tributary Unit j into k
ODTuk/Cn.ts	Optical Data Tributary Unit k/Cn with ts tributary slots
ODU	Optical Data Unit
ODUk/Cn	Optical Data Unit-k/Cn

ODUk/Cn.ts	Optical Data Unit k/Cn fitting in ts tributary slots
ODUk/CnP	Optical Data Unit-k/Cn Path monitoring level
ODUk/CnT	Optical Data Unit-k/Cn Tandem connection monitoring level
OH	Overhead
OMFI	OPU Multi-Frame Identifier
OMS	Optical Multiplex Section
OMS-O	Optical Multiplex Section Overhead
OMS-P	Optical Multiplex Section Payload
ONNI	Optical Network Node Interface
OPS	Optical Physical Section
OPSM	Optical Physical Section Multilane
OPU	Optical Payload Unit
OPUk/Cn	Optical Payload Unit-k/Cn
OSC	Optical Supervisory Channel
OSMC	OTN synchronization messaging channel
OSME	Optical Signal Maintenance Entity
OTL	Optical Transport Lane
OTLk.n	group of n Optical Transport Lanes that carry one OTUk
OTLC.n	group of n Optical Transport Lanes that carry one OTUC of an OTUCn
OTN	Optical Transport Network
OTS	Optical Transmission Section
OTS-O	Optical Transmission Section Overhead
OTS-P	Optical Transmission Section Payload
OTSi	Optical Tributary Signal
OTSiA	Optical Tributary Signal Assembly
OTSiG	Optical Tributary Signal Group
OTSiG-O	Optical Tributary Signal Group – Overhead
OTU	Optical Transport Unit
OTU0LL	Completely standardized Optical Transport Unit-0 Low Latency
OTU4-SC	Optical Transport Unit 4 with Stair Case FEC
OTUCn-M	Optical Transport Unit-Cn with n OxUC overhead instances and M 5G tributary slots
OTUk/Cn/25/50	completely standardized Optical Transport Unit-k/Cn/25/50
OTUkV	functionally standardized Optical Transport Unit-k
OTUk-v	Optical Transport Unit-k with vendor specific OTU FEC
OXC	Optical cross Connect
PCC	Protection Communication Channel

P-CMEP	Path-Connection Monitoring End Point
PCS	Physical Coding Sublayer
PJO	Positive Justification Opportunity
PKT	Packet
PLD	Payload
PM	Path Monitoring
PMA	Physical Medium Attachment sublayer
PMI	Payload Missing Indication
PMOH	Path Monitoring Overhead
PN	Pseudo-random Number
POS	Position field
ppm	parts per million
PRBS	Pseudo Random Binary Sequence
PSI	Payload Structure Identifier
PT	Payload Type
QDR	Quad Data Rate
RES	Reserved for future international standardization
RF	Remote Fault
RS	Reed-Solomon
RS-Ack	Re-sequence Acknowledge
SAPI	Source Access Point Identifier
SBCON	Single-Byte command code sets Connection
SDI	Serial Digital Interface
SDR	Single Data Rate
Sk	Sink
SM	Section Monitoring
SMOH	Section Monitoring Overhead
SNC	Subnetwork Connection
SNC/I	Subnetwork Connection protection with Inherent monitoring
SNC/N	Subnetwork Connection protection with Non-intrusive monitoring
SNC/S	Subnetwork Connection protection with Sublayer monitoring
So	Source
SSM	Synchronization Status Message
TC	Tandem Connection
TC-CMEP	Tandem Connection-Connection Monitoring End Point
TCM	Tandem Connection Monitoring
TCMOH	Tandem Connection Monitoring Overhead

TS	Tributary Slot
TSI	Transmitter Structure Identifier
TSOH	Tributary Slot Overhead
TTI	Trail Trace Identifier
TTT	Timing Transparent Transcoding
TxTI	Transmitted Trace Identifier
UNI	User-to-Network Interface
XC	Cross Connect
XGPON	10 Gigabit-capable Passive Optical Networks

## 5 Conventions

This Recommendation uses the following conventions:

- **k or Cn**: The index "k" is used to represent a supported bit rate and the different versions of OPUk, OPUCn, ODUk, ODUCn, OTUk and OTUCn. Examples for k are "0" for an approximate bit rate of 1.25 Gbit/s, "1" for an approximate bit rate of 2.5 Gbit/s, "2" for an approximate bit rate of 10 Gbit/s, "3" for an approximate bit rate of 40 Gbit/s, and "4" for an approximate bit rate of 100 Gbit/s. When the "Cn" index is used the approximate bit rate is n×100 Gbit/s. For example for Cn = C4 the approximate bit rate is 400 Gbit/s.
- **x**: The index **x** gives the approximate bit rate for a CBR signal. It is used in the form "unit value, unit, [fractional unit value]". The currently defined unit value is "G" for Gbit/s. Examples for x are "40G" for 40 Gbit/s and "2G5" for 2.5 Gbit/s.
- **-P**: The suffix -P is used to identify the payload element of the signal.
- **-O**: The suffix -O is used to identify the non-associated overhead element of the signal.
- **ODUj**: When two different ODUk information structures are involved, ODUj is used to denote the lower rate ODUk information structure (e.g., for ODUk multiplexing).

The functional architecture of the optical transport network as specified in [ITU-T G.872] is used to derive the ONNI. The ONNI is specified in terms of the adapted and characteristic information present in each layer as described in [ITU-T G.805].

**Transmission order**: The order of transmission of information in all the diagrams in this Recommendation is first from left to right and then from top to bottom. Within each byte the most significant bit is transmitted first. The most significant bit (bit 1) is illustrated at the left in all the diagrams.

**Mapping order**: The serial bit stream of a constant bit rate signal is inserted into the OPU payload so that the bits will be transmitted on the OPU/ODU in the same order that they were received at the input of the AMP, BMP or GMP mapper function. If m bits  $b_a, b_b, b_c$  up to  $b_m$  are client signal bits of which  $b_a$  is the bit that is received first and  $b_m$  is the bit that is received last, then  $b_a$  will be mapped into bit 1 of a first OPU byte and  $b_m$  will be mapped into bit 8 of an  $n^{\text{th}}$  OPU byte (with  $n = m/8$ ).

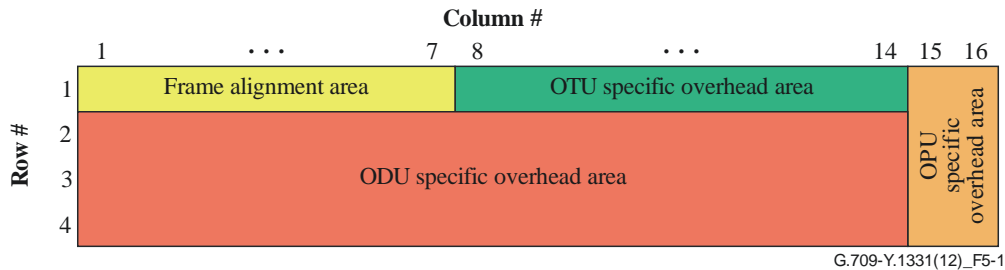
**Value of reserved bit(s)**: The value of an overhead bit, which is reserved or reserved for future international standardization shall be set to "0".

**Value of non-sourced bit(s)**: Unless stated otherwise, any non-sourced bits shall be set to "0".

**OTUk (k=0,1,2,3,4), OTUCn, OTU25, OTU50, ODUk (k=0,1,2,2e,3,4,flex,25,50), ODUCn, OPUk (k=0,1,2,2e,3,4,flex,25,50) and OPUCn overhead assignment**: The assignment of an overhead in the optical transport/data/payload unit signal to each part is defined in Figure 5-1. OTUk,

OTU25, OTU50, ODU<sub>k</sub>, OPU<sub>k</sub> contain one instance of OTU, ODU, OPU overhead. OTUC<sub>n</sub>, ODUC<sub>n</sub> and OPUC<sub>n</sub> contain n instances of OTU, ODU, OPU overhead, numbered 1 to n.

Interleaved versions of the OTU, ODU and OPU overhead may be present on OTUC<sub>n</sub> interfaces. This interleaving is interface specific and specified for OTN interfaces with standardized application codes in the interface specific Recommendations (ITU-T G.709.x series). Within the other clauses of this Recommendation an OTUC<sub>n</sub>, ODUC<sub>n</sub> and OPUC<sub>n</sub> are presented in an interface independent manner, by means of n OTUC, ODUC and OPUC instances that are marked #1 to #n.



**Figure 5-1 – OTU, ODU and OPU overhead**

## 6 Optical transport network interface structure

The optical transport network as specified in [ITU-T G.872] provides for two OTN interface types: point-to-point interfaces and optical networking interfaces. Both OTN interface types consist of one or more optical tributary signals.

The OTN point-to-point interfaces are defined with 3R processing at each end of the interface (terminating the optical tributary signals) and do not provide for optical layer overhead.

The OTN optical networking interfaces are defined with optical layer overhead and may not provide for 3R processing at each end of the interface, which allow optical tributary signals to be forwarded beyond the interface.

These two types of OTN interfaces consist of digital and management information defined in this Recommendation as carried by a physical interface, the specifications of which are outside the scope of this Recommendation.

Each OTN interface may be associated with one or more application identifiers. Each application identifier represents either a standardized application code or a vendor specific identifier. An interface with one or more application codes may be used to interconnect (OTN) equipment from different vendors. An interface with one or more vendor specific identifiers is to be used to interconnect (OTN) equipment from the same vendor. When considering interconnection over an interface between user and provider administrations or provider to provider administrations, 3R termination shall be used on either side of the interface, unless mutually agreed otherwise.

### 6.1 Basic signal structure

The basic structure is shown in Figures 6-1 and 6-2 and consists of a digital and an optical structure.

#### 6.1.1 OTN digital structure

The OTN digital structure (see Figure 6-1) is based on three classes of optical transport units (OTU); the OTU<sub>k</sub>, OTU25 and OTU50 and OTUC<sub>n</sub>.

- The OTU<sub>k</sub> signal consists of a 4080 column by 4 row frame, which includes 256 columns allocated to contain a forward error correction code (FEC) and is operated at various bit rates that are represented by the value of k.

- The OTU25 and OTU50 signals consist of a 3824 column by 4 row frame, which do not include a FEC area and are operated at 25 Gbit/s and 50 Gbit/s bit rates that are represented by the values 25 and 50. FEC for the OTU25 and OTU50 signals are interface specific and not included in the OTU25 and OTU50 definition.
- The OTUCn signal consists of n interleaved 3824 columns by 4 row frames, which do not include a FEC area and is operated at n times a basic rate that is represented by OTUC. FEC for the OTUCn signal is interface specific and not included in the OTUCn definition.

The OTUCn signal may be carried via a FlexO-x-<fec>-m interface group with  $m = \lceil n/x \rceil$  FlexO-x-<fec> interfaces; refer to [ITU-T G.709.1] and [ITU-T G.709.3].

The OTU25 and OTU50 signals are carried via OTU25-RS and OTU50-RS interfaces; refer to [ITU-T G.709.4].

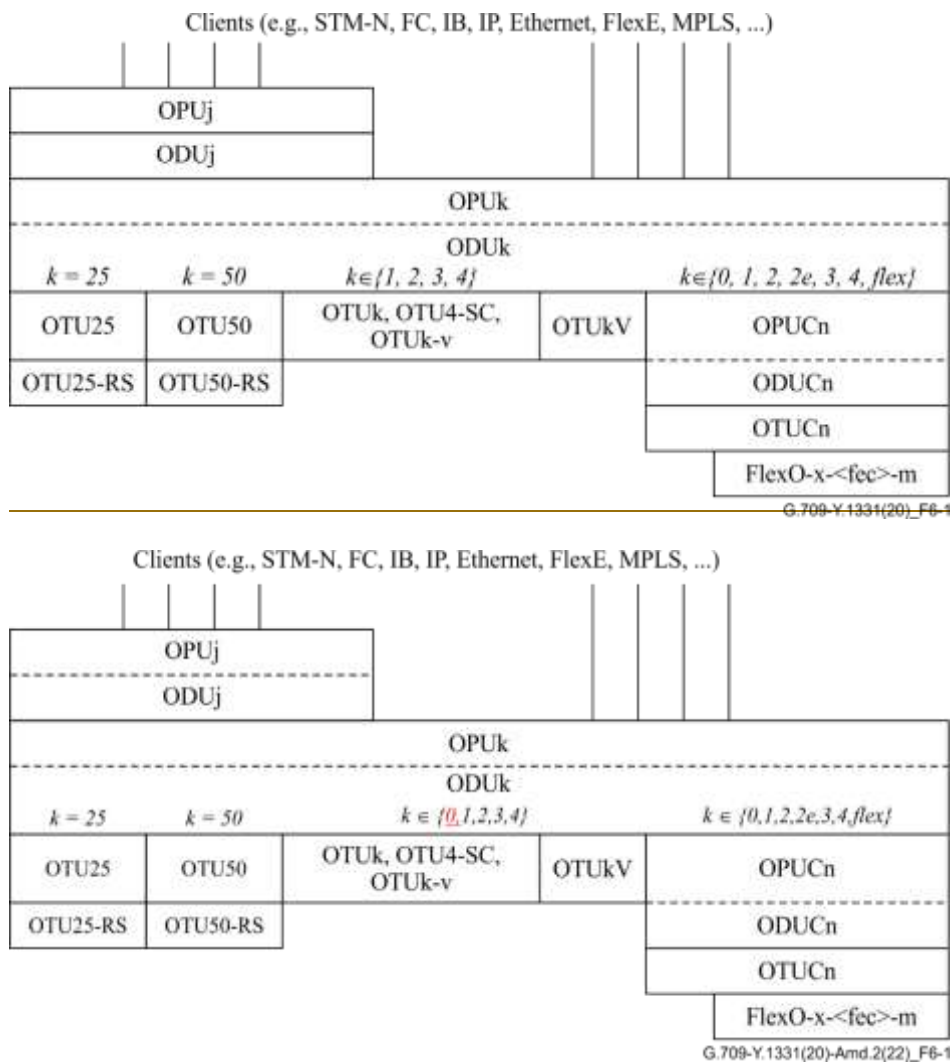
The OTU contains an optical data unit (ODU), which contains an optical payload unit (OPU). The OTUk, OTU25, OTU50, OTUCn and ODUCn are digital section layers. The ODUk (and ODUj) is a path layer.

The OTUk ( $k \in \{0, 1, 2, 3, 4, 4\text{-SC}\}$ ) is fully standardized. There are two functionally standardized alternatives: OTUk-v and OTUkV. In all cases, these provide supervision and condition the signal for transport between 3R regeneration points in the OTN.

The OTUCn, OTU25 and OTU50 provide supervision for transport between 3R regeneration points in the OTN. Note that the OTUCn, OTU25 and OTU50 do not condition the signal for transport between 3R regeneration points because encapsulation and forward error correction are not included in the OTUCn, OTU25 and OTU50 definition.

The ODU provides:

- Tandem connection monitoring (ODUjT, ODUkT, ODUCnT);
- end-to-end section supervision (ODUjP, ODUkP, ODUCnP);
- adaptation of client signals via the OPUk and OPUj ( $j \in \{0, 1, 2, 2e, 3, 4, \text{flex}\}$ ,  $k \in \{0, 1, 2, 2e, 3, 4, \text{flex}\}$ );
- adaptation of client ODUj signals via the OPUk ( $j \in \{0, 1, 2, 2e, 3, 4, \text{flex}\}$ ,  $k \in \{1, 2, 3, 4, 25, 50\}$ , the bit rate of the ODUj is less than the OPUk payload bit rate);
- adaptation of client ODUk signals via the OPUCn ( $k \in \{0, 1, 2, 2e, 3, 4, \text{flex}\}$ ).



**Figure 6-1 – Digital structure of the OTN interfaces**

### 6.1.2 OTN optical structure

The OTN optical structure (see Figure 6-2) is based on the presence of one or more optical tributary signals combined with three classes of optical overhead deployment:

- Absence of optical overhead in the case of OTN point-to-point interfaces.
- Optical overhead carried in the same fibre as the one or more optical tributary signals in the case of OTN optical networking interfaces, type I.
- Optical overhead carried via the overhead communication network (OCN) outside the fibre with one or more optical tributary signals in the case of OTN optical networking interfaces, type II.

The optical overhead is divided into three digital layers that coincide with the maintenance entities defined in [ITU-T G.872], as shown in Figure 6-2:

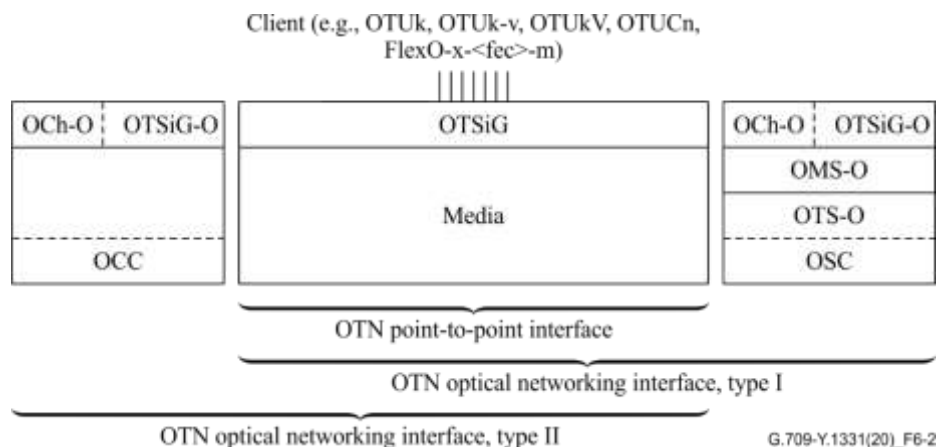
- Overhead to monitor the optical path maintenance entity (OCh-O and OTSiG-O), which extends between two OTSiG modulators and demodulators.
- Overhead to monitor the optical multiplex section maintenance entity, which extends between two points of optical multiplexing (OMS-O).
- Overhead to monitor the optical transmission section maintenance entity, which extends between two optical amplifiers, or between an optical multiplexer (without an amplifier) and the next optical amplifier (OTS-O).

The OTN optical networking interfaces may support optical layer overhead (represented by the entities described above). Such overhead may be transported within the optical supervisory channel (OSC), the overhead communication channel (OCC) that is provided by the overhead communication network (OCN) (refer to [ITU-T G.7712]) or an alternative communication channel. Interfaces that support OCh-O and/or OTSiG-O support switching in the optical layer of the OCh and/or OTSiA signals which carry one optical transport unit or FlexO-x-<fec>-m group signal between 3R regeneration points. Interfaces that support OTS-O and OMS-O also support deployment of in-line optical amplifiers between optical layer switching points.

The OTN point-to-point interfaces do not support optical layer overhead and are designed to transport the optical transport unit or FlexO-x-<fec>-m group signals over a single optical span with 3R regeneration points at each end. For such cases there is no optical path layer present in the interface stack.

OTN point-to-point interfaces carry one or more OTUk or OTUCn or FlexO-x-<fec> of an OTUCn/FlexO-x-<fec>-m group, which are monitored by means of OTUk or OTUCn or FlexO-x-<fec>-m group overhead.

OTN optical networking interfaces carry one or more optical tributary signals, each transporting an OTUk or an OTUCn or one FlexO-x-<fec> out of an OTUCn/FlexO-x-<fec>-m group or a non-OTN client signal.



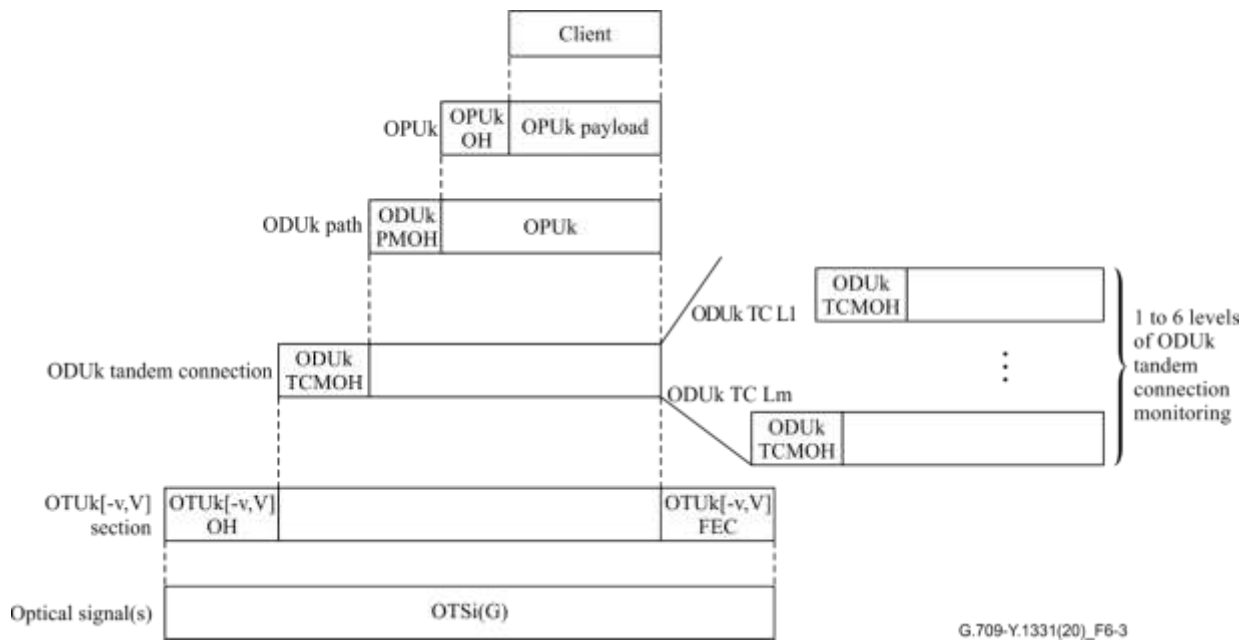
**Figure 6-2 – Optical structure of the OTN interfaces**

## 6.2 Information structure for OTN interfaces

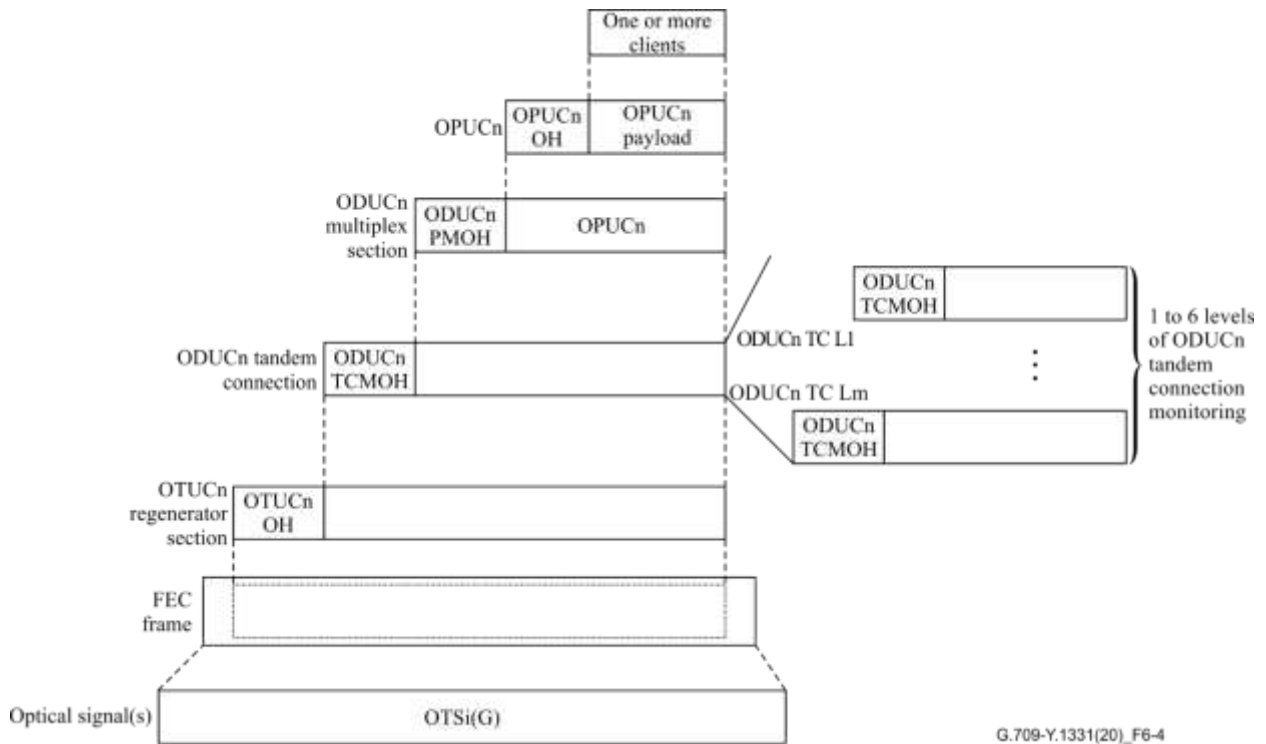
The information structure for OTN interfaces is represented by information containment relationships and flows. The principal information containment relationships of the digital structure of the OTUk and OTUCn are described in Figures 6-3 and 6-4.

For supervision purposes in OTN optical networking interfaces, the OTU signal is terminated whenever the OCh signal is terminated and the OTU signal may be terminated when the OTSiA signal is terminated. For supervision purposes in OTN point-to-point interfaces, the OTU signals are terminated whenever the interface signal is terminated.





**Figure 6-3 – Principal information containment relationship of digital structure of OTUk**



**Figure 6-4 – Principal information containment relationship of digital structure of OTUCn**

## 7 Multiplexing/mapping principles and bit rates

Figures 7-1A and 7-1B show the relationship between various information structure elements and illustrates the multiplexing structure and mappings for the OTU. In the multi-domain OTN any combination of the ODU multiplexing layers may be present at a given OTN NNI. The interconnection of and visibility of ODU multiplexing layers within an equipment or domain is outside the scope of this Recommendation. Figures 7-1A and 7-1B show that a (non-OTN) client signal is mapped into an OPU. This OPU signal is mapped into the associated ODU. This ODU signal is either mapped into the associated OTU[V] signal, or into an ODTU. This ODTU signal is multiplexed into an ODTU Group (ODTUG). The ODTUG signal is mapped into an OPU. This OPU signal is mapped into the associated ODU, etc.

The OPU<sub>k</sub> (k=0,1,2,2e,3,4,flex,25,50) are the same information structures, but with different client signals. The OPU<sub>Cn</sub> has a different information structure than the OPU<sub>k</sub>; the OPU<sub>Cn</sub> information structure consists of n times the information structure of the OPU while the OPU<sub>k</sub> contain a single instance of the OPU information structure.

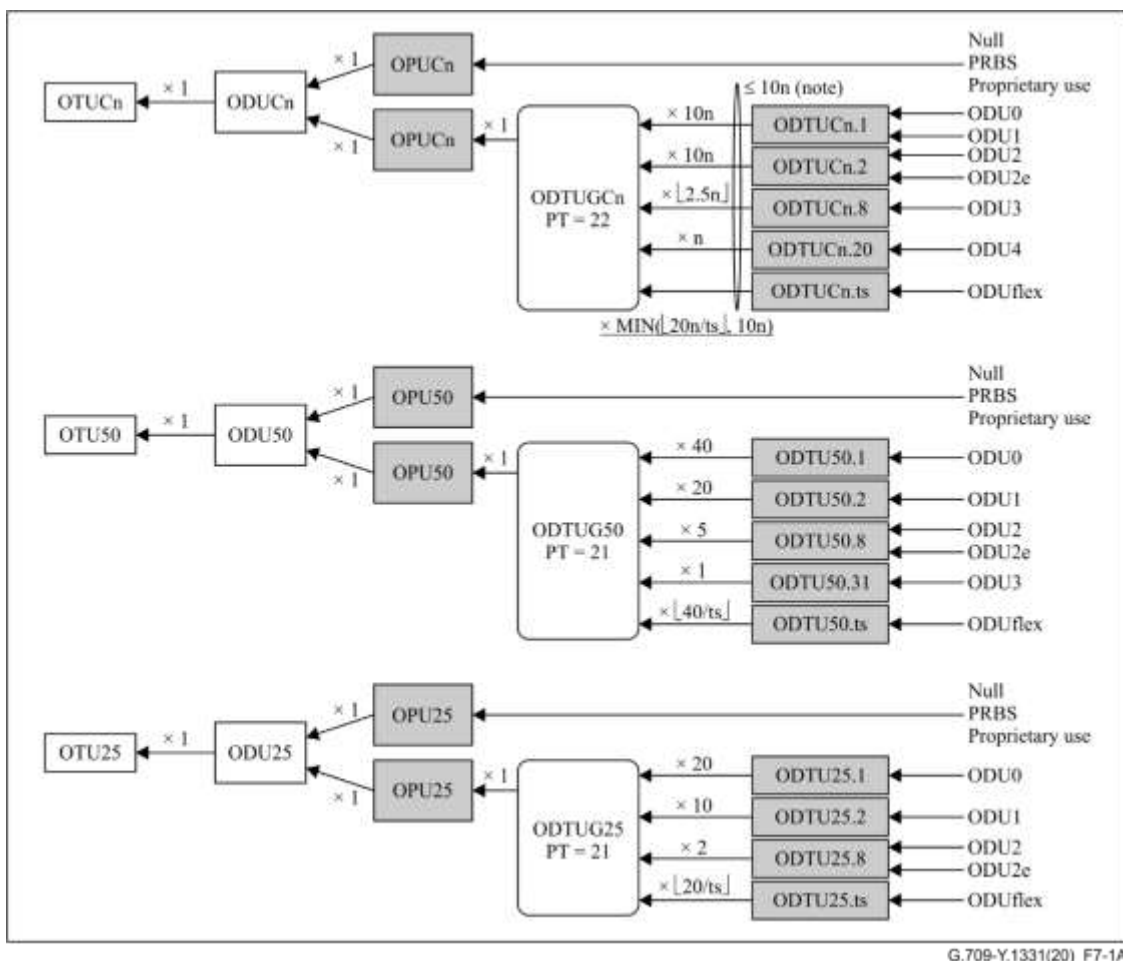
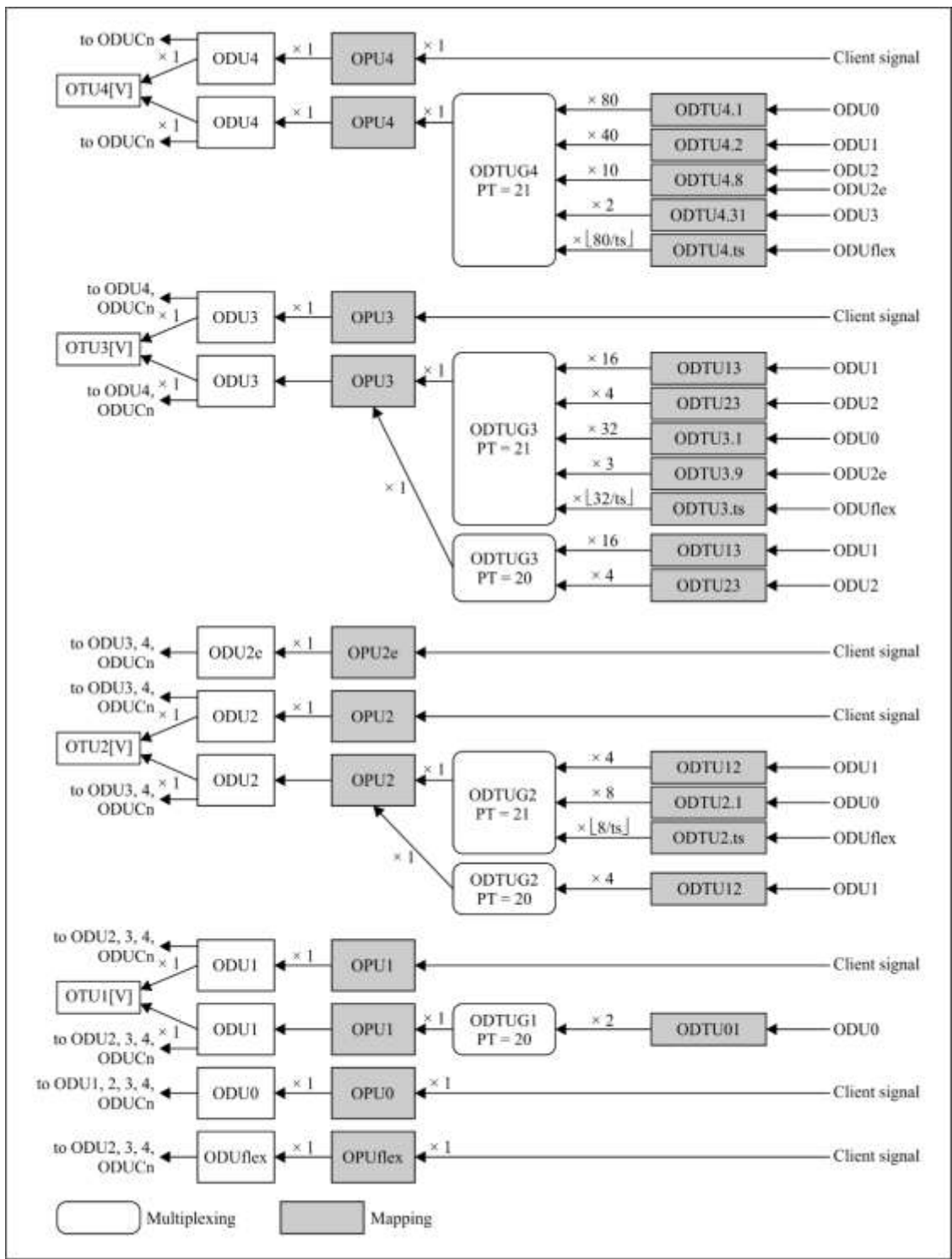
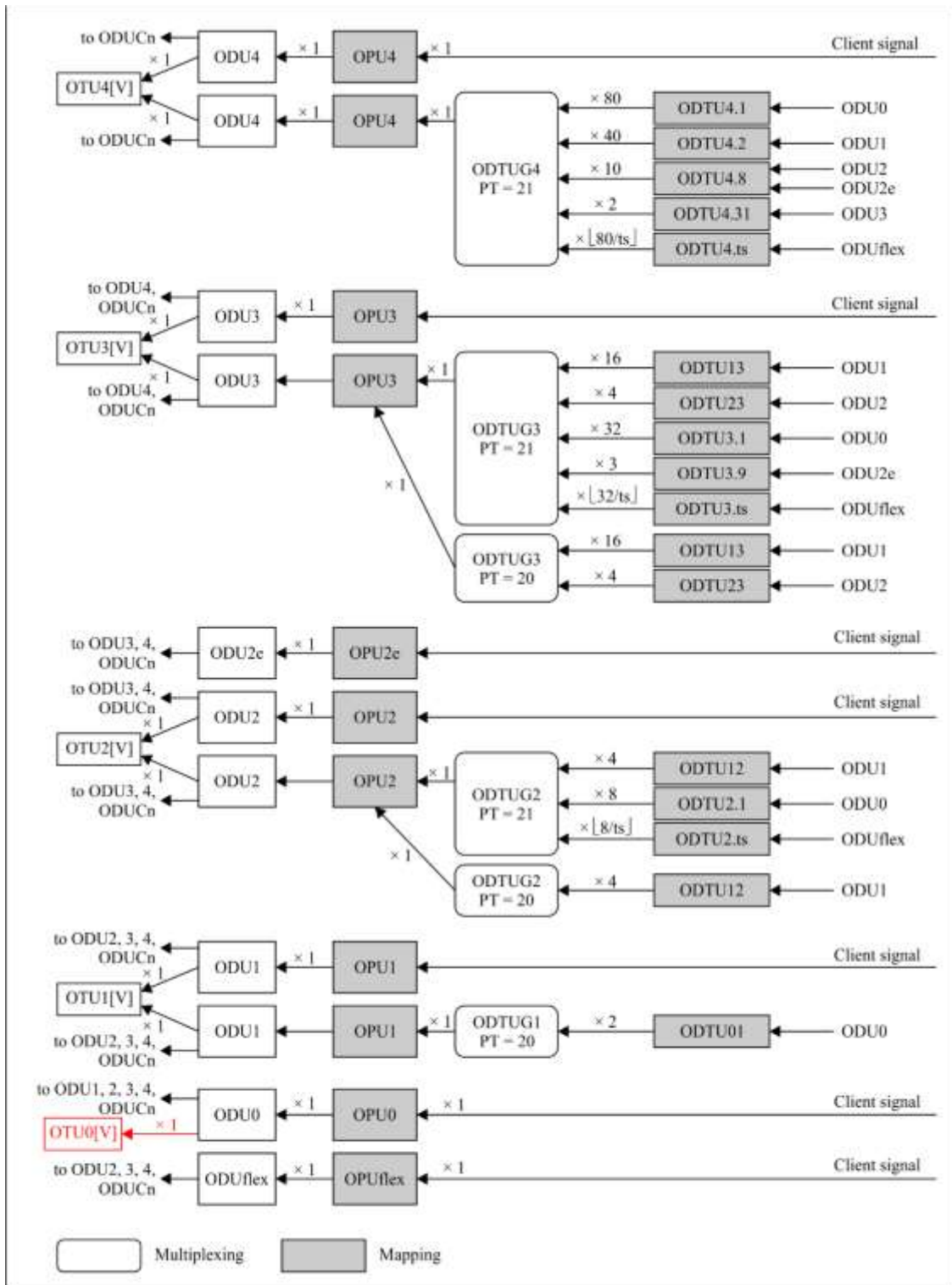


Figure 7-1A – OTN multiplexing and mapping structures



G.709 Y.1331(20)\_F7-18



G.709-Y.1331(20)-Amd.2(22)\_F7-1B

NOTE – Implementations should support the multiplexing of up to 10n ODU<sub>k</sub> (k=0,1,2,2e,3,4,flex) signals into an OPUC<sub>n</sub>.

**Figure 7-1B – OTN multiplexing and mapping structures**

## 7.1 Mapping

The client signal or an optical data tributary unit group (ODTUG) is mapped into the OPU. The OPU is mapped into an ODU and the ODU is mapped into an OTU. The OTU is mapped into an OTSiG. The OTU<sub>k</sub> may also be mapped into an OTL<sub>k.n</sub> and an OTL<sub>k.n</sub> is then mapped into an OTSiG.

## 7.2 Wavelength division multiplex

Wavelength division multiplexing is used to multiplex the OTSi of one or more OTSiG for transport over an OTN interface.

For the case of the OTN optical networking interfaces, type I, the OTSi of the OSC is multiplexed for transport over the interface using wavelength division multiplexing.

## 7.3 Bit rates and capacity

The bit rates and tolerance of the OTU signals are defined in Table 7-1.

The bit rates and tolerance of the ODU signals are defined in clause 12.2 and Table 7-2.

The bit rates and tolerance of the OPU payload are defined in Table 7-3.

The OTU, ODU and OPU frame periods are defined in Table 7-4.

The types and bit rates of the OTL signals are defined in Table 7-5.

The 2.5G and 1.25G tributary slot related OPUk multiframe periods and 5G tributary slot OPUCn multiframe periods are defined in Table 7-6.

The ODTU payload area bandwidths are defined in Table 7-7. The bandwidth depends on the OPU type and the mapping procedure (AMP or GMP). The AMP bandwidths include the bandwidth provided by the NJO overhead byte. GMP is defined without such NJO bytes.

The bit rates and tolerance of the ODUflex(GFP,n,k) are defined in Table 7-8.

The number of OPU tributary slots required by a client ODU are summarized in Table 7-9 and specified in clauses 19.6 and 20.5.

The bit rates and tolerance of the GCC signals are defined in Table 7-10.

**Table 7-1 – OTU types and bit rates**

OTU type	OTU nominal bit rate	OTU bit-rate tolerance
<u>OTU0</u>	<u><math>255/239 \times 1\,244\,160</math> kbit/s</u>	±20 ppm (Note 5)
OTU1	$255/238 \times 2\,488\,320$ kbit/s	
OTU2	$255/237 \times 9\,953\,280$ kbit/s	
OTU3	$255/236 \times 39\,813\,120$ kbit/s	
OTU4	$255/227 \times 99\,532\,800$ kbit/s	
OTUCn	$n \times 239/226 \times 99\,532\,800$ kbit/s	
OTU25	$61677/58112 \times 24\,883\,200$ kbit/s	
OTU50	$61677/58112 \times 49\,766\,400$ kbit/s	
<p>NOTE 1 – The nominal OTU rates are approximately: <u><math>1\,327\,451.046</math> kbit/s (OTU0)</u>, 2 666 057.143 kbit/s (OTU1), 10 709 225.316 kbit/s (OTU2), 43 018 413.559 kbit/s (OTU3), 111 809 973.568 kbit/s (OTU4), 26 409 711.013 kbit/s (OTU25), 52 819 422.026 kbit/s (OTU50) and <math>n \times 105\,258\,138.053</math> kbit/s (OTUCn).</p> <p>NOTE 2 – <del>OTU0, OTU2e and OTUflex are not specified in this Recommendation. ODU0 signals are to be transported over ODU1, ODU2, ODU3, ODU4, ODU25, ODU50 or ODUCn signals, ODU2e signals are to be transported over ODU3, ODU4, ODU25, ODU50 and ODUCn signals and ODUflex signals are transported over ODU2, ODU3, ODU4, ODU25, ODU50 and ODUCn signals.</del></p> <p>NOTE 3 – The OTUk (k=0,1,2,3,4) signal bit rates include the FEC overhead area. The OTUCn signal bit rates do not include a FEC overhead area.</p> <p>NOTE 4 – The OTU25 [OTU50] bit rate can be based on the OTU25-RS [OTU50-RS] bit rate as follows:  <math>514/544 \times 41118/41120 \times \text{OTU25-RS [OTU50-RS] bit rate} = 514/544 \times 41118/41120 \times 255/227 \times 24\,883\,200 [49\,766\,400]</math> kbit/s.</p> <p>NOTE 5 – Refer to clause 12.2.1.1 for the bit rate tolerance of synchronous OTUk (k=0,1,2,3,4), OTU25/50 and OTUCn.</p>		

**Table 7-2 – ODU types and bit rates**

ODU type	ODU nominal bit rate	ODU bit-rate tolerance
ODU0	1 244 160 kbit/s	±20 ppm (Note 4)
ODU1	$239/238 \times 2\,488\,320$ kbit/s	
ODU2	$239/237 \times 9\,953\,280$ kbit/s	
ODU3	$239/236 \times 39\,813\,120$ kbit/s	
ODU4	$239/227 \times 99\,532\,800$ kbit/s	
ODU25	$61677/58112 \times 24\,883\,200$ kbit/s	
ODU50	$61677/58112 \times 49\,766\,400$ kbit/s	
ODUCn	$n \times 239/226 \times 99\,532\,800$ kbit/s	
ODU2e	$239/237 \times 10\,312\,500$ kbit/s	±100 ppm
ODUflex for CBR client signals	$239/238 \times$ client signal bit rate	±100 ppm (Notes 2, 3)
ODUflex for GFP-F mapped client signals (ODUflex(GFP))	$239/238 \times$ OPUflex(GFP) payload signal rate	±100 ppm
ODUflex for GFP-F mapped client signals based on ODUk.ts and n 1.25G tributary slots (ODUflex(GFP,n,k))	Configured bit rate (see Table 7-8)	
ODUflex for IMP mapped client signals (ODUflex(IMP))	$239/238 \times$ OPUflex(IMP) payload signal rate	
ODUflex for IMP mapped FlexE Client signals (ODUflex(IMP,s))	$s \times 239/238 \times 5\,156\,250$ kbit/s $s = 2, 8, n \times 5$ with $n \geq 1$ (refer to clause 12.2.6)	
ODUflex for FlexE-aware client signals	$103\,125\,000 \times 240/238 \times n/20$ kbit/s ( $n = n_1 + n_2 + \dots + n_p$ )	
<p>NOTE 1 – The nominal ODU rates are approximately: 2 498 775.126 kbit/s (ODU1), 10 037 273.924 kbit/s (ODU2), 40 319 218.983 kbit/s (ODU3), 104 794 445.815 kbit/s (ODU4), 26 409 711.013 kbit/s (ODU25), 52 819 422.026 kbit/s (ODU50), 10 399 525.316 kbit/s (ODU2e), <math>n \times 105\,258\,138.053</math> kbit/s (ODUCn).</p> <p>NOTE 2 – The bit-rate tolerance for ODUflex(CBR) signals is specified as ±100 ppm. This value may be larger than the tolerance for the client signal itself (e.g., ±20 ppm). For such case, the tolerance is determined by the ODUflex(CBR) maintenance signals, which have a tolerance of ±100 ppm.</p> <p>NOTE 3 – For ODUflex(CBR) signals with nominal bit rates close to the maximum ODTUk.ts payload bit rate and client rate tolerances less than ±100 ppm (e.g., ±10 ppm), the ODUflex(CBR) maintenance signal bit rates may exceed the ODTUk.ts payload bit rate. For such cases either an additional tributary slot may be used (i.e., ODTUk.(ts+1)), or the nominal bit rate of the ODUflex(CBR) signal may be artificially reduced to a value of 100 ppm below the maximum ODUflex(CBR) signal bit rate.</p> <p>NOTE 4 – Refer to clause 12.2.1.1 for the bit rate tolerance of synchronous ODUk (k=1,2,3,4), ODU25/50 and ODUCn.</p>		

**Table 7-3 – OPU types and bit rates**

<b>OPU type</b>	<b>OPU payload nominal bit rate</b>	<b>OPU payload bit-rate tolerance</b>
OPU0	$238/239 \times 1\,244\,160$ kbit/s	±20 ppm (Note 2)
OPU1	2 488 320 kbit/s	
OPU2	$238/237 \times 9\,953\,280$ kbit/s	
OPU3	$238/236 \times 39\,813\,120$ kbit/s	
OPU4	$238/227 \times 99\,532\,800$ kbit/s	
OPU25	$7339563/6944384 \times 24\,883\,200$ kbit/s	
OPU50	$7339563/6944384 \times 49\,766\,400$ kbit/s	
OPUCn	$n \times 238/226 \times 99\,532\,800$ kbit/s	
OPU2e	$238/237 \times 10\,312\,500$ kbit/s	±100 ppm
OPUflex for CBR client signals	client signal bit rate	client signal bit-rate tolerance, with a maximum of ±100 ppm
OPUflex for GFP-F mapped client signals (OPUflex(GFP))	Configured bit rate (refer to clause 12.2.5)	±100 ppm
OPUflex for GFP-F mapped client signals based on ODUk.ts and n 1.25G tributary slots (ODUflex(GFP,n,k))	$238/239 \times \text{ODUflex(GFP,n,k)}$ signal rate	
OPUflex for IMP mapped client signals (OPUflex(IMP))	Configured bit rate (refer to clause 12.2.6)	
OPUflex for IMP mapped FlexE Client signals OPUflex(IMP,s)	$s \times 5\,156\,250$ kbit/s $s = 2, 8, n \times 5$ with $n \geq 1$ (refer to clause 12.2.6)	
OPUflex for FlexE-aware client signals	$103\,125\,000 \times 240/239 \times n/20$ kbit/s ( $n = n_1 + n_2 + .. + n_p$ )	
<p>NOTE 1 – The nominal OPU payload rates are approximately: 1 238 954.310 kbit/s (OPU0 Payload), 2 488 320.000 kbit/s (OPU1 Payload), 9 995 276.962 kbit/s (OPU2 Payload), 40 150 519.322 kbit/s (OPU3 Payload), 104 355 975.330 (OPU4 Payload), 26 299 210.130 kbit/s (OPU25 Payload), 52 598 420.261 kbit/s (OPU50 Payload), 10 356 012.658 kbit/s (OPU2e Payload), <math>n \times 104\,817\,727.434</math> kbit/s (OPUCn Payload).</p> <p>NOTE 2 – Refer to clause 12.2.1.1 for the bit rate tolerance of synchronous O<sub>x</sub>U<sub>k</sub> (k=1,2,3,4), O<sub>x</sub>U<sub>25/50</sub> and O<sub>x</sub>U<sub>Cn</sub>.</p>		

**Table 7-4 – OTU/ODU/OPU frame periods**

OTU/ODU/OPU type	Period (Note)
OTU0/ODU0/OPU0	98.354 μs
OTU1/ODU1/OPU1	48.971 μs
OTU2/ODU2/OPU2	12.191 μs
OTU3/ODU3/OPU3	3.035 μs
OTU4/ODU4/OPU4	1.168 μs
OTU25/ODU25/OPU25	4.633 μs
OTU50/ODU50/OPU50	2.317 μs
ODU2e/OPU2e	11.767 μs
OTUCn/ODUCn/OPUCn	1.163 μs
ODUflex/OPUflex	CBR client signals: 121856/client_signal_bit_rate
	GFP-F mapped client signals: 122368/ODUflex_bit_rate
	IMP mapped client signals: 122368/ODUflex_bit_rate
	FlexE-aware client signals: 122368/ODUflex_bit_rate
NOTE – The period is an approximated value, rounded to 3 decimal places.	

**Table 7-5 – OTL types and bit rates**

OTL type	OTL nominal bit rate	OTL bit-rate tolerance
OTL3.4	4 lanes of 255/236 × 9 953 280 kbit/s	±20 ppm
OTL4.4	4 lanes of 255/227 × 24 883 200 kbit/s	
NOTE – The nominal OTL rates are approximately: 10 754 603.390 kbit/s (OTL3.4) and 27 952 493.392 kbit/s (OTL4.4).		

**Table 7-6 – OPUk multiframe periods for 2.5G and 1.25G tributary slots and ODUCn multiframe periods for 5G tributary slots**

OPU type	1.25G tributary slot multiframe period (Note)	2.5G tributary slot multiframe period (Note)	5G tributary slot multiframe period (Note)
OPU1	97.942 μs	–	–
OPU2	97.531 μs	48.765 μs	–
OPU3	97.119 μs	48.560 μs	–
OPU4	93.416 μs	–	–
OPU25	92.669 μs	–	–
OPU50	92.669 μs	–	–
OPUCn	–	–	23.251 μs
NOTE – The period is an approximated value, rounded to 3 decimal places.			



**Table 7-7 – ODTU payload bandwidth (kbit/s)**

ODTU type	ODTU payload nominal bandwidth		ODTU payload bit-rate tolerance
<b>ODTU01</b>	(1904 + 1/8)/3824 × ODU1 bit rate		±20 ppm
<b>ODTU12</b>	(952 + 1/16)/3824 × ODU2 bit rate		
<b>ODTU13</b>	(238 + 1/64)/3824 × ODU3 bit rate		
<b>ODTU23</b>	(952 + 4/64)/3824 × ODU3 bit rate		
<b>ODTU2.ts</b>	ts × 476/3824 × ODU2 bit rate		
<b>ODTU3.ts</b>	ts × 119/3824 × ODU3 bit rate		
<b>ODTU4.ts</b>	ts × 47.5/3824 × ODU4 bit rate		
<b>ODTU25.ts</b>	ts × 190.4/3824 × ODU25 bit rate		
<b>ODTU50.ts</b>	ts × 95.2/3824 × ODU50 bit rate		
<b>ODTUCn.ts</b>	ts × 190.4/3824 × ODU <sub>Cn</sub> bit rate/n		
	<b>Minimum</b>	<b>Nominal</b>	
<b>ODTU01</b>	1 244 216.796	1 244 241.681	1 244 266.566
<b>ODTU12</b>	2 498 933.311	2 498 983.291	2 499 033.271
<b>ODTU13</b>	2 509 522.012	2 509 572.203	2 509 622.395
<b>ODTU23</b>	10 038 088.048	10 038 288.814	10 038 489.579
<b>ODTU2.ts</b>	ts × 1 249 384.632	ts × 1 249 409.620	ts × 1 249 434.608
<b>ODTU3.ts</b>	ts × 1 254 678.635	ts × 1 254 703.729	ts × 1 254 728.823
<b>ODTU4.ts</b>	ts × 1 301 683.217	ts × 1 301 709.251	ts × 1 301 735.285
<b>ODTU25.ts, ODTU50.ts</b>	ts × 1 314 934.207	ts × 1 314 960.507	ts × 1 314 986.806
<b>ODTUCn.ts</b>	ts × 5 240 781.554	ts × 5 240 886.372	ts × 5 240 991.189

NOTE – The bandwidth is an approximated value, rounded to 3 decimal places.

**Table 7-8 – Recommended ODUflex (GFP,n,k) bit rates and tolerance**

ODU type	Nominal bit-rate	Tolerance
ODU2.ts (Note 1)	1 249 177.230 kbit/s	
ODU3.ts (Note 1)	1 254 470.354 kbit/s	
ODU4.ts (Note 1)	1 301 467.133 kbit/s	
ODUflex(GFP,n,2) of n 1.25G tributary slots, 1 ≤ n ≤ 8	n × ODU2.ts	±100 ppm
ODUflex(GFP,n,3) of n 1.25G tributary slots, 9 ≤ n ≤ 32 (Note 3)	n × ODU3.ts	±100 ppm
ODUflex(GFP,n,4) of n 1.25G tributary slots, 33 ≤ n ≤ 80 (Note 2)	n × ODU4.ts	±100 ppm

NOTE 1 – The values of ODU<sub>k</sub>.ts are chosen to permit a variety of methods to be used to generate an ODUflex(GFP) clock. See Appendix XI for the derivation of these values and example ODUflex(GFP) clock generation methods.

NOTE 2 – Transport of packet clients via an ODUflex(GFP) is specified up to 100 Gbit/s.

NOTE 3 – The value of n may be larger than 8 for the case where an ODU25u or ODU50u is used as server. Refer to Annex L.

**Table 7-9 – Number of tributary slots required for ODUj into OPUCk  
and for ODUk into OPUCn**

	# 5G TS	# 2.5G tributary slots		# 1.25G tributary slots					
	OPUCn	OPU2	OPU3	OPU1	OPU2	OPU3	OPU4	OPU25	OPU50
ODU0	1	–	–	1	1	1	1	1	1
ODU1	1	1	1	–	2	2	2	2	2
ODU2	2	–	4	–	–	8	8	8	8
ODU2e	2	–	–	–	–	9	8	8	8
ODU3	8	–	–	–	–	–	31	–	31
ODU4	20	–	–	–	–	–	–	–	–
ODUflex(CBR)									
– ODUflex(IB SDR)	1	–	–	–	3	3	2	2	2
– ODUflex(IB DDR)	1	–	–	–	5	5	4	4	4
– ODUflex(IB QDR)	2	–	–	–	–	9	8	8	8
– ODUflex(FC-400)	1	–	–	–	4	4	4	4	4
– ODUflex(FC-800)	2	–	–	–	7	7	7	7	7
– ODUflex(FC-1600)	3	–	–	–	–	12	11	11	11
– ODUflex(FC-3200)	6	–	–	–	–	23	22	–	22
– ODUflex(3G SDI) (2 970 000)	1	–	–	–	3	3	3	3	3
– ODUflex(3G SDI) (2 970 000/1.001)	1	–	–	–	3	3	3	3	3
– ODUflex(25GBase-R)	5	–	–	–	–	21	20	20	20
– ODUflex(50GBase-R)	10	–	–	–	–	–	40	–	40
– ODUflex(200GBase-R)	40	–	–	–	–	–	–	–	–
– ODUflex(400GBase-R)	80	–	–	–	–	–	–	–	–
ODUflex(GFP)	Note	–	–	–	Note	Note	Note	Note	Note
– ODUflex(GFP,n,k)	Note	–	–	–	n	n	n	n	n
ODUflex(IMP)	Note	–	–	–	Note	Note	Note	Note	Note
– ODUflex(IMP,s)	Note	–	–	–	–	Note	Note	Note	Note
ODUflex(FlexE)	Note	–	–	–	–	Note	Note	Note	Note

NOTE – Refer to equations 19-1a, 19-1b, 20-1a and 20-1b in clauses 19.6 and 20.5.

**Table 7-10 – GCC types and bit rates (kbit/s)**

OTU/ODU type	Nominal bit rate GCC0	Nominal bit rate GCC <sub>i</sub> (i = 1,2)	Nominal bit rate GCC1+GCC2	Bit-rate tolerance
OTU0/ODU0	N/A/162.687	162.687	325.356	±20 ppm
OTU1/ODU1	326.723	326.723	653.445	
OTU2/ODU2	1 312.405	1 312.405	2 624.810	
OTU3/ODU3	5 271.864	5 271.864	10 543.729	
OTU4/ODU4	13 702.203	13 702.203	27 404.405	
OTUC <sub>n</sub> /ODUC <sub>n</sub>	n × 13 762.832	n × 13 762.832	n × 27 525.664	
OTU25/ODU25	3 453.153	3 453.153	6 906.305	
OTU50/ODU50	6 906.305	6 906.305	13 812.610	
ODU2 <sub>e</sub>	N/A	1 359.771	2 719.541	±100 ppm
ODUflex for CBR client signals	N/A	ODUflex(CBR) / 7648	ODUflex(CBR) / 3824	
ODUflex(GFP)	N/A	ODUflex(GFP) / 7648	ODUflex(GFP) / 3824	
ODUflex(GFP,n,k)	N/A	ODUflex(GFP,n,k) / 7648	ODUflex(GFP,n,k) / 3824	
ODUflex(IMP)	N/A	ODUflex(IMP) / 7648	ODUflex(IMP) / 3824	
ODUflex(IMP,s)	N/A	ODUflex(IMP,s) / 7648	ODUflex(IMP,s) / 3824	
ODUflex for FlexE-aware client signals	N/A	ODUflex(FlexE) / 7648	ODUflex(FlexE) / 3824	
NOTE – The bandwidth is an approximated value, rounded to 3 decimal places.				

#### 7.4 ODU<sub>k</sub> time-division multiplex

Figure 7-1 shows the relationship between various time-division multiplexing elements that are defined below and illustrates possible multiplexing structures. Table 7-11 provides an overview of valid tributary slot types and mapping procedure configuration options.

Up to 2 ODU0 signals are multiplexed into an ODTUG1 (PT=20) using time-division multiplexing. The ODTUG1 (PT=20) is mapped into the OPU1.

Up to 4 ODU1 signals are multiplexed into an ODTUG2 (PT=20) using time-division multiplexing. The ODTUG2 (PT=20) is mapped into the OPU2.

A mixture of p (p ≤ 4) ODU2 and q (q ≤ 16) ODU1 signals can be multiplexed into an ODTUG3 (PT=20) using time-division multiplexing. The ODTUG3 (PT=20) is mapped into the OPU3.

A mixture of p (p ≤ 8) ODU0, q (q ≤ 4) ODU1, r (r ≤ 8) ODUflex signals can be multiplexed into an ODTUG2 (PT=21) using time-division multiplexing. The ODTUG2 (PT=21) is mapped into the OPU2.

A mixture of p (p ≤ 32) ODU0, q (q ≤ 16) ODU1, r (r ≤ 4) ODU2, s (s ≤ 3) ODU2<sub>e</sub> and t (t ≤ 32) ODUflex signals can be multiplexed into an ODTUG3 (PT=21) using time-division multiplexing. The ODTUG3 (PT=21) is mapped into the OPU3.

A mixture of p (p ≤ 80) ODU0, q (q ≤ 40) ODU1, r (r ≤ 10) ODU2, s (s ≤ 10) ODU2<sub>e</sub>, t (t ≤ 2) ODU3 and u (u ≤ 80) ODUflex signals can be multiplexed into an ODTUG4 (PT=21) using time-division multiplexing. The ODTUG4 (PT=21) is mapped into the OPU4.

NOTE 1 – The ODTUG<sub>k</sub> is a logical construct and is not defined further. ODTU<sub>jk</sub> and ODTU<sub>k</sub>.ts signals are directly time-division multiplexed into the tributary slots of an OPU<sub>k</sub>.

A mixture of  $p$  ( $p \leq 20$ ) ODU0,  $q$  ( $q \leq 10$ ) ODU1,  $r$  ( $r \leq 2$ ) ODU2,  $s$  ( $s \leq 2$ ) ODU2e and  $u$  ( $u \leq 20$ ) ODUflex signals can be multiplexed into an ODTUG25 (PT=21) using time-division multiplexing. The ODTUG25 (PT=21) is mapped into the OPU25.

A mixture of  $p$  ( $p \leq 40$ ) ODU0,  $q$  ( $q \leq 20$ ) ODU1,  $r$  ( $r \leq 5$ ) ODU2,  $s$  ( $s \leq 5$ ) ODU2e,  $t$  ( $t \leq 1$ ) ODU3 and  $u$  ( $u \leq 40$ ) ODUflex signals can be multiplexed into an ODTUG50 (PT=21) using time-division multiplexing. The ODTUG50 (PT=21) is mapped into the OPU50.

A mixture of  $p$  ( $p \leq 10n$ ) ODU0,  $q$  ( $q \leq 10n$ ) ODU1,  $r$  ( $r \leq 10n$ ) ODU2,  $s$  ( $s \leq 10n$ ) ODU2e,  $t$  ( $t \leq \text{int}(10n/4)$ ) ODU3,  $u$  ( $u \leq n$ ) ODU4 and  $v$  ( $v \leq 10n$ ) ODUflex signals can be multiplexed into an ODTUGC $n$  (PT=22) using time-division multiplexing. The ODTUGC $n$  (PT=22) is mapped into the OPUC $n$ .

NOTE 2 – The ODTUG $k$  and ODTUGC $n$  are logical constructs and are not defined further. ODTU $jk$  and ODTU $k.ts$  signals are directly time-division multiplexed into the tributary slots of an OPU $k$ . ODTUC $n.ts$  signals are directly time-division multiplexed into the tributary slots of an OPUC $n$ .

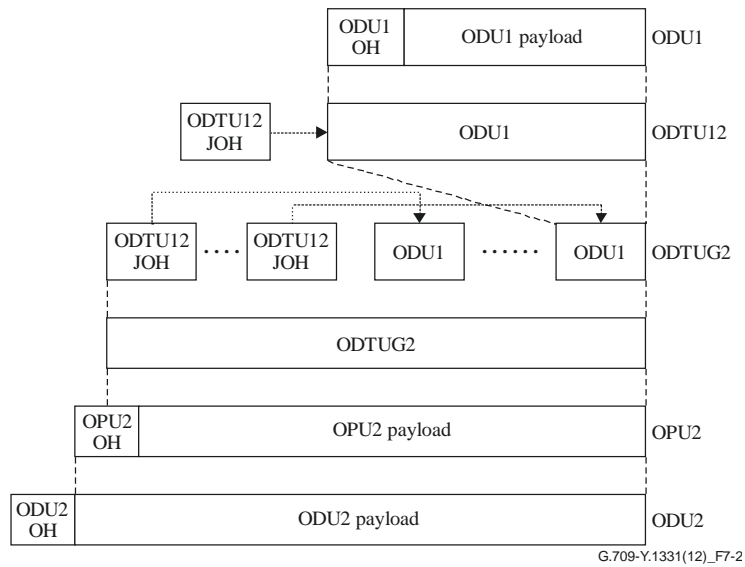
NOTE 3 – Implementations should support the multiplexing of up to  $10n$  ODU $k$  ( $k=0,1,2,2e,3,4,\text{flex}$ ) signals into an OPUC $n$ . Support for the multiplexing of up to  $20n$  ODU $k$  ( $k=0,1,\text{flex}$ ) signals into the OPUC $n$  is not required.

**Table 7-11 – Overview of ODU $j$  into OPU $k$  and ODU $k$  into OPUC $n$  mapping types**

	5G tributary slots	2.5G tributary slots		1.25G tributary slots					
	OPUC $n$ (PT=22)	OPU2 (PT=20)	OPU3 (PT=20)	OPU1 (PT=20)	OPU2 (PT=21)	OPU3 (PT=21)	OPU4 (PT=21)	OPU25 (PT=21)	OPU50 (PT=21)
ODU0	GMP – Note	–	–	AMP	GMP	GMP	GMP	GMP	GMP
ODU1	GMP – Note	AMP	AMP	–	AMP	AMP	GMP	GMP	GMP
ODU2	GMP	–	AMP	–	–	AMP	GMP	GMP	GMP
ODU2e	GMP	–	–	–	–	GMP	GMP	GMP	GMP
ODU3	GMP	–	–	–	–	–	GMP	–	GMP
ODU4	GMP	–	–	–	–	–	–	–	–
ODUflex	GMP	–	–	–	GMP	GMP	GMP	GMP	GMP

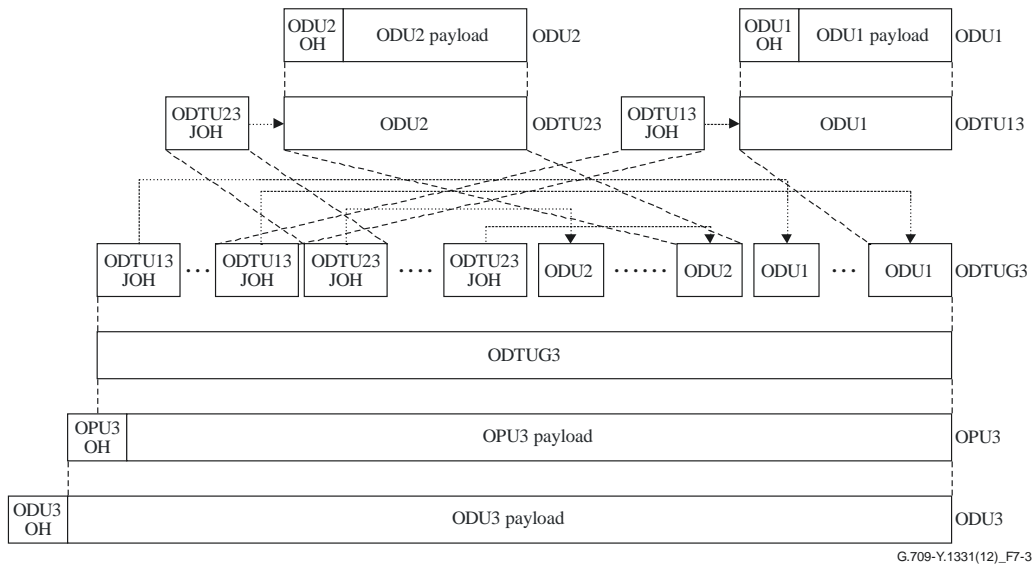
NOTE – Mapping ODU0 and ODU1 into a 5G tributary slot of the OPUC $n$  does not fully occupy the tributary slot's bandwidth.

Figures 7-2, 7-3 and 7-4 show how various signals are multiplexed using the ODTUG1/2/3 (PT=20) multiplexing elements. Figure 7-2 presents the multiplexing of four ODU1 signals into the OPU2 signal via the ODTUG2 (PT=20). An ODU1 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 1 into 2 (ODTU12) using the AMP justification overhead (JOH). The four ODTU12 signals are time-division multiplexed into the optical data tributary unit group 2 (ODTUG2) with payload type 20, after which this signal is mapped into the OPU2.



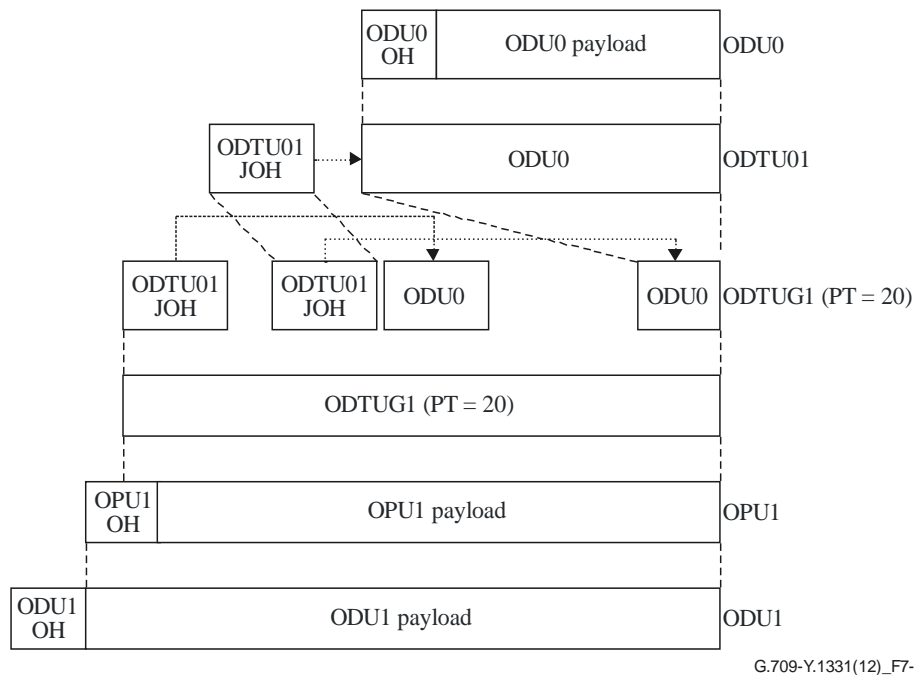
**Figure 7-2 – ODU1 into ODU2 multiplexing method via ODTUG2 (PT=20)**

Figure 7-3 presents the multiplexing of up to 16 ODU1 signals and/or up to 4 ODU2 signals into the OPU3 signal via the ODTUG3 (PT=20). An ODU1 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 1 into 3 (ODTU13) using the AMP justification overhead (JOH). An ODU2 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 2 into 3 (ODTU23) using the AMP justification overhead (JOH). "x" ODTU23 ( $0 \leq x \leq 4$ ) signals and "16-4x" ODTU13 signals are time-division multiplexed into the optical data tributary unit group 3 (ODTUG3) with payload type 20, after which this signal is mapped into the OPU3.



**Figure 7-3 – ODU1 and ODU2 into ODU3 multiplexing method via ODTUG3 (PT=20)**

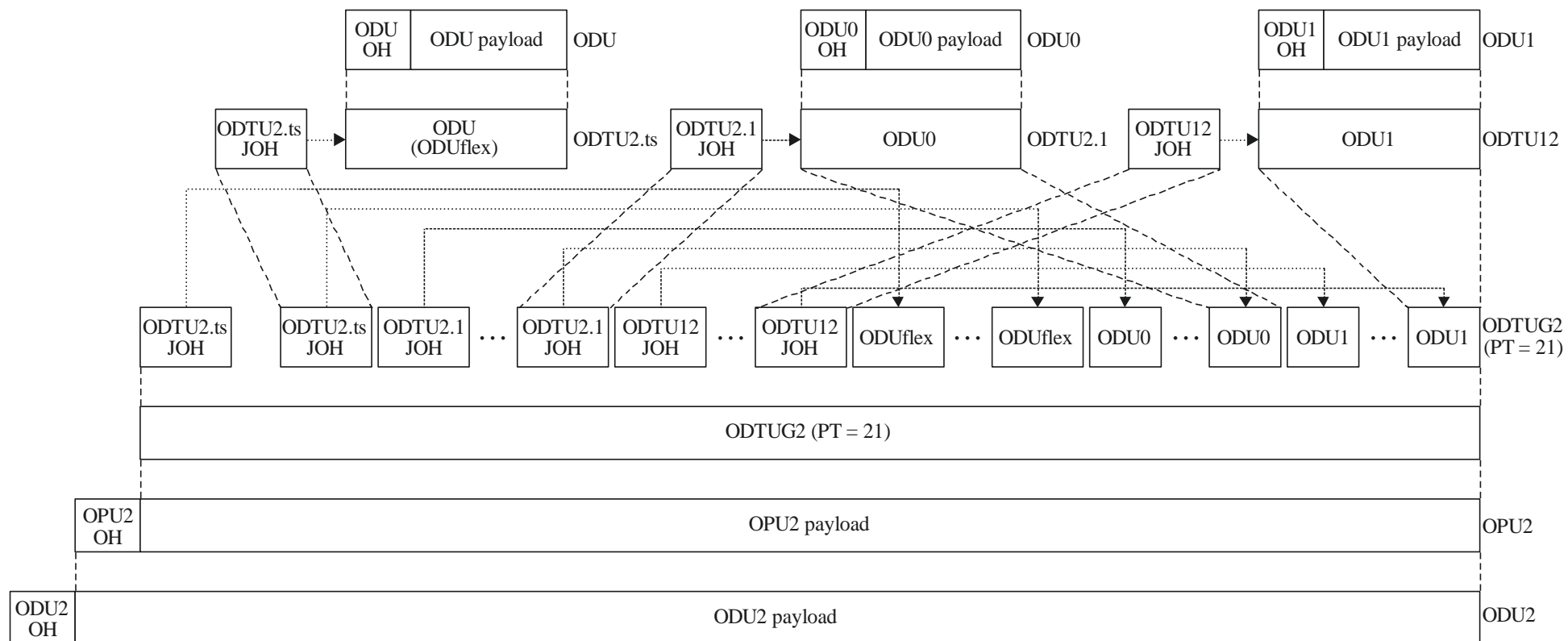
Figure 7-4 presents the multiplexing of two ODU0 signals into the OPU1 signal via the ODTUG1 (PT=20). An ODU0 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 0 into 1 (ODTU01) using the AMP justification overhead (JOH). The two ODTU01 signals are time-division multiplexed into the optical data tributary unit group 1 (ODTUG1) with payload type 20, after which this signal is mapped into the OPU1.



**Figure 7-4 – ODU0 into ODU1 multiplexing method via ODTUG1 (PT=20)**

Figures 7-5, 7-6 and 7-7 show how various signals are multiplexed using the ODTUG2/3/4 (PT=21) multiplexing elements.

Figure 7-5 presents the multiplexing of up to eight ODU0 signals, and/or up to four ODU1 signals and/or up to eight ODUflex signals into the OPU2 signal via the ODTUG2 (PT=21). An ODU1 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 1 into 2 (ODTU12) using the AMP justification overhead (JOH). An ODU0 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 2.1 (ODTU2.1) using the GMP justification overhead. An ODUflex signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 2.ts (ODTU2.ts) using the GMP justification overhead. Up to eight ODTU2.1 signals, up to four ODTU12 signals and up to eight ODTU2.ts signals are time-division multiplexed into the optical data tributary unit group 2 (ODTUG2) with payload type 21, after which this signal is mapped into the OPU2.

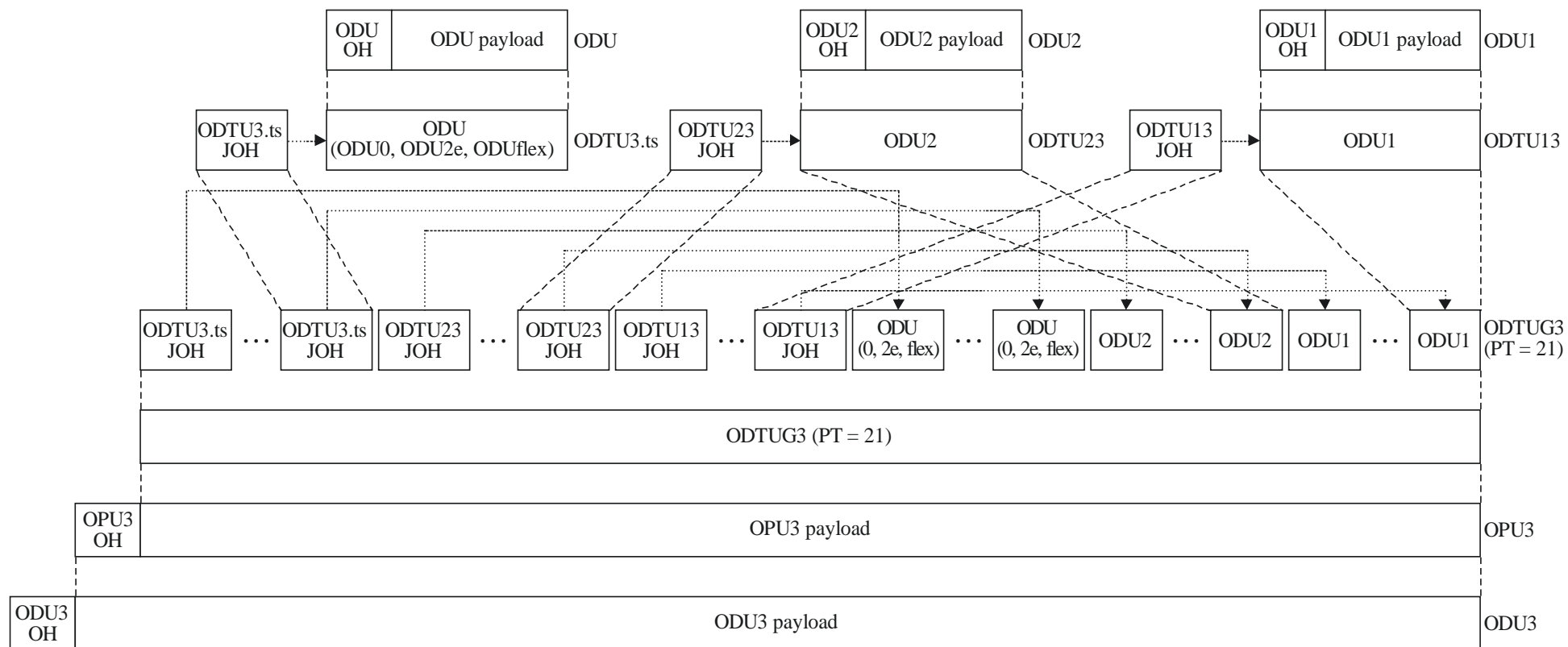


G.709-Y.1331(12)\_F7-5

**Figure 7-5 – ODU0, ODU1 and ODUflex into ODU2 multiplexing method via ODTUG2 (PT=21)**

Figure 7-6 presents the multiplexing of up to thirty-two ODU0 signals and/or up to sixteen ODU1 signals and/or up to four ODU2 signals and/or up to three ODU2e signals and/or up to thirty-two ODUflex signals into the OPU3 signal via the ODTUG3 (PT=21). An ODU1 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 1 into 3 (ODTU13) using the AMP justification overhead (JOH). An ODU2 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 2 into 3 (ODTU23) using the AMP justification overhead. An ODU0 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 3.1 (ODTU3.1) using the GMP justification overhead. An ODU2e signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 3.9 (ODTU3.9) using the GMP justification overhead. An ODUflex signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 3.ts (ODTU3.ts) using the GMP justification overhead. Up to thirty-two ODTU3.1 signals, up to sixteen ODTU13 signals, up to four ODTU23 signals, up to three ODTU3.9 and up to thirty-two ODTU3.ts signals are time-division multiplexed into the optical data tributary unit group 3 (ODTUG3) with payload type 21, after which this signal is mapped into the OPU3.

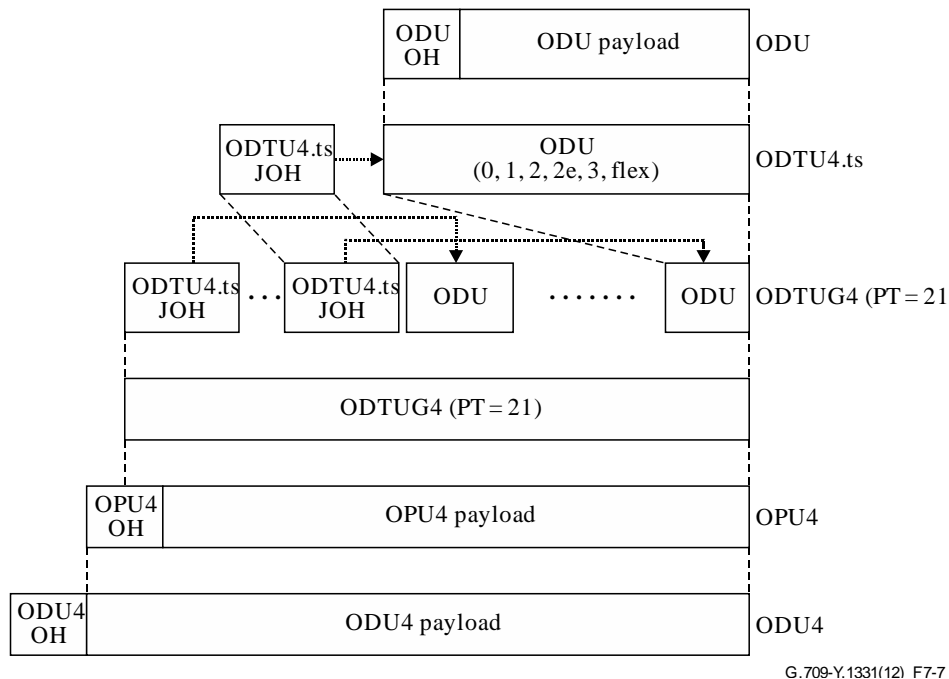




G.709-Y.1331(12)\_F7-6

Figure 7-6 – ODU0, ODU1, ODU2, ODU2e and ODUflex into ODU3 multiplexing method via ODTUG3 (PT=21)

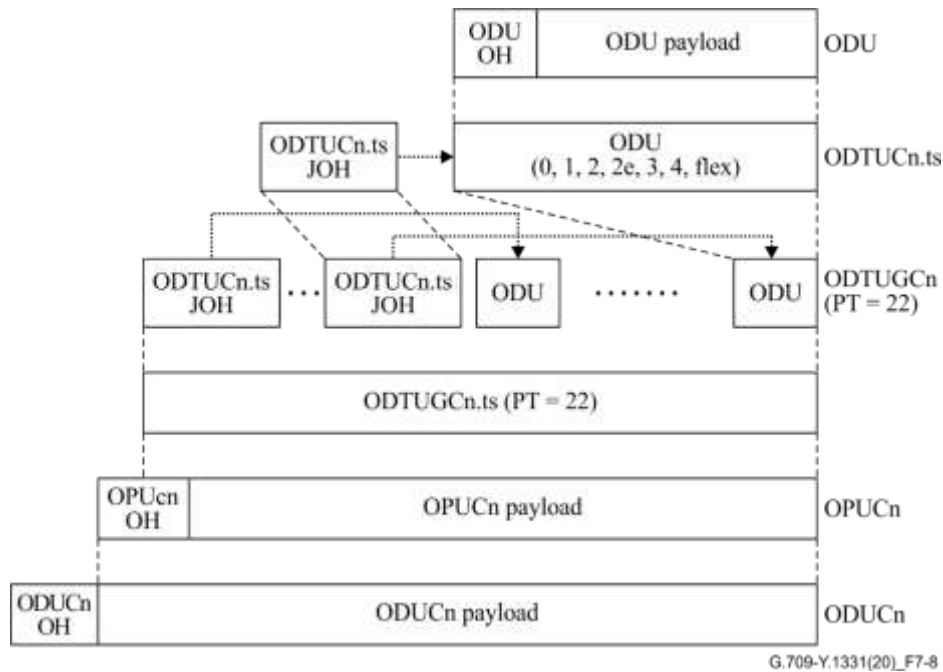
Figure 7-7 presents the multiplexing of up to eighty ODU0 signals and/or up to forty ODU1 signals and/or up to ten ODU2 signals and/or up to ten ODU2e signals and/or up to two ODU3 signals and/or up to eighty ODUflex signals into the OPU4 signal via the ODTUG4 (PT=21). An ODU0 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 4.1 (ODTU4.1) using the GMP justification overhead (JOH). An ODU1 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 4.2 (ODTU4.2) using the GMP justification overhead. An ODU2 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 4.8 (ODTU4.8) using the GMP justification overhead (JOH). An ODU2e signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 4.8 (ODTU4.8) using the GMP justification overhead. An ODU3 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 4.31 (ODTU4.31) using the GMP justification overhead. An ODUflex signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 4.ts (ODTU4.ts) using the GMP justification overhead (JOH). Up to eighty ODTU4.1 signals, up to forty ODTU4.2 signals, up to ten ODTU4.8 signals, up to two ODTU4.31 and up to eighty ODTU4.ts signals are time-division multiplexed into the optical data tributary unit group 4 (ODTUG4) with payload type 21, after which this signal is mapped into the OPU4.



G.709-Y.1331(12) F7-7

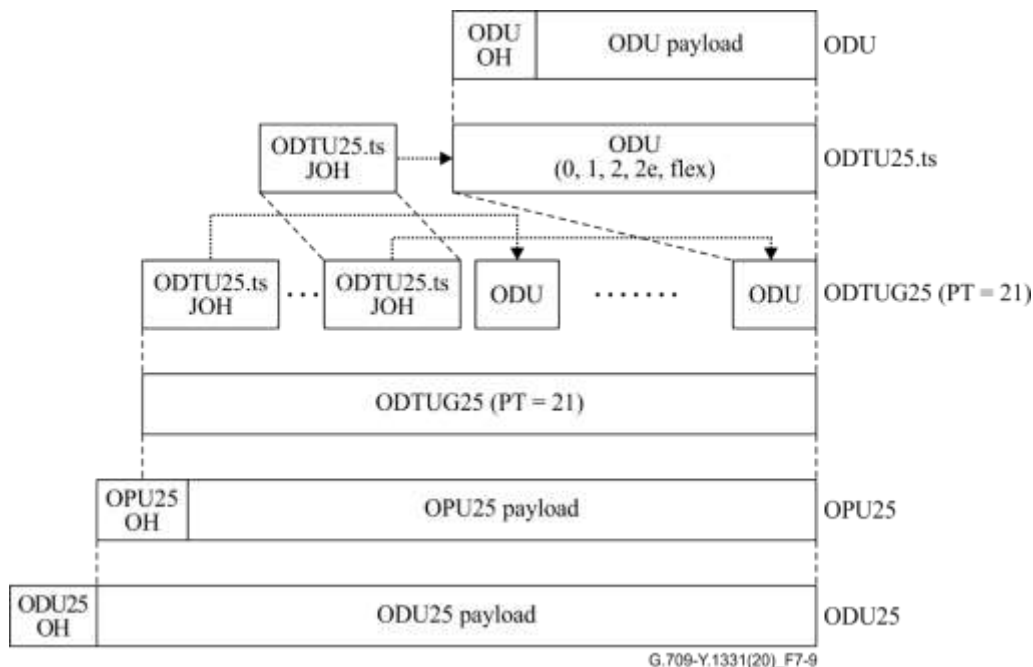
**Figure 7-7 – ODU0, ODU1, ODU2, ODU2e, ODU3 and ODUflex into ODU4 multiplexing method via ODTUG4 (PT=21)**

Figure 7-8 presents the multiplexing of up to  $10n$  ODU0 signals and/or up to  $10n$  ODU1 signals and/or up to  $10n$  ODU2 signals and/or up to  $10n$  ODU2e signals and/or up to  $\lfloor 2.5n \rfloor$  ODU3 signals and/or up to  $n$  ODU4 signals and/or up to  $10n$  ODUflex signals into the OPUCn signal via the ODTUGCn (PT=22). An ODU<sub>k</sub> signal is extended with frame alignment overhead and asynchronously mapped into the Optical Data Tributary Unit Cn.ts (ODTUCn.ts) ( $\langle k,ts \rangle = \langle 0,1 \rangle, \langle 1,1 \rangle, \langle 2,2 \rangle, \langle 2e,2 \rangle, \langle 3,8 \rangle, \langle 4,20 \rangle, \langle flex,ts \rangle$ ) using the GMP justification overhead (JOH). Up to  $10n$  ODTUCn.1 signals, up to  $10n$  ODTUCn.2 signals, up to  $\lfloor 2.5n \rfloor$  ODTUCn.8 signals, up to  $n$  ODTUCn.10 signals and up to  $10n$  ODTUCn.ts signals are time-division multiplexed into the Optical Data Tributary Unit Group Cn (ODTUGCn) with Payload Type 22, after which this signal is mapped into the OPUCn.



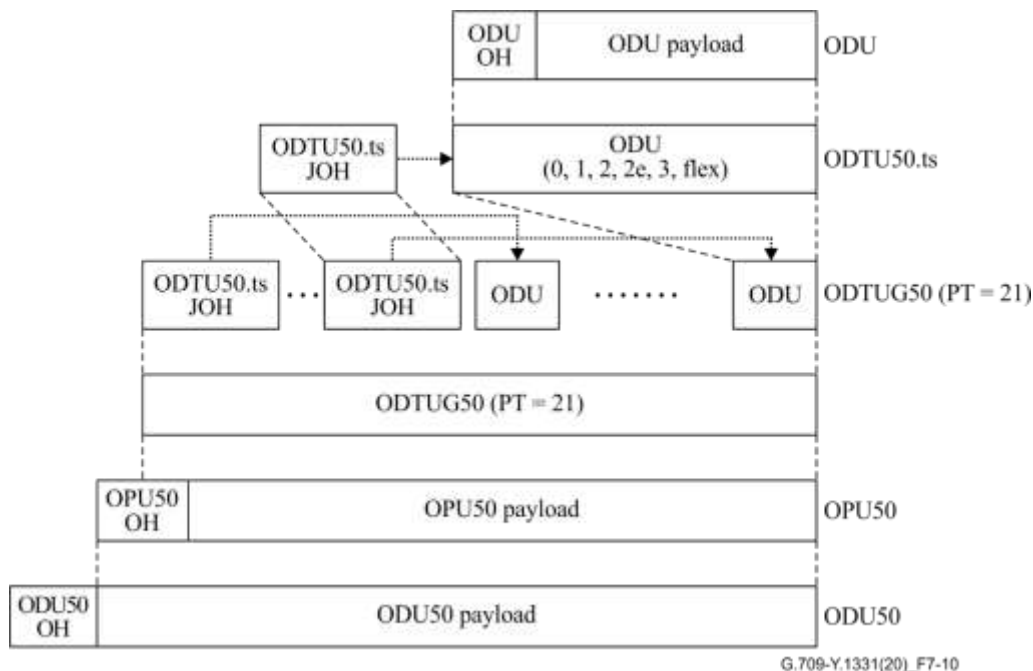
**Figure 7-8 – ODU0, ODU1, ODU2, ODU2e, ODU3, ODU4 and ODUflex into ODUcN multiplexing method via ODTUGcN (PT=22)**

Figure 7-9 presents the multiplexing of up to twenty ODU0 signals and/or up to ten ODU1 signals and/or up to two ODU2 signals and/or up to two ODU2e signals and/or up to twenty ODUflex signals into the OPU25 signal via the ODTUG25 (PT=21). An ODU0 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 25.1 (ODTU25.1) using the GMP justification overhead (JOH). An ODU1 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 25.2 (ODTU25.2) using the GMP justification overhead. An ODU2 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 25.8 (ODTU25.8) using the GMP justification overhead (JOH). An ODU2e signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 25.8 (ODTU25.8) using the GMP justification overhead. An ODUflex signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 25.ts (ODTU25.ts) using the GMP justification overhead (JOH). Up to twenty ODTU25.1 signals, up to ten ODTU25.2 signals, up to two ODTU25.8 signals and up to twenty ODTU25.ts signals are time-division multiplexed into the optical data tributary unit group 25 (ODTUG25) with payload type 21, after which this signal is mapped into the OPU25.



**Figure 7-9 – ODU0, ODU1, ODU2, ODU2e and ODUflex into ODU25 multiplexing method via ODTUG25 (PT=21)**

Figure 7-10 presents the multiplexing of up to forty ODU0 signals and/or up to twenty ODU1 signals and/or up to five ODU2 signals and/or up to five ODU2e signals and/or up to one ODU3 signals and/or up to forty ODUflex signals into the OPU50 signal via the ODTUG50 (PT=21). An ODU0 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 50.1 (ODTU50.1) using the GMP justification overhead (JOH). An ODU1 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 50.2 (ODTU50.2) using the GMP justification overhead. An ODU2 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 50.8 (ODTU50.8) using the GMP justification overhead (JOH). An ODU2e signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 50.8 (ODTU50.8) using the GMP justification overhead. An ODU3 signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 50.31 (ODTU50.31) using the GMP justification overhead. An ODUflex signal is extended with a frame alignment overhead and asynchronously mapped into the optical data tributary unit 50.ts (ODTU50.ts) using the GMP justification overhead (JOH). Up to forty ODTU50.1 signals, up to twenty ODTU50.2 signals, up to five ODTU50.8 signals, up to one ODTU50.31 and up to forty ODTU50.ts signals are time-division multiplexed into the optical data tributary unit group 50 (ODTUG50) with payload type 21, after which this signal is mapped into the OPU50.



**Figure 7-10 – ODU0, ODU1, ODU2, ODU2e, ODU3 and ODUflex into ODU50 multiplexing method via ODTUG50 (PT=21)**

Details of the multiplexing method and mappings are given in clause 19 for OPU<sub>k</sub> and clause 20 for OPU<sub>Cn</sub>.

Some examples illustrating the multiplexing of 2 ODU0 signals into an ODU1 and of 4 ODU1 signals into an ODU2 are presented in Appendix III.

### 7.5 Interconnection of Ethernet UNI and FlexE Group UNI in two administrative domains in the OTN

Ethernet PCS encoded client signals and Ethernet MAC client signals can be applied to the OTN via an Ethernet UNI and a FlexE group UNI.

The mapping method specified in clause 17 for the Ethernet PCS encoded client signals when applied via an Ethernet UNI are BMP, TTT+GMP and GMP, and via a FlexE group UNI is IMP.

The mapping method specified in clause 17 for the Ethernet MAC client signals with a bit rate up to and including 100 Gbit/s when applied via an Ethernet UNI is GFP-F and optionally can be IMP, and via a FlexE group UNI is IMP. The mapping method specified in clause 17 for both Ethernet MAC client and FlexE Client signals with a bit rate including and beyond 100 Gbit/s is IMP.

For the case of Ethernet PCS encoded client services between an Ethernet UNI in one administrative domain and a FlexE group UNI in another administrative domain, the rule for interconnecting an Ethernet PCS encoded client signal will be to use BMP, TTT+GMP or GMP on the interface between the two administrative domains.

For the case of Ethernet MAC client services with a bit rate up to and including 100 Gbit/s between an Ethernet UNI that applies the GFP-F mapping method in one administrative domain and a FlexE group UNI or an Ethernet UNI that applies the IMP mapping method in another administrative domain, the rule for interconnecting an Ethernet MAC client signal with a bit rate up to 100 Gbit/s will be to use GFP-F on the interface between the two administrative domains.

NOTE – For the case of Ethernet MAC client services with a bit rate including and beyond 100 Gbit/s between an Ethernet UNI in one administrative domain and a FlexE group UNI or an Ethernet UNI in another administrative domain, IMP mapping is used as the interconnect for the interface between the two administrative domains.

## 8 OTN Interfaces

### 8.1 Point-to-point interface, type I

The OTN point-to-point interface type I supports either one OTU on one OTSiG or one FlexO-x- $\langle$ fec $\rangle$  (out of one OTUCn/FlexO-x- $\langle$ fec $\rangle$ -m group) on one OTSiG on a single optical span with 3R regeneration at each end. The OTSiG is composed of one or more OTSi.

Application codes of the optical interface signal carrying the OTU or FlexO-x- $\langle$ fec $\rangle$  are contained in [ITU-T G.959.1] and [ITU-T G.693] and [ITU-T G.695].

Vendor specific application identifiers of the interfaces carrying these OTUs and FlexOs are outside the scope of this Recommendation.

### 8.2 Point-to-point interface, type II

The OTN point-to-point interface, type II supports n OTU and/or OTUCn/FlexO-x-RS- $\langle$ fec $\rangle$ -m signals on n OTSiG on a single optical span with 3R regeneration at each end. Each OTSiG is composed of one or more OTSi.

At least one of the OTU signals is present during normal operation.

There is no predefined order in which the OTU signals are taken into service.

NOTE – OTN point-to-point optical layer interface overhead is not defined. The interface will use the OTU SMOH in this multi-channel interface for supervision and management. The interface connectivity (TIM) failure reports will be computed from the individual OTU reports by means of failure correlation in fault management. Refer to the equipment Recommendations for further details.

Application codes of the optical interface signal carrying n OTU or FlexO-x- $\langle$ fec $\rangle$  signals are contained in [ITU-T G.959.1] and [ITU-T G.695].

Vendor specific application identifiers of the interfaces carrying these OTUs are outside the scope of this Recommendation.

### 8.3 Optical networking interface, type II

The OTN optical networking interfaces, type II carry one or more optical tributary signals, each transporting an OTUk or an OTUCn or one FlexO-x- $\langle$ fec $\rangle$  out of an OTUCn/FlexO-x- $\langle$ fec $\rangle$ -m group or a non-OTN client signal and OCh-O or OTSiG-O carried by an OCC. The OTUk, OTUCn or FlexO-x- $\langle$ fec $\rangle$  is carried over an OTSi.

The OTN optical networking interfaces, type II may carry one optical tributary signal, transporting an OTUk or an OTUCn or one FlexO-x- $\langle$ fec $\rangle$  out of an OTUCn/FlexO-x- $\langle$ fec $\rangle$ -m group or a non-OTN client signal and OCh-O or OTSiG-O carried by an OCC. The OTUk, OTUCn or FlexO-x- $\langle$ fec $\rangle$  is carried over an OTSi.

The OTN optical networking interfaces, type II may carry more than one optical tributary signals, each transporting an OTUCn or one FlexO-x- $\langle$ fec $\rangle$  out of an OTUCn/FlexO-x- $\langle$ fec $\rangle$ -m group or a non-OTN client signal and OCh-O or OTSiG-O carried by an OCC. The OTUCn or FlexO-x- $\langle$ fec $\rangle$  is carried over an OTSi.

Application codes of the optical tributary signal carrying the OTUk or FlexO-x- $\langle$ fec $\rangle$  are contained in [ITU-T G.698.1] and [ITU-T G.698.2].

Specifications of the OCC carrying the OCh-O or OTSiG-O are contained in [ITU-T G.7712].

Vendor specific application identifiers of the OTSi carrying these OTUks or OTUCns or FlexO-x- $\langle$ fec $\rangle$ s are outside the scope of this Recommendation.

## 8.4 Optical networking interface, type I

The OTN optical networking interfaces, type I carry one or more optical tributary signals, each transporting an OTUk or an OTUCn or one FlexO-x- $\langle fec \rangle$  out of an OTUCn/FlexO-x- $\langle fec \rangle$ -m group or a non-OTN client signal and OTS-O, OMS-O and OCh-O carried by an OSC and OTSiG-O carried by an OSC or partly carried by other means. 3R regeneration is not required at the interface.

Application codes of the optical tributary signal carrying the OTUk or FlexO-x- $\langle fec \rangle$  are contained in [ITU-T G.698.1] and [ITU-T G.698.2].

Vendor specific application identifiers of the OTSi or OTSiG carrying these OTUs or FlexO-x- $\langle fec \rangle$ s are outside the scope of this Recommendation.

## 9 Media Element

A description of the media element will be provided in [ITU-T G.872].

## 10 OCh and OTSiA

The OCh and OTSiA transport a digital client signal between 3R regeneration points. The OCh and OTSiA client signals defined in this Recommendation are the OTUk, OTUk-v, OTUkV and OTUCn signals.

### 10.1 OCh

The OCh structure is conceptually shown in Figure 10-1. The OCh contains two parts: an overhead part (OCh-O) and a payload part (OTSiG).

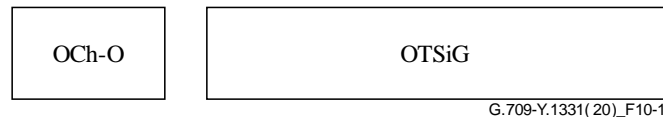


Figure 10-1 – OCh information structure

### 10.2 Optical tributary signal assembly (OTSiA)

The OTSiA structure is conceptually shown in Figure 10-2. The OTSiA contains two parts: a payload part (OTSiG) and an overhead part (OTSiG-O).



Figure 10-2 – OTSiA information structure

## 11 Optical transport unit (OTU)

The OTUk[V] conditions the ODUk for transport over an OCh network connection. The OTUk frame structure, including the OTUk FEC is completely standardized. The OTUkV is a frame structure, including the OTUkV FEC that is only functionally standardized (i.e., only the required functionality is specified); refer to Appendix II. Besides these two, there is an OTUkV in which the completely standardized OTUk frame structure is combined with a functionally standardized OTUkV FEC; refer to appendix II. This combination is identified as OTUk-v.

The OTUCn frame structure is defined without an OTUCn FEC area. The FEC associated with an OTUCn is interface dependent and specified as an element of each interface.

The OTU25 and OTU50 frame structure is defined without an OTU FEC area. The FEC associated with an OTU25 and OTU50 is interface dependent and specified as an element of each interface.

### 11.1 OTUk (k=0,1,2,3,4-SC) frame structure

The OTUk (k=0,1,2,3,4-SC) frame structure is based on the ODUk frame structure and extends it with a forward error correction (FEC) as shown in Figure 11-1. 256 columns are added to the ODUk frame for the FEC and the reserved overhead bytes in row 1, columns 8 to 14 of the ODUk overhead are used for an OTUk specific overhead, resulting in an octet-based block frame structure with four rows and 4080 columns. The MSB in each octet is bit 1, the LSB is bit 8.

NOTE – This Recommendation does not specify an OTUk frame structure for k=0, k=2e or k=flex. See Annex G for the specification of OTU0LL.

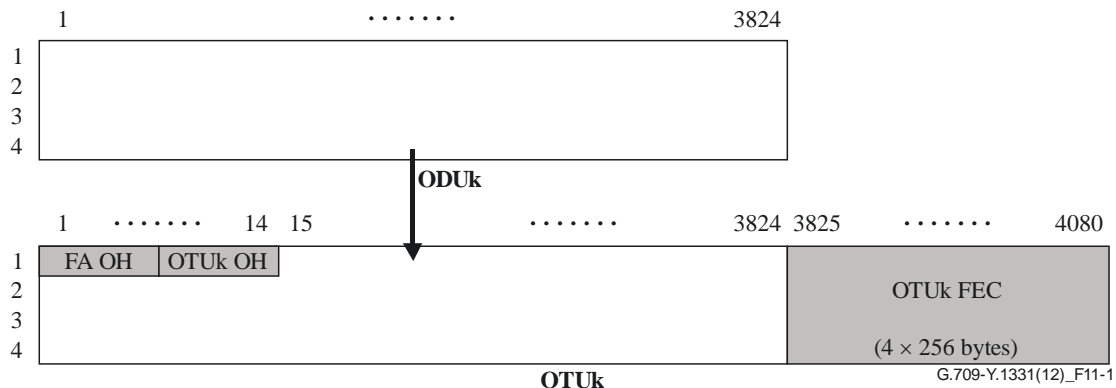


Figure 11-1 – OTUk frame structure

The bit rates of the OTUk signals are defined in Table 7-1.

The OTUk forward error correction (FEC) area contains an interface specific FEC type. Two FEC types are specified:

#### Reed-Solomon RS(255,239) FEC

The OTUk (k=0,1,2,3,4) FEC area contains the Reed-Solomon RS(255,239) FEC codes. Transmission of the OTUk FEC is mandatory for k=4 and optional for k=0,1,2,3. If no FEC is transmitted, fixed stuff bytes (all-0s pattern) are to be used.

The RS(255,239) FEC code shall be computed as specified in Annex A.

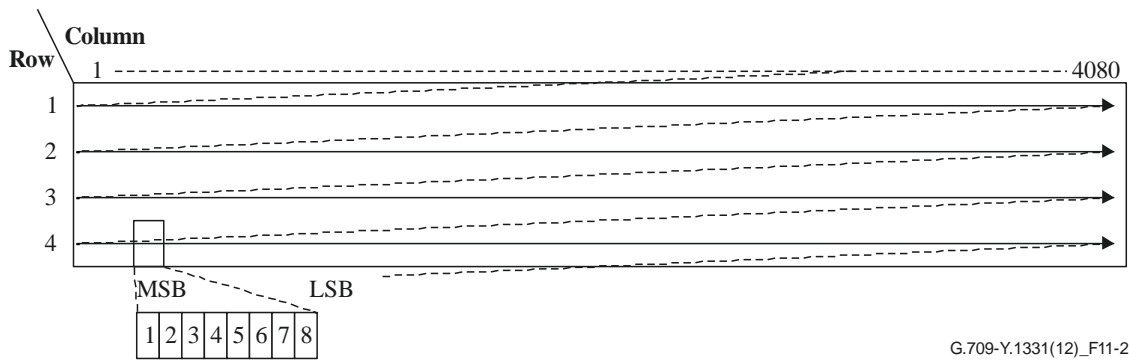
For interworking of equipment supporting FEC, with equipment not supporting FEC (inserting fixed stuff all-0s pattern in the OTUk (k=0,1,2,3) FEC area), the FEC supporting equipment shall support the capability to disable the FEC decoding process (ignore the content of the OTUk (k=0,1,2,3) FEC).

#### Staircase FEC

The OTU4 FEC area contains the Stair Case FEC codes as specified in [ITU-T G.709.2] and the resulting signal is referred to as OTU4-SC.

The transmission order of the bits in the OTUk frame is left to right, top to bottom, and MSB to LSB (see Figure 11-2).





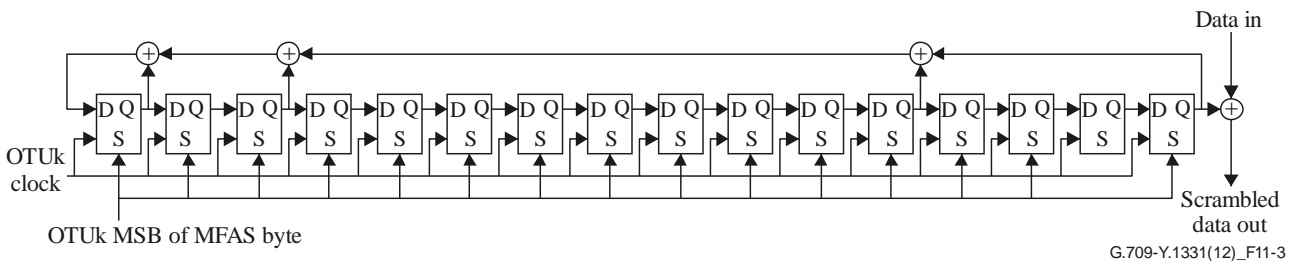
**Figure 11-2 – Transmission order of the OTUk frame bits**

**11.2 Scrambling for OTUk (k=0,1,2,3,4)**

The OTUk (k=0,1,2,3,4) signal must have sufficient bit timing content at the ONNI. A suitable bit pattern, which prevents a long sequence of "1"s or "0"s, is provided by using a scrambler.

The operation of the scrambler shall be functionally identical to that of a frame synchronous scrambler of sequence length 65535 operating at the OTUk rate.

The generating polynomial shall be  $1 + x + x^3 + x^{12} + x^{16}$ . Figure 11-3 shows a functional diagram of the frame synchronous scrambler.



**Figure 11-3 – Frame synchronous scrambler**

The scrambler shall be reset to "FFFF" (HEX) on the most significant bit of the byte following the last framing byte in the OTUk frame, i.e., the MSB of the MFAS byte. This bit, and all subsequent bits to be scrambled shall be added modulo 2 to the output from the  $x^{16}$  position of the scrambler. The scrambler shall run continuously throughout the complete OTUk frame. The framing bytes (FAS) of the OTUk overhead shall not be scrambled.

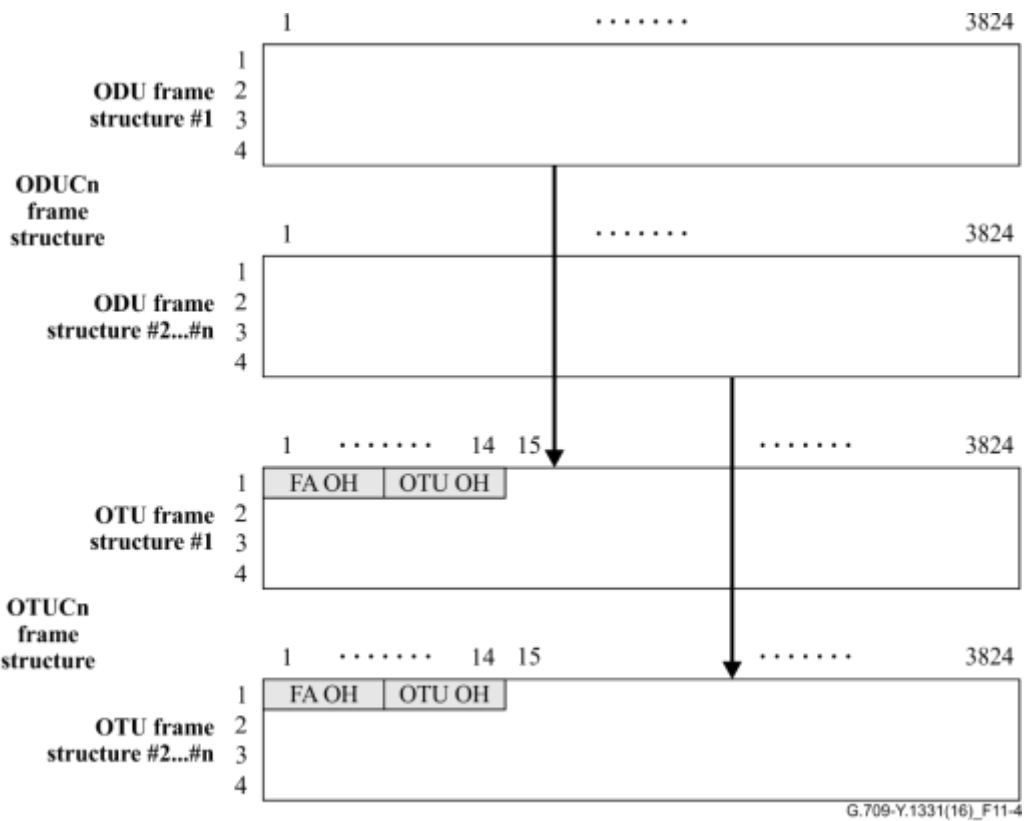
Scrambling is performed after FEC computation and insertion into the OTUk signal.

**11.3 OTUCn frame structure**

The OTUCn frame structure (Figure 11-4) is based on the ODUCn frame structure and deploys the reserved overhead bytes in row 1, columns 8 to 14 of each ODU frame structure in the ODUCn overhead for an OTUCn specific overhead, resulting in an octet-based block frame structure with  $n \times$  four rows and 3824 columns. The MSB in each octet is bit 1, the LSB is bit 8.

Interleaving of the n frame and multi-frame synchronous OTU frame structure instances within the OTUCn, forward error correction, encoding (e.g., scrambling), deskewing and transmission order of the OTUCn are interface specific and specified for inter-domain OTN interfaces with application codes in the interface specific Recommendations (ITU-T G.709.x series). For OTN interfaces with vendor specific application identifiers these specifications are vendor specific and out of scope of this Recommendation.

The bit rates of the OTUCn signals are defined in Table 7-1.



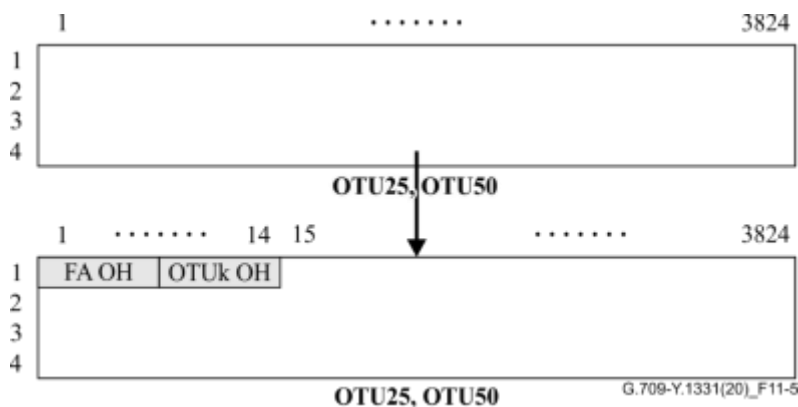
**Figure 11-4 – OTUCn frame structure**

#### 11.4 OTU25 and OTU50 frame structure

The OTU25 and OTU50 frame structure is based on the ODU<sub>k</sub> (k=25, 50) frame structure and deploys the reserved overhead bytes in row 1, columns 8 to 14 of the ODU<sub>k</sub> overhead for an OTU specific overhead, resulting in an octet-based block frame structure with four rows and 3824 columns. The MSB in each octet is bit 1, the LSB is bit 8.

Forward error correction, encoding (e.g., scrambling), deskewing and transmission order of the OTU25 and OTU50 are specified for inter-domain OTN interfaces with application codes in the interface specific Recommendations [ITU-T G.709.4].

The bit rates of the OTU25 and OTU50 signals are defined in Table 7-1.



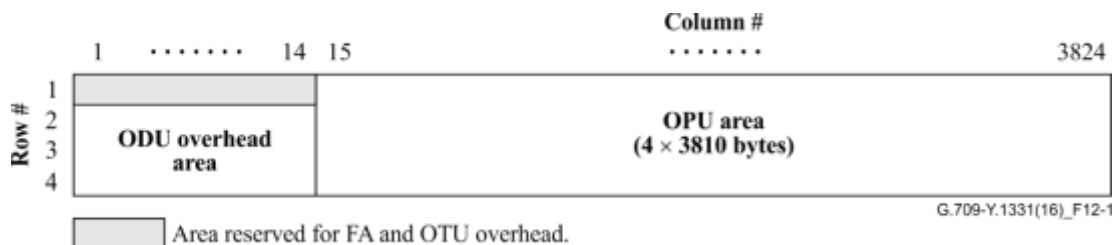
**Figure 11-5 – OTU25 and OTU50 frame structure**

## 12 Optical data unit (ODU)

### 12.1 ODU frame structure

The ODU frame structure is shown in Figure 12-1. It is organized in an octet-based block frame structure with four rows and 3824 columns.

The ODU<sub>k</sub> (k=0,1,2,2e,3,4,flex) frame structure contains one instance of the ODU frame structure. The ODU<sub>Cn</sub> frame structure contains n frame and multi-frame synchronous instances of the ODU frame structures, numbered 1 to n (ODU #1 to ODU #n).



**Figure 12-1 – ODU frame structure**

The two main areas of the ODU frame are:

- ODU overhead area
- OPU area.

Columns 1 to 14 of the ODU are dedicated to ODU overhead area.

NOTE – Columns 1 to 14 of row 1 are reserved for a frame alignment and OTU specific overhead.

Columns 15 to 3824 of the ODU are dedicated to OPU area.

### 12.2 ODU bit rates and bit-rate tolerances

ODU<sub>k</sub> signals may be generated using either a local clock, or the recovered clock of the client signal. In the latter case the ODU<sub>k</sub> frequency and frequency tolerance are locked to the client signal's frequency and frequency tolerance. In the former case the ODU<sub>k</sub> frequency and frequency tolerance are locked to the local clock's frequency and frequency tolerance. The local clock frequency tolerance for the OTN is specified to be  $\pm 20$  ppm.

ODU<sub>Cn</sub> signals are generated using a local clock. The ODU<sub>Cn</sub> frequency and frequency tolerance are locked to the local clock's frequency and frequency tolerance. The local clock frequency tolerance for the OTN is specified to be  $\pm 20$  ppm.

ODU maintenance signals (ODU AIS, OCI, LCK) are generated using a local clock. In a number of cases this local clock may be the clock of a server ODU signal over which the ODU signal is transported between equipment or through equipment (in one or more of the tributary slots). For these cases, the nominal justification ratio should be deployed to comply with the ODU's bit-rate tolerance specification.

#### 12.2.1 ODU0, ODU1, ODU2, ODU3, ODU4, ODU25, ODU50, ODU<sub>Cn</sub>

The local clocks used to create the ODU0, ODU1, ODU2, ODU3, ODU4, ODU25, ODU50 and ODU<sub>Cn</sub> signals are generated by clock crystals that are also used for the generation of SDH STM-N signals. The bit rates of these ODU<sub>k</sub> (k=0,1,2,3,4,25,50) and ODU<sub>Cn</sub> signals are therefore related to the STM-N bit rates and the bit-rate tolerances are the bit-rate tolerances of the STM-N signals.

The ODU0 bit rate is 50% of the STM-16 bit rate.

The ODU1 bit rate is 239/238 times the STM-16 bit rate.

The ODU2 bit rate is  $239/237$  times 4 times the STM-16 bit rate.

The ODU3 bit rate is  $239/236$  times 16 times the STM-16 bit rate.

The ODU4 bit rate is  $239/227$  times 40 times the STM-16 bit rate.

The ODU25 bit rate is  $41118/41120$  times  $514/544$  times  $255/227$  times 10 times the STM-16 bit rate, which is equal to  $61677/58112$  times 10 times the STM-16 bit rate.

The ODU50 bit rate is  $41118/41120$  times  $514/544$  times  $255/227$  times 20 times the STM-16 bit rate, which is equal to  $61677/58112$  times 20 times the STM-16 bit rate.

The ODUCn bit rate is n times  $239/226$  times 40 times the STM-16 bit rate.

ODU1, ODU2 and ODU3 signals which carry an STM-N (N = 16, 64, 256) signal may also be generated using the timing of these client signals.

Refer to Table 7-2 for the nominal bit rates and bit-rate tolerances.

#### **12.2.1.1 ODUk (k=0,1,2,3,4), ODU25/50 and ODUCn transporting frequency synchronization information**

The local clocks used to create the frequency synchronous OPU0/ODU0/OTU0, OPU1/ODU1/OTU1, OPU2/ODU2/OTU2, OPU3/ODU3/OTU3, OPU4/ODU4/OTU4, OPU25/ODU25/OTU25, OPU50/ODU50/OTU50 and OPUCn/ODUCn/OTUCn/FlexO signals are generated by a synchronous equipment clock (SEC) function that is nominally locked to a primary reference clock (PRC). The bit rate tolerance of these frequency synchronous ODUk (and its OTUk) (k=0,1,2,3,4,4-SC), ODU25/50 (and their OTU25/50) and ODUCn (and its OTUCn and FlexO) signals are therefore related to the bit-rate tolerances of the SEC. Refer to [ITU-T G.8262].

During signal fail conditions, the frequency synchronous OTU and/or ODU signals are replaced by replacement signals (OTU-AIS and/or ODU-AIS) with a bit rate tolerance of  $\pm 20$  ppm.

#### **12.2.2 ODU2e**

An ODU2e signal is generated using the timing of its client signal.

The ODU2e bit rate is  $239/237$  times the 10GBASE-R client bit rate.

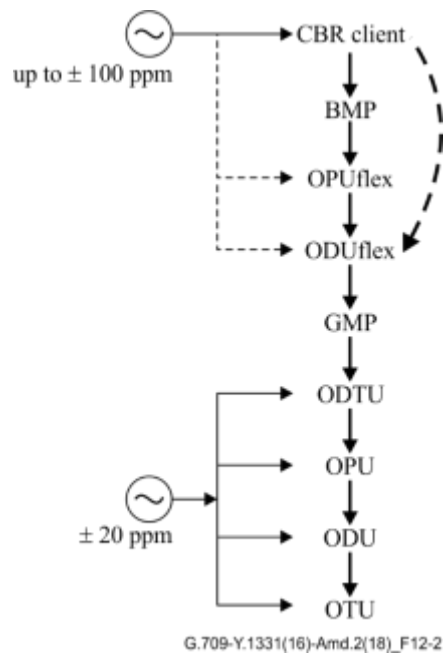
Refer to Table 7-2 for the nominal bit rate and bit-rate tolerances.

#### **12.2.3 ODUflex for CBR client signals**

An ODUflex(CBR) signal is generated using the timing of its client signal.

The ODUflex bit rate is  $239/238$  times the adapted CBR client bit rate.

The client signal may have a bit-rate tolerance up to  $\pm 100$  ppm.



**Figure 12-2 – ODUflex clock generation for CBR signals**

#### 12.2.4 ODUflex for PRBS and Null test signals

ODUflex(CBR) connections may be tested using a PRBS or NULL test signal as the client signal instead of the CBR client signal. For such a case, the ODUflex(PRBS) or ODUflex(NULL) signal should be generated with a frequency within the tolerance range of the ODUflex(CBR) signal.

If the CBR client clock is present such ODUflex(PRBS) or ODUflex(NULL) signal may be generated using the CBR client clock, otherwise the ODUflex(PRBS) or ODUflex(NULL) signal is generated using a local clock.

#### 12.2.5 ODUflex for GFP-F mapped packet client signals

ODUflex(GFP) signals are generated using a local clock. This clock may be the local server ODU<sub>k</sub> (or OTU<sub>k</sub>) clock, the local ODU<sub>Cn</sub> (or OTU<sub>Cn</sub>) clock, or an equipment internal clock of the signal over which the ODUflex is carried through the equipment. Refer to Appendix XV for examples on ODUflex(GFP) clock generation methods.

Any bit rate is possible for an ODUflex(GFP) signal. The ODUflex(GFP) bit rate is specified as  $239/238 \times X$  Gbit/s  $\pm 100$  ppm, in which X represents the configured GFP-F encapsulated packet client nominal bidirectional bit rate.

For ODUflex hitless resizing applications or for the case that the ODUflex(GFP) should fill an integral number of 1.25G tributary slots of the smallest server ODU<sub>k</sub> path over which the ODUflex(GFP) may be carried, a set of bit-rates with values  $n \times \text{ODU}_{k.ts}$  that meet this criterion are specified in Table 7-8. The derivation of the specific ODUflex(GFP,*n*,*k*) values is provided in Appendix XI.

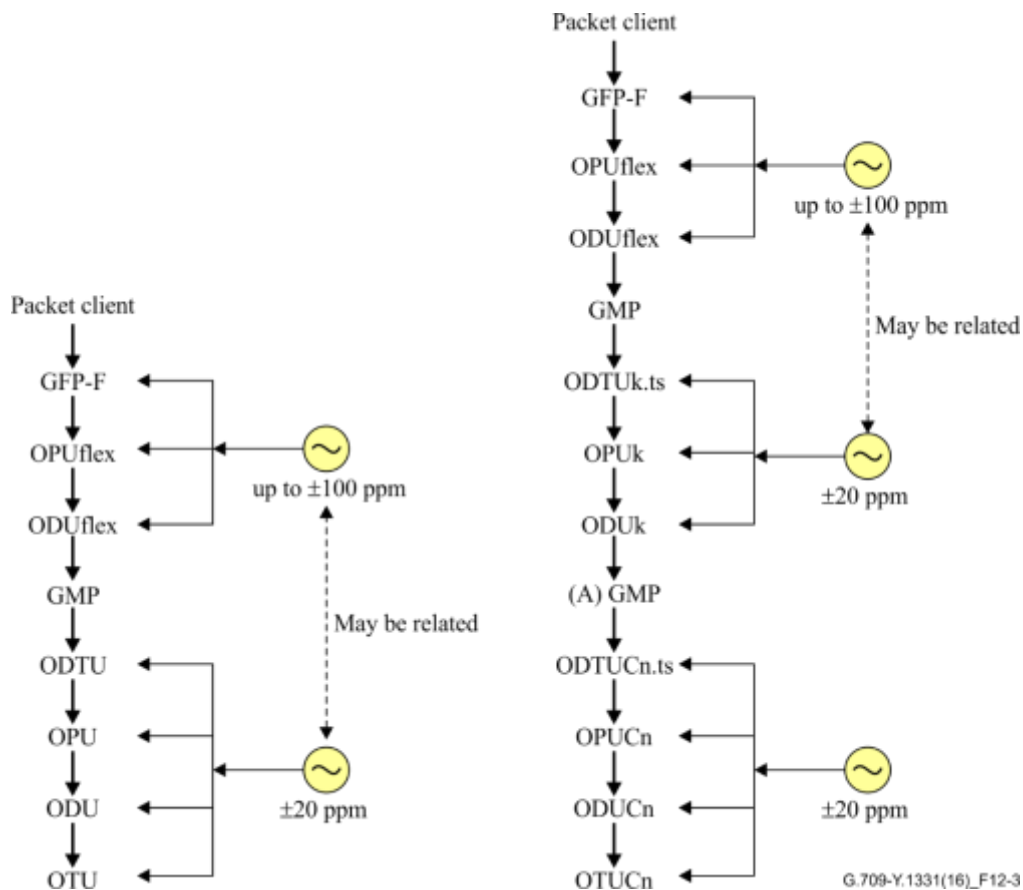


Figure 12-3 – ODUflex clock generation for GFP-F mapped packet client signals

### 12.2.6 ODUflex for IMP mapped client signals

ODUflex(IMP) signals are generated using a local clock or the timing of its client signal. The local clock may be the local server ODUk (or OTUk) clock, the local ODUCn (or OTUCn) clock, or an equipment internal clock of the signal over which the ODUflex is carried through the equipment. Refer to Appendix XV for examples on ODUflex(IMP) clock generation methods.

Any bit rate is possible for an ODUflex(IMP) signal. The ODUflex(IMP) bit rate is specified as  $239/238 \times X \text{ Gbit/s} \pm 100 \text{ ppm}$ , in which X represents the configured 64B/66B encoded packet client nominal bidirectional bit rate.

For the case that the ODUflex(IMP) would carry a FlexE Client signal with a bit rate of  $s \times 5,156,250.000 \text{ kbit/s} \pm 100 \text{ ppm}$  and  $s = 2, 8$  or  $n \times 5$  ( $n \geq 1$ ), the ODUflex(IMP,s) bit rate is  $s \times 239/238 \times 5,156,250.000 \text{ kbit/s} \pm 100 \text{ ppm}$ .

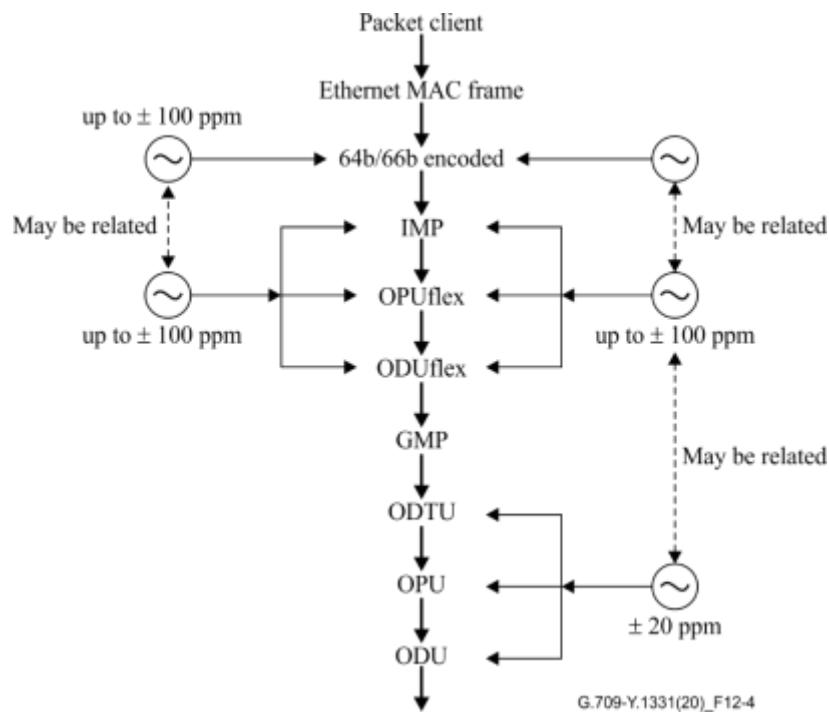


Figure 12-4 – ODUflex clock generation for IMP mapped packet client signals

### 13 Optical payload unit (OPU)

The OPU frame structure is shown in Figure 13-1. It is organized in an octet-based block frame structure with four rows and 3810 columns.

The OPU<sub>k</sub> (k=0,1,2,2e,3,4,flex,25,50) frame structure contains one instance of the OPU frame structure. The OPU<sub>Cn</sub> frame structure contains n frame and multi-frame synchronous instances of the OPU frame structure, numbered 1 to n (OPU #1 to OPU #n).

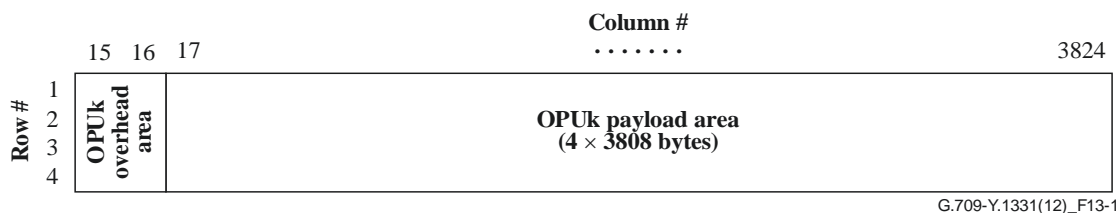


Figure 13-1 – OPU frame structure

The two main areas of the OPU frame are:

- OPU overhead area;
- OPU payload area.

Columns 15 to 16 of the OPU are dedicated to an OPU overhead area.

Columns 17 to 3824 of the OPU are dedicated to an OPU payload area.

NOTE – OPU column numbers are derived from the OPU columns in the ODU frame.

## **14 Overhead information carried over the OSC and OCC**

### **14.1 OSC**

The overhead information carried over the OSC consists of the OTS-O, OMS-O, OCh-O and OTSiG-O. The information content of this overhead is defined in clause 15. The format, structure and bit rate of this overhead is not defined in this Recommendation.

#### **General management communications (COMMS)**

Depending on an operator's logical management overlay network design, general management communications (COMMS) may also be transported within the OSC. Therefore, the OSC for some applications may also transport general management communications. General management communications may include signalling, voice/voiceband communications, software download, operator-specific communications, etc.

#### **OTN synchronisation message channel (OSMC)**

For synchronisation purposes, the OSC OSMC signal is defined as an OTN synchronisation message channel to transport SSM and PTP messages.

NOTE 1 – Support of OSC OSMC is optional.

NOTE 2 – Equipment designed prior to Edition 4.6 of this recommendation may not be able to support OSC OSMC.

### **14.2 OCC**

The overhead information carried over the OCC consists of the OCh-O or OTSiG-O. The information content of this overhead is defined in clause 15. The format, structure and bit rate of this overhead is defined in [ITU-T G.7712].

#### **14.2.1 OCh-O transport over OTN optical networking interface, type II**

For an OTN optical networking interface, type II, the OCh-O is transferred over the overhead communication network (OCN) as described in [ITU-T G.7712].

NOTE – An OTN optical networking interface which transfers OCh-O over an OCN cannot provide fate-sharing of the OCh-O with the OTSiG across this interface.

The OCh FDI-P, FDI-O and OCI Overhead primitives are communicated over the OCN. The specification of the encapsulation, identification and transmission of this information is outside the scope of this Recommendation and specified in [ITU-T G.7712]. This information must be communicated with the peers such that the OCh-O primitives come into sync within one second in the absence of changes to OCh FDI-P, FDI-O or OCI. In the event of changes to any OCh-O primitive, the update must be sent within 10 ms of the change and with a mechanism to guarantee receipt in the event of packet loss.

#### **14.2.2 OTSiG-O transport over OTN optical networking interface, type II**

For an OTN optical networking interface, type II, the OTSiG-O is transferred over the overhead communication network (OCN) as described in [ITU-T G.7712].

NOTE – An OTN optical networking interface which transfers OTSiG-O over an OCN cannot provide fate-sharing of the OTSiG-O with the OTSiG across this interface.

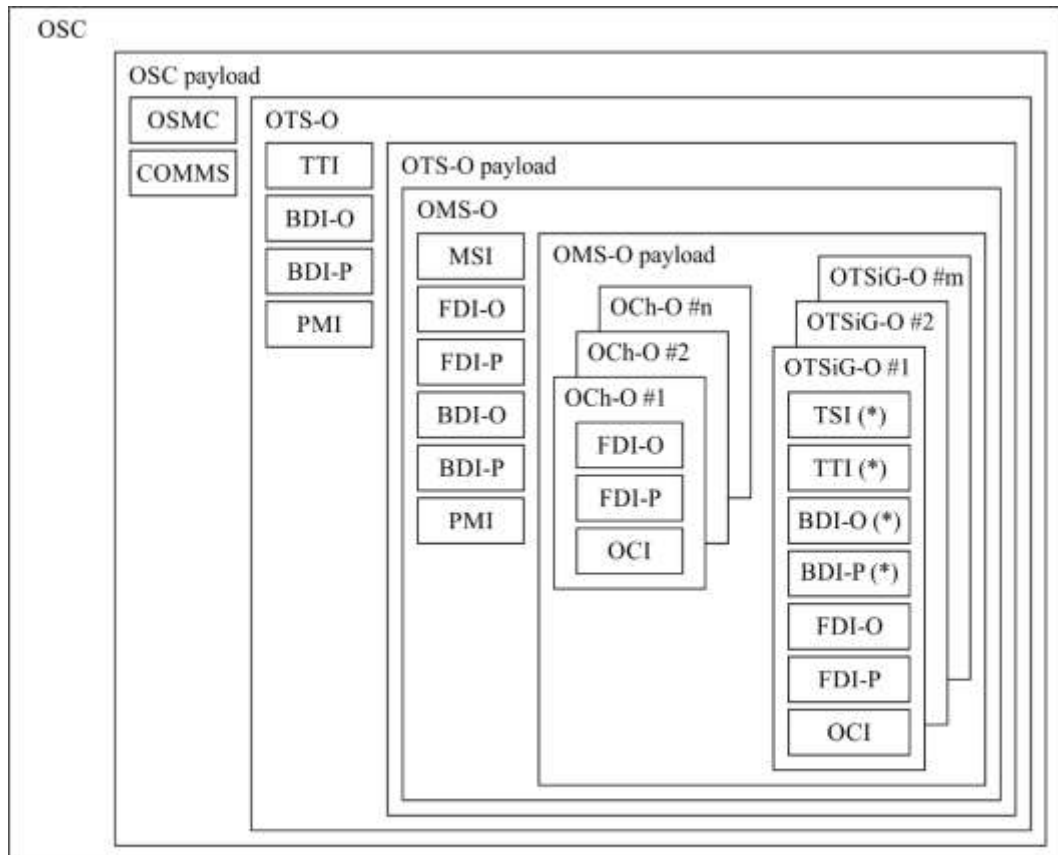
The OTSiG-O FDI-P, FDI-O, OCI, TTI, BDI-P, BDI-O and TSI Overhead primitives are communicated over the OCN. The specification of the encapsulation, identification and transmission of this information is outside the scope of this Recommendation and specified in [ITU-T G.7712]. This information must be communicated with the peers such that the OTSiG-O primitives come into sync within one second in the absence of changes to OTSiG FDI-P, FDI-O, OCI, TTI, BDI-P, BDI-O



or TSI. In the event of changes to any OTSiG-O primitive, the update must be sent within 10 ms of the change and with a mechanism to guarantee receipt in the event of packet loss.

## 15 Overhead description

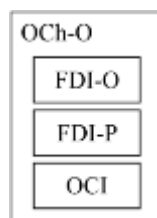
An overview of OTS-O, OMS-O, OCh-O and OTSiG-O information carried within the OSC is presented in Figure 15-1. An overview of OCh-O information carried within the OCC is presented in Figure 15-2.



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(\*) This overhead may be carried over the OSC or over a communication channel modulated on one or more OTSi within the OTSiG.

**Figure 15-1 – OTS-O, OMS-O, OCh-O and OTSiG-O information carried within the OSC**



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**Figure 15-2 – OCh-O information carried within the OCC**

An overview of OTUk, ODUk and OPUk overhead is presented in Figures 15-3A and 15-5. An overview of OTUCn, ODUCn and OPUCn overhead is presented in Figures 15-4 and 15-6. An overview of OTU25 and OTU50 overhead is presented in Figure 15-3B. It is the same as OTUk overhead.

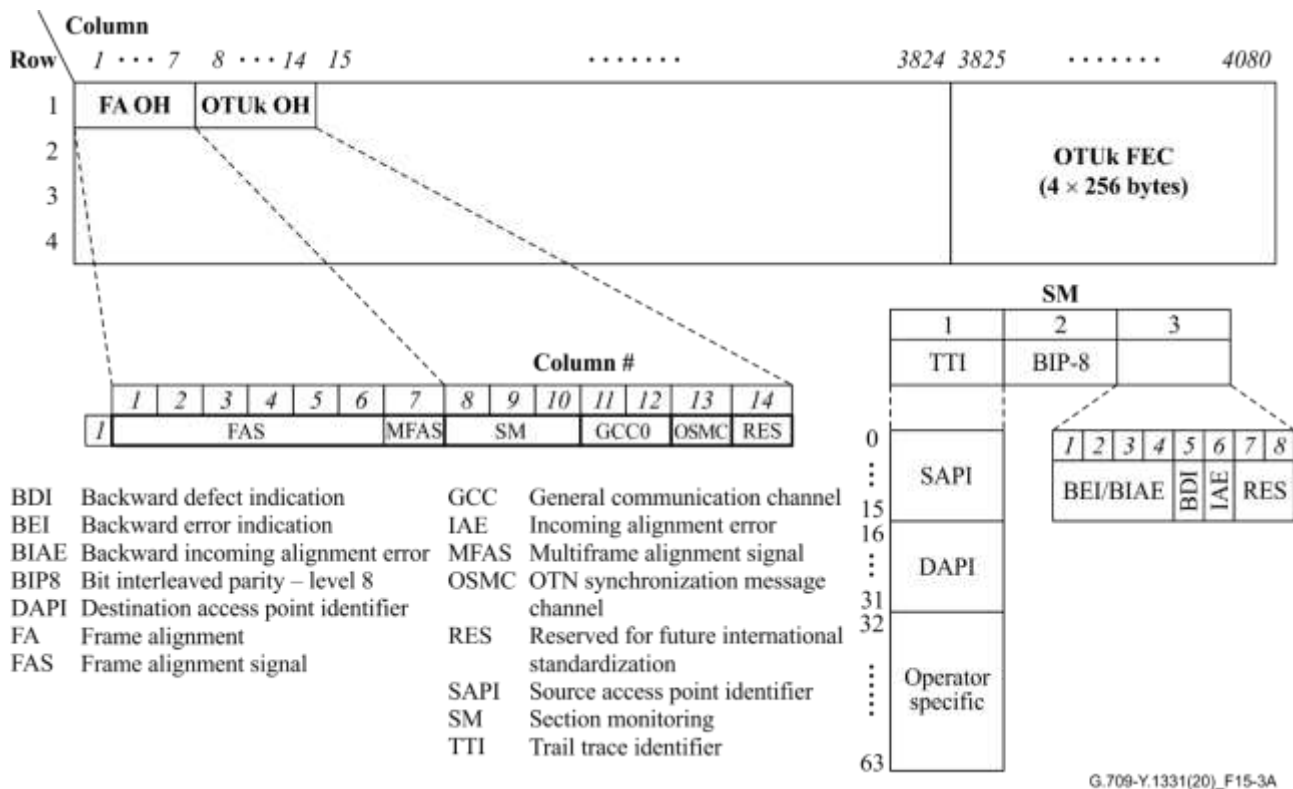


Figure 15-3A – OTUk frame structure, frame alignment and OTUk overhead

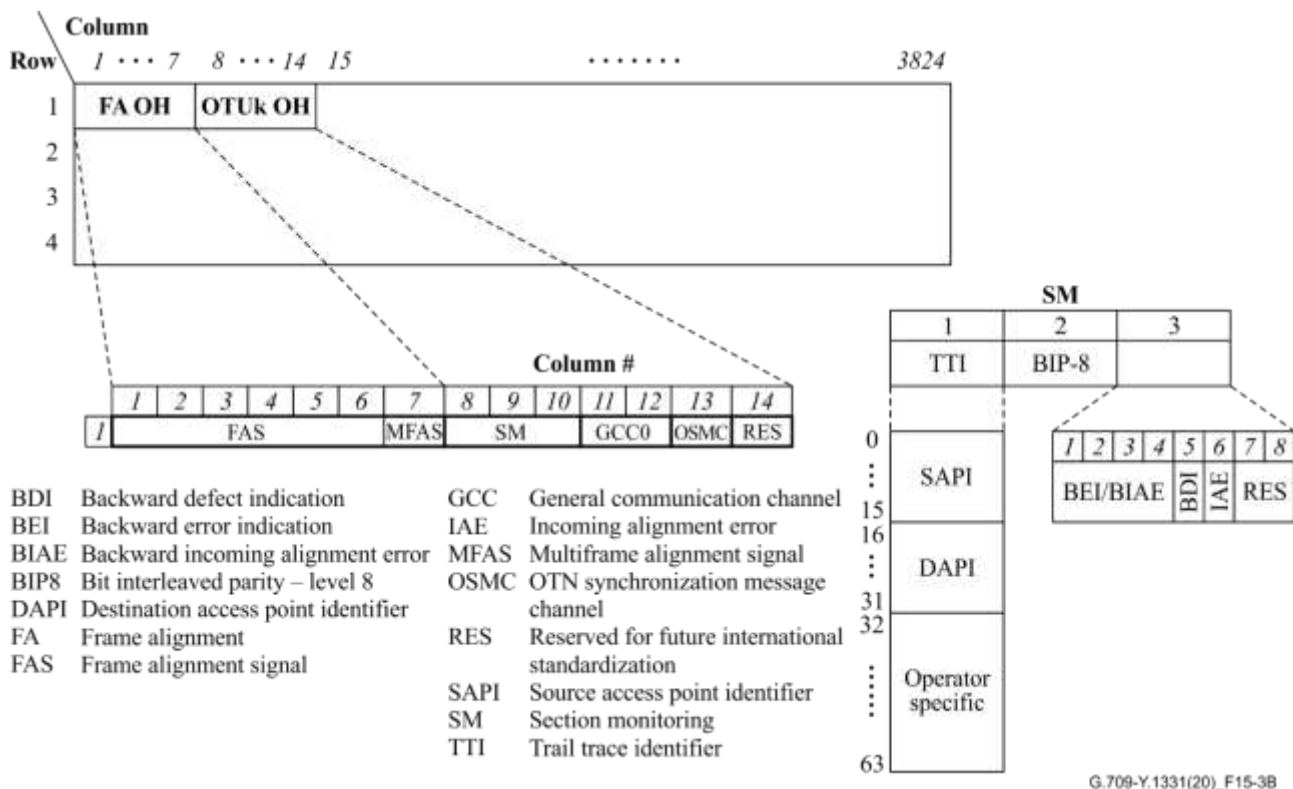
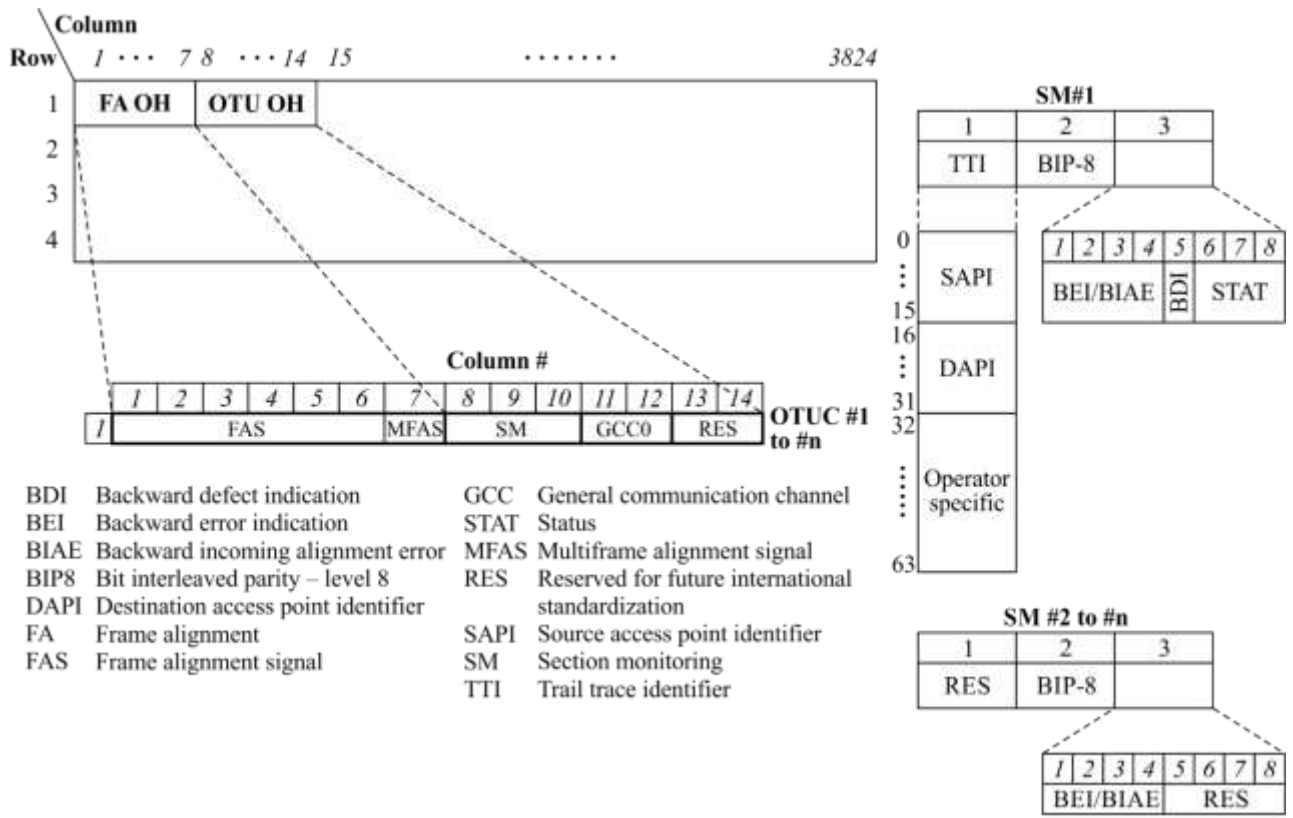
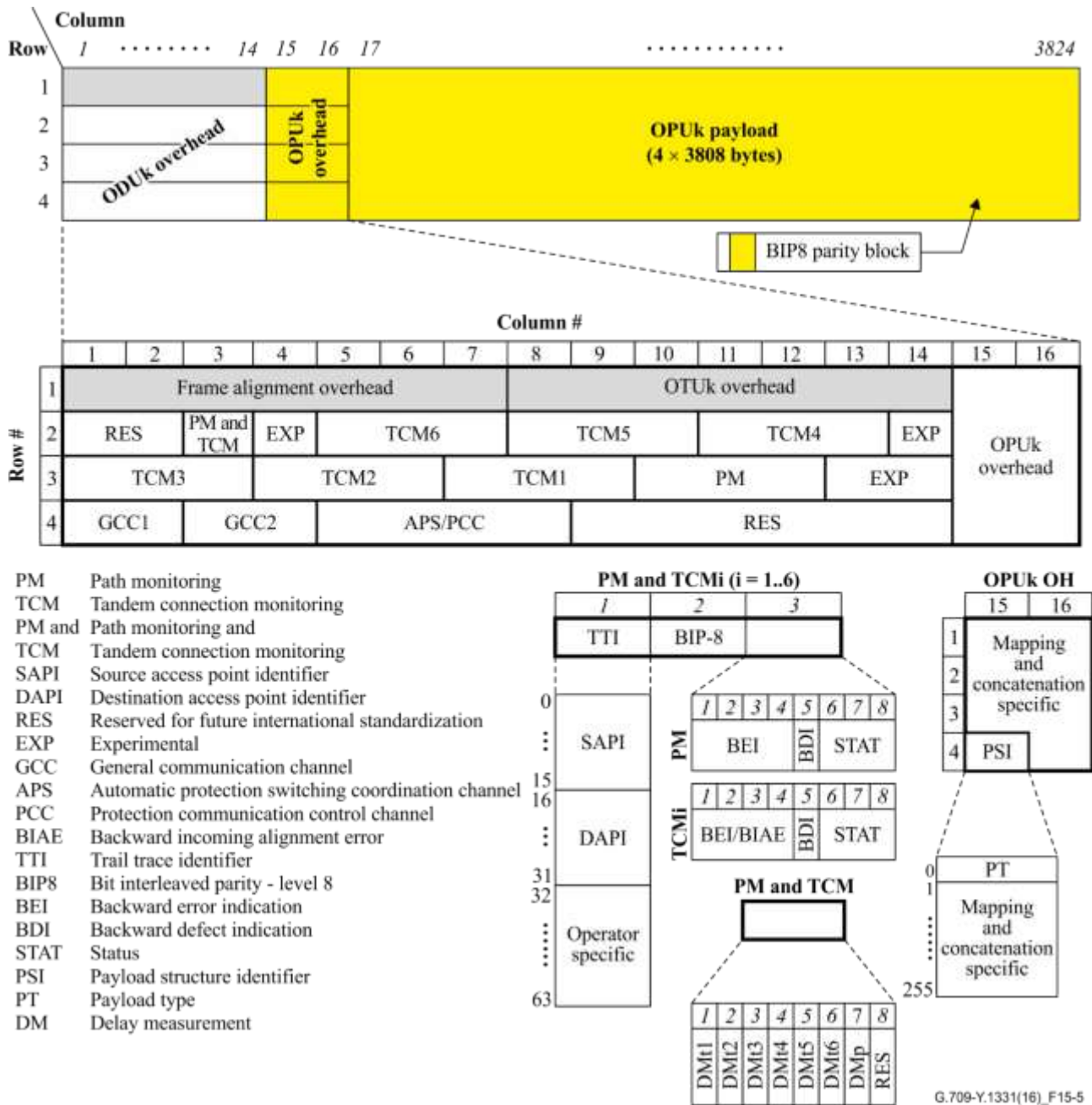


Figure 15-3B – OTU25 and OTU50 frame structure, frame alignment and OTU overhead



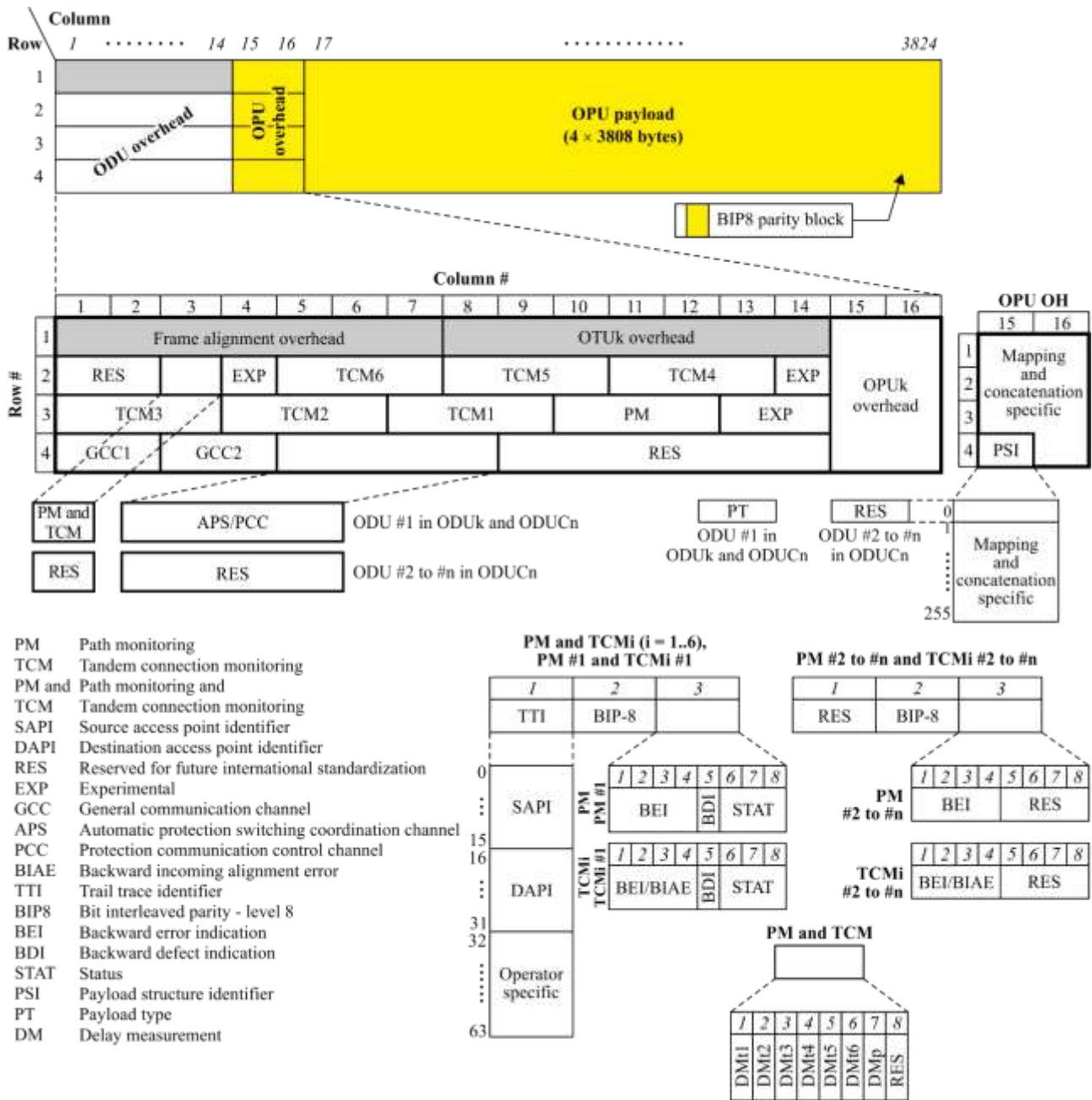
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Figure 15-4 – OTUCn frame structure, frame alignment and OTUCn overhead



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Figure 15-5 – ODUk frame structure, ODUk and OPUk overhead



**Figure 15-6 – ODUcN frame structure, ODUcN and OPUCn overhead**

## 15.1 Types of overhead

### 15.1.1 Optical payload unit overhead (OPU OH)

OPU OH information is added to the OPU information payload to create an OPU. It includes information to support the adaptation of client signals. The OPU OH is terminated where the OPU is assembled and disassembled. The specific OH format and coding is defined in clause 15.9.

### 15.1.2 Optical data unit overhead (ODU OH)

ODU OH information is added to the ODU information payload to create an ODU. It includes information for maintenance and operational functions to support ODU connections. The ODU OH consists of portions dedicated to the end-to-end ODU path and to six levels of tandem connection monitoring. The ODU path OH is terminated where the ODU is assembled and disassembled. The TC OH is added and terminated at the source and sink of the corresponding tandem connections, respectively. The specific OH format and coding is defined in clauses 15.6 and 15.8.

### **15.1.3 Optical transport unit overhead (OTU OH)**

OTU OH information is added to the OTU information payload to create an OTU. It includes information for maintenance and operational functions to support OTU connections. The OTU OH is terminated where the OTU signal is assembled and disassembled. The specific OH format and coding is defined in clauses 15.6 and 15.7.

The specific frame structure and coding for the non-standard OTUkV OH is outside the scope of this Recommendation. Only the required basic functionality that has to be supported is defined in clause 15.7.3.

### **15.1.4 OCh-O**

OCh-O is the non-associated overhead information that accompanies an OTSiG. It includes information for maintenance functions to support fault management. The OCh-O is generated or modified at intermediate points along the OCh trail. All information elements of the OCh-O are terminated where the OTSiG signal is terminated.

The OCh-O information is defined in clause 15.5.

### **15.1.5 OMS-O**

OMS-O is the non-associated overhead information that accompanies an OMS OSME. It includes information for maintenance and operational functions to support optical multiplex sections. The OMS-O is generated or modified at intermediate points along the OMS OSME and OMS-O trail and generated and terminated at the endpoints of the OMS OSME where the OMS-O trail is terminated.

OMS-O information elements other than OMS FDI-P and FDI-O are generated and terminated at the ends of the OMS-O trail. OMS FDI-P and FDI-O are generated at intermediate points along the OMS-O trail and terminated at the ends of the OMS-O trail.

The OMS-O information is defined in clause 15.4.

### **15.1.6 OTS-O**

OTS-O is the non-associated overhead information that accompanies an OTS OSME. It includes information for maintenance and operational functions to support optical transmission sections. The OTS-O is terminated at the endpoints of the OTS OSME where the OTS-O trail is terminated.

The OTS-O information is defined in clause 15.3.

### **15.1.7 General management communications overhead (COMMS OH)**

COMMS OH information provides general management communication between network elements. The specific frame structure and coding for the COMMS OH is outside the scope of this Recommendation.

### **15.1.8 OTSiG-O**

OTSiG-O is the non-associated overhead information that accompanies an OTSiG. It includes information for maintenance functions to support fault management. The OTSiG-O TSI, TTI, BDI-P and BDI-O are generated where the OTSiA signal is assembled and the OCI, FDI-P and FDI-O are modified or generated at intermediate points along the OTSiA trail. All information elements of the OTSiG-O are terminated where the OTSiA is disassembled.

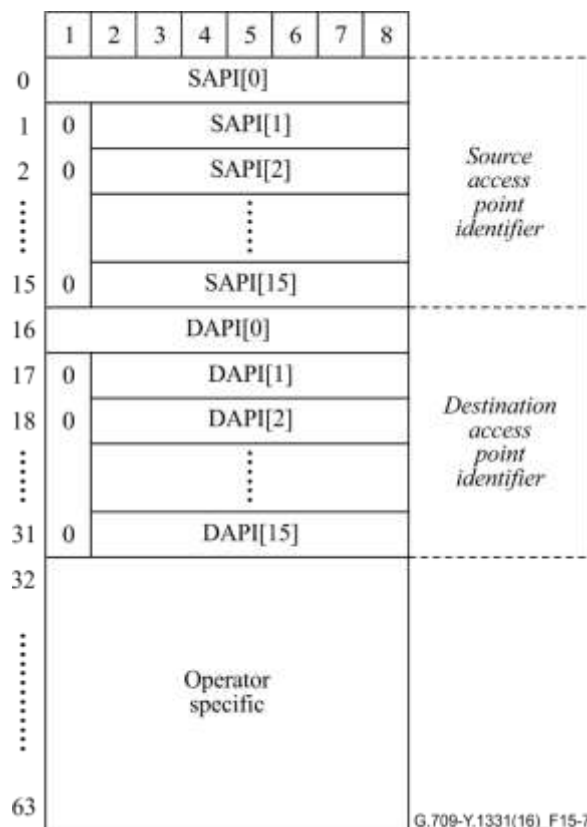
The OTSiG-O information is defined in clause 15.5.

NOTE – OSC signals designed prior to Edition 5 of this recommendation may only be able to transport a subset of the OTSiG-O (possibly excluding TSI, TTI, BDI-P and BDI-O) overhead.

## 15.2 Trail trace identifier and access point identifier definition

A trail trace identifier (TTI) is defined as a 64-byte string with the following structure (see Figure 15-7):

- TTI[0] contains the SAPI[0] character, which is fixed to all-0s.
- TTI[1] to TTI[15] contain the 15-character source access point identifier (SAPI[1] to SAPI[15]).
- TTI[16] contains the DAPI[0] character, which is fixed to all-0s.
- TTI[17] to TTI[31] contain the 15-character destination access point identifier (DAPI[1] to DAPI[15]).
- TTI[32] to TTI[63] are operator specific.



**Figure 15-7 – TTI structure**

The features of access point identifiers (APIs) are:

- Each access point identifier must be globally unique in its layer network.
- Where it may be expected that the access point may be required for path set-up across an inter-operator boundary, the access point identifier must be available to other network operators.
- The access point identifier should not change while the access point remains in existence.
- The access point identifier should be able to identify the country and network operator which is responsible for routing to and from the access point.
- The set of all access point identifiers belonging to a single administrative layer network should form a single access point identification scheme.
- The scheme of access point identifiers for each administrative layer network can be independent from the scheme in any other administrative layer network.

It is recommended that the ODUk, OTUk and OTS should each have the access point identification scheme based on a tree-like format to aid routing control search algorithms. The access point identifier should be globally unambiguous.

The access point identifier (SAPI, DAPI) shall consist of a three-character international segment and a twelve-character national segment (NS) (see Figure 15-8). These characters shall be coded according to [ITU-T T.50] (International Reference Alphabet – 7-bit coded character set for information exchange).

IS character #			NS character #											
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CC			ICC	UAPC										
CC			ICC			UAPC								
CC			ICC				UAPC							
CC			ICC						UAPC					
CC			ICC						UAPC					
CC			ICC						UAPC					

**Figure 15-8 – Access point identifier structure**

The international segment field provides a three-character ISO 3166 geographic/political country code (G/PCC). The country code shall be based on the three-character uppercase alphabetic ISO 3166 country code (e.g., USA, FRA).

The national segment field consists of two subfields: the ITU carrier code (ICC) followed by a unique access point code (UAPC).

The ITU carrier code is a code assigned to a network operator/service provider, maintained by the ITU-T Telecommunication Standardization Bureau (TSB) as per [ITU-T M.1400]. This code shall consist of 1-6 left-justified characters, alphabetic, or leading alphabetic with trailing numeric.

The unique access point code shall be a matter for the organization to which the country code and ITU carrier code have been assigned, provided that uniqueness is guaranteed. This code shall consist of 6-11 characters, with trailing NUL, completing the 12-character national segment.

### 15.3 OTS-O description

The following OTS-O information elements are defined:

- OTS-TTI
- OTS-BDI-P
- OTS-BDI-O
- OTS-PMI

#### 15.3.1 OTS trail trace identifier (TTI)

The OTS-TTI is defined to transport a 64-byte TTI as specified in clause 15.2 for OTS connectivity monitoring.

#### 15.3.2 OTS backward defect indication – Payload (BDI-P)

For OTS OSME and OTS-O trail monitoring, the OTS-BDI-P signal is defined to convey in the upstream direction the OTS OSME and OTS-O trail signal fail status detected in the sink point of the OTS OSME and OTS-O trail termination sink function.



### **15.3.3 OTS backward defect indication – Overhead (BDI-O)**

For OTS-O trail monitoring, the OTS-BDI-O signal is defined to convey in the upstream direction the OTS-O signal fail status detected in the OTS-O trail termination sink function.

### **15.3.4 OTS payload missing indication (PMI)**

The OTS PMI is a signal sent downstream as an indication that upstream at the source point of the OTS OSME no optical signal is present, in order to suppress the report of the consequential loss of signal condition at the sink point of the OTS OSME.

## **15.4 OMS-O description**

The following OMS-O information elements are defined:

- OMS-FDI-P
- OMS-FDI-O
- OMS-BDI-P
- OMS-BDI-O
- OMS-PMI
- OMS-MSI

### **15.4.1 OMS forward defect indication – Payload (FDI-P)**

For OMS OSME and OMS-O trail monitoring, the OMS-FDI-P signal is defined to convey in the downstream direction the signal status (normal or failed).

### **15.4.2 OMS forward defect indication – Overhead (FDI-O)**

For OMS-O trail monitoring, the OMS-FDI-O signal is defined to convey in the downstream direction the OMS-O signal status (normal or failed).

### **15.4.3 OMS backward defect indication – Payload (BDI-P)**

For OMS OSME and OMS-O trail monitoring, the OMS-BDI-P signal is defined to convey in the upstream direction the OMS-P signal fail status detected in the sink point of the OMS OSME and OMS-O trail termination sink function.

### **15.4.4 OMS backward defect indication – Overhead (BDI-O)**

For OMS-O trail monitoring, the OMS-BDI-O signal is defined to convey in the upstream direction the OMS-O signal fail status detected in the OMS-O trail termination sink function.

### **15.4.5 OMS payload missing indication (PMI)**

The OMS PMI is a signal sent downstream as an indication that upstream at the source point of the OMS OSME none of the frequency slots contain an optical tributary signal, in order to suppress the report of the consequential loss of signal condition at the sink point of the OMS OSME.

### **15.4.6 OMS multiplex structure identifier (MSI)**

The OMS multiplex structure identifier (MSI) signal encodes the OTSiG multiplex structure and occupied frequency slots in the OMS OSME at the source end point. It is sent downstream to enable detection of OTSiG multiplex structure configuration mismatches between sink and source end points.

The OMS multiplex structure identifier (MSI) signal also encodes the media channel structure which is independent of the OTSiG in the OMS OSME at the source and sink end points. It is sent downstream to enable detection of media channel structure configuration mismatches between sink and source end points.

The OMS MSI is defined for flex grid OTN optical networking interfaces, type I. Fixed grid OTN optical networking interfaces may not support the OMS MSI. Flex grid OTN optical networking interfaces, type I designed prior to Edition 5.0 of this Recommendation may not support the OMS MSI.

## **15.5 OCh-O and OTSiG-O description**

The following OCh-O and OTSiG-O information elements are defined:

- OCh-FDI-P and OTSiA-FDI-P
- OCh-FDI-O and OTSiA-FDI-O
- OCh-OCI and OTSiA-OCI
- OTSiA-BDI-P
- OTSiA-BDI-O
- OTSiA-TTI
- OTSiG-TSI

### **15.5.1 OCh and OTSiA forward defect indication – Payload (FDI-P)**

For OCh and OTSiA trail monitoring, the OCh-FDI-P or OTSiA-FDI-P signal is defined to convey in the downstream direction the OTSiG signal status (normal or failed).

### **15.5.2 OCh and OTSiA forward defect indication – Overhead (FDI-O)**

For OCh and OTSiA trail monitoring, the OCh-FDI-O or OTSiA-FDI-O signal is defined to convey in the downstream direction the OCh-O or OTSiG-O overhead signal status (normal or failed).

### **15.5.3 OCh and OTSiA open connection indication (OCI)**

The OCh and OTSiA OCI is a signal sent downstream as an indication that upstream in a connection function the OCh (i.e., OTSiG and OCh-O) or OTSiA (i.e., OTSiG and OTSiG-O) matrix connection is opened as a result of a management command. The consequential detection of the OCh or OTSiA loss of signal condition at the OCh or OTSiA termination point can now be related to an open matrix.

### **15.5.4 Blank clause**

*This clause is intentionally left blank.*

### **15.5.5 OTSiA backward defect indication – Payload (BDI-P)**

For OTSiA path monitoring, the OTSiA-BDI-P signal is defined to convey in the upstream direction the OTSiG signal fail status detected in the OTSiG termination sink function.

### **15.5.6 OTSiA backward defect indication – Overhead (BDI-O)**

For OTSiA path monitoring, the OTSiA-BDI-O signal is defined to convey in the upstream direction the OTSiG-O signal fail status detected in the OTSiG-O termination sink function.

### **15.5.7 OTSiA trail trace identifier (TTI)**

The OTSiA-TTI is defined to transport a 64-byte TTI as specified in clause 15.2 for OTSiA path monitoring.

### **15.5.8 OTSiG transmitter structure identifier (TSI)**

The OTSiG-TSI is defined to transport a TSI for monitoring consistent configuration of the OTSiG transmitter(s) at source end points and OTSiG receiver(s) at sink end points.

## 15.6 OTU/ODU frame alignment OH description

### 15.6.1 OTU/ODU frame alignment overhead location

The OTU/ODU frame alignment overhead location is shown in Figure 15-9. The OTU/ODU frame alignment overhead is applicable for both the OTU and ODU signals.

The OTUk/ODUk, OTU25/ODU25 and OTU50/ODU50 contain one instance of OTU/ODU frame alignment overhead. The OTUCn/ODUCn contains n instances of OTU/ODU frame alignment overhead, numbered 1 to n.

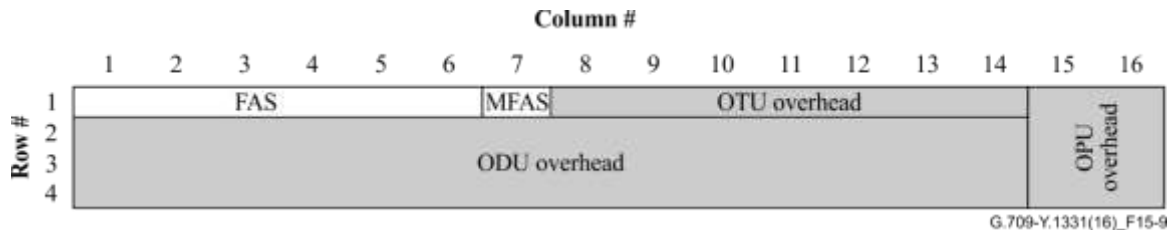


Figure 15-9 – OTU/ODU frame alignment overhead

### 15.6.2 OTU/ODU frame alignment overhead definition

#### 15.6.2.1 Frame alignment signal (FAS)

A six byte OTU-FAS signal (see Figure 15-10) is defined in row 1, columns 1 to 6 of the OTU overhead. OA1 is "1111 0110". OA2 is "0010 1000".

The OTUk, OTU25 and OTU50 contain one instance of OTU multi-frame alignment overhead. The OTUCn contains n instances of OTU multi-frame alignment overhead, numbered 1 to n.

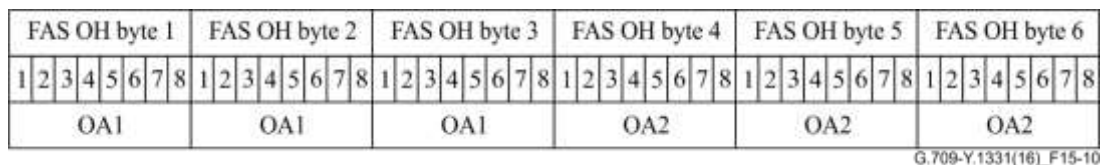


Figure 15-10 – Frame alignment signal overhead structure

#### 15.6.2.2 Multiframe alignment signal (MFAS)

Some of the OTU and ODU overhead signals will span multiple OTU/ODU frames. Examples are the TTI and TCM-ACT overhead signals. These and other multiframe structured overhead signals require multiframe alignment processing to be performed, in addition to the OTU/ODU frame alignment.

A single multiframe alignment signal (MFAS) byte is defined in row 1, column 7 of the OTU/ODU overhead for this purpose (see Figure 15-11). The value of the MFAS byte will be incremented each OTU/ODU frame and provides as such a 256-frame multiframe.

The OTUk, OTU25 and OTU50 contain one instance of OTU multi-frame alignment overhead. The OTUCn contains n instances of OTU multi-frame alignment overhead, numbered 1 to n. All n MFAS bytes carry the same 256-frame sequence and in each frame all n MFAS bytes carry the same value.



**Figure 15-11 – Multiframe alignment signal overhead**

Individual OTU/ODU overhead signals may use this central multiframe to lock their 2-frame, 4-frame, 8-frame, 16-frame, 32-frame, etc., multiframe to the principal frame.

NOTE 1 – The 80-frame OPU4 multiframe cannot be supported. A dedicated 80-frame OPU4 multiframe indicator (OMFI) is used instead.

NOTE 2 – The 20-frame OPUCn and OPUk (k = 25) multiframe cannot be supported by MFAS. A dedicated 20-frame OPUCn and OPUk multiframe indicator (OMFI) is used instead.

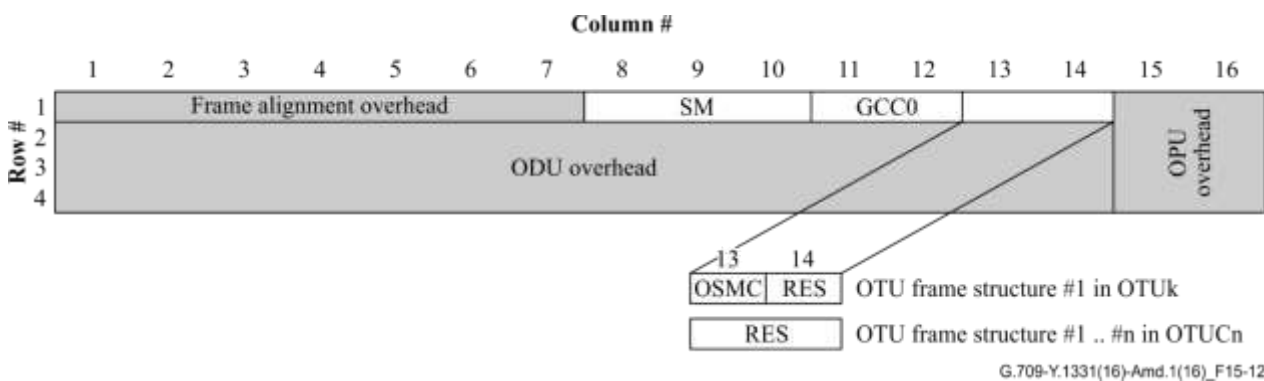
NOTE 3 – The 40-frame OPUk (k = 50) multiframe cannot be supported by MFAS. A dedicated 40-frame OPUk multiframe indicator (OMFI) is used instead.

## 15.7 OTU OH description

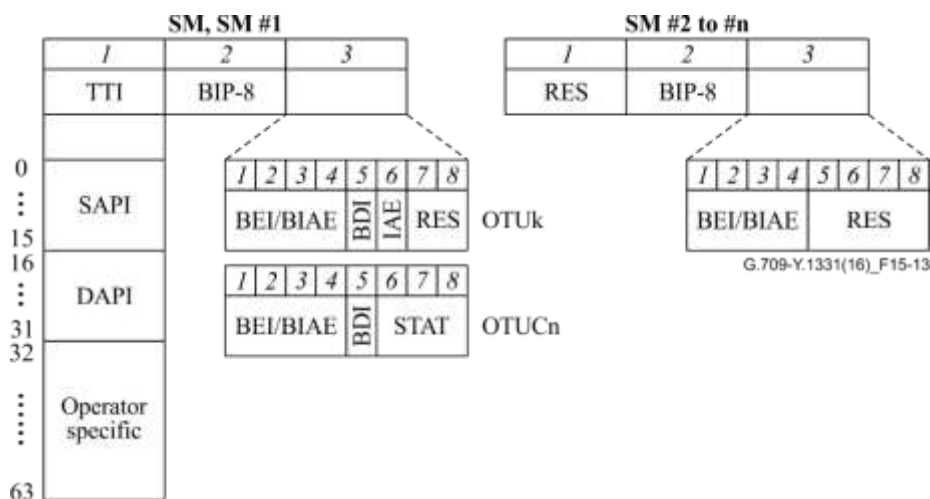
### 15.7.1 OTU overhead location

The OTU overhead location is shown in Figures 15-12 and 15-13.

The OTUk contains one instance of OTU overhead. The OTUCn contains n instances of OTU overhead, numbered 1 to n (OTU OH #1 to OTU OH #n).



**Figure 15-12 – OTU overhead**



**Figure 15-13 – OTU section monitoring overhead**

## 15.7.2 OTU overhead definition

### 15.7.2.1 OTU section monitoring (SM) overhead

One field of OTU section monitoring (SM) overhead is defined in row 1, columns 8 to 10 to support section monitoring.

The OTU<sub>k</sub>, OTU<sub>25</sub> and OTU<sub>50</sub> contain one instance of OTU SM overhead. The OTU<sub>Cn</sub> contains *n* instances of the OTU SM overhead, numbered 1 to *n* (SM #1 to SM #*n*).

The SM and SM #1 field contains the following subfields (see Figure 15-13):

- trail trace identifier (TTI);
- bit interleaved parity (BIP-8);
- backward defect indication (BDI);
- backward error indication and backward incoming alignment error (BEI/BIAE);
- incoming alignment error (IAE);
- status bits indicating the presence of an incoming alignment error or a maintenance signal (STAT);
- bits reserved for future international standardization (RES).

The SM #2 to #*n* fields contain the following subfields (see Figure 15-13):

- bit interleaved parity (BIP-8);
- backward error indication and backward incoming alignment error (BEI/BIAE);
- bits reserved for future international standardization (RES).

#### 15.7.2.1.1 OTU SM trail trace identifier (TTI)

For section monitoring, a one-byte trail trace identifier (TTI) overhead is defined to transport the 64-byte TTI signal specified in clause 15.2 or a discovery message as specified in [ITU-T G.7714.1].

The OTU<sub>k</sub>, OTU<sub>25</sub> and OTU<sub>50</sub> and OTU<sub>Cn</sub> contain one instance of OTU TTI overhead.

The 64-byte TTI signal shall be aligned with the OTU multiframe (see clause 15.6.2.2) and transmitted four times per multiframe. Byte 0 of the 64-byte TTI signal shall be present at OTU multiframe positions 0000 0000 (0x00), 0100 0000 (0x40), 1000 0000 (0x80) and 1100 0000 (0xC0).

### 15.7.2.1.2 OTU SM error detection code (BIP-8)

For section monitoring, a one-byte error detection code signal is defined in the OTU SM overhead. This byte provides a bit interleaved parity-8 (BIP-8) code.

NOTE – The notation *BIP-8* refers only to the number of BIP bits and not to the EDC usage (i.e., what quantities are counted). For definition of BIP-8 refer to BIP-X definition in [ITU-T G.707].

The OTU BIP-8 is computed over the bits in the OPU (columns 15 to 3824) area of OTU frame *i*, and inserted in the OTU BIP-8 overhead location in OTU frame *i+2* (see Figure 15-14).

The OTU<sub>k</sub>, OTU<sub>25</sub> and OTU<sub>50</sub> contain one instance of OTU BIP-8 overhead. The OTU<sub>Cn</sub> contains *n* instances of the OTU BIP-8 overhead, numbered 1 to *n* (BIP-8 #1 to BIP-8 #*n*).

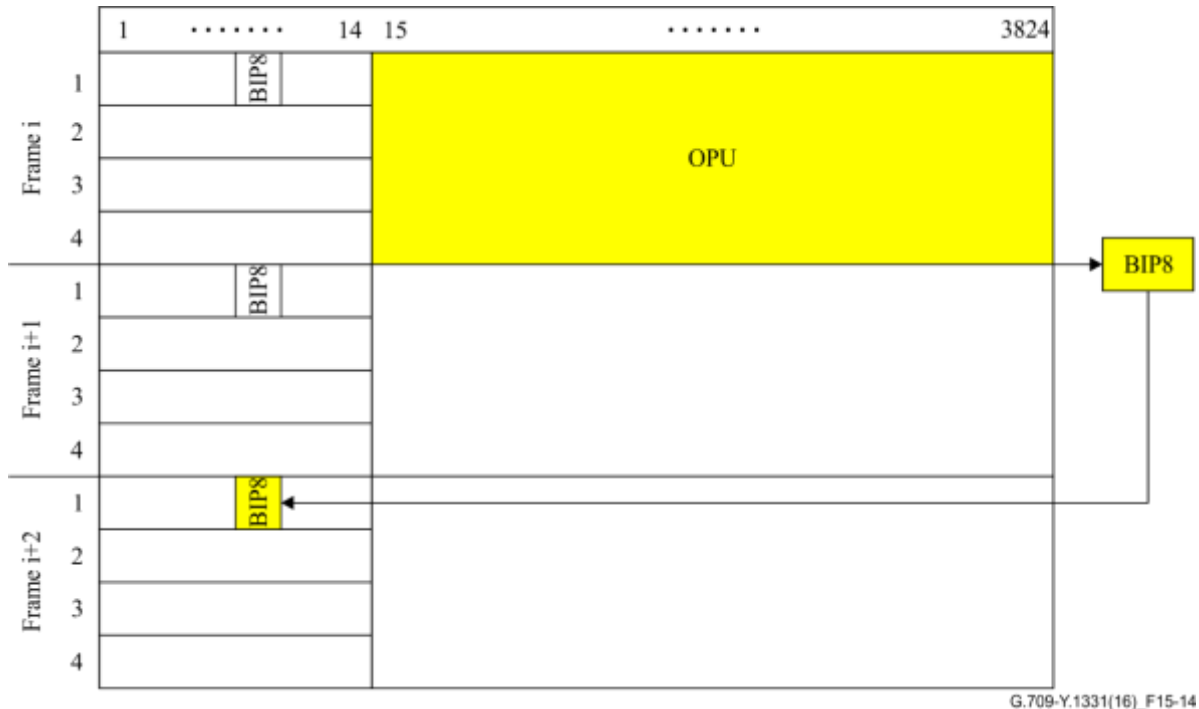


Figure 15-14 – OTU SM BIP-8 computation

### 15.7.2.1.3 OTU SM backward defect indication (BDI)

For section monitoring, a single-bit backward defect indication (BDI) signal is defined to convey the signal fail status detected in a section termination sink function in the upstream direction.

BDI is set to "1" to indicate an OTU backward defect indication; otherwise, it is set to "0".

The OTU<sub>k</sub>, OTU<sub>25</sub> and OTU<sub>50</sub> and OTU<sub>Cn</sub> contain one instance of OTU BDI overhead.

### 15.7.2.1.4 OTU SM backward error indication and backward incoming alignment error (BEI/BIAE)

For section monitoring, a four-bit backward error indication (BEI) and backward incoming alignment error (BIAE) signal is defined. This signal is used to convey in the upstream direction the count of interleaved-bit blocks that have been detected in error by the corresponding OTU section monitoring sink using the BIP-8 code. It is also used to convey in the upstream direction an incoming alignment error (IAE) condition that is detected in the corresponding OTU section monitoring sink in the IAE overhead.

During an IAE condition the code "1011" is inserted into the BEI/BIAE field and the error count is ignored. Otherwise the error count (0-8) is inserted into the BEI/BIAE field. The remaining six possible values represented by these four bits can only result from some unrelated condition and shall be interpreted as zero errors (see Table 15-1) and BIAE not active.

The OTUk, OTU25 and OTU50 contain one instance of OTU BEI/BIAE overhead. The OTUCn contains n instances of the OTU BEI/BIAE overhead, numbered 1 to n (BEI/BIAE #1 to BEI/BIAE #n).

NOTE – The BIAE indication of an OTUCn is transported n times (ie. in OTUC SM # 1 to SM #n) and detected in OTUC SM #1 only.

**Table 15-1 – OTU SM BEI/BIAE interpretation**

<b>OTU SM BEI/BIAE bits</b>	<b>1 2 3 4</b>	<b>BIAE</b>	<b>BIP violations</b>
	0 0 0 0	false	0
	0 0 0 1	false	1
	0 0 1 0	false	2
	0 0 1 1	false	3
	0 1 0 0	false	4
	0 1 0 1	false	5
	0 1 1 0	false	6
	0 1 1 1	false	7
	1 0 0 0	false	8
	1 0 0 1, 1 0 1 0	false	0
	1 0 1 1	true	0
	1 1 0 0 to 1 1 1 1	false	0

#### **15.7.2.1.5 OTUk, OTU25 and OTU50 SM incoming alignment error overhead (IAE)**

A single-bit incoming alignment error (IAE) signal is defined to allow the S-CMEP ingress point to inform its peer S-CMEP egress point that an alignment error in the incoming signal has been detected.

IAE is set to "1" to indicate a frame alignment error, otherwise it is set to "0".

The S-CMEP egress point may use this information to suppress the counting of bit errors, which may occur as a result of a frame phase change of the OTUk, OTU25, OTU50 at the ingress of the section.

#### **15.7.2.1.6 OTU SM reserved overhead (RES)**

For section monitoring of the OTUk, OTU25 and OTU50, two bits in the SM overhead are reserved (RES) for future international standardization. They are set to "00".

For section monitoring of the OTUCn, 12 bits in the SM overhead in the OTU frame structures #2 to #n are reserved for future international standardization. The value of these bits is set to "0".

#### **15.7.2.1.7 OTUCn SM status (STAT)**

For section monitoring, three bits are defined as status bits (STAT). They indicate the presence of a maintenance signal or if there is an incoming alignment error at the source S-CMEP, (see Table 15-2).

**Table 15-2 – OTUCn SM status interpretation**

bits	SM byte 3 6 7 8	Status
	0 0 0	Reserved for future international standardization
	0 0 1	In use without IAE
	0 1 0	In use with IAE
	0 1 1	Reserved for future international standardization
	1 0 0	Reserved for future international standardization <u>(Note)</u>
	1 0 1	Reserved for future international standardization
	1 1 0	Reserved for future international standardization
	1 1 1	Maintenance signal: OTUCn-AIS
<u>NOTE – This bit pattern may appear temporarily due to the presence of the FlexO SquelchText pattern. Refer to [ITU-T G.709.1].</u>		

A S-CMEP ingress point sets these bits to either "001" to indicate to its peer S-CMEP egress point that there is no incoming alignment error (IAE), or to "010" to indicate that there is an incoming alignment error.

The S-CMEP egress point may use this information to suppress the counting of bit errors, which may occur as a result of a frame phase change of the ODUCn at the ingress of the section.

### 15.7.2.2 OTU general communication channel 0 (GCC0)

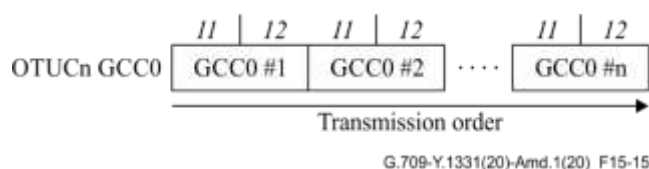
Two bytes are allocated in the OTU overhead to support a general communications channel or a discovery channel as specified in [ITU-T G.7714.1] between OTU termination points.

This general communication channel is a clear channel and any format specification is outside of the scope of this Recommendation. These bytes are located in row 1, columns 11 and 12 of the OTU overhead.

The OTUk, OTU25 and OTU50 contain one instance of OTU GCC0 overhead. The OTUCn contains n instances of the OTU GCC0 overhead, numbered 1 to n (GCC0 #1 to GCC0 #n).

The GCC0 #1 to #n overhead are combined to provide one communication channel as illustrated in Figure 15-15.

NOTE – For vendor specific interfaces it is an option not to combine the GCC0 #1 to #n and instead use only the first GCC0 (GCC0 #1) as communication channel. GCC0 #2 to #n are not used.



**Figure 15-15 – OTUCn GCC0 transmission order**

### 15.7.2.3 OTU reserved overhead (RES)

One byte of the OTU overhead in OTU frame structure #1 is reserved for future international standardization. This byte is located in row 1, column 14. This byte is set to all-0s.



Two bytes of the OTU overhead in OTU frame structures #2 to #n are reserved for future international standardization. These bytes are located in the OTU overhead in row 1, columns 13 and 14. These bytes are set to all-0s.

#### 15.7.2.4 OTU OTN synchronisation message channel (OSMC)

For synchronisation purposes, one byte is defined in the OTU overhead as an OTN synchronisation message channel to transport SSM, eSSM and PTP messages within SOTU and MOTU interfaces. The OSMC bandwidth is listed in Table 15-3.

The OTUk, OTU25 and OTU50 contain one instance of OTU OSMC overhead.

NOTE 1 – Support of OTU OSMC in an OTN interface is optional.

NOTE 2 – Equipment designed prior to Edition 5.0 of this Recommendation may not be able to support OTU OSMC via their OTN point-to-point interfaces.

NOTE 3 – OTN interfaces with vendor specific application identifiers may support an OSMC function. The encapsulation of the messages and overhead location are then vendor specific.

NOTE 4 – Equipment designed prior to Edition 6.0 of this Recommendation may not be able to support OTU OSMC via their OTN optical networking interfaces.

**Table 15-3 – OSMC bandwidth**

OTUk	OSMC Bandwidth (kbit/s)
<u>OTU0</u>	<u>81.339</u>
OTU1	163.361
OTU2	656.203
OTU3	2,635.932
OTU4	6,851.101
OTU25	1,726.576
OTU50	3,453.153

The SSM, eSSM and PTP messages are encapsulated into GFP-F frames as specified into [ITU-T G.7041]. PTP event messages are timestamped and after encapsulation into GFP-F frames inserted into the OSMC as specified in clause 15.7.2.4.1. GFP-F encapsulated SSM and eSSM messages (and PTP non-event messages) are inserted into the OSMC at the earliest opportunity. GFP Idle frames may be inserted between successive GFP frames.

The mapping of generic framing procedure (GFP) frames is performed by aligning the byte structure of every GFP frame with the byte of the OSMC overhead field. Since the GFP frames are of variable length and longer than one byte, a frame crosses the OTUk (k=0,1,2,3,4), OTU25 or OTU50 frame boundary.

##### 15.7.2.4.1 Generation of event message timestamps

###### 15.7.2.4.1.1 OTN interface event message timestamp point

The OTN interface message timestamp point [ITU-T G.8260] for a PTP event message transported over the OSMC shall be the X-frame multiframe event preceding the beginning of the GFP frame in which the PTP event message is carried. See Figure 15-16. Since the GFP frames may be longer than X-4 bytes, a frame may cross the X-frame multiframe boundary. The X-frame multiframe contains frames numbered 0, 1, ..., X-1.

### 15.7.2.4.1.2 Event timestamp generation

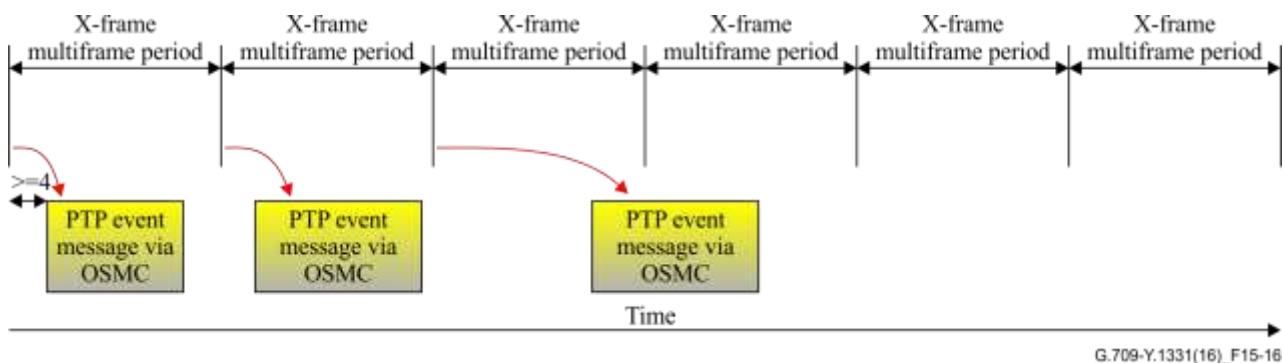
All PTP event messages are timestamped on egress and ingress OTN interfaces. The timestamp shall be the time at which the event message timestamp point passes the reference plane [ITU-T G.8260] marking the boundary between the PTP node (i.e., OTN node) and the network.

#### **OTUk, OTU25 and OTU50**

Event message timestamps are generated every X-frame multiframe period at the OTUk, OTU25 and OTU50 Access Point. X is 64 for k = 0,1 and 256 for k = 2,3,4 and OTU25 and OTU50.

The first byte of a GFP(PTP event message) frame is inserted into the OTUk, OTU25 or OTU50 OSMC between 4 and X-1 frames after the X-frame multiframe boundary.

NOTE 1 – The first byte of a GFP(PTP event message) frame is not inserted into the OTUk, OTU25 or OTU50 OSMC in frame 0...3 of the X-frame multiframe.



**Figure 15-16 – Timing diagram example for OTUk**

NOTE 2 – This time synchronization over OTN interface implementation does not generate event message timestamps using a point other than the message timestamp point [ITU-T G.8260].

In this time synchronization over OTN interface implementation, the timestamps are generated at a point removed from the reference plane. Furthermore, the time offset from the reference plane is likely to be different for inbound and outbound event messages. To meet the requirement of this subclause, the generated timestamps should be corrected for these offsets. Figure 19 in [b-IEEE 1588] illustrates these offsets. Based on this model, the appropriate corrections are as follows:

$$\langle \text{egressTimestamp} \rangle = \langle \text{egressMeasuredTimestamp} \rangle + \text{egressLatency}$$

$$\langle \text{ingressTimestamp} \rangle = \langle \text{ingressMeasuredTimestamp} \rangle - \text{ingressLatency}$$

where the actual timestamps  $\langle \text{egressTimestamp} \rangle$  and  $\langle \text{ingressTimestamp} \rangle$  measured at the reference plane are computed from the detected, i.e., measured, timestamps by their respective latencies. Failure to make these corrections results in a time offset between the slave and master clocks.

### 15.7.3 OTUkV overhead

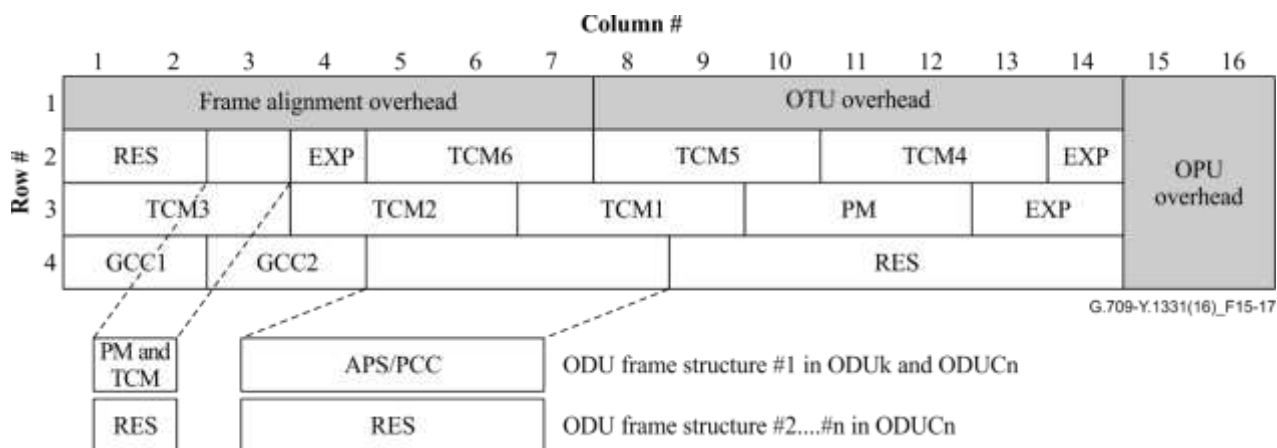
The functionally standardized OTUkV frame should support, as a minimum capability, section monitoring functionality comparable to the OTUk section monitoring (see clause 15.7.2.1) with a trail trace identifier as specified in clause 15.2. Further specification of this overhead is outside the scope of this Recommendation.

## 15.8 ODU OH description

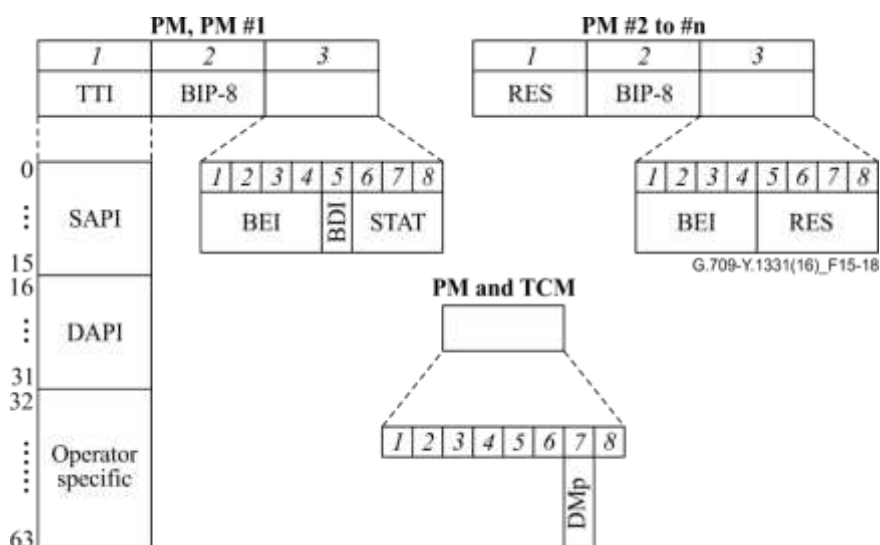
### 15.8.1 ODU OH location

The ODU overhead location is shown in Figures 15-17, 15-18 and 15-19.

The ODUk contains one instance of ODU overhead. The ODUCn contains n instances of ODU overhead, numbered 1 to n (ODU OH #1 to ODU OH #n).



**Figure 15-17 – ODU overhead**



**Figure 15-18 – ODU path monitoring overhead**

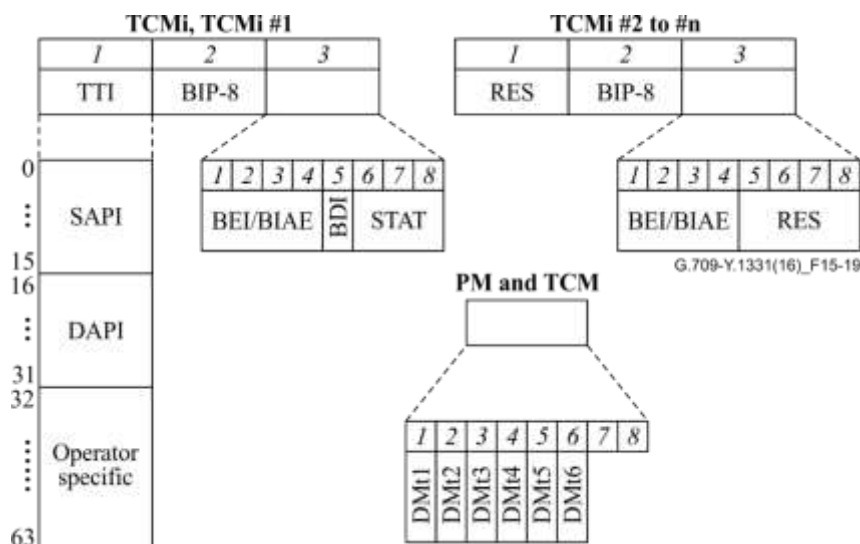


Figure 15-19 – ODU tandem connection monitoring #i overhead

## 15.8.2 ODU OH definition

### 15.8.2.1 ODU path monitoring (PM) overhead

One field of an ODU path monitoring overhead (PM) is defined in row 3, columns 10 to 12 to support path monitoring and one additional bit of path monitoring is defined in row 2, column 3, bit 7.

The ODU<sub>k</sub> contains one instance of ODU PM overhead. The ODU<sub>Cn</sub> contains n instances of the ODU PM overhead, numbered 1 to n (PM #1 to PM #n).

The PM and PM #1 field contains the following subfields (see Figure 15-18):

- trail trace identifier (TTI);
- bit interleaved parity (BIP-8);
- backward defect indication (BDI);
- backward error indication (BEI);
- status bits indicating the presence of a maintenance signal (STAT).

The PM #2 to #n fields contain the following subfields (see Figure 15-18):

- bit interleaved parity (BIP-8)
- backward error indication (BEI)
- reserved (RES).

The PM&TCM field contains the following PM subfield (see Figure 15-18):

- path delay measurement (DMp).

For the case of ODU<sub>k</sub>, the content of the PM field, except the STAT subfield, will be undefined (pattern will be all-1s, 0110 0110 or 0101 0101 repeating) during the presence of a maintenance signal (e.g., ODU-AIS, ODU-OCI, ODU-LCK). The content of the PM&TCM field will be undefined (pattern will be all-1s, 0110 0110 or 0101 0101 repeating) during the presence of a maintenance signal. Refer to clause 16.5.

For the case of ODU<sub>Cn</sub>, the content of the PM field, except the STAT subfield, will be undefined (pattern will be all-1s or 0101 0101 repeating) during the presence of a maintenance signal (e.g., ODU<sub>Cn</sub>-AIS, ODU<sub>Cn</sub>-LCK). Refer to clause 16.5.

### 15.8.2.1.1 ODU PM trail trace identifier (TTI)

For path monitoring, a one-byte trail trace identifier (TTI) overhead is defined to transport the 64-byte TTI signal specified in clause 15.2 or a discovery message as specified in [ITU-T G.7714.1].

The ODU<sub>k</sub> and ODU<sub>Cn</sub> contain one instance of ODU PM TTI overhead.

The 64-byte TTI signal shall be aligned with the ODU multiframe (see clause 15.6.2.2) and transmitted four times per multiframe. Byte 0 of the 64-byte TTI signal shall be present at ODU multiframe positions 0000 0000 (0x00), 0100 0000 (0x40), 1000 0000 (0x80) and 1100 0000 (0xC0).

### 15.8.2.1.2 ODU PM error detection code (BIP-8)

For path monitoring, a one-byte error detection code signal is defined in the ODU PM overhead. This byte provides a bit interleaved parity-8 (BIP-8) code.

NOTE – The notation BIP-8 refers only to the number of BIP bits and not to the EDC usage (i.e., what quantities are counted). For definition of BIP-8, refer to the BIP-X definition in [ITU-T G.707].

Each ODU BIP-8 is computed over the bits in the OPU (columns 15 to 3824) area of ODU frame *i*, and inserted in the ODU PM BIP-8 overhead location in the ODU frame *i+2* (see Figure 15-20).

The ODU<sub>k</sub> contains one instance of ODU PM BIP-8 overhead. The ODU<sub>Cn</sub> contains *n* instances of the ODU PM BIP-8 overhead, numbered 1 to *n* (BIP-8 #1 to BIP-8 #*n*).

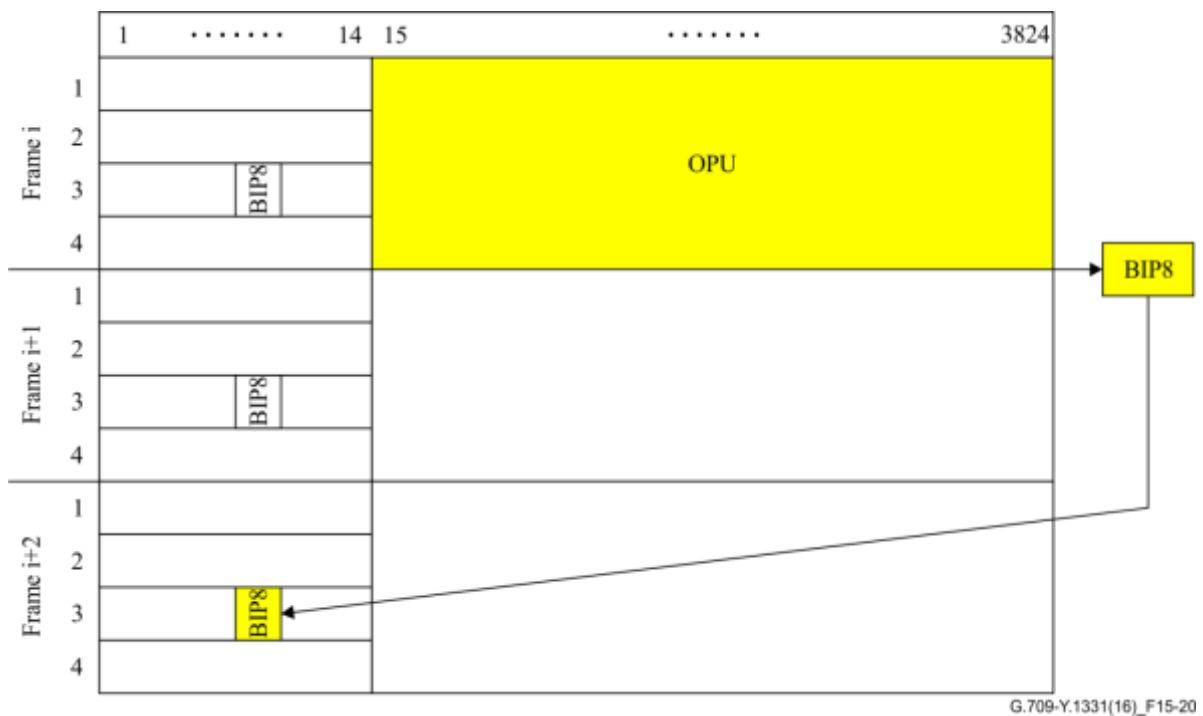


Figure 15-20 – ODU PM BIP-8 computation

### 15.8.2.1.3 ODU PM backward defect indication (BDI)

For path monitoring, a single-bit backward defect indication (BDI) signal is defined to convey the signal fail status detected in a path termination sink function in the upstream direction.

BDI is set to "1" to indicate an ODU backward defect indication, otherwise it is set to "0".

The ODU<sub>k</sub> and ODU<sub>Cn</sub> contain one instance of ODU PM BDI overhead.

### 15.8.2.1.4 ODU PM backward error indication (BEI)

For path monitoring, a four-bit backward error indication (BEI) signal is defined to convey in the upstream direction the count of interleaved-bit blocks that have been detected in error by the

corresponding ODU path monitoring sink using the BIP-8 code. This count has nine legal values, namely 0-8 errors. The remaining seven possible values represented by these four bits can only result from some unrelated condition and shall be interpreted as zero errors (see Table 15-2).

The ODU<sub>k</sub> contains one instance of ODU PM BEI overhead. The ODU<sub>Cn</sub> contains n instances of the ODU PM BEI overhead, numbered 1 to n (BEI #1 to BEI #n).

**Table 15-4 – ODU PM BEI interpretation**

bits	ODU PM BEI 1 2 3 4	BIP violations
	0 0 0 0	0
	0 0 0 1	1
	0 0 1 0	2
	0 0 1 1	3
	0 1 0 0	4
	0 1 0 1	5
	0 1 1 0	6
	0 1 1 1	7
	1 0 0 0	8
	1 0 0 1 to 1 1 1 1	0

#### 15.8.2.1.5 ODU PM status (STAT)

For path monitoring, three bits are defined as status bits (STAT). They indicate the presence of a maintenance signal (see Table 15-3).

A P-CMEP sets these bits to "001".

The ODU<sub>k</sub> and ODU<sub>Cn</sub> contain one instance of ODU PM STAT overhead.

**Table 15-5 – ODU PM status interpretation**

bits	PM byte 3 6 7 8	Status
	0 0 0	Reserved for future international standardization
	0 0 1	Normal path signal
	0 1 0	Reserved for future international standardization
	0 1 1	Reserved for future international standardization
	1 0 0	Reserved for future international standardization <a href="#">(Note)</a>
	1 0 1	Maintenance signal: ODU-LCK
	1 1 0	ODU <sub>k</sub> : Maintenance signal: ODU-OCI ODU <sub>Cn</sub> : Reserved for future international standardization
	1 1 1	Maintenance signal: ODU-AIS
<p><a href="#">NOTE – This bit pattern may appear temporarily due to the presence of the FlexO SquelchText pattern. Refer to [ITU-T G.709.1].</a></p>		

### 15.8.2.1.6 ODU PM delay measurement (DMp)

For ODU path monitoring, a one-bit path delay measurement (DMp) signal is defined to convey the start of the delay measurement test.

The ODU<sub>k</sub> and ODU<sub>Cn</sub> contain one instance of ODU PM DMp overhead.

The DMp signal consists of a constant value (0 or 1) that is inverted at the beginning of a two-way delay measurement test. The transition from 0→1 in the sequence ...0000011111..., or the transition from 1→0 in the sequence ...1111100000... represents the path delay measurement start point. The new value of the DMp signal is maintained until the start of the next delay measurement test.

This DMp signal is inserted by the DMp originating P-CMEP and sent to the far-end P-CMEP. This far-end P-CMEP loops back the DMp signal towards the originating P-CMEP. The originating P-CMEP measures the number of frame periods between the moment the DMp signal value is inverted and the moment this inverted DMp signal value is received back from the far-end P-CMEP. The receiver should apply a persistency check on the received DMp signal to be tolerant for bit errors emulating the start of delay measurement indication. The additional frames that are used for such persistency checking should not be added to the delay frame count. The looping P-CMEP should loop back each received DMp bit within approximately 100 µs.

Refer to [ITU-T G.798] for the specific path delay measurement process specifications.

NOTE 1 – Path delay measurements can be performed on-demand, to provide the momentary two-way transfer delay status, and pro-active, to provide 15-minute and 24-hour two-way transfer delay performance management snapshots.

NOTE 2 – Equipment designed according to the 2008 or earlier versions of this Recommendation may not be capable of supporting this path delay monitoring. For such equipment, the DMp bit is a bit reserved for future international standardization and set to zero.

NOTE 3 – This process measures a round trip delay. The one way delay may not be half of the round trip delay in the case where the transmit and receive directions of the ODU network connection are of unequal lengths (e.g., in networks deploying unidirectional protection switching).

### 15.8.2.1.7 ODU PM reserved overhead (RES)

For path monitoring of the OTUC<sub>n</sub>, 12 bits in the PM overhead in the ODU OH #2 to #n are reserved for future international standardization. The value of these bits is set to "0".

The ODU<sub>k</sub> contains no ODU PM RES overhead. The ODU<sub>Cn</sub> contains n-1 instances of the ODU PM RES overhead.

### 15.8.2.2 ODU tandem connection monitoring (TCM) overhead

Six fields of an ODU tandem connection monitoring (TCM) overhead are defined in row 2, columns 5 to 13 and row 3, columns 1 to 9 of the ODU overhead; and six additional bits of tandem connection monitoring are defined in row 2, column 3, bits 1 to 6.

TCM supports monitoring of ODU<sub>k</sub> connections for one or more of the following network applications (refer to [ITU-T G.805], [ITU-T G.872], [ITU-T G.873.2] and [ITU-T G.7714.1]):

- optical UNI-to-UNI tandem connection monitoring; monitoring the ODU connection through the public transport network (from public network ingress network termination to egress network termination);
- optical NNI-to-NNI tandem connection monitoring; monitoring the ODU connection through the network of a network operator (from operator network ingress network termination to egress network termination);
- sublayer monitoring for linear 1+1, 1:1 and 1:n ODU<sub>k</sub> subnetwork connection protection switching, to determine the signal fail and signal degrade conditions;

- sublayer monitoring for ODUk shared ring protection (SRP-1) protection switching as specified in [ITU-T G.873.2], to determine the signal fail and signal degrade conditions;
- sublayer monitoring for ODUk connection passing through two or more concatenated ODUk link connections (supported by back-to-back OTU trails), to provide a discovery message channel as specified in [ITU-T G.7714.1];
- monitoring an ODUk tandem connection for the purpose of detecting a signal fail or signal degrade condition in a switched ODUk connection, to initiate automatic restoration of the connection during fault and error conditions in the network;
- monitoring an ODUk tandem connection for, e.g., fault localization or verification of delivered quality of service.

TCM supports monitoring of segments of ODUCn connections which span multiple OTSiA subnetworks. The ODUCn TC-CMEP are located on OTUCn interface ports at the edge of OTSiA subnetworks and/or on OTUCn interface ports in ODUCn terminating nodes (e.g., in ODUk cross connects).

The six TCM fields are numbered TCM1, TCM2, ..., TCM6.

The ODUk contains one instance of ODU TCM1 to TCM6 overhead. The ODUCn contains n instances of the ODU TCM1 to TCM6 overhead, numbered 1 to n (TCMi #1 to TCMi #n).

Each TCMi and TCMi #1 field contains the following subfields (see Figure 15-19):

- trail trace identifier (TTI);
- bit interleaved parity 8 (BIP-8);
- backward defect indication (BDI);
- backward error indication and backward incoming alignment error (BEI/BIAE);
- status bits indicating the presence of a TCM overhead, incoming alignment error, or a maintenance signal (STAT).

Each TCMi #2 to #n field contains the following subfields (see Figure 15-19):

- bit interleaved parity 8 (BIP-8);
- backward error indication and backward incoming alignment error (BEI/BIAE);
- reserved (RES).

The PMandTCM field contains the following TCM subfields (see Figure 15-19):

- tandem connection delay measurement (DMti, i=1 to 6).

For the case of ODUk, the content of the TCM fields, except the STAT subfield, will be undefined (pattern will be all-1s, 0110 0110 or 0101 0101 repeating) during the presence of a maintenance signal (e.g., ODUk-AIS, ODUk-OCI, ODUk-LCK). The content of the PM&TCM field will be undefined (pattern will be all-1s, 0110 0110 or 0101 0101 repeating) during the presence of a maintenance signal. Refer to clause 16.5.

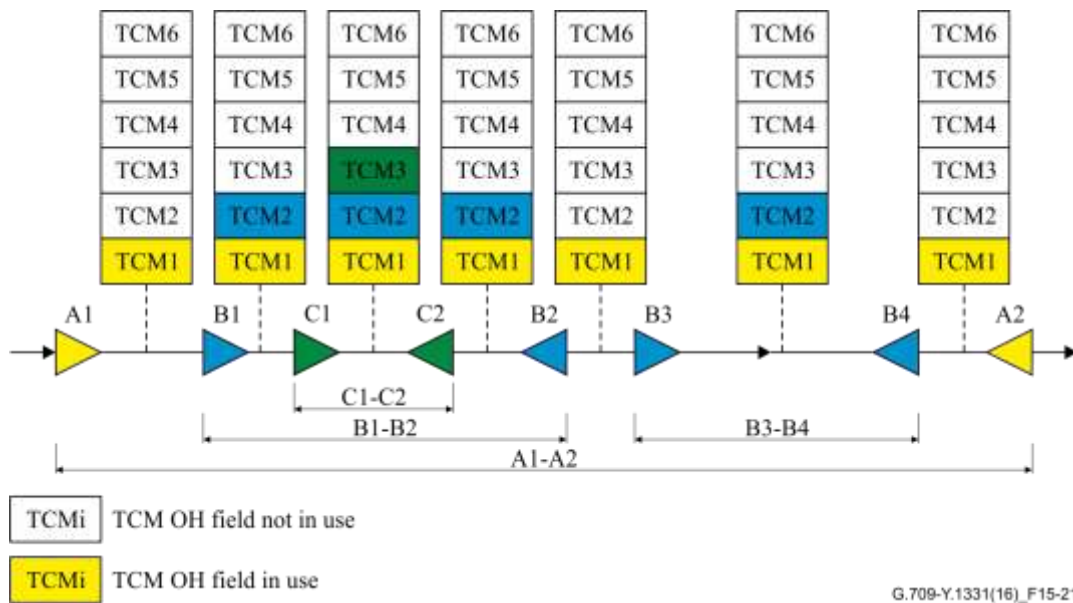
For the case of ODUCn, the content of the TCM field groups, except the STAT subfield, will be undefined (pattern will be all-1s or 0101 0101 repeating) during the presence of a maintenance signal (e.g., ODUCn-AIS, ODUCn-LCK). The content of the PMand TCM field will be undefined (pattern will be all-1s or 0101 0101 repeating) during the presence of a maintenance signal. Refer to clause 6.5.

A TCM field and PM&TCM bit is assigned to a monitored connection as described in clause 15.8.2.2.6. The number of monitored connections along an ODU trail may vary between 0 and 6. These monitored connections may be nested, cascaded or both. Nesting and cascading are the default operational configurations. Overlapping is an additional configuration for testing purposes only. Overlapped monitored connections must be operated in a non-intrusive mode

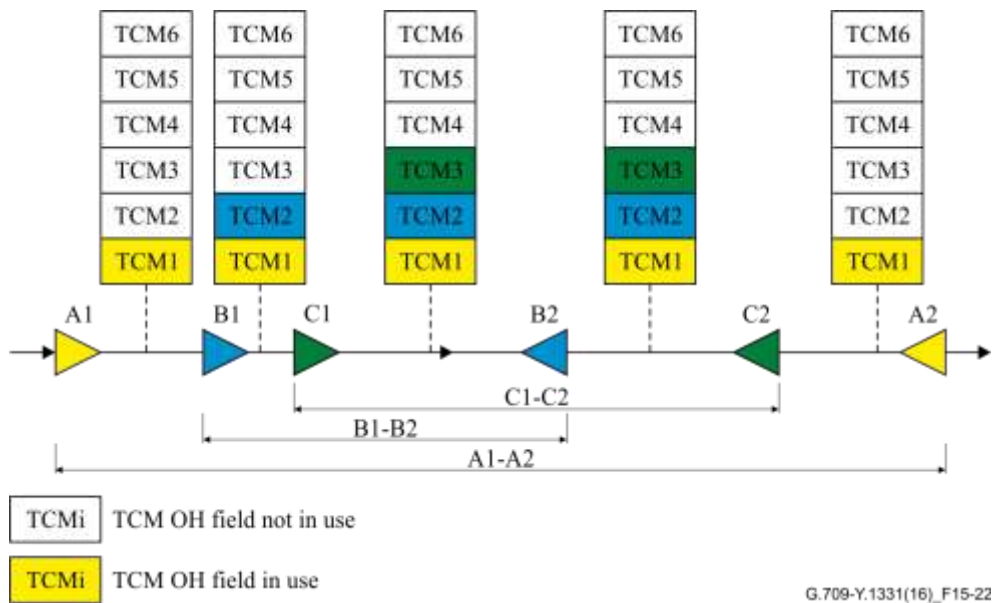


in which the maintenance signals ODU-AIS and ODU-LCK are not generated. For the case where one of the endpoints in an overlapping monitored connection is located inside an SNC protected domain while the other endpoint is located outside the protected domain, the SNC protection should be forced to working when the endpoint of the overlapping monitored connection is located on the working connection, and forced to protection when the endpoint is located on the protection connection.

Nesting and cascading configurations are shown in Figure 15-21. Monitored connections A1-A2/B1-B2/C1-C2 and A1-A2/B3-B4 are nested, while B1-B2/B3-B4 are cascaded. Overlapping is shown in Figure 15-22 (B1-B2 and C1-C2).



**Figure 15-21 – Example of nested and cascaded ODU monitored connections**



**Figure 15-22 – Example of overlapping ODU monitored connections**

### 15.8.2.2.1 ODU TCM trail trace identifier (TTI)

For each tandem connection monitoring field, one byte of overhead is allocated for the transport of the 64-byte trail trace identifier (TTI) specified in clause 15.2 or a discovery message as specified in [ITU-T G.7714.1] for TCM6.

The ODU<sub>k</sub> and ODU<sub>Cn</sub> contain one instance of ODU TTI overhead.

The 64-byte TTI signal shall be aligned with the ODU multiframe (see clause 15.6.2.2) and transmitted four times per multiframe. Byte 0 of the 64-byte TTI signal shall be present at ODU multiframe positions 0000 0000 (0x00), 0100 0000 (0x40), 1000 0000 (0x80) and 1100 0000 (0xC0).

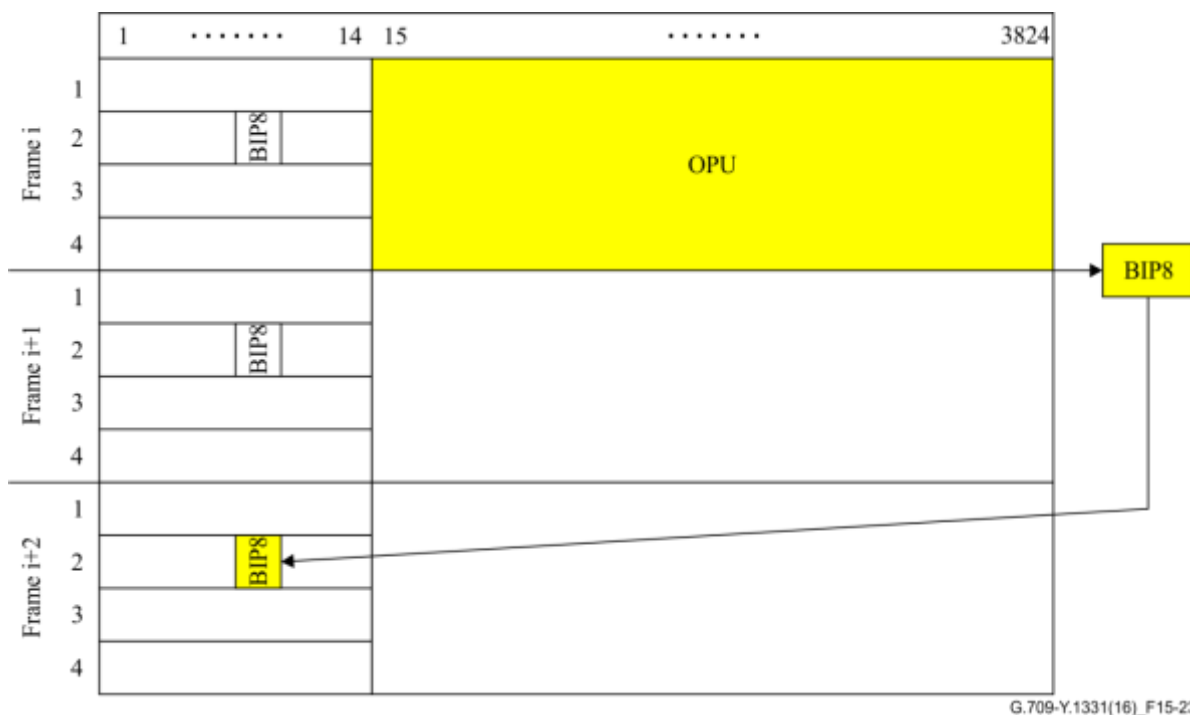
**15.8.2.2.2 ODU TCM error detection code (BIP-8)**

For each tandem connection monitoring field, a one-byte error detection code signal is defined in the ODU TCM<sub>i</sub> overhead. This byte provides a bit interleaved parity-8 (BIP-8) code.

NOTE – The notation *BIP-8* refers only to the number of BIP bits, and not to the EDC usage (i.e., what quantities are counted). For definition of BIP-8 refer to the BIP-X definition in [ITU-T G.707].

Each ODU TCM BIP-8 is computed over the bits in the OPU (columns 15 to 3824) area of ODU frame *i*, and inserted in the ODU TCM BIP-8 overhead location (associated with the tandem connection monitoring level) in ODU frame *i*+2 (see Figure 15-23).

The ODU<sub>k</sub> contains one instance of ODU TCM<sub>i</sub> BIP-8 overhead. The ODU<sub>Cn</sub> contains *n* instances of the ODU TCM<sub>i</sub> BIP-8 overhead, numbered 1 to *n* (BIP-8 #1 to BIP-8 #*n*).



**Figure 15-23 – ODU TCM BIP-8 computation**

**15.8.2.2.3 ODU TCM backward defect indication (BDI)**

For each tandem connection monitoring field, a single-bit backward defect indication (BDI) signal is defined to convey the signal fail status detected in a tandem connection termination sink function in the upstream direction.

BDI is set to "1" to indicate an ODU<sub>k</sub> backward defect indication; otherwise, it is set to "0".

The ODU<sub>k</sub> and ODU<sub>Cn</sub> contain one instance of ODU TCM<sub>i</sub> BDI overhead.

**15.8.2.2.4 ODU TCM backward error indication (BEI) and backward incoming alignment error (BIAE)**

For each tandem connection monitoring field, a 4-bit backward error indication (BEI) and backward incoming alignment error (BIAE) signal is defined. This signal is used to convey in the upstream direction the count of interleaved-bit blocks that have been detected as being in error by the

corresponding ODU tandem connection monitoring sink using the BIP-8 code. It is also used to convey in the upstream direction an incoming alignment error (IAE) condition that is detected in the corresponding ODU tandem connection monitoring sink in the IAE overhead.

During an IAE condition the code "1011" is inserted into the BEI/BIAE field and the error count is ignored. Otherwise the error count (0-8) is inserted into the BEI/BIAE field. The remaining six possible values represented by these four bits can only result from some unrelated condition and shall be interpreted as zero errors (see Table 15-4) and BIAE not active.

The ODU<sub>k</sub> contains one instance of ODU TCM BEI/BIAE overhead. The ODU<sub>Cn</sub> contains n instances of the ODU TCM<sub>i</sub> BEI/BIAE overhead, numbered 1 to n (BEI/BIAE #1 to BEI/BIAE #n).

**Table 15-6 – ODU TCM BEI/BIAE interpretation**

<b>ODU<sub>k</sub> TCM BEI/BIAE bits</b>	<b>BIAE</b>	<b>BIP violations</b>
1 2 3 4 0 0 0 0	false	0
0 0 0 1	false	1
0 0 1 0	false	2
0 0 1 1	false	3
0 1 0 0	false	4
0 1 0 1	false	5
0 1 1 0	false	6
0 1 1 1	false	7
1 0 0 0	false	8
1 0 0 1, 1 0 1 0	false	0
1 0 1 1	true	0
1 1 0 0 to 1 1 1 1	false	0

#### 15.8.2.2.5 ODU TCM status (STAT)

For each tandem connection monitoring field, three bits are defined as status bits (STAT). They indicate the presence of a maintenance signal, if there is an incoming alignment error at the source TC-CMEP, or if there is no source TC-CMEP active (see Table 15-7).

The ODU<sub>k</sub> and ODU<sub>Cn</sub> contain one instance of ODU TCM STAT overhead.

**Table 15-7 – ODU TCM status interpretation**

<b>TCM byte 3 bits</b>	<b>Status</b>
6 7 8 0 0 0	No source TC
0 0 1	In use without IAE
0 1 0	In use with IAE
0 1 1	Reserved for future international standardization
1 0 0	Reserved for future international standardization <a href="#">(Note)</a>
1 0 1	Maintenance signal: ODU-LCK
1 1 0	ODU <sub>k</sub> : Maintenance signal: ODU <sub>k</sub> -OCI ODU <sub>Cn</sub> : Reserved for future international standardization
1 1 1	Maintenance signal: ODU-AIS

[NOTE – This bit pattern may appear temporarily due to the presence of the FlexO SquelchText pattern. Refer to \[ITU-T G.709.1\].](#)

A P-CMEP sets these bits to "000".

A TC-CMEP ingress point sets these bits to either "001" to indicate to its peer TC-CMEP egress point that there is no incoming alignment error (IAE), or to "010" to indicate that there is an incoming alignment error.

The TC-CMEP egress point may use this information to suppress the counting of bit errors, which may occur as a result of a frame phase change of the ODU at the ingress of the tandem connection.

#### 15.8.2.2.6 TCM overhead field assignment

Each TC-CMEP will be inserting/extracting its TCM overhead from one of the 6 TCM<sub>i</sub> overhead fields and one of the 6 DMt<sub>i</sub> fields. The specific TCM<sub>i</sub>/DMt<sub>i</sub> overhead field is provisioned by the network operator, network management system or switching control plane.

At a domain interface, it is possible to provision the maximum number (0 to 6) of tandem connection levels which will be passed through the domain. The default is three. These tandem connections should use the lower TCM<sub>i</sub>/DMt<sub>i</sub> overhead fields TCM<sub>1</sub>/DMt<sub>1</sub>...TCM<sub>MAX</sub>/DMt<sub>MAX</sub>. Overhead in TCM/DMt fields beyond the maximum (TCM<sub>max+1</sub>/DMt<sub>max+1</sub> and above) may/will be overwritten in the domain.

The TCM6 overhead field is assigned to monitor an ODUk connection which is supported by two or more concatenated ODUk link connections (supported by back-to-back OTUk trails). [ITU-T G.7714.1] specifies a discovery application which uses the TCM6 TTI SAPI field as discovery message channel. [ITU-T G.873.2] specifies an ODUk SRP-1 protection application which uses the TCM6 field to monitor the status/performance of the ODUk connection between two adjacent ODUk SRP-1 nodes.

#### Example

For the case of an ODUk leased circuit, the user may have been assigned one level of TCM, the service provider one level of TCM and each network operator (having a contract with the service provider) four levels of TCM. For the case where a network operator subcontracts part of its ODUk connection to another network operator, these four levels are to be split; e.g., two levels for the subcontracting operator.

This would result in the following TCM OH allocation:

- User: TCM1/DMt1 overhead field between the two user subnetworks, and TCM1/DMt1..TCM6/DMt6 within its own subnetwork;
- Service provider (SP): TCM2/DMt2 overhead field between two UNIs;
- Network operators NO1, NO2, NO3 having contract with service provider: TCM3/DMt3, TCM4/DMt4, TCM5/DMt5, TCM6/DMt6. Note that NO2 (which is subcontracting) cannot use TCM5/DMt5 and TCM6/DMt6 in the connection through the domain of NO4;
- NO4 (having subcontract with NO2): TCM5/DMt5, TCM6/DMt6.

See Figure 15-24.

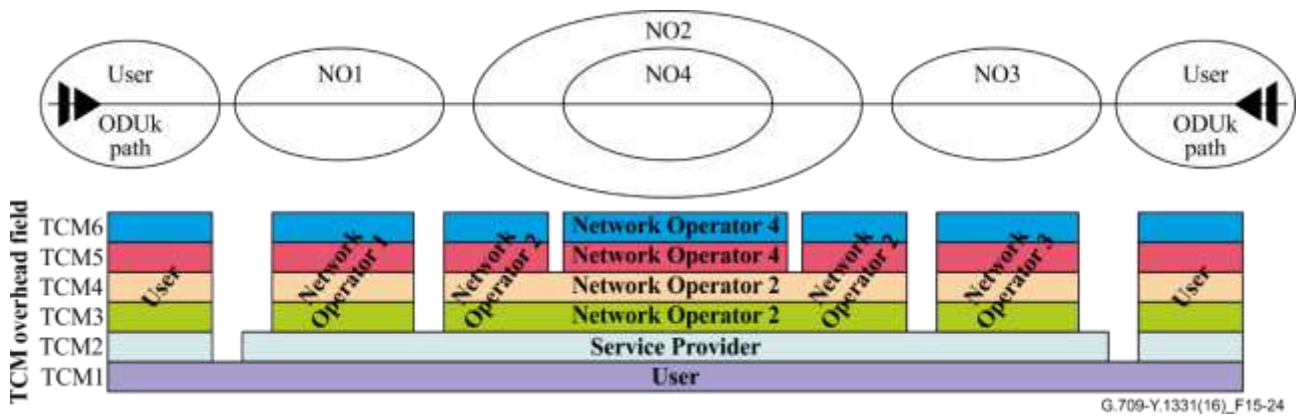


Figure 15-24 – Example of TCM overhead field assignment

#### 15.8.2.2.7 Blank clause

This clause is intentionally left blank.

#### 15.8.2.2.8 ODU TCM delay measurement (DM<sub>ti</sub>, i=1 to 6)

For ODU tandem connection monitoring, a one-bit tandem connection delay measurement (DM<sub>ti</sub>) signal is defined to convey the start of the delay measurement test.

The ODU<sub>k</sub> and ODU<sub>Cn</sub> contain one instance of ODU TCM DM<sub>ti</sub> overhead.

The DM<sub>ti</sub> signal consists of a constant value (0 or 1) that is inverted at the beginning of a two-way delay measurement test. The transition from 0→1 in the sequence ...0000011111..., or the transition from 1→0 in the sequence ...1111100000... represents the path delay measurement start point. The new value of the DM<sub>ti</sub> signal is maintained until the start of the next delay measurement test.

This DM<sub>ti</sub> signal is inserted by the DM<sub>ti</sub> originating TC-CMEP and sent to the far-end TC-CMEP. This far-end TC-CMEP loops back the DM<sub>ti</sub> signal towards the originating TC-CMEP. The originating TC-CMEP measures the number of frame periods between the moment the DM<sub>ti</sub> signal value is inverted and the moment this inverted DM<sub>ti</sub> signal value is received back from the far-end TC-CMEP. The receiver should apply a persistency check on the received DM<sub>ti</sub> signal to be tolerant for bit errors emulating the start of delay measurement indication. The additional frames that are used for such persistency checking should not be added to the delay frame count. The looping TC-CMEP should loop back each received DM<sub>ti</sub> bit within approximately 100 μs.

Refer to [ITU-T G.798] for the specific tandem connection delay measurement process specifications.

NOTE 1 – Tandem connection delay measurements can be performed on-demand, to provide the momentary two-way transfer delay status, and pro-active, to provide 15-minute and 24-hour two-way transfer delay performance management snapshots.

NOTE 2 – Equipment designed according to the 2008 or earlier versions of this Recommendation may not be capable of supporting this tandem connection delay monitoring. For such equipment, the DM<sub>ti</sub> bit is a bit reserved for future international standardization.

NOTE 3 – This process measures a round trip delay. The one way delay may not be half of the round trip delay in the case where the transmit and receive directions of the ODU<sub>k</sub> tandem connection are of unequal lengths (e.g., in networks deploying unidirectional protection switching).

#### 15.8.2.2.9 ODU TCM reserved overhead (RES)

For tandem connection monitoring, 12 bits in the TCM<sub>i</sub> overhead are reserved for future international standardization in TCM<sub>i</sub> OH #2 to #n. The value of these bits is set to "0".

The ODU<sub>k</sub> contains no ODU TCM<sub>i</sub> RES overhead. The ODU<sub>Cn</sub> contains n-1 instances of the ODU TCM<sub>i</sub> RES overhead.

### 15.8.2.3 ODU general communication channels (GCC1, GCC2)

Two fields of two bytes are allocated in the ODU overhead to support two general communications channels or two discovery channels as specified in [ITU-T G.7714.1] between any two network elements with access to the ODU frame structure (i.e., at 3R regeneration points).

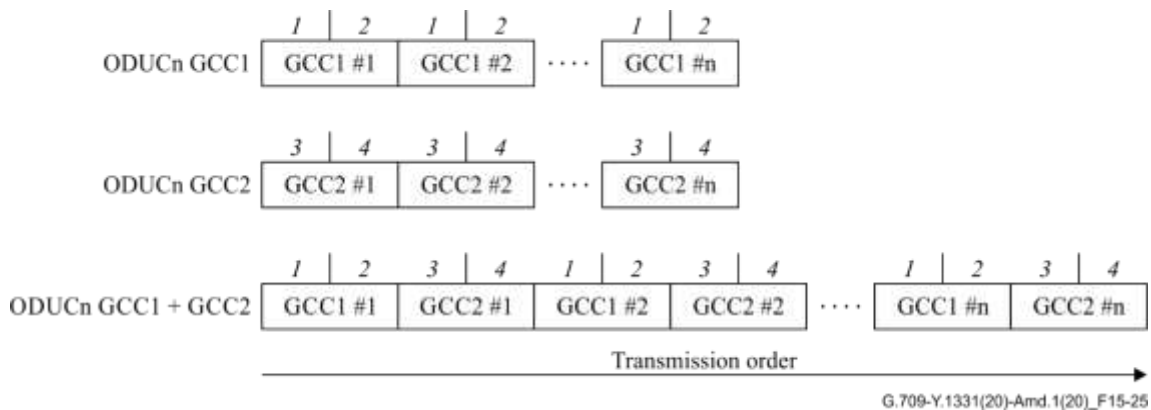
These general communication channels are clear channels and any format specification is outside of the scope of this Recommendation. The bytes for GCC1 are located in row 4, columns 1 and 2, and the bytes for GCC2 are located in row 4, columns 3 and 4 of the ODU overhead.

The ODU<sub>k</sub> contains one instance of ODU GCC1, GCC2 overhead. The ODU<sub>Cn</sub> contains n instances of the ODU GCC1, GCC2 overhead, numbered 1 to n (GCC1 #1 to GCC1 #n, GCC2 #1 to GCC2 #n).

The GCC1 #1 to #n overhead are combined to provide one communication channel as illustrated in Figure 15-25.

The GCC2 #1 to #n overhead are combined to provide another communication channel as illustrated in Figure 15-25.

The GCC1 #1 to #n plus GCC2 #1 to #n overhead may be combined to provide one communication channel as illustrated in Figure 15-25.



**Figure 15-25 – ODU<sub>Cn</sub> GCC1, GCC2 and GCC1+2 transmission order**

### 15.8.2.4 ODU automatic protection switching and protection communication channel (APS/PCC)

A four-byte ODU-APS/PCC signal is defined in row 4, columns 5 to 8 of the ODU overhead. Up to eight levels of nested APS/PCC signals may be present in this field.

The ODU<sub>k</sub> and ODU<sub>Cn</sub> contain one instance of ODU APS/PCC overhead.

For ODU<sub>k</sub>, the APS/PCC bytes in a given frame are assigned to a dedicated connection monitoring level depending on the value of MFAS as follows:

**Table 15-8 – Multiframe to allow separate APS/PCC for each monitoring level**

<b>MFAS bits</b> <b>6 7 8</b>	<b>APS/PCC channel applies to connection monitoring level</b>	<b>Protection scheme using the APS/PCC channel (Note 1)</b>
0 0 0	ODUk Path	ODUk SNC/Ne, ODUj CL-SNCG/I, Client SNC/I, ODU SRP-p
0 0 1	ODUk TCM1	ODUk SNC/S, ODUk SNC/Ns
0 1 0	ODUk TCM2	ODUk SNC/S, ODUk SNC/Ns
0 1 1	ODUk TCM3	ODUk SNC/S, ODUk SNC/Ns
1 0 0	ODUk TCM4	ODUk SNC/S, ODUk SNC/Ns
1 0 1	ODUk TCM5	ODUk SNC/S, ODUk SNC/Ns
1 1 0	ODUk TCM6	ODUk SNC/S, ODUk SNC/Ns, ODU SRP-1
1 1 1	ODUk server layer trail (Note 2)	ODUk SNC/I

NOTE 1 – An APS channel may be used by more than one protection scheme and/or protection scheme instance. In case of nested protection schemes, care should be taken when an ODUk protection is to be set up in order not to interfere with the APS channel usage of another ODUk protection on the same connection monitoring level, e.g., protection can only be activated if that APS channel of the level is not already being used.

NOTE 2 – Examples of ODUk server layer trails are an OTUk or a server ODUk (e.g., an ODU3 transporting an ODU1).

For ODU<sub>Cn</sub>, the APS/PCC signal is used to support coordination of the end points in linear (ODUk CL-SNCG/I) and ring (ODUk SRP) protection applications.

For linear protection schemes, the bit assignments for these bytes and the bit-oriented protocol are given in [ITU-T G.873.1]. Bit assignment and byte-oriented protocol for ring protection schemes are given in [ITU-T G.873.2].

#### **15.8.2.5 Blank clause**

*This clause is intentionally left blank.*

#### **15.8.2.6 ODU experimental overhead (EXP)**

Four bytes are allocated in the ODU overhead for experimental use. These bytes are located in row 2, columns 4 and 14 and row 3, columns 13 and 14 of the ODU overhead.

The ODU<sub>k</sub> contains one instance of ODU EXP overhead. The ODU<sub>Cn</sub> contains n instances of the ODU EXP overhead, numbered 1 to n (EXP #1 to EXP #n).

The use of these bytes is not subject to standardization and outside the scope of this Recommendation.

An experimental overhead is provided in the ODU OH to allow a vendor and/or a network operator within their own (sub)network to support an application, which requires an additional ODU overhead.

There is no requirement to forward the EXP overhead beyond the (sub)network; i.e., the operational span of the EXP overhead is limited to the (sub)network with the vendor's equipment, or the network of the operator.

#### **15.8.2.7 ODU reserved overhead (RES)**

For the case of an ODU<sub>k</sub>, eight bytes and one bit are reserved in the ODU overhead for future international standardization. These bytes are located in row 2, columns 1 to 2 and row 4, columns 9 to 14 of the ODU overhead. The bit is located in row 2, column 3, bit 8 of the ODU overhead. These bytes are set to all-0s.

For the case of an ODU<sub>Cn</sub>, eight bytes and one bit in the ODU OH #1 and thirteen bytes in the ODU OH #2 to #n are reserved for future international standardization. These bytes are located in row 2, columns 1 to 2 and row 4, columns 9 to 14 of the ODU OH #1 and in row 2, columns 1 to 3 and row 4, columns 5 to 14 of the ODU OH #2 to #n. The bit is located in row 2, column 3, bit 8 of the ODU OH #1. These bytes and bit are set to all-0s.

## 15.9 OPU OH description

### 15.9.1 OPU OH location

The OPU overhead consists of: payload structure identifier (PSI) including the payload type (PT), the overhead associated with the mapping of client signals into the OPU payload and the overhead associated with the hitless adjustment of ODUflex client signals. The OPU PSI and PT overhead locations are shown in Figure 15-26.

The OPU<sub>k</sub> contains one instance of OPU overhead. The OPU<sub>Cn</sub> contains n instances of OPU overhead, numbered 1 to n (OPU OH #1 to #n).

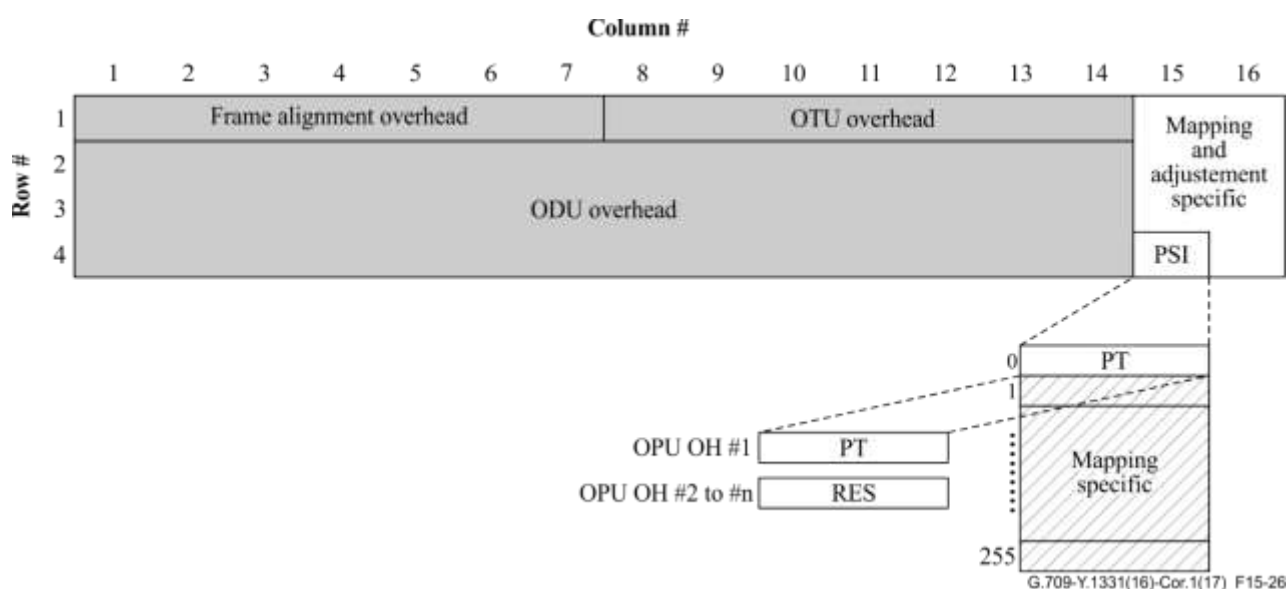


Figure 15-26 – OPU overhead

### 15.9.2 OPU OH definition

#### 15.9.2.1 OPU payload structure identifier (PSI)

One byte is allocated in the OPU overhead to transport a 256-byte payload structure identifier (PSI) signal. The byte is located in row 4, column 15 of the OPU overhead.

The OPU<sub>k</sub> contains one instance of OPU PSI overhead. The OPU<sub>Cn</sub> contains n instances of the OPU PSI overhead, numbered 1 to n (PSI #1 to PSI #n).

The 256-byte PSI signal is aligned with the ODU multiframe (i.e., PSI[0] is present at ODU multiframe position 0000 0000, PSI[1] at position 0000 0001, PSI[2] at position 0000 0010, etc.).

PSI[0] contains a one-byte payload type or is reserved for future international standardization. PSI[1] to PSI[255] are mapping specific, except for PT 0x01 (experimental mapping) and PTs 80-0x8F (for proprietary use).

##### 15.9.2.1.1 OPU payload type (PT)

A one-byte payload type signal is defined in the PSI[0] byte of the payload structure identifier to indicate the composition of the OPU signal. The code points are defined in Table 15-9.



The OPU<sub>k</sub> and OPUC<sub>n</sub> contain one instance of OPU PT overhead.

**Table 15-9 – Payload type code points**

<b>MSB 1 2 3 4</b>	<b>LSB 5 6 7 8</b>	<b>Hex code (Note 1)</b>	<b>Interpretation</b>
0 0 0 0	0 0 0 1	01	Experimental mapping (Note 3)
0 0 0 0	0 0 1 0	02	Asynchronous CBR mapping, see clause 17.2
0 0 0 0	0 0 1 1	03	Bit-synchronous CBR mapping, see clause 17.2
0 0 0 0	0 1 0 0	04	Not available (Notes 2,7)
0 0 0 0	0 1 0 1	05	GFP mapping, see clause 17.4
0 0 0 0	0 1 1 0	06	Not available (Note 2)
0 0 0 0	0 1 1 1	07	PCS codeword transparent Ethernet mapping: 1000BASE-X into OPU0, see clauses 17.7.1 and 17.7.1.1 40GBASE-R into OPU3, see clauses 17.7.4 and 17.7.4.1 100GBASE-R into OPU4, see clauses 17.7.5 and 17.7.5.1
0 0 0 0	1 0 0 0	08	FC-1200 into OPU2e mapping, see clause 17.8.2
0 0 0 0	1 0 0 1	09	GFP mapping into extended OPU2 payload, see clause 17.4.1 (Note 5)
0 0 0 0	1 0 1 0	0A	STM-1 mapping into OPU0, see clause 17.7.1
0 0 0 0	1 0 1 1	0B	STM-4 mapping into OPU0, see clause 17.7.1
0 0 0 0	1 1 0 0	0C	FC-100 mapping into OPU0, see clause 17.7.1
0 0 0 0	1 1 0 1	0D	FC-200 mapping into OPU1, see clause 17.7.2
0 0 0 0	1 1 1 0	0E	FC-400 mapping into OPUflex, see clause 17.9
0 0 0 0	1 1 1 1	0F	FC-800 mapping into OPUflex, see clause 17.9
0 0 0 1	0 0 0 0	10	Bit stream with octet timing mapping, see clause 17.6.1
0 0 0 1	0 0 0 1	11	Bit stream without octet timing mapping, see clause 17.6.2
0 0 0 1	0 0 1 0	12	IB SDR mapping into OPUflex, see clause 17.9
0 0 0 1	0 0 1 1	13	IB DDR mapping into OPUflex, see clause 17.9
0 0 0 1	0 1 0 0	14	IB QDR mapping into OPUflex, see clause 17.9
0 0 0 1	0 1 0 1	15	SDI mapping into OPU0, see clause 17.7.1
0 0 0 1	0 1 1 0	16	(1.485/1.001) Gbit/s SDI mapping into OPU1, see clause 17.7.2
0 0 0 1	0 1 1 1	17	1.485 Gbit/s SDI mapping into OPU1, see clause 17.7.2
0 0 0 1	1 0 0 0	18	(2.970/1.001) Gbit/s SDI mapping into OPUflex, see clause 17.9
0 0 0 1	1 0 0 1	19	2.970 Gbit/s SDI mapping into OPUflex, see clause 17.9
0 0 0 1	1 0 1 0	1A	SBCON/ESCON mapping into OPU0, see clause 17.7.1
0 0 0 1	1 0 1 1	1B	DVB_ASI mapping into OPU0, see clause 17.7.1
0 0 0 1	1 1 0 0	1C	FC-1600 mapping into OPUflex, see clause 17.9
0 0 0 1	1 1 0 1	1D	<del>FlexE Packet Client</del> mapping into OPUflex(IMP) and ODUflex(IMP,s), see clauses 17.10 and 17.11
0 0 0 1	1 1 1 0	1E	FlexE aware (partial rate) mapping into OPUflex, see clause 17.12

**Table 15-9 – Payload type code points**

<b>MSB 1 2 3 4</b>	<b>LSB 5 6 7 8</b>	<b>Hex code (Note 1)</b>	<b>Interpretation</b>
0 0 0 1	1 1 1 1	1F	FC-3200 mapping into OPUflex, see clause 17.9
0 0 1 0	0 0 0 0	20	ODU multiplex structure supporting ODTUjk only, see clause 19 (AMP only)
0 0 1 0	0 0 0 1	21	ODU multiplex structure supporting ODTUk.ts or ODTUk.ts and ODTUjk, see clause 19 (GMP capable) (Note 6)
0 0 1 0	0 0 1 0	22	ODU multiplex structure supporting ODTUCn.ts, see clause 20 (GMP capable)
0 0 1 1	0 0 0 0	30	25GBASE-R mapping into OPUflex, see clause 17.13
0 0 1 1	0 0 0 1	31	200GBASE-R mapping into OPUflex, see clause 17.13
0 0 1 1	0 0 1 0	32	400GBASE-R mapping into OPUflex, see clause 17.13
0 0 1 1	0 0 1 1	33	50GBASE-R mapping into OPUflex, see clause 17.13
0 1 0 1	0 1 0 1	55	Not available (Note 2)
0 1 1 0	0 1 1 0	66	Not available (Note 2)
1 0 0 0	x x x x	80-8F	Reserved codes for proprietary use (Note 4)
1 1 1 1	1 1 0 1	FD	NULL test signal mapping, see clause 17.5.1
1 1 1 1	1 1 1 0	FE	PRBS test signal mapping, see clause 17.5.2
1 1 1 1	1 1 1 1	FF	Not available (Note 2)

NOTE 1 – There are 197 spare codes left for future international standardization. Refer to Annex A of [ITU-T G.806] for the procedure to obtain one of these codes for a new payload type.

NOTE 2 – These values are excluded from the set of available code points. These bit patterns are present in ODUk maintenance signals or were used to represent client types that are no longer supported.

NOTE 3 – Value "01" is only to be used for experimental activities in cases where a mapping code is not defined in this table. Refer to Annex A of [ITU-T G.806] for more information on the use of this code.

NOTE 4 – These 16 code values will not be subject to further standardization. Refer to Annex A of [ITU-T G.806] for more information on the use of these codes.

NOTE 5 – Supplement 43 (2008) to the ITU-T G-series of Recommendations indicated that this mapping recommended using payload type 87.

NOTE 6 – Equipment supporting ODTUk.ts for OPU2 or OPU3 must be backward compatible with equipment which supports only the ODTUjk. ODTUk.ts capable equipment transmitting PT=21 which receives PT=20 from the far end shall revert to PT=20 and operate in ODTUjk only mode. Refer to [ITU-T G.798] for the specification.

**NOTE 7 – This bit pattern may appear temporarily due to the presence of the FlexO SquelchText pattern. Refer to [ITU-T G.709.1].**

### 15.9.2.2 OPU mapping specific overhead

Seven bytes are reserved in the OPUk overhead for the mapping and hitless adjustment specific overhead. These bytes are located in rows 1 to 3, columns 15 and 16 and column 16 row 4. In addition, 255 bytes in the PSI #1 and 256 byte in PSI #2 to #n are reserved for specific purposes.

The use of these bytes depends on the specific client signal mapping (defined in clauses 17, 19 and 20) and use of hitless adjustment of ODUflex(GFP) (see [ITU-T G.7044]).

## 16 Maintenance signals

An alarm indication signal (AIS) is a signal sent downstream as an indication that an upstream defect has been detected. An AIS signal is generated in an adaptation sink function. An AIS signal is detected in a trail termination sink function to suppress defects or failures that would otherwise be detected as a consequence of the interruption of the transport of the original signal at an upstream point.

A forward defect indication (FDI) is a signal sent downstream as an indication that an upstream defect has been detected. An FDI signal is generated in an adaptation sink function. An FDI signal is detected in a trail termination sink function to suppress defects or failures that would otherwise be detected as a consequence of the interruption of the transport of the original signal at an upstream point.

NOTE – AIS and FDI are similar signals. AIS is used as the term when the signal is in the digital domain. FDI is used as the term when the signal is in the optical domain; FDI is transported as a non-associated overhead.

An open connection indication (OCI) is a signal sent downstream as an indication that upstream the signal is not connected to a trail termination source. An OCI signal is generated in a connection function and output by this connection function on each of its output connection points, which are not connected to one of its input connection points. An OCI signal is detected in a trail termination sink function.

~~A~~Hlocked (LCK) is a signal sent downstream as an indication that, upstream to the receiver, the connection is administratively "locked", and the normal signal has not passed through.

A payload missing indication (PMI) is a signal sent downstream as an indication that upstream at the source point of the signal none of the frequency slots have an optical tributary signal. This indicates that the transport of the optical tributary signals is interrupted or no optical tributary signals are present.

A PMI signal is generated in the trail termination source function and it is detected in the trail termination sink function which suppresses the LOS defect that arises under this condition.

### 16.1 OTS maintenance signals

#### 16.1.1 OTS payload missing indication (OTS-PMI)

OTS-PMI is generated as an indication that the OTS payload does not contain an optical signal.

### 16.2 OMS maintenance signals

Three OMS maintenance signals are defined: OMS-FDI-P, OMS-FDI-O and OMS-PMI.

#### 16.2.1 OMS forward defect indication – Payload (OMS-FDI-P)

OMS-FDI-P is generated as an indication of an OMS server layer defect in the OTS network layer.

#### 16.2.2 OMS forward defect indication – Overhead (OMS-FDI-O)

OMS-FDI-O is generated as an indication when the transport of OMS OH via the OSC is interrupted due to a signal fail condition in the OSC.

#### 16.2.3 OMS payload missing indication (OMS-PMI)

OMS-PMI is generated as an indication when none of the frequency slots contain an optical tributary signal.

### 16.3 OCh and OTiSA maintenance signals

Three OCh and OTiSA maintenance signals are defined: OCh-FDI-P, OCh-FDI-O, OCh-OCI and OTSiA-FDI-P, OTSiA-FDI-O, OTSiA-OCI.

### 16.3.1 OCh and OTiSA forward defect indication – Payload (OCh-FDI-P, OTSiA-FDI-P)

OCh-FDI-P and OTSiA-FDI-P are generated as an indication for an OCh and OTSiA server layer defect in the OMS network layer.

When the OTUk or OTUCn is terminated, the OCh-FDI-P and OTSiA\_FDI-P is continued as an ODUk-AIS signal.

When the OTUCn is not terminated, the OCh-FDI-P and OTSiA\_FDI-P are continued as an OTUCn-AIS signal.

OTSiA-FDI-O is generated as an indication when the transport of OTSiA OH via the OSC is interrupted due to a signal fail condition in the OSC.

### 16.3.2 OCh and OTiSA forward defect indication – Overhead (OCh-FDI-O, OTSiA-FDI-O)

OCh-FDI-O is generated as an indication when the transport of OCh OH via the OSC or OCC is interrupted due to a signal fail condition in the OSC or OCC.

### 16.3.3 OCh and OTiSA open connection indication (OCh-OCI, OTSiA-OCI)

The OCh-OCI/OTSiA-OCI signal indicates to downstream transport processing functions that the OCh/OTSiA connection is not bound to, or not connected (via a matrix connection) to a termination source function. The indication is used in order to distinguish downstream between a missing OCh/OTSiA signal due to a defect or due to the open connection (resulting from a management command).

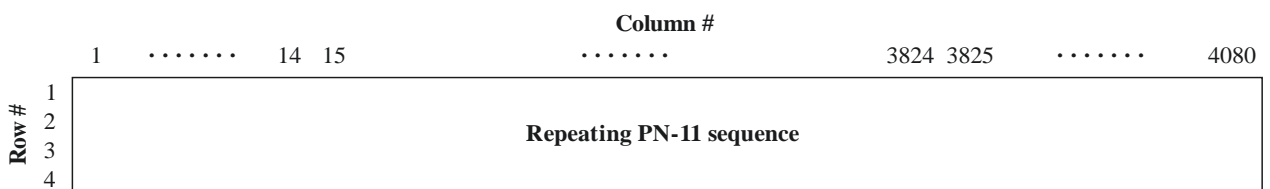
NOTE – OCI is detected at the next downstream OCh or OTSiA trail terminating equipment. If the connection was opened intentionally, the related alarm report from this trail termination should be disabled by using the alarm reporting control mode (refer to [ITU-T M.3100]).

## 16.4 OTU maintenance signals

### 16.4.1 OTUk (k=1,2,3) alarm indication signal (OTUk-AIS)

The OTUk-AIS (k=1,2,3) (see Figure 16-1) is a generic-AIS signal (see clause 16.6.1). Since the OTUk capacity (130 560 bits) is not an integer multiple of the PN-11 sequence length (2047 bits), the PN-11 sequence may cross an OTUk frame boundary.

NOTE – OTUk-AIS is defined to support a future server layer application. OTN equipment should be capable of detecting the presence of such a signal within OTUk (k=1,2,3) on OTN point-to-point interface signals; it is not required to generate such a signal.



G.709-Y.1331(12)\_F16-1

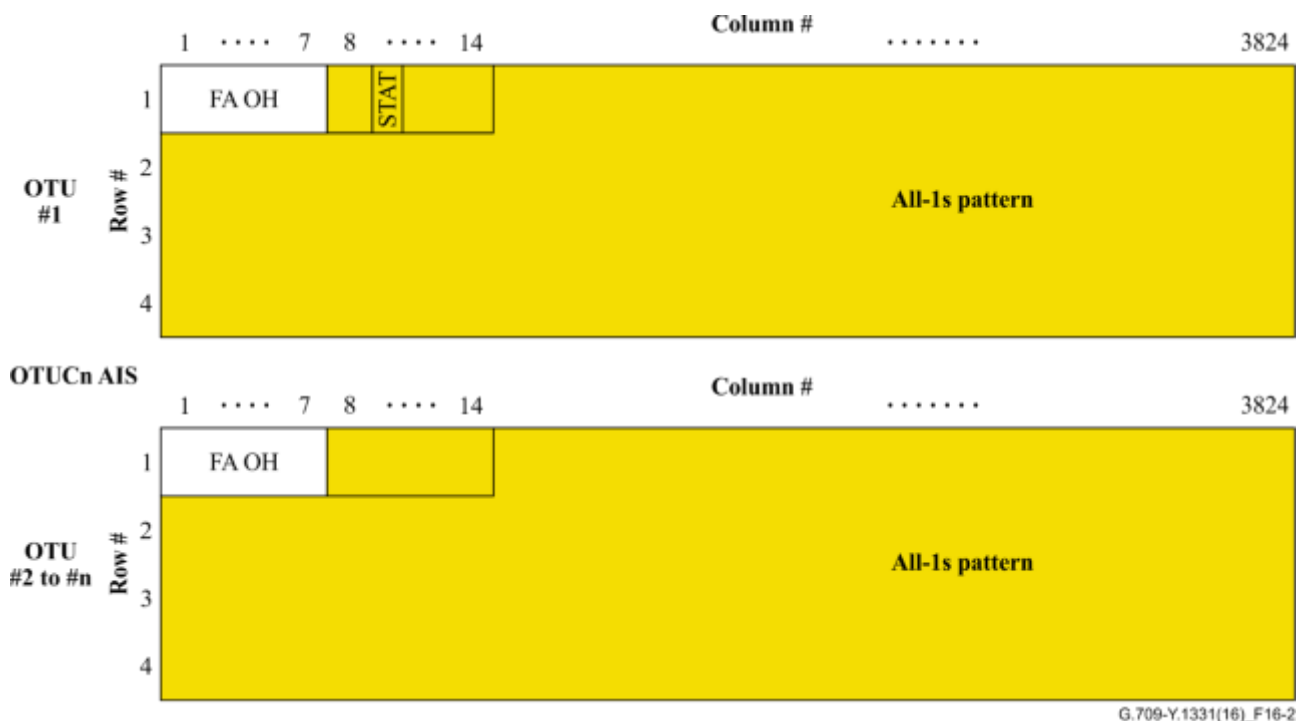
**Figure 16-1 – OTUk-AIS**

### 16.4.2 OTUCn alarm indication signal (OTUCn-AIS)

The OTUCn-AIS is specified as all "1"s in the entire OTUCn signal, excluding the frame alignment overhead (FA OH) (see Figure 16-2).

The presence of the OTUCn-AIS is detected by monitoring the OTUCn SM STAT bits in the SM overhead fields.

NOTE – OTUCn-AIS is defined to support a future 3R regenerator application in which the OTUCn is not terminated and an OTUCn subrating application. OTN equipment should be capable of detecting the presence of such a signal within OTUCn signals on OTN optical networking interfaces. OTU0-AIS is not defined.



**Figure 16-2 – OTUCn-AIS**

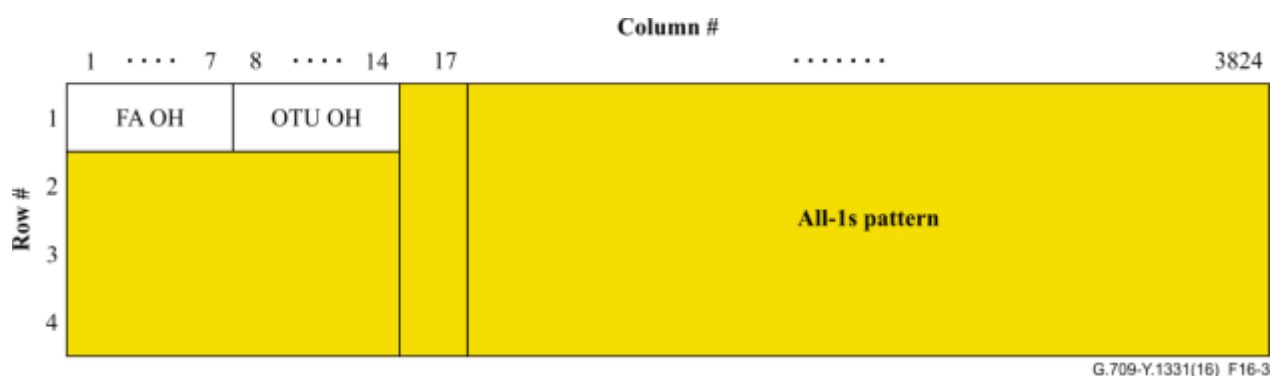
## 16.5 ODU maintenance signals

Three ODU maintenance signals are defined: ODU-AIS, ODU-OCI and ODU-LCK.

### 16.5.1 ODU alarm indication signal (ODU-AIS)

ODUK-AIS is specified as all "1"s in the entire ODU signal, excluding the frame alignment overhead (FA OH), OTU overhead (OTU OH) (see Figure 16-3).

The ODUk contains one instance of ODU AIS. The ODUCn contains n instances of ODU AIS, numbered 1 to n (ODU AIS #1 to #n).



**Figure 16-3 – ODU-AIS**

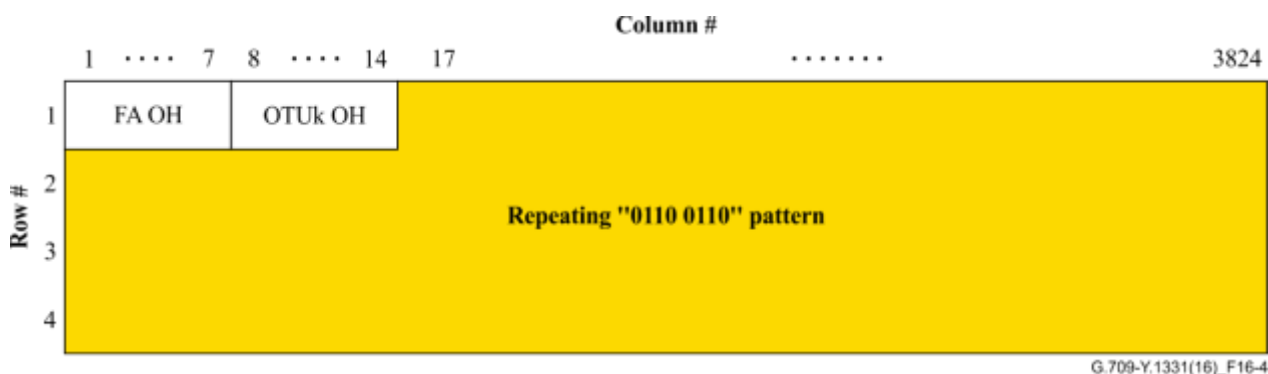
In addition, the ODU-AIS signal may be extended with one or more levels of ODU tandem connection, GCC1, GCC2, EXP and/or APS/PCC overhead before it is presented at the OTN interface. This is dependent on the functionality between the ODU-AIS insertion point and the OTN interface.

The presence of the ODU-AIS is detected by monitoring the ODU STAT bits in the PM and TCMi overhead fields.

### 16.5.2 ODUk open connection indication (ODUk-OCI)

ODUk-OCI is specified as a repeating "0110 0110" pattern in the entire ODUk signal, excluding the frame alignment overhead (FA OH) and OTUk overhead (OTUk OH) (see Figure 16-4).

NOTE – ODUCn OCI is not defined.



**Figure 16-4 – ODUk-OCI**

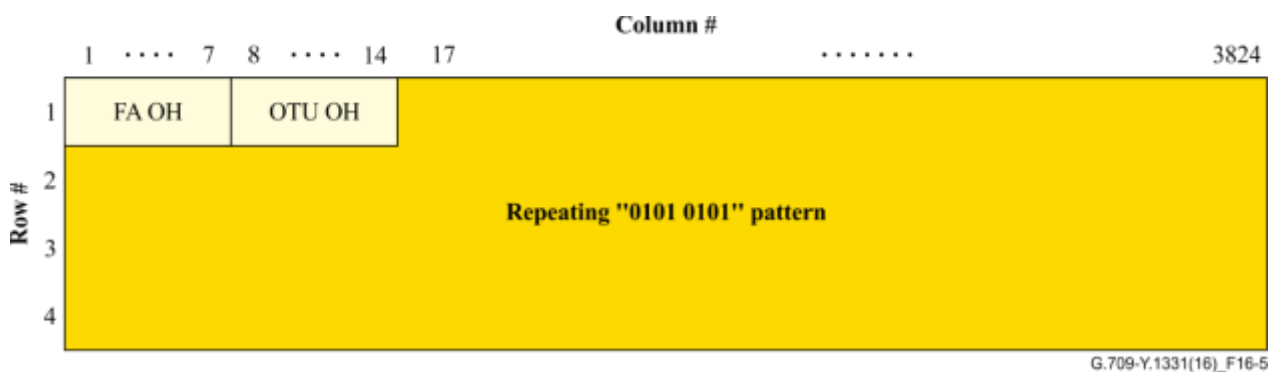
NOTE – The repeating "0110 0110" pattern is the default pattern; other patterns are also allowed as long as the STAT bits in the PM and TCMi overhead fields are set to "110".

In addition, the ODUk-OCI signal may be extended with one or more levels of ODUk tandem connection, GCC1, GCC2, EXP and/or APS/PCC overhead before it is presented at the OTM interface. This is dependent on the functionality between the ODUk-OCI insertion point and the OTM interface.

The presence of ODUk-OCI is detected by monitoring the ODUk STAT bits in the PM and TCMi overhead fields.

### 16.5.3 ODU locked (ODU-LCK)

ODU-LCK is specified as a repeating "0101 0101" pattern in the entire ODU signal, excluding the frame alignment overhead (FA OH) and OTU overhead (OTU OH) (see Figure 16-5).



**Figure 16-5 – ODU-LCK**

NOTE – The repeating "0101 0101" pattern is the default pattern; other patterns are also allowed as long as the STAT bits in the PM and TCMi overhead fields are set to "101".

In addition, the ODU-LCK signal may be extended with one or more additional levels of ODU tandem connection, GCC1, GCC2, EXP and/or the APS/PCC overhead before it is presented at the OTN interface. This is dependent on the functionality between the ODU-LCK insertion point and the OTN interface.

The presence of ODU-LCK is detected by monitoring the ODU STAT bits in the PM and TCMi overhead fields.

## 16.6 Client maintenance signal

### 16.6.1 Generic AIS for constant bit rate signals

The generic-AIS signal is a signal with a 2 047-bit polynomial number 11 (PN-11) repeating sequence.

The PN-11 sequence is defined by the generating polynomial  $1 + x^9 + x^{11}$  as specified in clause 5.2 of [ITU-T O.150]. (See Figure 16-6.)

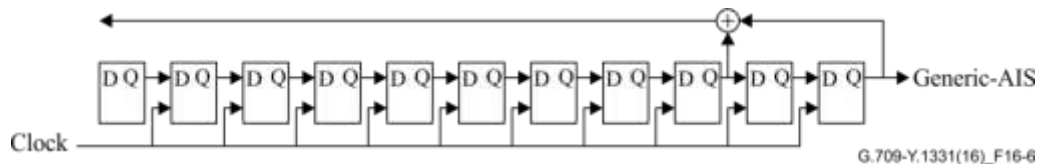


Figure 16-6 – Generic-AIS generating circuit

## 17 Mapping of client signals

This clause specifies the mapping of:

- STM-16, STM-64, STM-256 constant bit rate client signals into OPUk using client/server specific asynchronous or bit-synchronous mapping procedures (AMP, BMP);
- 10GBASE-R constant bit rate client signal into OPU2e using client/server specific bit-synchronous mapping procedure (BMP);
- FC-1200 constant bit rate client signal after timing transparent transcoding (TTT) providing a 50/51 rate compression into OPU2e using client/server specific byte-synchronous mapping procedure;
- constant bit rate client signals with bit rates up to 1.238 Gbit/s into OPU0 and up to 2.488 Gbit/s into OPU1 using a client agnostic generic mapping procedure (GMP) possibly preceded by a timing transparent transcoding (TTT) of the client signal to reduce the bit rate of the signal to fit the OPUk payload bandwidth;
- constant bit rate client signals into OPU1, OPU2, OPU3 or OPU4 respectively using a client agnostic generic mapping procedure (GMP) possibly preceded by a timing transparent transcoding (TTT) of the client signal to reduce the bit rate of the signal to fit the OPUk payload bandwidth;
- other constant bit rate client signals into OPUflex using a client agnostic bit-synchronous mapping procedure (BMP);
- packet streams (e.g., Ethernet, MPLS, IP) which are encapsulated with the generic framing procedure (GFP-F);
- test signals;
- continuous mode GPON constant bit rate client signal into OPU1 using asynchronous mapping procedure (AMP);
- continuous mode XGPON constant bit rate client signal into OPU2 using asynchronous mapping procedure (AMP);
- FlexE-aware client signal into OPUflex using bit synchronous mapping procedure (BMP);
- FlexE Client client signal into OPUflex using idle mapping procedure;
- packet streams (e.g., Ethernet, MPLS, IP) which are encapsulated with the Idle mapping procedure (IMP) into OPU.

## 17.1 OPU client signal fail (CSF)

For support of local management systems, a single-bit OPU client signal fail (CSF) indicator is defined to convey the signal fail status of the CBR and Ethernet private line client signal mapped into an OPU at the ingress of the OTN to the egress of the OTN.

OPU CSF is located in bit 1 of the PSI[2] byte of the payload structure identifier. Bits 2 to 8 of the PSI[2] byte are reserved for future international standardization. These bits are set to all-0s.

OPU CSF is set to "1" to indicate a client signal fail indication, otherwise it is set to "0".

NOTE – Equipment designed prior to Edition 3.0 of the Recommendation will generate a "0" in the OPUk CSF and will ignore any value in OPUk CSF.

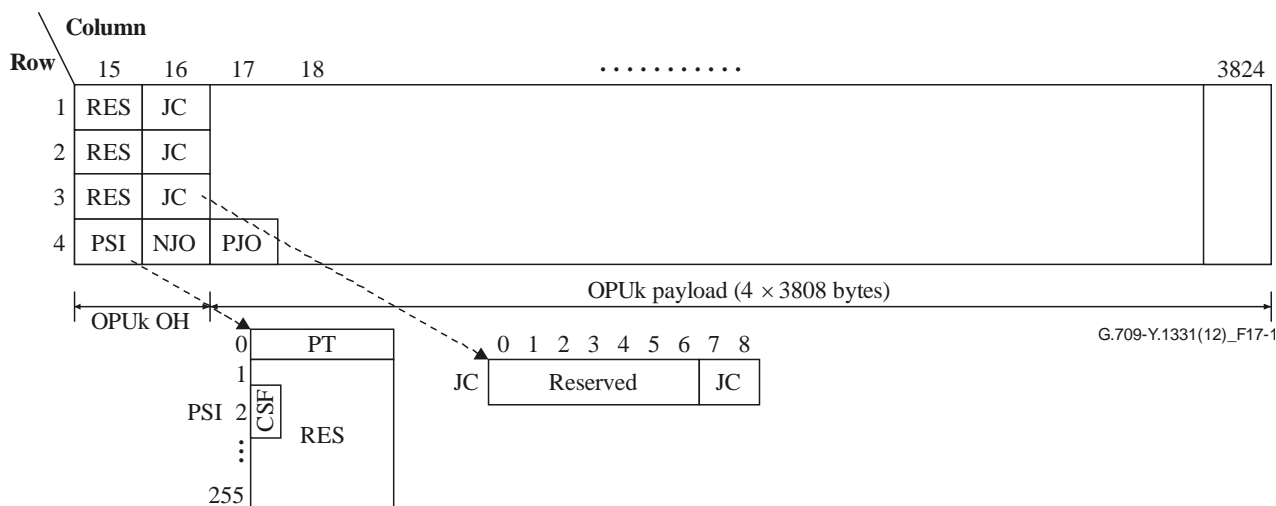
## 17.2 Mapping of CBR2G5, CBR10G, CBR10G3 and CBR40G signals into OPUk

The mapping of a CBR2G5, CBR10G or CBR40G signal (with up to  $\pm 20$  ppm bit-rate tolerance) into an OPUk ( $k = 1,2,3$ ) may be performed according to the bit-synchronous mapping procedure based on one generic OPUk frame structure (see Figure 17-1). The mapping of a CBR2G5, CBR10G or CBR40G signal (with up to  $\pm 45$  ppm bit-rate tolerance) into an OPUk ( $k = 1,2,3$ ) may be performed according to the asynchronous mapping procedure. The mapping of a CBR10G3 signal (with up to  $\pm 100$  ppm bit-rate tolerance) into an OPUk ( $k = 2e$ ) is performed using the bit-synchronous mapping procedure.

NOTE 1 – Examples of CBR2G5, CBR10G and CBR40G signals are STM-16 and CMGPON\_D/U2 (refer to [ITU-T G.984.6]), STM-64 and CMXGPON\_D/U2 [ITU-T G.987.4] and STM-256. An example of a CBR10G3 signal is 10GBASE-R.

NOTE 2 – The maximum bit-rate tolerance between an OPUk and the client signal clock, which can be accommodated by the asynchronous mapping scheme, is  $\pm 65$  ppm. With a bit-rate tolerance of  $\pm 20$  ppm for the OPUk clock, the client signal's bit-rate tolerance can be  $\pm 45$  ppm.

NOTE 3 – For OPUk ( $k=1,2,3$ ) the clock tolerance is  $\pm 20$  ppm. For OPU2e the clock tolerance is  $\pm 100$  ppm and asynchronous mapping cannot be supported with this justification overhead.



**Figure 17-1 – OPUk frame structure for the mapping of a CBR2G5, CBR10G or CBR40G signal**

The OPUk overhead for these mappings consists of a payload structure identifier (PSI) including the payload type (PT), a client signal fail (CSF) indicator and 254 bytes plus 7 bits reserved for future international standardization (RES), three justification control (JC) bytes, one negative justification opportunity (NJO) byte, and three bytes reserved for future international standardization (RES).



The JC bytes consist of two bits for justification control and six bits reserved for future international standardization.

The OPUk payload for these mappings consists of  $4 \times 3808$  bytes, including one positive justification opportunity (PJO) byte.

The justification control (JC) signal, which is located in rows 1, 2 and 3 of column 16, bits 7 and 8, is used to control the two justification opportunity bytes NJO and PJO that follow in row 4.

The asynchronous and bit-synchronous mapping processes generate the JC, NJO and PJO according to Tables 17-1 and 17-2, respectively. The de-mapping process interprets JC, NJO and PJO according to Table 17-3. Majority vote (two out of three) shall be used to make the justification decision in the de-mapping process to protect against an error in one of the three JC signals.

**Table 17-1 – JC, NJO and PJO generation by an asynchronous mapping process**

bits	JC 7 8	NJO	PJO
	0 0	justification byte	data byte
	0 1	data byte	data byte
	1 0	not generated	
	1 1	justification byte	justification byte

**Table 17-2 – JC, NJO and PJO generation by a bit-synchronous mapping process**

bits	JC 7 8	NJO	PJO
	0 0	justification byte	data byte
	0 1	not generated	
	1 0		
	1 1		

**Table 17-3 – JC, NJO and PJO interpretation**

bits	JC 7 8	NJO	PJO
	0 0	justification byte	data byte
	0 1	data byte	data byte
	1 0 (Note)	justification byte	data byte
	1 1	justification byte	justification byte
NOTE – A mapper circuit does not generate this code. Due to bit errors a de-mapper circuit might receive this code.			

The value contained in NJO and PJO when they are used as justification bytes is all-0s. The receiver is required to ignore the value contained in these bytes whenever they are used as justification bytes.

During a signal fail condition of the incoming CBR2G5, CBR10G or CBR40G client signal (e.g., in the case of a loss of input signal), this failed incoming signal is replaced by the generic-AIS signal as specified in clause 16.6.1, and is then mapped into the OPUk.

During a signal fail condition of the incoming 10GBASE-R type CBR10G3 client signal (e.g., in the case of a loss of input signal), this failed incoming 10GBASE-R signal is replaced by a stream of 66B blocks, with each block carrying two local fault sequence ordered sets (as specified in [IEEE 802.3]). This 66B block stream replacement signal is scrambled before mapping into the OPU2e. A self-synchronizing scrambler with generator polynomial  $1 + x^{39} + x^{58}$  shall be used, which is identical to the scrambler specified in clause 49.2.6 of [IEEE 802.3].

During the signal fail condition of the incoming ODUk/OPUk signal (e.g., in the case of an ODUk-AIS, ODUk-LCK, ODUk-OCI condition) the generic-AIS pattern as specified in clause 16.6.1 is generated as a replacement signal for the lost CBR2G5, CBR10G or CBR40G signal.

During the signal fail condition of the incoming ODU2e/OPU2e signal (e.g., in the case of an ODU2e-AIS, ODU2e-LCK, ODU2e-OCI condition) a stream of 66B blocks, with each block carrying two local fault sequence ordered sets (as specified in [IEEE 802.3]) is generated as a replacement signal for the lost 10GBASE-R signal. This 66B block stream replacement signal is scrambled using a self-synchronizing scrambler with generator polynomial  $1 + x^{39} + x^{58}$ , which is identical to the scrambler specified in clause 49.2.6 of [IEEE 802.3].

NOTE 4 – Local fault sequence ordered set is /K28.4/D0.0/D0.0/D1.0/. The 66B block contains the following value SH=10 0x55 00 00 01 00 00 00 01.

NOTE 5 – Equipment developed prior to Edition 2.5 of this Recommendation may generate a different 10GBASE-R replacement signal (e.g., Generic-AIS) than the local fault sequence ordered set.

### **Asynchronous mapping**

The OPUk signal for the asynchronous mapping is created from a locally generated clock (within the limits specified in Table 7-3), which is independent of the CBR2G5, CBR10G or CBR40G (i.e.,  $4^{(k-1)} \times 2\,488\,320$  kbit/s ( $k = 1,2,3$ )) client signal.

The CBR2G5, CBR10G, CBR40G (i.e.,  $4^{(k-1)} \times 2\,488\,320$  kbit/s ( $k = 1,2,3$ )) signal is mapped into the OPUk using a positive/negative/zero (pnz) justification scheme.

### **Bit-synchronous mapping**

The OPUk clock for bit-synchronous mapping is derived from the CBR2G5, CBR10G, CBR40G or CBR10G3 client signal. During signal fail conditions of the incoming CBR2G5, CBR10G, CBR40G or CBR10G3 signal (e.g., in the case of a loss of input signal), the OPUk payload signal bit rate shall be within the limits specified in Table 7-3 and the limits defined for the ODCb clock in [ITU-T G.8251] and no OPUk frame phase discontinuity shall be introduced in this case and when resynchronizing on the incoming CBR2G5, CBR10G, CBR40G or CBR10G3 signal.

The CBR2G5, CBR10G, CBR40G or CBR10G3 signal is mapped into the OPUk without using the justification capability within the OPUk frame: NJO contains a justification byte, PJO contains a data byte, and the JC signal is fixed to 00.

#### **17.2.1 Mapping a CBR2G5 signal (e.g., STM-16, CMGPON\_D/CMGPON\_U2) into OPU1**

Groups of eight successive bits (not necessarily being a byte) of the CBR2G5 signal are mapped into a data (D) byte of the OPU1 (see Figure 17-2). Once per OPU1 frame, it is possible to perform either a positive or a negative justification action.

Row #	Column #				3824	
	15	16	17	18		
1	RES	JC	D	D	3805D	D
2	RES	JC	D	D	3805D	D
3	RES	JC	D	D	3805D	D
4	PSI	NJO	PJO	D	3805D	D

G.709-Y.1331(12)\_F17-2

**Figure 17-2 – Mapping of a CBR2G5 signal into OPU1**

### 17.2.2 Mapping a CBR10G signal (e.g., STM-64, CMXGPON\_D/CMXGPON\_U2) into OPU2

Groups of eight successive bits (not necessarily being a byte) of the CBR10G signal are mapped into a data (D) byte of the OPU2 (see Figure 17-3). 64 fixed stuff (FS) bytes are added in columns 1905 to 1920. Once per OPU2 frame, it is possible to perform either a positive or a negative justification action.

Row #	Column #										3824		
	15	16	17	.....	1904	1905	.....	1920	1921	.....			
1	RES	JC	118 × 16D						16FS	119 × 16D			
2	RES	JC	118 × 16D						16FS	119 × 16D			
3	RES	JC	118 × 16D						16FS	119 × 16D			
4	PSI	NJO	PJO	15D + 117 × 16D						16FS	119 × 16D		

G.709-Y.1331(12)\_F17-3

**Figure 17-3 – Mapping of a CBR10G signal into OPU2**

### 17.2.3 Mapping a CBR40G signal (e.g., STM-256) into OPU3

Groups of eight successive bits (not necessarily being a byte) of the CBR40G signal are mapped into a data (D) byte of the OPU3 (see Figure 17-4). 128 fixed stuff (FS) bytes are added in columns 1265 to 1280 and 2545 to 2560. Once per OPU3 frame, it is possible to perform either a positive or a negative justification action.

Row #	Column #														3824	
	15	16	17	.....	1264	1265	... 1280	1281	.....	2544	2545	... 2560	2561	...		
1	RES	JC	78 × 16D				16FS	79 × 16D			16FS	79 × 16D				
2	RES	JC	78 × 16D				16FS	79 × 16D			16FS	79 × 16D				
3	RES	JC	78 × 16D				16FS	79 × 16D			16FS	79 × 16D				
4	PSI	NJO	PJO	15D + 77 × 16D				16FS	79 × 16D			16FS	79 × 16D			

G.709-Y.1331(12)\_F17-4

**Figure 17-4 – Mapping of a CBR40G signal into OPU3**

### 17.2.4 Mapping a CBR10G3 signal (e.g., 10GBASE-R) into OPU2e

Groups of eight successive bits (not necessarily being a byte) of the CBR10G3 signal are bit-synchronously mapped into a data (D) byte of the OPU2e (see Figure 17-5). 64 fixed stuff (FS) bytes are added in columns 1905 to 1920.

NOTE – The NJO byte will always carry a stuff byte, the PJO byte will always carry a data (D) byte and the JC bytes will always carry the all-0s pattern.

Row #	Column #				Column #						
	15	16	17	.....	1904	1905	.....	1920	1921	.....	3824
1	RES	JC	118 × 16D			16FS		119 × 16D			
2	RES	JC	118 × 16D			16FS		119 × 16D			
3	RES	JC	118 × 16D			16FS		119 × 16D			
4	PSI	NJO	PJO	15D + 117 × 16D			16FS		119 × 16D		

G.709-Y.1331(12)\_F17-5

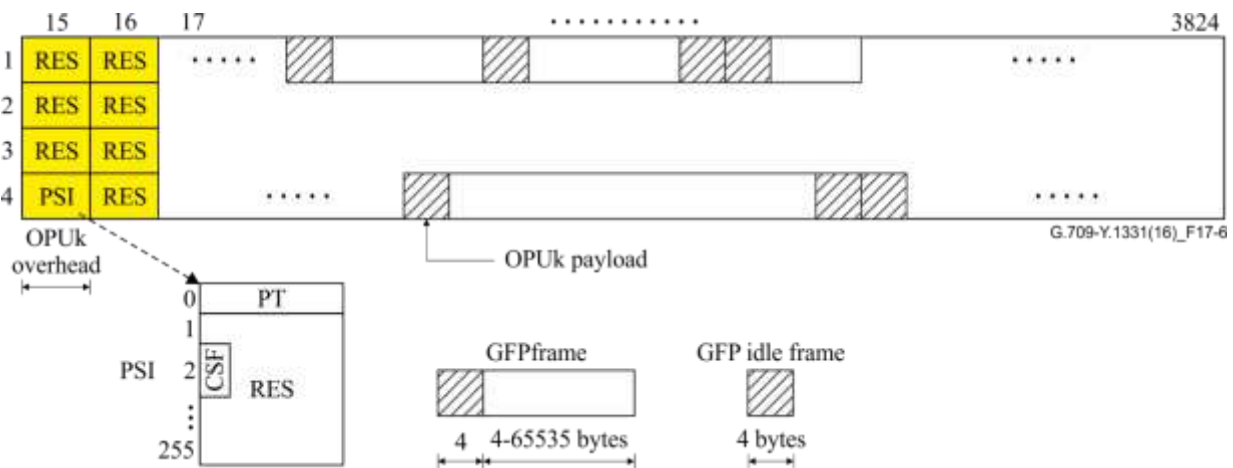
**Figure 17-5 – Mapping of a CBR10G3 signal into OPU2e**

### 17.3 Blank clause

*This clause is intentionally left blank.*

### 17.4 Mapping of GFP frames into OPUk (k=0,1,2,3,4,flex)

The mapping of generic framing procedure (GFP) frames is performed by aligning the byte structure of every GFP frame with the byte structure of the OPUk payload (see Figure 17-6). Since the GFP frames are of variable length (the mapping does not impose any restrictions on the maximum frame length), a frame may cross the OPUk (k=0,1,2,3,4,flex) frame boundary.



**Figure 17-6 – OPUk frame structure and mapping of GFP frames into OPUk**

GFP frames arrive as a continuous bit stream with a capacity that is identical to the OPUk payload area, due to the insertion of idle frames at the GFP encapsulation stage. The GFP frame stream is scrambled during encapsulation.

NOTE 1 – There is no rate adaptation or scrambling required at the mapping stage; this is performed by the GFP encapsulation process.

The OPUk overhead for the GFP mapping consists of a payload structure identifier (PSI) including the payload type (PT), a client signal fail (CSF) indicator and 254 bytes plus 7 bits reserved for future international standardization (RES), and seven bytes reserved for future international standardization (RES). The CSF indicator should be used only for Ethernet private line type 1 services; for other packet clients the CSF bit is fixed to 0.

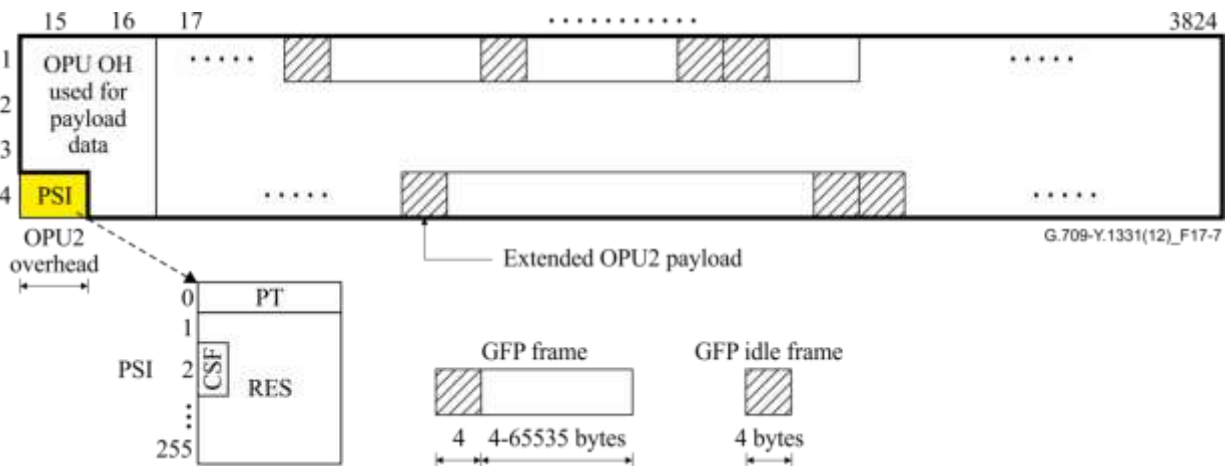
The OPUk payload for the GFP mapping consists of 4 × 3808 bytes.

NOTE 2 – The OPUflex(GFP) bit rate may be any configured bit rate as specified in Tables 7-3 and 7-8.

#### 17.4.1 Mapping of GFP frames into an extended OPU2 payload area

The mapping of generic framing procedure (GFP) frames in an extended OPU2 payload area is performed by aligning the byte structure of every GFP frame with the byte structure of the extended

OPU2 payload (see Figure 17-7). Since the GFP frames are of variable length (the mapping does not impose any restrictions on the maximum frame length), a frame may cross the OPU2 frame boundary.



**Figure 17-7 – OPU2 frame structure and mapping of GFP frames into an extended OPU2 payload area**

GFP frames arrive as a continuous bit stream with a capacity that is identical to the OPU2 payload area, due to the insertion of GFP-idle frames at the GFP encapsulation stage. The GFP frame stream is scrambled during encapsulation.

NOTE – There is no rate adaptation or scrambling required at the mapping stage; this is performed by the GFP encapsulation process.

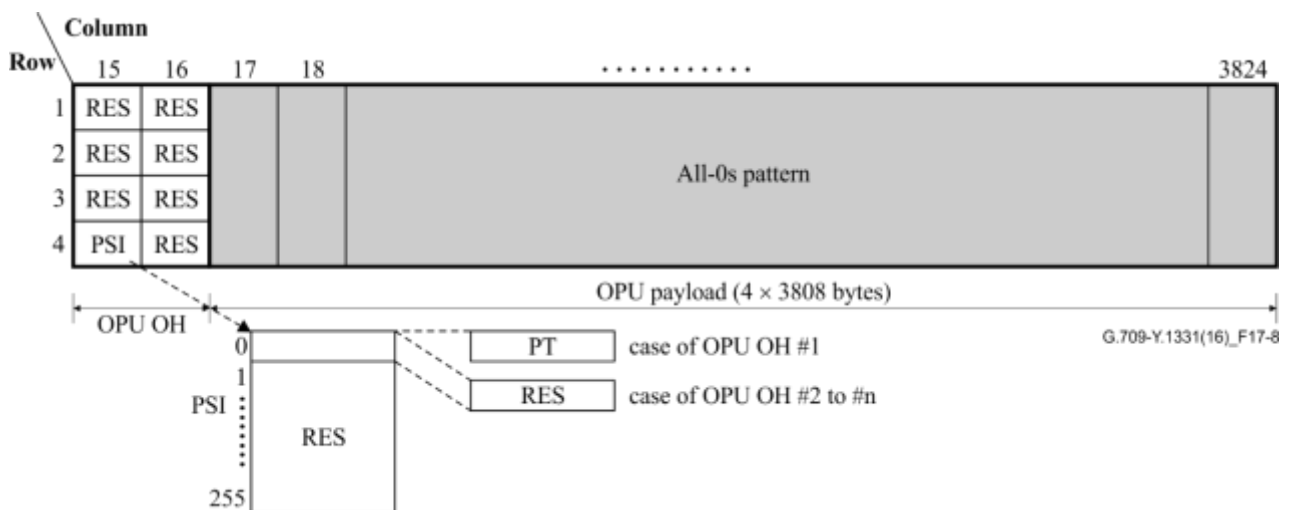
The OPU2 overhead for the GFP mapping consists of a payload structure identifier (PSI) including the payload type (PT), a client signal fail (CSF) indicator and 254 bytes plus 7 bits of reserved for future international standardization (RES).

The extended OPU2 payload for the GFP mapping consists of  $4 \times 3808$  bytes from the OPU2 payload plus 7 bytes from the OPU2 overhead.

## 17.5 Mapping of test signal into OPU

### 17.5.1 Mapping of a NULL client into OPU

An OPU payload signal with an all-0s pattern (see Figure 17-8) is defined for test purposes. This is referred to as the NULL client.



**Figure 17-8 – OPU frame structure and mapping of a NULL client into OPU**

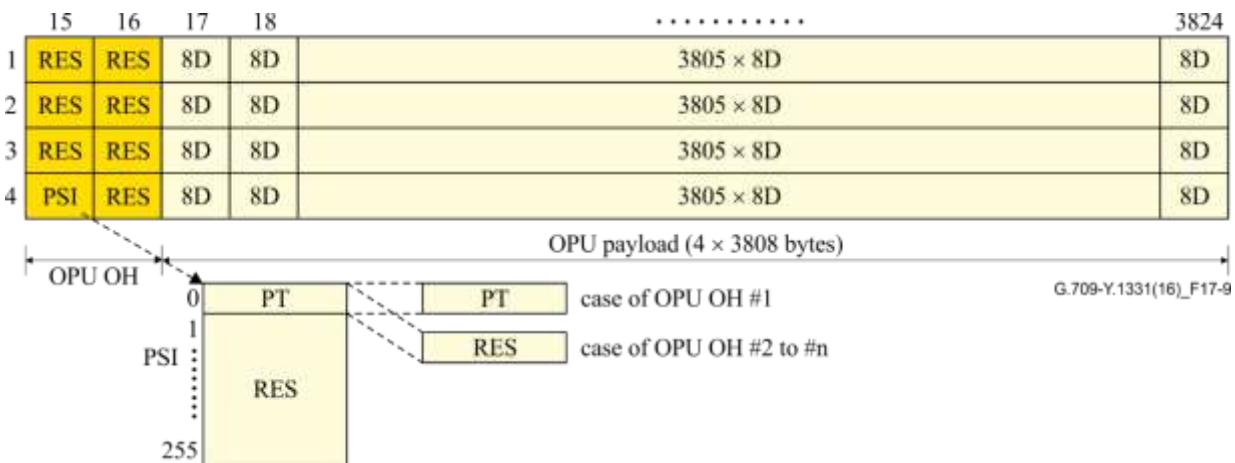
The OPU overhead for the NULL mapping consists of a payload structure identifier (PSI) including the payload type (PT) and 255 bytes reserved for future international standardization (RES), and seven bytes reserved for future international standardization (RES).

The OPU payload for the NULL mapping consists of  $4 \times 3808$  bytes.

The OPU<sub>k</sub> contains one instance of the NULL client. The OPU<sub>Cn</sub> contains n instances of the NULL client, numbered 1 to n.

### 17.5.2 Mapping of PRBS test signal into OPU

For end-to-end and segment turn-up test purposes, a 2 147 483 647-bit pseudo-random test sequence ( $2^{31} - 1$ ) as specified in clause 5.8 of [ITU-T O.150] can be mapped into the OPU payload. Groups of eight successive bits of the 2 147 483 647-bit pseudo-random test sequence signal are mapped into 8 data bits (8D) (i.e., one byte) of the OPU payload (see Figure 17-9).



**Figure 17-9 – OPU frame structure and mapping of 2 147 483 647-bit pseudo-random test sequence into OPU**

The OPU overhead for the PRBS mapping consists of a payload structure identifier (PSI) including the payload type (PT) and 255 bytes reserved for future international standardization (RES), and seven bytes reserved for future international standardization (RES).

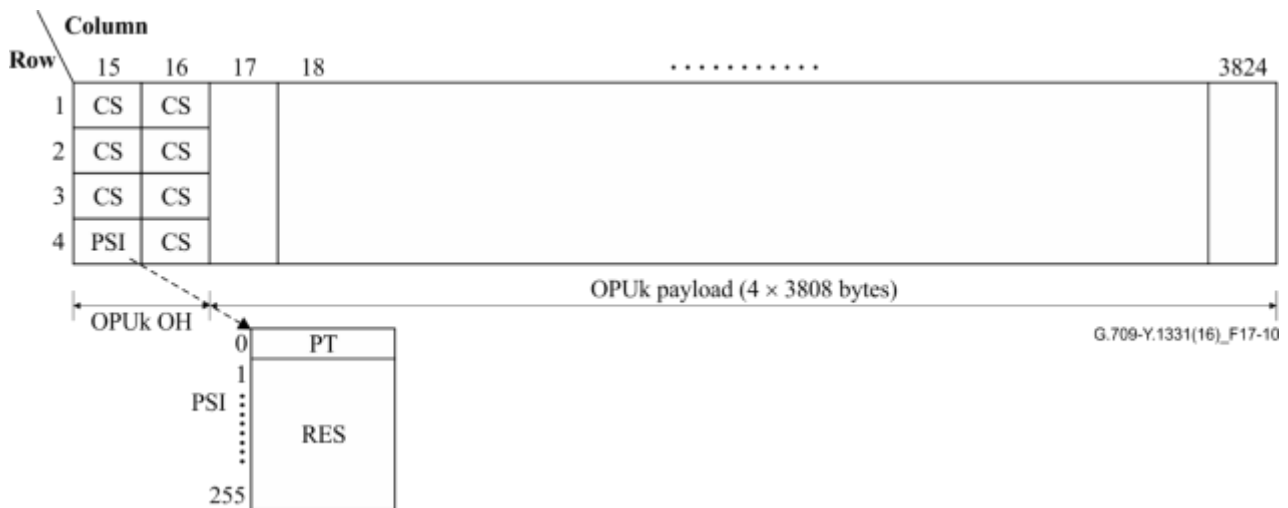
The OPU payload for the PRBS mapping consists of  $4 \times 3808$  bytes.

The OPU<sub>k</sub> contains one instance of the 2 147 483 647-bit pseudo-random test sequence. The OPU<sub>Cn</sub> contains n instances of the 2 147 483 647-bit pseudo-random test sequence, numbered 1 to n.

NOTE – This PRBS test pattern is not intended to be deployed for stress testing of the physical interface.

### 17.6 Mapping of a non-specific client bit stream into OPU<sub>k</sub>

In addition to the mappings of specific client signals as specified in the other subclauses of this clause, a non-specific client mapping into OPU<sub>k</sub> is specified. Any (set of) client signal(s), which after encapsulation into a continuous bit stream with a bit rate of the OPU<sub>k</sub> payload, can be mapped into the OPU<sub>k</sub> payload (see Figure 17-10). The bit stream must be synchronous with the OPU<sub>k</sub> signal. Any justification must be included in the continuous bit stream creation process. The continuous bit stream must be scrambled before mapping into the OPU<sub>k</sub> payload.



**Figure 17-10 – OPUk frame structure for the mapping of a synchronous constant bit stream**

The OPUk overhead for the mapping consists of a payload structure identifier (PSI) including the payload type (PT) and 255 bytes reserved for future international standardization (RES), and seven bytes for client-specific (CS) purposes. The definition of these CS overhead bytes is performed within the encapsulation process specification.

The OPUk payload for this non-specific mapping consists of  $4 \times 3808$  bytes.

### 17.6.1 Mapping bit stream with octet timing into OPUk

If octet timing is available, each octet of the incoming data stream will be mapped into a data byte (octet) of the OPUk payload.

### 17.6.2 Mapping bit stream without octet timing into OPUk

If octet timing is not available, groups of eight successive bits (not necessarily an octet) of the incoming data stream will be mapped into a data byte (octet) of the OPUk payload.

## 17.7 Mapping of other constant bit-rate signals with justification into OPUk

Mapping of other CBR client signals (with up to  $\pm 100$  ppm bit-rate tolerance) into an OPUk ( $k = 0, 1, 2, 3, 4$ ) is performed by the generic mapping procedure as specified in Annex D.

During a signal fail condition of the incoming CBR client signal (e.g., in the case of a loss of input signal), this failed incoming signal is replaced by the appropriate replacement signal as defined in the clauses hereafter.

During a signal fail condition of the incoming ODUk/OPUk signal (e.g., in the case of an ODUk-AIS, ODUk-LCK, ODUk-OCI condition), the failed client signal is replaced by the appropriate replacement signal as defined in the clauses hereafter.

The OPUk overhead for this mapping consists of a:

- payload structure identifier (PSI) including the payload type (PT) as specified in Table 15-9, the client signal fail (CSF) and 254 bytes plus 7 bits reserved for future international standardization (RES);
- three justification control (JC1, JC2, JC3) bytes carrying the value of GMP overhead  $C_m$ ;
- three justification control (JC4, JC5, JC6) bytes carrying the value of GMP overhead  $\Sigma C_{nD}$  and
- one byte reserved for future international standardization (RES).

The JC1, JC2 and JC3 bytes consist of a 14-bit  $C_m$  field (bits C1, C2, ..., C14), a 1-bit Increment Indicator (II) field, a 1-bit Decrement Indicator (DI) field and an 8-bit CRC-8 field which contains an error check code over the JC1, JC2 and JC3 fields.

The JC4, JC5 and JC6 bytes consist of a 10-bit  $\Sigma C_{nD}$  field (bits D1, D2, ..., D10), a 5-bit CRC-5 field which contains an error check code over the bits 4 to 8 in the JC4, JC5 and JC6 fields and nine bits reserved for future international standardization (RES). The default value of  $n$  in  $\Sigma C_{nD}$  is 8. The support for  $n=1$  is client dependent and specified in the clauses hereafter when required.

The values of  $m$ ,  $C_{m,\min}$ ,  $C_{m,\max}$ ,  $n$ ,  $C_{n,\min}$  and  $C_{n,\max}$  for CBR client into OPUk are as follows:

$$m = 8,16,64,256,640 \quad (17-1)$$

$$c_{m,nom} = \left( \frac{CBR\_nom\_client\_bit\_rate \times Number\_of\_GMP\_blocks\_in\_OPUk}{OPUk\_nom\_bit\_rate} \right) \quad (17-2)$$

$$c_{m,\min} = c_{m,nom} \times \left( \frac{1 - CBR\_client\_bit\_rate\_tolerance}{1 + OPUk\_bit\_rate\_tolerance} \right) \quad (17-3)$$

$$c_{m,\max} = c_{m,nom} \times \left( \frac{1 + CBR\_client\_bit\_rate\_tolerance}{1 - OPUk\_bit\_rate\_tolerance} \right) \quad (17-4)$$

$$C_{m,\min} = floor(c_{m,\min}) \quad (17-5)$$

$$C_{m,\max} = ceiling(c_{m,\min}) \quad (17-6)$$

$$n = 8,1 \quad (17-7)$$

$$c_{n,nom} = \left( \frac{CBR\_client\_nom\_bit\_rate \times Number\_of\_GMP\_blocks\_in\_OPUk}{OPUk\_nom\_bit\_rate} \right) \quad (17-8)$$

$$c_{n,\min} = c_{n,nom} \times \left( \frac{1 - CBR\_client\_bit\_rate\_tolerance}{1 + OPUk\_bit\_rate\_tolerance} \right) \quad (17-9)$$

$$c_{n,\max} = c_{n,nom} \times \left( \frac{1 + CBR\_client\_bit\_rate\_tolerance}{1 - OPUk\_bit\_rate\_tolerance} \right) \quad (17-10)$$

$$C_{n,\min} = floor(c_{n,\min}) \quad (17-11)$$

$$C_{n,\max} = ceiling(c_{n,\min}) \quad (17-12)$$

$C_{m,\min}$ ,  $C_{n,\min}$ ,  $C_{m,\max}$  and  $C_{n,\max}$  values represent the boundaries of client/OPU ppm offset combinations (i.e., min. client/max. OPU and max. client/min. OPU). In steady state, given instances of client/OPU offset combinations should not result in generated  $C_m$  and  $C_n$  values throughout this range but rather should be within as small a range as possible.

Under transient ppm offset conditions (e.g., AIS to normal signal), it is possible that  $C_n$  and  $C_m$  values outside the range  $C_{n,\min}$  to  $C_{n,\max}$  and  $C_{m,\min}$  to  $C_{m,\max}$  may be generated and a GMP de-mapper should be tolerant of such occurrences. Refer to Annex D for a general description of the GMP principles.

### 17.7.1 Mapping a sub-1.238 Gbit/s CBR client signal into OPU0

Table 17-4 specifies the clients defined by this Recommendation and their GMP  $m_n$  and  $C_{nD}$  parameter values. Table 17-5 specifies the replacement signals for those clients.



The support for 1-bit timing information ( $C_1$ ) is client dependent. Clients for which the 8-bit timing information in  $C_m$  with  $m=8$  is sufficient will not deploy the ability to transport  $\Sigma C_{1D}$  and the JC4/5/6 value will be fixed to all-0s.

The OPU0 payload for this mapping consists of  $4 \times 3808$  bytes. The bytes in the OPU0 payload area are numbered from 1 to 15232. The OPU0 payload byte numbering for GMP 1-byte (8-bit) blocks is illustrated in Figure 17-11. In row 1 of the OPU0 frame the first byte will be labelled 1, the next byte will be labelled 2, etc.

Groups of eight successive bits (not necessary being a byte) of the client signal are mapped into a byte of the OPU0 payload area under control of the GMP data/stuff control mechanism. Each byte in the OPU0 payload area may either carry 8 client bits, or carry 8 stuff bits. The stuff bits are set to zero.

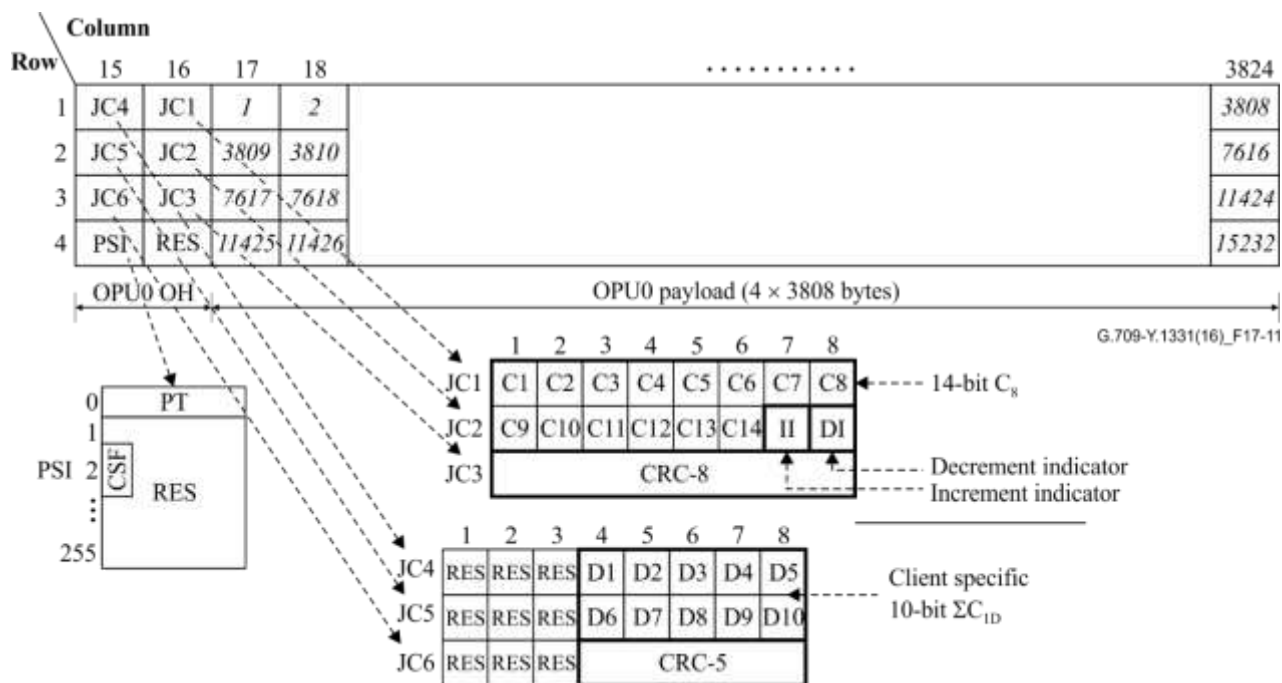


Figure 17-11 – OPU0 frame structure for the mapping of a sub-1.238 Gbit/s client signal

Table 17-4 –  $m$ ,  $n$  and  $C_{nD}$  for sub-1.238G clients into OPU0

Client signal	Nominal bit rate (kbit/s)	Bit rate tolerance (ppm)	$m$	$n$	$C_{nD}$
Transcoded 1000BASE-X (see clause 17.7.1.1)	$15/16 \times 1\,250\,000$	$\pm 100$	8	8	No
STM-1	155 520	$\pm 20$	8	1	Yes
STM-4	622 080	$\pm 20$	8	1	Yes
FC-100	1 062 500	$\pm 100$	8	8	No
SBCON/ESCON	200 000	$\pm 200$	8	8	No
DVB-ASI	270 000	$\pm 100$	8	8	No
SDI	270 000	$\pm 2.8$	8	TBD	TBD

**Table 17-5 – Replacement signal for sub-1.238G clients**

Client signal	Replacement signal	Bit-rate tolerance (ppm)
STM-1	Generic-AIS	±20
STM-4	Generic-AIS	±20
1000BASE-X	Link Fault	±100
FC-100	NOS	±100
SBCON/ESCON	NOS	±200
DVB-ASI	Generic-AIS	±100
SDI	Generic-AIS	For further study

### 17.7.1.1 1000BASE-X transcoding

The 1000BASE-X signal (8B/10B coded, nominal bit rate of 1 250 000 kbit/s and a bit-rate tolerance up to ±100 ppm) is synchronously mapped into a 75-octet GFP-T frame stream with a bit rate of  $15/16 \times 1\,250\,000$  kbit/s ±100 ppm (approximately 1 171 875 kbit/s ±100 ppm). This process is referred to as "timing transparent transcoding (TTT)". The  $15/16 \times 1\,250\,000$  kbit/s ±100 ppm signal is then mapped into an OPU0 by means of the generic mapping procedure as specified in clause 17.7.1 and Annex D.

For 1000BASE-X client mapping, 1-bit timing information (C<sub>1</sub>) is not needed, so OPU0 JC4/JC5/JC6 OH value will be fixed to all-0s.

The mapping of the 1000BASE-X signal into GFP-T is performed as specified in [ITU-T G.7041] with the following parameters:

- Each GFP-T frame contains one superblock
- The 65B\_PAD character is not used
- GFP idle frames are not used
- The GFP frame pFCS is not used.

During a signal fail condition of the incoming 1000BASE-X client signal (e.g., in the case of a loss of input signal), either:

- This failed incoming 1000BASE-X signal is replaced by a stream of 10B blocks, with a bit rate of 1 250 000 kbit/s ±100 ppm, each carrying a link fault indication as specified in [IEEE 802.3], which stream is then applied at the GFP-T mapper, or
- The GFP-T signal is replaced by a stream of GFP client signal fail (CSF) and GFP-idle frames as specified in [ITU-T G.7041] with a bit rate of  $15/16 \times 1\,250\,000$  kbit/s ±100 ppm.

During either

- A signal fail condition of the incoming ODU0/OPU0 signal (e.g., in the case of an ODU0-AIS, ODU0-LCK, ODU0-OCI condition), or
- Incoming CSF frames as specified in [ITU-T G.7041].

The GFP-T de-mapper process generates a stream of 10B blocks, with each block carrying a link fault indication as specified in [IEEE 802.3] as a replacement signal for the lost 1000BASE-X signal.

NOTE – The Ethernet link fault indication is a stream of repeating /C1/C2/C1/C2/ ... ordered sets, where C1 = /K28.5/D21.5/D0.0/D0.0/ and C2 = /K28.5/D2.2/D0.0/D0.0/. This character stream is then processed by the GFP-T mapper process in the same manner as if it were the received 8B/10B data stream, mapping it into GFP-T superblocks for transmission.

### 17.7.1.2 FC-100

During a signal fail condition of the incoming FC-100 signal (e.g., in the case of a loss of input signal), this failed incoming FC-100 signal is replaced by an NOS primitive sequence as specified in [b-INCITS 470].

NOTE – The NOS primitive sequence ordered set is defined as /K28.5/D21.2/D31.5/D5.2/.

During a signal fail condition of the incoming ODU0 signal (e.g., in the case of an ODU0-AIS, ODU0-LCK, ODU0-OCI condition), NOS primitive sequence ordered sets as specified in [b-INCITS 470] are generated as a replacement signal for the lost FC-100 signal.

### 17.7.1.3 SBCON/ESCON

During a signal fail condition of the incoming SBCON/ESCON signal (e.g., in the case of a loss of input signal), this failed incoming SBCON/ESCON signal is replaced by an NOS sequence as specified in [b-ANSI INCITS 296].

NOTE – The NOS sequence ordered set is defined as /K28.5/D0.2/.

During a signal fail condition of the incoming ODU0 signal (e.g., in the case of an ODU0-AIS, ODU0-LCK, ODU0-OCI condition), NOS sequence ordered sets as specified in [b-ANSI INCITS 296] are generated as a replacement signal for the lost SBCON/ESCON signal.

## 17.7.2 Mapping a supra-1.238 to sub-2.488 Gbit/s CBR client signal into OPU1

Table 17-6 specifies the clients defined by this Recommendation and their GMP  $m$ ,  $n$  and  $C_{nD}$  parameter values. Table 17-7 specifies the replacement signals for those clients.

The support for 8-bit timing information ( $\Sigma C_{8D}$ ) in the OPU1 JC4/JC5/JC6 OH is required.

The support for 1-bit timing information ( $\Sigma C_{1D}$ ) in the OPU1 JC4/JC5/JC6 OH is client dependent.

The OPU1 payload for this mapping consists of  $4 \times 3808$  bytes. The groups of 2 bytes in the OPU1 payload area are numbered from 1 to 7616. The OPU1 payload byte numbering for GMP 2-byte (16-bit) blocks is illustrated in Figure 17-12. In row 1 of the OPU1 frame the first 2-bytes will be labelled 1, the next 2-bytes will be labelled 2, etc.

Groups of sixteen successive bits of the client signal are mapped into a group of 2 successive bytes of the OPU1 payload area under control of the GMP data/stuff control mechanism. Each group of 2 bytes in the OPU1 payload area may either carry 16 client bits, or carry 16 stuff bits. The stuff bits are set to zero.

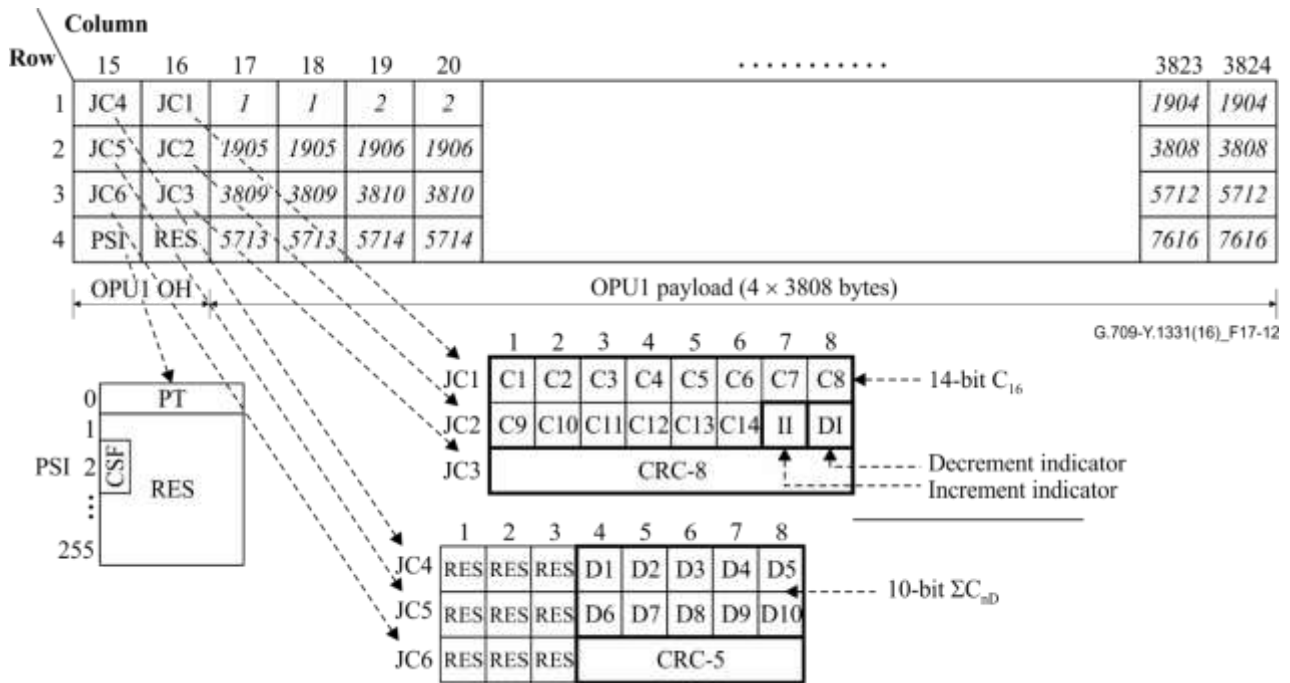


Figure 17-12 – OPU1 frame structure for the mapping of a supra-1.238 to sub-2.488 Gbit/s client signal

Table 17-6 –  $C_m$  ( $m=16$ ) for supra-1.238 to sub-2.488G clients into OPU1

Client signal	Nominal bit rate (kbit/s)	Bit-rate tolerance (ppm)	m	n	$C_{nD}$
FC-200	2 125 000	±100	16	8	Yes
1.5G SDI	1 485 000	±10	16	TBD	Yes
1.5G SDI	1 485 000/1.001	±10	16	TBD	Yes

Table 17-7 – Replacement signal for supra-1.238 to sub-2.488 Gbit/s clients

Client signal	Replacement signal	Bit-rate tolerance (ppm)
FC-200	NOS	±100
1.5G SDI	Generic-AIS	For further study

### 17.7.2.1 FC-200

During a signal fail condition of the incoming FC-200 signal (e.g., in the case of a loss of input signal), this failed incoming FC-200 signal is replaced by an NOS primitive sequence as specified in [b-INCITS 470].

NOTE – The NOS primitive sequence ordered set is defined as /K28.5/D21.2/D31.5/D5.2/.

During a signal fail condition of the incoming ODU1 signal (e.g., in the case of an ODU1-AIS, ODU1-LCK, ODU1-OCI condition), NOS primitive sequence ordered sets as specified in [b-INCITS 470] are generated as a replacement signal for the lost FC-200 signal.

### 17.7.3 Mapping CBR client signals into OPU2

Table 17-8 specifies the clients defined by this Recommendation and their GMP m, n and  $C_{nD}$  parameter values. Table 17-9 specifies the replacement signals for those clients.

The support for 8-bit timing information ( $\Sigma C_{8D}$ ) in the OPU2 JC4/JC5/JC6 OH is required.

The support for 1-bit timing information ( $\Sigma C_{1D}$ ) in the OPU2 JC4/JC5/JC6 OH is client dependent.

The OPU2 payload for this mapping consists of  $4 \times 3808$  bytes. The groups of eight bytes in the OPU2 payload area are numbered from 1 to 1904. The OPU2 payload byte numbering for GMP 8-byte (64-bit) blocks is illustrated in Figure 17-13. In row 1 of the OPU2 frame the first 8-bytes will be labelled 1, the next 8-bytes will be labelled 2, etc.

Groups of sixty-four successive bits of the client signal are mapped into a group of eight successive bytes of the OPU2 payload area under control of the GMP data/stuff control mechanism. Each group of eight bytes in the OPU2 payload area may either carry 64 client bits, or carry 64 stuff bits. The stuff bits are set to zero.

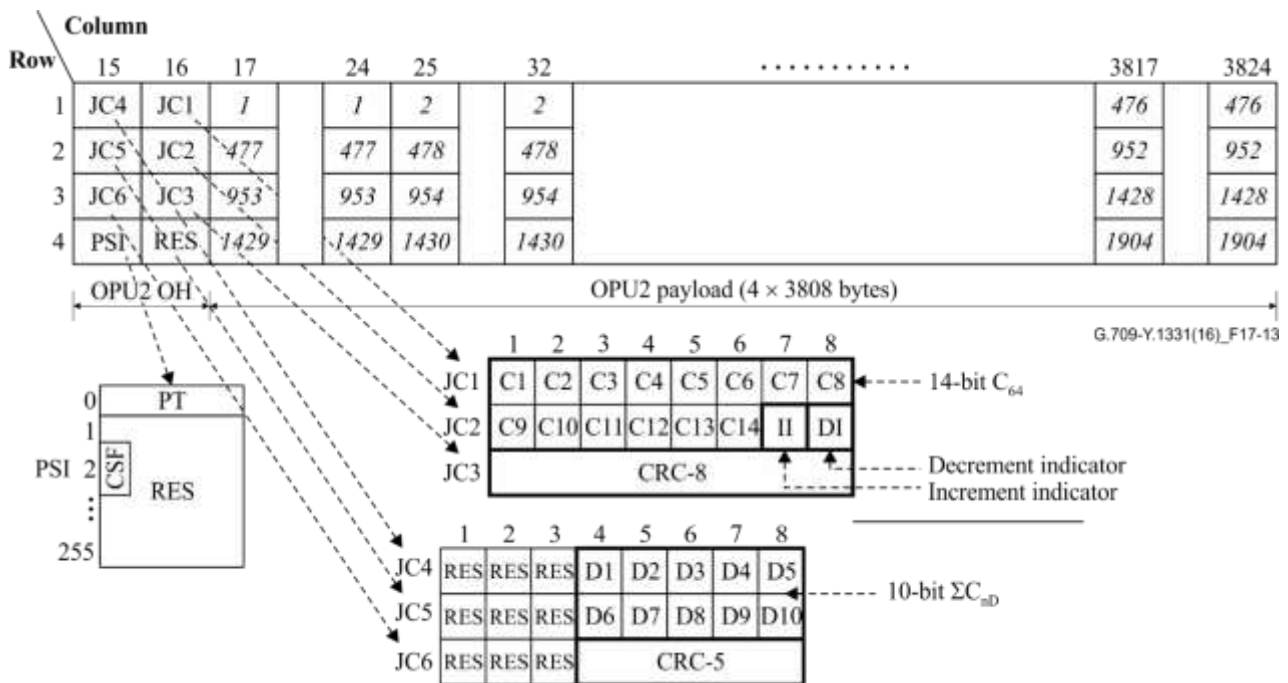


Figure 17-13 – OPU2 frame structure for the mapping of a CBR client signal

Table 17-8 – m, n and  $C_{nD}$  for CBR clients into OPU2

Client signal	Nominal bit rate (kbit/s)	Bit rate tolerance (ppm)	m	n	$C_{nD}$
For further study					

Table 17-9 – Replacement signal for CBR clients

Client signal	Replacement signal	Bit-rate tolerance (ppm)
For further study		

#### 17.7.4 Mapping CBR client signals into OPU3

Table 17-10 specifies the clients defined by this Recommendation and their GMP m, n and  $C_{nD}$  parameter values. Table 17-11 specifies the replacement signals for those clients.

The support for 8-bit timing information ( $\Sigma C_{8D}$ ) in the OPU3 JC4/JC5/JC6 OH is required.

The support for 1-bit timing information ( $\Sigma C_{1D}$ ) in the OPU3 JC4/JC5/JC6 OH is client dependent.

The OPU3 payload for this mapping consists of  $4 \times 3808$  bytes. The groups of 32 bytes in the OPU3 payload area are numbered from 1 to 476. The OPU3 payload byte numbering for GMP 32-byte (256-bit) blocks is illustrated in Figure 17-14. In row 1 of the OPU3 frame the first 32-bytes will be labelled 1, the next 32-bytes will be labelled 2, etc.

Groups of two hundred-fifty-six successive bits of the client signal are mapped into a group of 32 successive bytes of the OPU3 payload area under control of the GMP data/stuff control mechanism. Each group of 32 bytes in the OPU3 payload area may either carry 256 client bits, or carry 256 stuff bits. The stuff bits are set to zero.

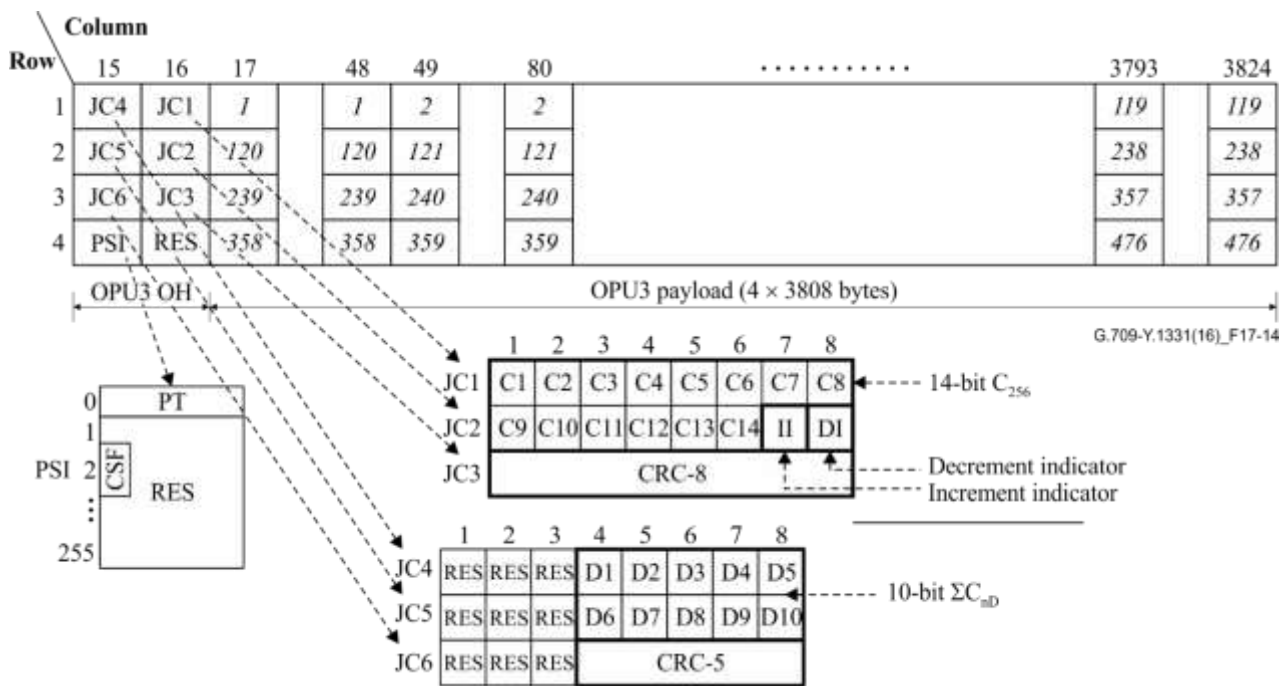


Figure 17-14 – OPU3 frame structure for the mapping of a CBR client signal

Table 17-10 – m, n and  $C_{nD}$  for CBR clients into OPU3

Client signal	Nominal bit rate (kbit/s)	Bit rate tolerance (ppm)	m	n	$C_{nD}$
Transcoded 40GBASE-R (see clause 17.7.4.1)	$1027/1024 \times 64/66 \times 41\,250\,000$	$\pm 100$	256	8	Yes

Table 17-11 – Replacement signal for CBR clients

Client signal	Replacement signal	Bit-rate tolerance (ppm)
40GBASE-R	Continuous 40GBASE-R local fault sequence ordered sets with four PCS lane alignment markers inserted after each 16383 x 4 sixty-six-bit blocks	$\pm 100$

A 40GBASE-R local fault sequence ordered set is a 66B control block (sync header = 10) with a block type of 0x4B, an "O" code of 0x00, a value of 0x01 to indicate "local fault" in lane 3, and all of the other octets (before scrambling) equal to 0x00.

#### **17.7.4.1 40GBASE-R multi-lane processing and transcoding**

The 40GBASE-R client signal (64B/66B encoded, nominal aggregate bit-rate of 41 250 000 kbit/s,  $\pm 100$  ppm) is recovered using the process described in Annex E for parallel 64B/66B interfaces. The lane(s) of the physical interface are bit-disinterleaved, if necessary, into four streams of 10 312 500 kbit/s. 66B block lock and lane alignment marker lock are acquired on each PCS lane, allowing the 66B blocks to be de-skewed and reordered.

The resulting sequence is descrambled and transcoded according to the process described in Annex B into 513B code blocks. Each pair of two 513B code blocks is combined according to the process described in Annex F into a 1027B block, resulting in a bit stream of  $1027/1024 \times 40\,000\,000$  kbit/s  $\pm 100$  ppm (40,117,187.500 kbit/s  $\pm 100$  ppm). This process is referred to as "timing transparent transcoding (TTT)", mapping a bit stream which is 1027/1056 times the bit-rate of the aggregate Ethernet signal.

In the mapper, the received Ethernet PCS lane BIP may be compared with the expected Ethernet PCS lane BIP as a non-intrusive monitor.

The de-mapper will insert a compensated Ethernet PCS lane BIP as described in Annex E. In addition, as described in Annex E, the combined error mask resulting from the PCS BIP-8 error mask and the OTN BIP-8 error mask may be used as a non-intrusive monitor.

For 40GBASE-R client mapping, 1-bit timing information ( $C_1$ ) is not needed.

The de-mapper will recover from the output of the GMP processor 1027B block lock, and then trans-decode each 1027B block to sixteen 66B blocks as described in Annex E. Trans-decoded lane alignment markers are constructed with a compensated BIP-8. The 66B blocks are then re-distributed round-robin to PCS lanes. If the number of PCS lanes is greater than the number of physical lanes of the egress interface, the appropriate numbers of PCS lanes are bit-multiplexed onto the physical lanes of the egress interface.

#### **17.7.5 Mapping CBR client signals into OPU4**

Table 17-12 specifies the clients defined by this Recommendation and their GMP  $m$ ,  $n$  and  $C_{nD}$  parameter values. Table 17-13 specifies the replacement signals for those clients.

The support for 8-bit timing information ( $\Sigma C_{8D}$ ) in the OPU4 JC4/JC5/JC6 OH is required.

The support for 1-bit timing information ( $\Sigma C_{1D}$ ) in the OPU4 JC4/JC5/JC6 OH is client dependent.

The OPU4 payload for this mapping consists of  $4 \times 3800$  bytes for client data and  $4 \times 8$  bytes with fixed stuff. The groups of 80 bytes in the OPU4 payload area are numbered from 1 to 190. The OPU4 payload byte numbering for GMP 80-byte (640-bit) blocks is illustrated in Figure 17-15. In row 1 of the OPU4 frame the first 80-bytes will be labelled 1, the next 80-bytes will be labelled 2, etc.

Groups of six hundred and forty successive bits of the client signal are mapped into a group of 80 successive bytes of the OPU4 payload area under control of the GMP data/stuff control mechanism. Each group of 80 bytes in the OPU4 payload area may either carry 640 client bits, or carry 640 stuff bits. The stuff bits are set to zero.

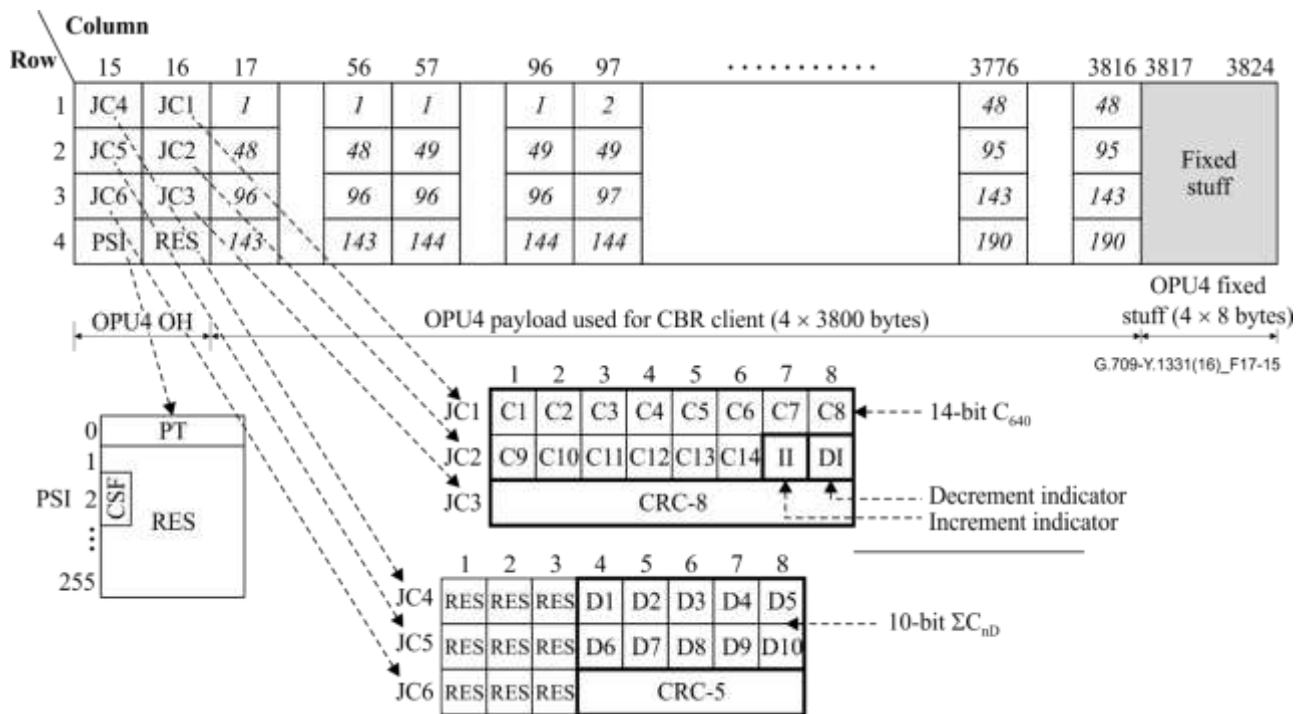


Figure 17-15 – OPU4 frame structure for the mapping of a CBR client signal

Table 17-12 – m, n and C<sub>nd</sub> for CBR clients into OPU4

Client signal	Nominal bit rate (kbit/s)	Bit-rate tolerance (ppm)	m	n	C <sub>nd</sub>
100GBASE-R (see 17.7.5.1)	103 125 000	±100	640	8	Yes

Table 17-13 – Replacement signal for CBR clients

Client signal	Replacement signal	Bit-rate tolerance (ppm)
100GBASE-R (see 17.7.5.1)	Continuous 66B encoded and scrambled 100GBASE-R local fault sequence ordered sets with 20 PCS lane alignment markers inserted after each 16383 x 20 sixty-six-bit blocks	±100

A 66B encoded and scrambled 100GBASE-R local fault sequence ordered set is a 66B control block (sync header = 10) with a block type of 0x4B, an "O" code of 0x00, a value of 0x01 to indicate a "local fault" in lane 3, and all of the other octets (before scrambling) equal to 0x00. A self-synchronizing scrambler with generator polynomial  $1 + x^{39} + x^{58}$  shall be used, which is identical to the scrambler specified in clause 49.2.6 of [IEEE 802.3].

### 17.7.5.1 100GBASE-R multi-lane processing

The 100GBASE-R client signal (64B/66B encoded, nominal aggregate bit-rate of 103 125 000 kbit/s ±100 ppm) is recovered using the process described in Annex E for parallel 64B/66B interfaces. The lane(s) of the physical interface are bit-disinterleaved, if necessary, into twenty streams of 5 161 250 kbit/s. 66B block lock and lane alignment marker lock are acquired on each PCS lane, allowing the 66B blocks to be de-skewed and reordered.

In the mapper, the received Ethernet PCS lane BIP may be compared with the expected Ethernet PCS lane BIP as a non-intrusive monitor.



The de-mapper will pass through the PCS lane BIP from the ingress as described in Annex E. In addition, the received Ethernet PCS lane BIP may be compared with the expected Ethernet PCS lane BIP as a non-intrusive monitor.

For 100GBASE-R client mapping, 1-bit timing information ( $C_1$ ) is not needed.

The de-mapper will recover from the output of the GMP processor 64B/66B block lock per the state diagram in Figure 82-10 [IEEE 802.3]. The 66B blocks are re-distributed round-robin to PCS lanes. If the number of PCS lanes is greater than the number of physical lanes of the egress interface, the appropriate numbers of PCS lanes are bit-multiplexed onto the physical lanes of the egress interface.

## **17.8 Mapping a 1000BASE-X and FC-1200 signal via timing transparent transcoding into OPUk**

### **17.8.1 Mapping a 1000BASE-X signal into OPU0**

Refer to clause 17.7.1 for the mapping of the transcoded 1000BASE-X signal and to clause 17.7.1.1 for the transcoding of the 1000BASE-X signal.

### **17.8.2 Mapping an FC-1200 signal into OPU2e**

The nominal line rate for FC-1200 is 10 518 750 kbit/s  $\pm$  100 ppm, and must therefore be compressed to a suitable rate to fit into an OPU2e.

The adaptation of the 64B/66B encoded FC-1200 client is done by transcoding a group of eight 66B blocks into one 513B block (as described in Annex B), assembling eight 513B blocks into one 516-octet superblock and encapsulating seventeen 516-octet superblocks into an 8800 octet GFP frame as illustrated in Figure 17-17. The GFP frame consists of 2200 rows with 32 bits per row. The first row contains the GFP core header, the second row the GFP payload header. The next four rows contain 16 bytes reserved for future international standardization. The next seventeen times 129 rows contain the seventeen superblocks #1 to #17. The last row contains the GFP payload FCS. The flag (F) bit of 513B block # $i$  ( $i = 0..7$ ) is carried in Flag # $i$  bit located in the superblock flags field. The remaining 512 bits of each of the eight 513B blocks of a superblock are carried in 16 rows of the superblock data field; bits of 513B block #0 in the first 16 rows of the superblock, bits of 513B block #1 in the next 16 rows, etc. Each 513B block contains 'j' ( $j = 0..8$ ) control blocks (CB1 to CBj) and '8-j' all-data blocks (DB1..DB8-j) as specified in Annex B. Figure 17-17 presents a 513B block with three control blocks and five all-data blocks. A 513B block may contain zero to eight control blocks and a superblock may contain thus zero to sixty-four control blocks.

NOTE 1 – The GFP encapsulation stage does not generate GFP-idle frames and therefore the generated GFP stream is synchronous to the FC-1200 client stream. The adaptation process performs a 50/51 rate compression, so the resulting GFP stream has a signal bit rate of  $50/51 \times 10.51875$  Gbit/s  $\pm$  100 ppm (i.e., 10 312 500 kbit/s  $\pm$  100 ppm).

The stream of 8800 octet GFP frames is byte-synchronous mapped into the OPU2e payload by aligning the byte structure of every GFP frame with the byte structure of the OPU2e payload (see Figure 17-16). Sixty-four fixed stuff (FS) bytes are added in columns 1905 to 1920 of the OPU2e payload. All the GFP frames have the same length (8800 octets). The GFP frames are not aligned with the OPU2e payload structure and may cross the boundary between two OPU2e frames.

During a signal fail condition of the incoming FC-1200 signal (e.g., in the case of a loss of input signal), this failed incoming FC-1200 signal is replaced by a stream of 66B blocks, with each block carrying two local fault sequence ordered sets as specified in [b-ANSI INCITS 364]. This replacement signal is then applied at the transcoding process.

NOTE 2 – Local fault sequence ordered set is /K28.4/D0.0/D0.0/D1.0/. The 66B block contains the following value SH=10 0x55 00 00 01 00 00 00 01.

During a signal fail condition of the incoming ODU2e/OPU2e signal (e.g., in the case of an ODU2e-AIS, ODU2e-LCK, ODU2e-OCI condition) a stream of 66B blocks, with each block carrying

two local fault sequence ordered sets as specified in [b-ANSI INCITS 364] is generated as a replacement signal for the lost FC-1200 signal.

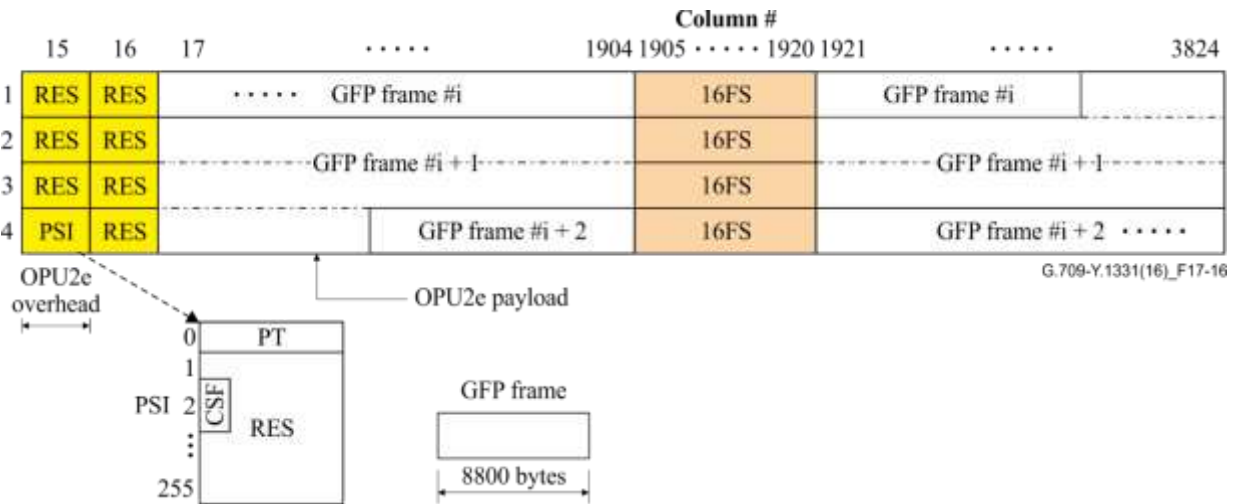


Figure 17-16 – Mapping of transcoded FC-1200 into OPU2e

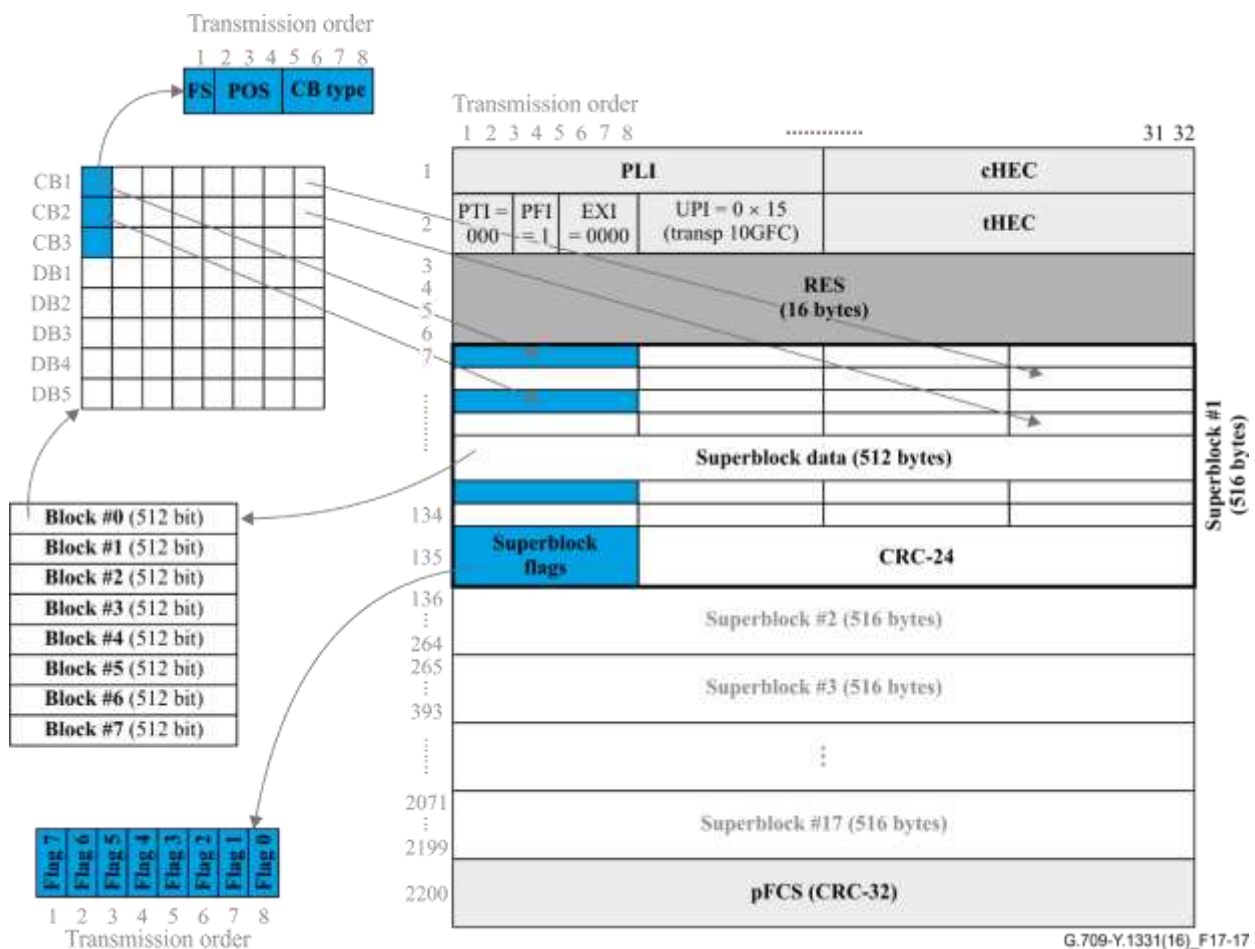


Figure 17-17 – GFP frame format for FC-1200

GFP framing is used to facilitate delineation of the superblock structure by the receiver. The leading flag bits from each of the eight 513B blocks are relocated into a single octet at the end of the 513-octet superblock data field (labelled "Superblock flags").

To minimize the risk of incorrect decoding due to errors in the 1 to 65 octets of "control" information (Flags, FC, POS, CB\_Type), a CRC-24 is calculated over the 65 octets within each superblock that may contain such "control" information and appended to form a 516 octet superblock. The 65 octets in the 516-octet superblock over which the CRC-24 is calculated are the octets  $(1+8n)$  with  $n=0..64$  (i.e., octets 1, 9, 17, ..., 513). The generator polynomial for the CRC-24 is  $G(x) = x^{24} + x^{21} + x^{20} + x^{17} + x^{15} + x^{11} + x^9 + x^8 + x^6 + x^5 + x + 1$  with an all-ones initialization value, where  $x^{24}$  corresponds to the MSB and  $x^0$  to the LSB. This superblock CRC is generated by the source adaptation process using the following steps:

- 1) The 65 octets of "control" information (Flags, POS, CB\_Type) are taken in network octet order (see Figure 17-17), most significant bit first, to form a 520-bit pattern representing the coefficients of a polynomial  $M(x)$  of degree 519.
- 2)  $M(x)$  is multiplied by  $x^{24}$  and divided (modulo 2) by  $G(x)$ , producing a remainder  $R(x)$  of degree 23 or less.
- 3) The coefficients of  $R(x)$  are considered to be a 24-bit sequence, where  $x^{23}$  is the most significant bit.
- 4) After inversion, this 24-bit sequence is the CRC-24.

Exactly 17 of these 516-octet superblocks are prefixed with the standard GFP core and type headers and 16 octets of "reserved" (padding). Because the number of 516-octet superblocks per GFP frame is known a priori, it is possible for this mapping scheme to operate in a cut-through (as opposed to store and forward) fashion, thus minimizing the mapping latency.

The payload FCS (a CRC-32) is appended to the end of each GFP frame and is calculated across the payload information field of the GFP frame as per [ITU-T G.7041]. The purpose of the payload FCS is to provide visibility of bit errors occurring anywhere in the GFP payload information field and thus augments the coverage provided by the per-superblock CRC-24 (which only provides coverage for the "control" overhead in each superblock). The payload FCS is only for the purposes of gathering statistics.

All octets in the GFP payload area are scrambled using the  $X^{43} + 1$  self-synchronous scrambler, again as per [ITU-T G.7041].

## 17.9 Mapping a supra-2.488 Gbit/s CBR signal into OPUflex using BMP

Mapping of a supra-2.488 Gbit/s CBR client signal (with up to  $\pm 100$  ppm bit-rate tolerance) into an OPUflex is performed by a bit-synchronous mapping procedure (BMP). Table 17-14 specifies the clients defined by this Recommendation.

The bit-synchronous mapping process deployed to map constant bit rate client signals into an OPUflex does not generate any justification control signals.

The OPUflex clock for the bit-synchronous mapping is derived from the client signal. During a signal fail condition of the incoming client signal (e.g., in the case of a loss of input signal), this failed incoming signal is replaced by the appropriate replacement signal as defined in Table 17-15. The OPUflex payload signal bit rate shall be within the limits specified in Table 7-3 and the limits for the ODCb clock defined in [ITU-T G.8251] and no frame phase discontinuity shall be introduced in this case and when resynchronization on the incoming client signal.

During a signal fail condition of the incoming ODUflex/OPUflex signal (e.g., in the case of an ODUflex-AIS, ODUflex-LCK, ODUflex-OCI condition), the failed client signal is replaced by the appropriate replacement signal as defined in Table 17-15.

The OPUflex overhead for this mapping consists of:

- A payload structure identifier (PSI) including the payload type (PT) as specified in Table 15-9, the client signal fail (CSF) and 254 bytes plus 7 bits reserved for future international standardization (RES);
- Three justification control (JC) bytes, consisting of two bits for justification control (with fixed 00 value) and six bits reserved for future international standardization;
- One negative justification opportunity (NJO) byte (carrying a justification byte); and
- Three bytes reserved for future international standardization (RES).

NOTE – To allow the use of a common asynchronous/bit-synchronous de-mapper circuit for CBR client signals into ODUk (k=1,2,3 and flex), JC, NJO and PJO fields are assumed to be present in the OPUflex frame structure for the mapping of a supra-2.488G CBR client signal (Figure 17-18). This OPUflex frame structure is now compatible with the OPUk frame structure for the mapping of a CBR2G5, CBR10G or CBR40G signal (Figure 17-1). As a CBR signal is mapped into the OPUflex without justification, the NJO field contains a justification byte (stuff), the PJO field contains a data byte (D), and the JC bits are fixed to 00.

The OPUflex payload for this mapping consists of  $4 \times 3808$  bytes (Figure 17-18). Groups of eight successive bits (not necessarily being a byte) of the client signal are mapped into a data (D) byte of the OPUflex payload area under control of the BMP control mechanism. Each data byte in the OPUflex payload area carries 8 client bits.

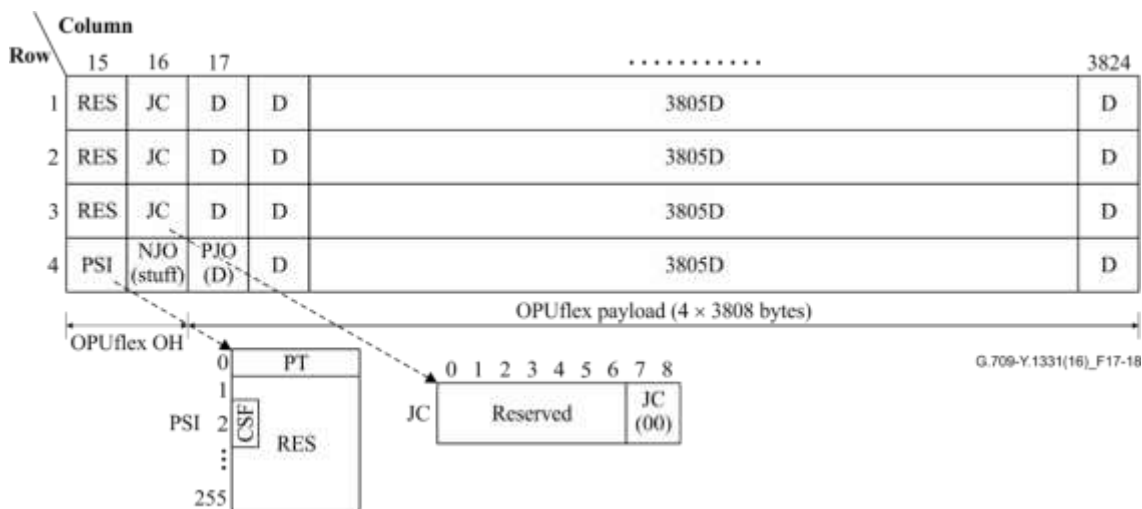


Figure 17-18 – OPUflex frame structure for the mapping of a supra-2.488 Gbit/s client signal

Table 17-14 – supra-2.488G CBR clients

Client signal	Nominal bit rate (kbit/s)	Bit-rate tolerance (ppm)
<b>FC-400</b>	4 250 000	±100
<b>FC-800</b>	8 500 000	±100
<b>FC-1600</b>	14 025 000	±100
<b>FC-3200</b>	28 050 000	±100
<b>IB SDR</b>	2 500 000	±100
<b>IB DDR</b>	5 000 000	±100
<b>IB QDR</b>	10 000 000	±100
<b>3G SDI</b>	2 970 000	± 10
<b>3G SDI</b>	2 970 000/1.001	±10

**Table 17-15 – Replacement signal for supra-2.488 Gbit/s clients**

Client signal	Replacement signal	Bit-rate tolerance (ppm)
<b>FC-400</b>	NOS	±100
<b>FC-800</b>	NOS	±100
<b>FC-1600</b>	NOS	±100
<b>FC-3200</b>	NOS	±100
<b>IB SDR</b>	For further study	±100
<b>IB DDR</b>	For further study	±100
<b>IB QDR</b>	For further study	±100
<b>3G SDI</b>	Generic-AIS	For further study

**17.9.1 FC-400 and FC-800**

During a signal fail condition of the incoming FC-400/FC-800 signal (e.g., in the case of a loss of input signal), this failed incoming FC-400/FC-800 signal is replaced by an NOS primitive sequence as specified in [b-INCITS 470].

NOTE – The NOS primitive sequence ordered set is defined as /K28.5/D21.2/D31.5/D5.2/.

During a signal fail condition of the incoming ODUflex signal (e.g., in the case of an ODUflex-AIS, ODUflex-LCK, ODUflex-OCI condition), NOS primitive sequence ordered sets as specified in [b-INCITS 470] are generated as a replacement signal for the lost FC-400/FC-800 signal.

**17.9.2 FC-1600**

The characteristic information of the mapped FC-1600 client signal consists of a sequence of 64B/66B encoded blocks with a nominal bit-rate of 14 025 000 kbit/s, ±100 ppm.

In case the FC-1600 interface at the mapper has FEC enabled the mapper must recover the FEC code word synchronization, extract the FEC parity bits, perform error correction and transdecode the 64B/65B blocks to 64B/66B blocks as specified in [b-INCITS 470].

In case the FC-1600 interface at the demapper has FEC enabled the demapper must recover 66B block lock from the demapped CBR signal, transcode the 64B/66B blocks to 64/65B blocks, generate and insert the FEC parity bits as specified in [b-INCITS 470].

NOTE – FC-1600 interface ports designed prior to Edition 4.6 may not be able to support termination of the FEC or transdecoding of 64B/65B blocks.

During a signal fail condition of the incoming FC-1600 signal (e.g., in the case of a loss of input signal), this failed incoming FC-1600 signal is replaced by a NOS primitive sequence as specified in [b-INCITS 470].

During signal fail condition of the incoming ODUflex signal (e.g., in the case of an ODUflex-AIS, ODUflex-LCK, ODUflex-OCI condition), NOS primitive sequence ordered sets as specified in [b-INCITS 470] are generated as a replacement signal for the lost FC-1600 signal.

**17.9.3 FC-3200**

The characteristic information of the mapped FC-3200 client signal consists of a sequence of 64B/66B encoded blocks with a nominal bit-rate of 28 050 000 kbit/s, ±100 ppm.

The mapper must recover the FEC code word synchronization, extract the FEC parity bits, perform error correction and transdecode the 256B/257B blocks to 64B/66B blocks as specified in [b-INCITS 488]. Uncorrectable FEC code words shall be replaced with error control blocks at the output of the transdecoder.

The demapper must recover 66B block lock from the demapped CBR signal, transcode the 64B/66B blocks to 256B/257B blocks, generate and insert the FEC parity bits as specified in [b-INCITS 488].

During a signal fail condition of the incoming FC-3200 signal (e.g., in the case of a loss of input signal), this failed incoming FC-3200 signal is replaced by a NOS primitive sequence as specified in [b-INCITS 488] at the output of the transdecoder.

During signal fail condition of the incoming ODUflex signal (e.g., in the case of an ODUflex-AIS, ODUflex-LCK, ODUflex-OCI condition), NOS primitive sequence ordered sets as specified in [b-INCITS 488] are generated as a replacement signal for the lost FC-3200 signal at the input of the transcoder.

### 17.10 Mapping of packet client signals into OPUk

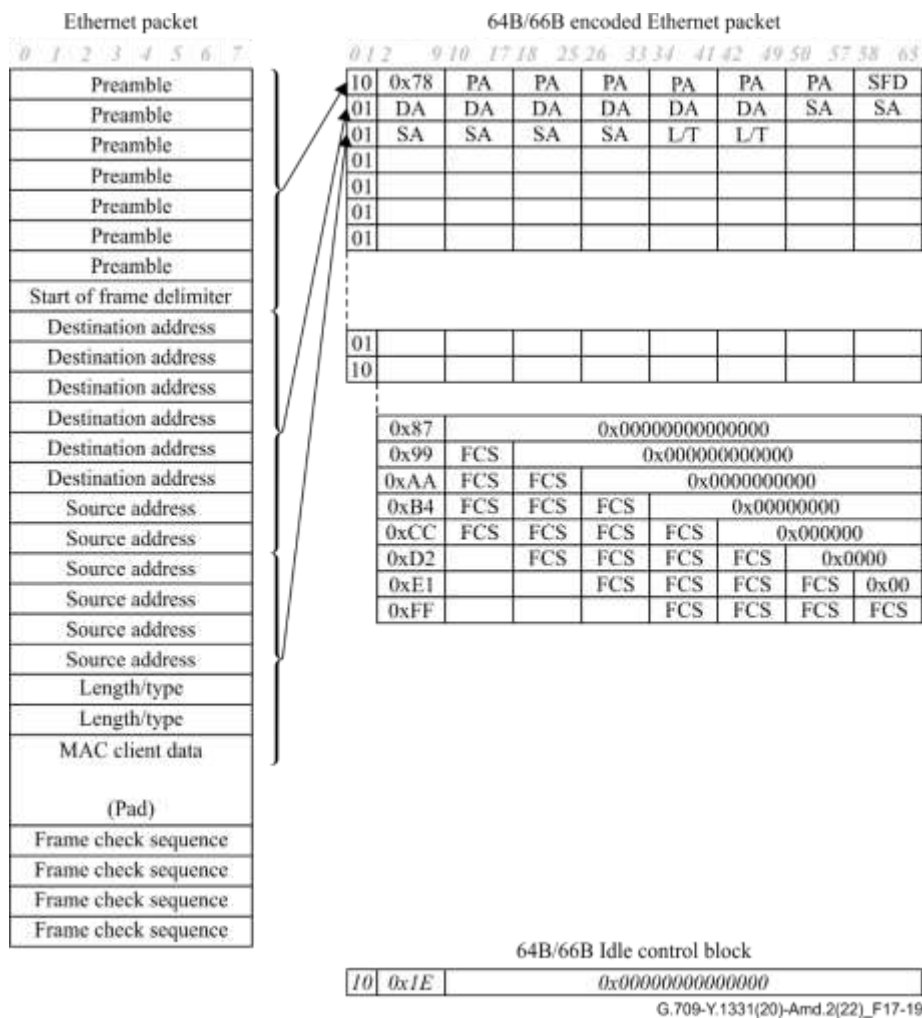
A set of packet client signals with an aggregated bandwidth of less than or equal than-to 100 Gbit/s is encapsulated into GFP-F as specified in [ITU-T G.7041] and then mapped into an OPUk, OPUflex(GFP) or OPUflex(GFP,n,k) as specified in clause 17.4 and 12.2.5.

A set of packet client signals with an aggregate bandwidth of any rate may be presented (see Note) as a stream of Ethernet MAC frames-packets (consisting of preamble (PA) to frame check sequence (FCS) fields) and interframepacket gaps and then 64B/66B encoded as specified in [IEEE 802.3] Table-Figure 82-5 and illustrated in Figure 17-19. This 64B/66B encoded packet client signal is then mapped into an OPUflex(IMP) as specified in clause 17.11.

A set of packet client signals with an aggregated bandwidth of more than 100 Gbit/s may be presented (see Note) as an n×25 Gbit/s stream of Ethernet MAC frames-packets and interframepacket gaps and then 64B/66B encoded as specified in [IEEE 802.3] Table-Figure 82-5 into a FlexE Client signal [OIF FlexE IA] which is then mapped into an OPUflex(IMP,s) as specified in clause 17.11.

A set of packet client signals with an aggregated bandwidth of less than or equal than-to 100 Gbit/s may be presented (see Note) as a 10, 25, 40, 50, 75 or 100 Gbit/s stream of Ethernet MAC frames packets and interframepacket gaps and then 64B/66B encoded as specified in [IEEE 802.3] Table Figure 82-5 into a FlexE Client signal [OIF FlexE IA] which is then mapped into an OPUflex(IMP,s) as specified in clause 17.11.

NOTE – Non Ethernet packet clients are assumed to be encapsulated into Ethernet MAC framespackets before they are presented. Encapsulation is outside the scope of this Recommendation. Ethernet MAC framed-packet clients are presented directly.



**Figure 17-19 – Illustration of 64B/66B encoded Ethernet packet and interpacket gaps**

### 17.11 Mapping of 64B/66B encoded packet client signals into OPUflex using IMP

64B/66B encoded packet client signal bit rates can have any value. Refer to clause 17.10. FlexE Client signal bit rates are  $s \times 5,156,250.000 \text{ kbit/s} \pm 100 \text{ ppm}$ , with  $s = 2, 8, n \times 5$  ( $n \geq 1$ ). Refer to [OIF FlexE IA].

The 66B block stream shall be scrambled after rate adaptation and before mapping into the OPUflex. In the reverse operation, following termination of the OPUflex signal, the 66 block stream will be descrambled before being passed to the packet client (e.g., FlexE Client) layer.

A self-synchronizing scrambler with generator polynomial  $1 + x^{39} + x^{58}$  shall be used, that is identical to the scrambler specified in clause 49.2.6 [IEEE 802.3]. 66B block stream scrambling is required to provide security against false 66B block delineation (as the two sync header bits bypass the scrambler), the 66B code words replicating the OTU and ODU frame alignment signal and the 66B code words combined with the OTU scrambler pattern used for the interface replicating the OTU and ODU frame alignment signal.

Mapping of a 64B/66B encoded packet client (e.g., FlexE Client) signal (with up to  $\pm 100 \text{ ppm}$  bit-rate tolerance) into an OPUflex is performed by the idle mapping procedure (IMP).

- The OPUflex(IMP) payload bit rate is  $X \text{ kbit/s} \pm 100 \text{ ppm}$  and  $X$  is a configured bit rate that can have any value. The ODUflex(IMP) bit rate is  $239/238 \times X \text{ kbit/s} \pm 100 \text{ ppm}$ .
- The OPUflex(IMP,s) payload bit rate is  $s \times 5,156,250.000 \text{ kbit/s} \pm 100 \text{ ppm}$ , with  $s = 2, 8, n \times 5$  ( $n \geq 1$ ). The ODUflex bit rate is  $s \times 239/238 \times 5,156,250.000 \text{ kbit/s} \pm 100 \text{ ppm}$ .

The Idle mapping procedure deploys a clock rate adaptation scheme based on Idle control character (/I) insert/delete as per clause 82.2.3.6 of [IEEE 802.3] and/or sequence ordered set (/O) delete as per clause 82.2.3.9 of [IEEE 802.3].

The OPUflex overhead for this mapping consists of a:

- payload structure identifier (PSI) including the payload type (PT) as specified in Table 15-9, the client signal fail (CSF) and 254 bytes plus 7 bits reserved for future international standardization (RES);
- seven bytes reserved for future international standardization (RES).

The OPUflex payload for this mapping consists of  $4 \times 3808$  bytes (Figure 17-1920). Scrambled 66B blocks of the client signal are mapped into 66-bits of the OPUflex payload area under control of the IMP control mechanism. The 66B blocks are aligned so that the first bit of the sync header appears in one of the bit positions 1, 3, 5, or 7 of a byte in the OPUflex payload.

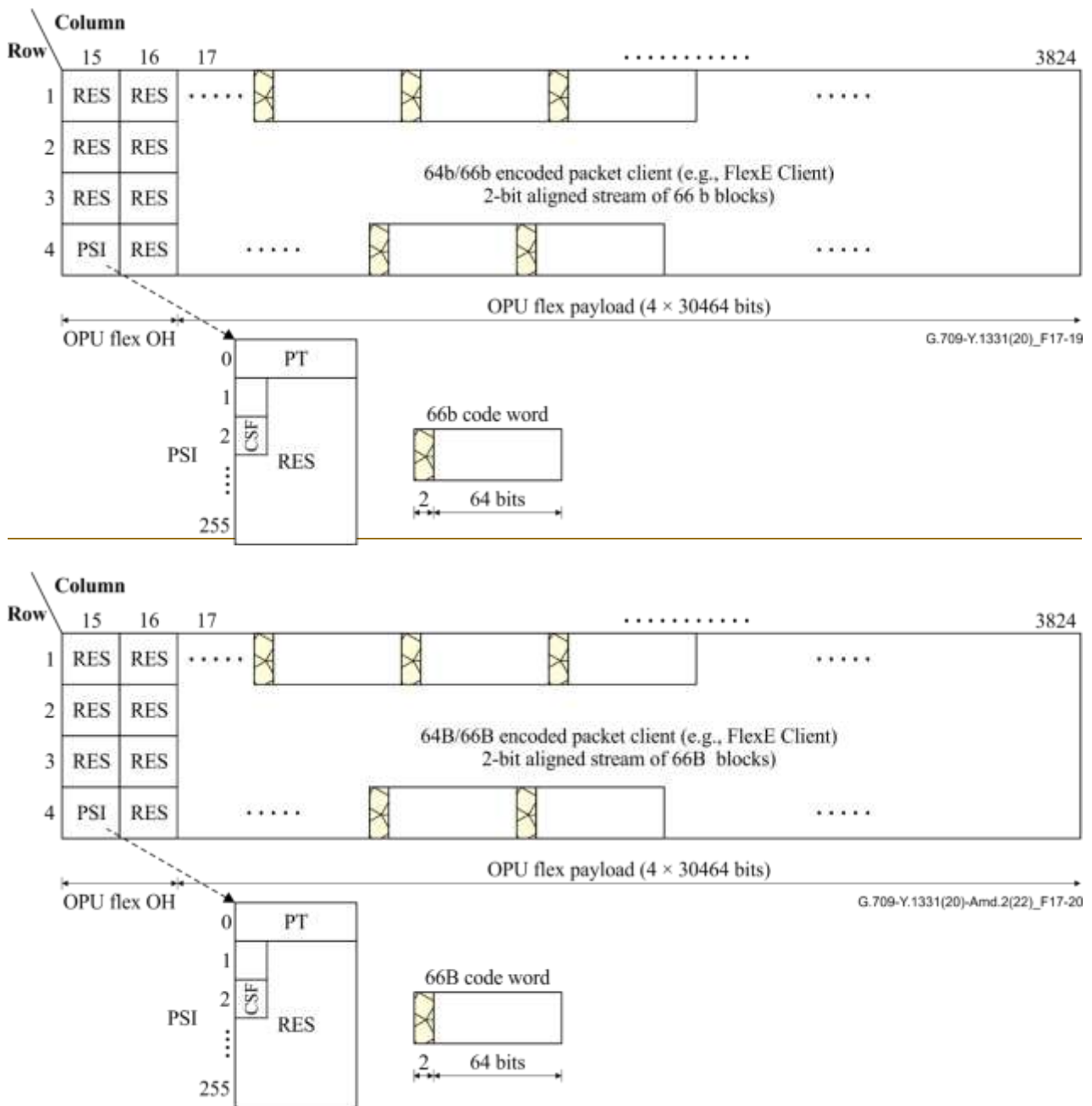


Figure 17-1920 – OPUflex frame structure for the mapping of a FlexE Client signal



During a signal fail condition of the incoming 64B/66B encoded packet client (e.g., FlexE Client) signal (e.g., in the case of a loss of input signal), this failed incoming client signal is replaced by a stream of 66B blocks, with each block carrying one local fault sequence ordered set (as specified in [FlexE IA], [IEEE 802.3]). This replacement signal is then mapped into the OPUflex.

During a signal fail condition of the incoming ODUflex/OPUflex signal (e.g., in the case of an ODUflex-AIS, ODUflex-LCK, ODUflex-OCI condition), a stream of 66B blocks, with each block carrying one local fault sequence ordered sets (as specified in [FlexE IA], [IEEE 802.3]) is generated as a replacement signal for the lost client signal.

NOTE – A 64B/66B encoded packet client (e.g., FlexE Client) signal local fault sequence ordered set is a 66B control block (sync header = 10) with a block type of 0x4B, an "O" code of 0x00, a value of 0x01 to indicate a "local fault" in lane 3, and all of the other octets (before scrambling) equal to 0x00.

## 17.12 Mapping of FlexE aware signals into OPUflex

In the FlexE aware service  $p$  ( $1 \leq p \leq m \leq 252$ ) 100G FlexE Instances – out of an  $m \times 100\text{G}$  FlexE Instance Group signal – are crunched, padded and interleaved as per Figure 17-201. This results in a FlexE partial rate (sub)group signal with a length of  $1024 \times n$  blocks, with  $n = n_1 + n_2 + \dots + n_p$  (FlexEp-n):

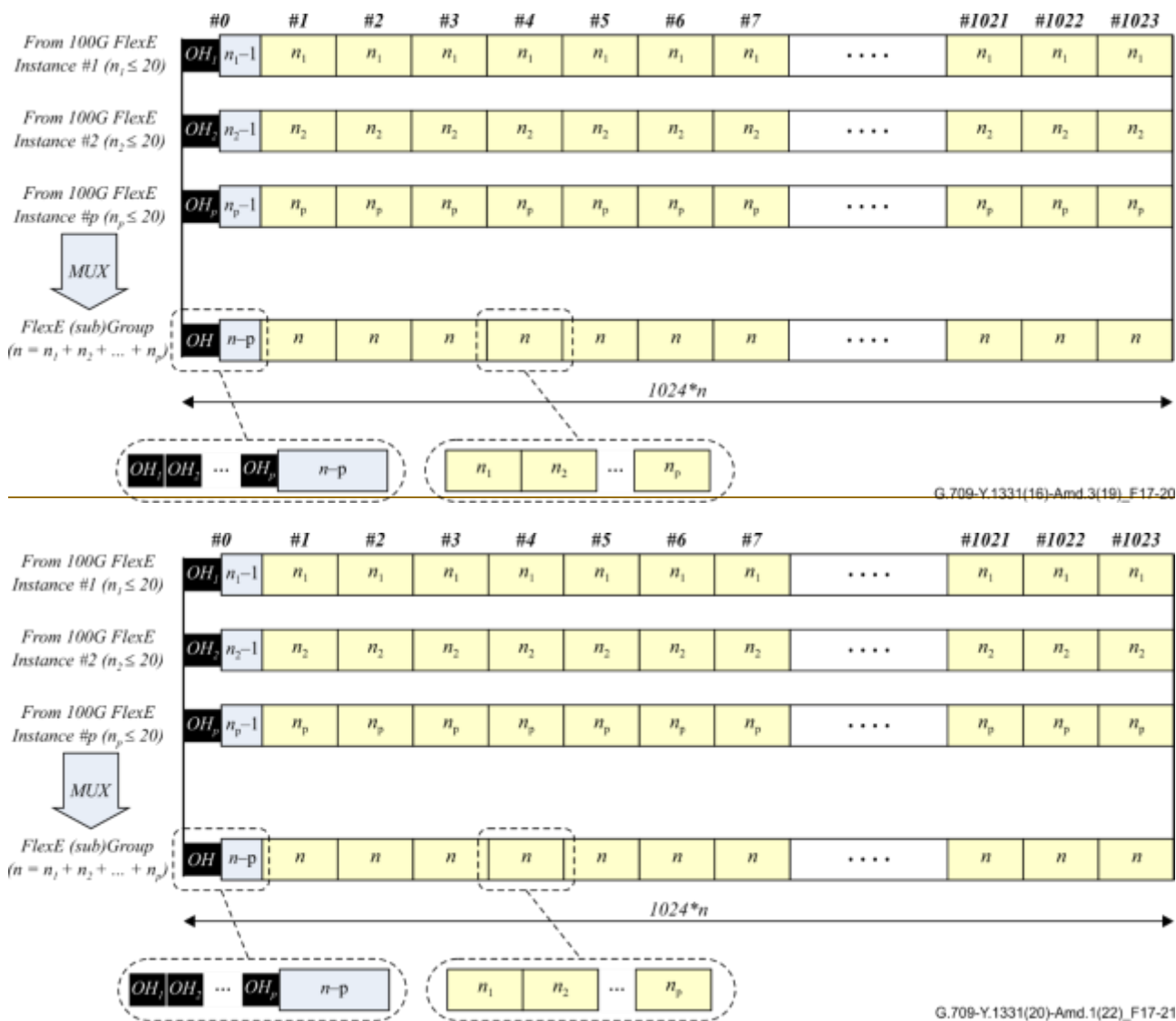
- $i = 1 \dots p$  represent the FlexE Instances in ascending FlexE Instance number order.
- $n_i$  ( $i = 1..p$ ) represents the number of FlexE 5G-equivalent calendar slots that are to be transferred. Supported calendar slots are of 5G or 25G type. A 25G calendar slots is equivalent to five consecutive 5G calendar slots, so if  $N_i$  25G calendar slots must be transferred,  $n_i = 5 \times N_i$ .
- The value of  $n_i$  for each of the  $p$  FlexE Instances is negotiated between the FlexE partial rate (sub)group mapping port and the FlexE Shim in the customer equipment.  $q$  ( $0 \leq q \leq p$ ) out of the  $p$  FlexE Instances may have their  $n_i$  set to 20 while the other  $p-q$  FlexE Instances may have their  $n_i$  set to values of 5, 10 and 15.
- Bits of the Ethernet error control blocks in  $20-n_i$  5G-equivalent calendar slots that are marked unavailable are located at the end of the sub-calendar and are dropped by the mapper to reduce the rate and reinserted by the demapper to restore the original rate.
- The FlexE partial rate (sub)group interleaving is simplified by adding  $n_i-1$  padding blocks between the overhead block and the first sub-calendar block in each of the  $p$  FlexE Instances. The value of each padding block is an Ethernet error control block.
- The  $p$  OH blocks are interleaved in the order #1, #2 to # $p$ . The  $p$   $n_i-1$  padding blocks are interleaved in the order #1, #2 to # $p$ . The  $p$  sub-calendar blocks (of length  $n_1, n_2$  to  $n_p$ ) are interleaved in the order #1, #2 to # $p$ .

NOTE 1 – An Ethernet error control block is a 66B control block (sync header = 10) with a block type of 0x1E and the other eight 7-bit characters equal to 0x1E.

NOTE 2 – The remaining  $m-p$  100G FlexE Instances – out of an  $m \times 100\text{G}$  FlexE Instance\_group signal – are carried via other ODUflex signals carried in other ODUc<sub>n</sub>/OTUC<sub>n</sub>/OTSiA signals.

NOTE 3 – Values of  $p$  and  $n$  (in FlexEp-n) supported and the subset of the  $p \times 20$  5G-equivalent calendar slots that are included in the FlexEp-n mapped into the OPUflex are vendor specific and outside the scope of this Recommendation.

NOTE 4 – Each 100G FlexE Instance in the FlexE Aware service is an equipped 100G FlexE Instance extracted from a 100G, 200G or 400G Ethernet PHY. The first FlexE Instance of a PHY is always equipped. So, there are one or two equipped FlexE Instances per PHY in a FlexE Group over  $k \times 200\text{GBASE-R}$  PHYs, and one to four equipped FlexE Instances per PHY in a FlexE Group over  $k \times 400\text{GBASE-R}$  PHYs. If the last 100G FlexE Instances of a 200G or 400G Ethernet PHY are unequipped, they do not belong to the FlexE (sub)Group and shall not be carried over the OPUflex payload. Unequipped is indicated with a FlexE Group number set to all-zeros. An unequipped FlexE Instance carries LF in all blocks except in its first OH block (Order Set with 0x5 "O" code used for alignment).



**Figure 17-201 – Full/partial rate FlexE Instance interleaving**

The 66B block stream of the FlexE partial rate (sub)group signal shall be scrambled after rate adaptation and before mapping into the OPUflex. In the reverse operation, following termination of the OPUflex signal, the 66B block stream will be descrambled before being passed to the FlexE deinterleaving, depadding and decrunching process.

A self-synchronizing scrambler with generator polynomial  $1 + x^{39} + x^{58}$  shall be used, that is identical to the scrambler specified in clause 49.2.6 [IEEE 802.3]. 66B block stream scrambling is required to provide security against false 66B block delineation (as the two sync header bits bypass the scrambler), the 66B codewords replicating the OTU and ODU frame alignment signal and the 66B codewords combined with the OTU scrambler pattern used for the interface replicating the OTU and ODU frame alignment signal.

The FlexE partial rate (sub)group signal (with up to  $\pm 100$  ppm bit-rate tolerance) is mapped into the OPUflex as per the encoding and stuffing distribution described below. The OPUflex payload bit rate is  $100GE\_bit\_rate \times 240/239 \times n/20$  kbit/s  $\pm 100$  ppm, with  $n = n_1 + n_2 + .. + n_p$ . The ODUflex bit rate is  $100GE\_bit\_rate \times 240/238 \times n/20$  kbit/s  $\pm 100$  ppm.

On the transmit side, the stuffing is inserted as 16-byte blocks and systematically controlled using a 15 bit sigma-delta as:

$$100GE\_rate \times (16k-1)/16k \times n \times 1024/(1+20 \times 1023) = 100GE\_rate \times n/20 \times 240/238 \times 238/239 \times (4 \times 238 - 3 - s)/(4 \times 238) \rightarrow s = 3373/23384 \text{ (Numerator}=3373, \text{ Denominator}=23384)$$

This encoding uses a bit synchronous generic mapping procedure (BGMP) for the distribution and encoding of the stuffing. The GMP is operated in a special mode, where the  $C_m$  value does not come from a synchronizer but is generated deterministically, and  $\sum C_{nD}$  is unused ( $C_n = C_m$ ).

As shown in the Figure 17-223, a value of  $n = m = 128$  (16-Byte) is chosen. Given the deterministic generation of the stuffing, only two  $C_{128}(t)$  values are used for this mapping ( $C_{128} = 948$  or  $949$ ). Generating  $C_{128} = 949$  (vs.  $C_{128} = 948$ ) is deterministic at the source ( $s = 3373/23384$ , 15-bit sigma-delta).

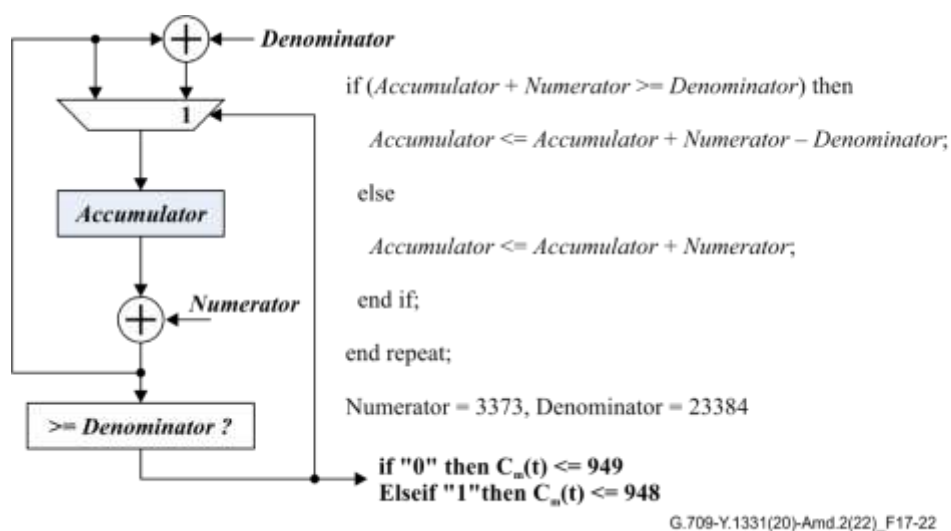
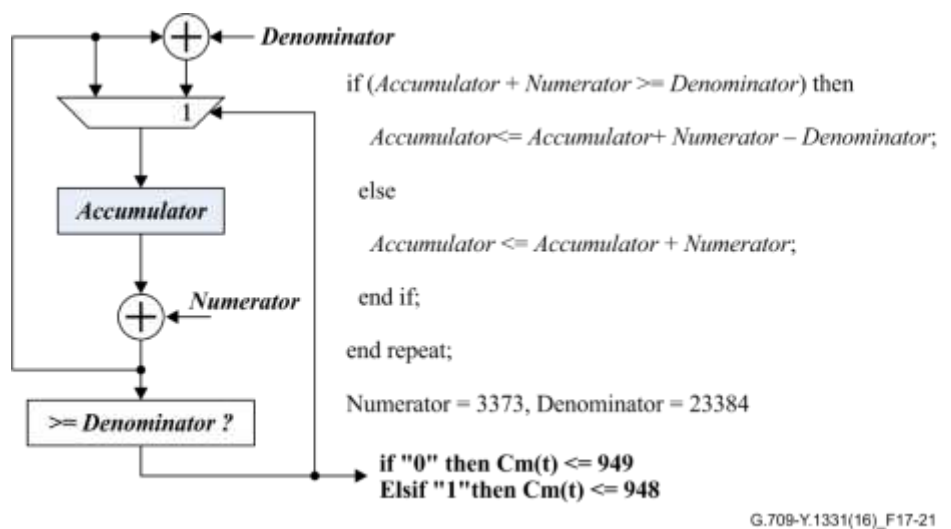
$C_m(t)$  is deterministically generated using a sigma-delta  $C_m=948/C_m=949$  justification distribution with  $s = 3373/23384$ :

The distribution of the deterministic justification ( $C_m(t) = 948$ , instead of  $C_m(t) = 949$ ) follows the sigma-delta equation below:

$$- \quad C_m(t) = 948 \quad \text{if } (j \times 3373) \bmod 23384 < 3373 \quad (17-13)$$

$$- \quad C_m(t) = 949 \quad \text{if } (j \times 3373) \bmod 23384 \geq 3373 \quad (17-14)$$

The index 'j' in equations (17-13) and (17-14) enumerates frames in the 23384 frame sequence. It counts from 1 to 23384.



**Figure 17-212 – Sigma-delta accumulator for deterministic justification generation**

The OPUflex overhead for this mapping consists of a:

- payload structure identifier (PSI) including the payload type (PT) as specified in Table 15-9, the client signal fail (CSF) and 253-p bytes plus 7 bits reserved for future international standardization (RES);
- PSI[3] carries the value of p
- PSI[4] to PSI[3+p] carries the values of n<sub>1</sub> to n<sub>p</sub>
- three justification control (JC1, JC2, JC3) bytes carrying the value of GMP overhead C<sub>m</sub>;
- four bytes reserved for future international standardization (RES).

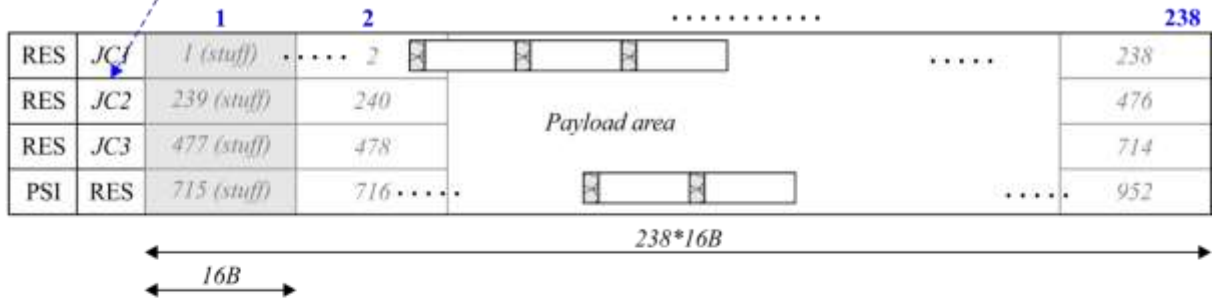
The JC1, JC2 and JC3 bytes consist of a 14-bit C<sub>m</sub> field (bits C1, C2, ..., C14), a 1-bit increment indicator (II) field, a 1-bit decrement indicator (DI) field and an 8-bit CRC-8 field which contains an error check code over the JC1, JC2 and JC3 fields.

The OPUflex payload for this mapping consists of 4 × 3808 bytes (Figure 17-223). Blocks of 16 bytes in the OPUflex payload area are numbered from 1 to 952. The OPUflex payload byte numbering for GMP 16-byte (128-bit) blocks is illustrated in Figure 17-223. In row 1 of the OPUflex frame the first 16-byte block will be labelled 1, the next 16-byte block will be labelled 2, etc.

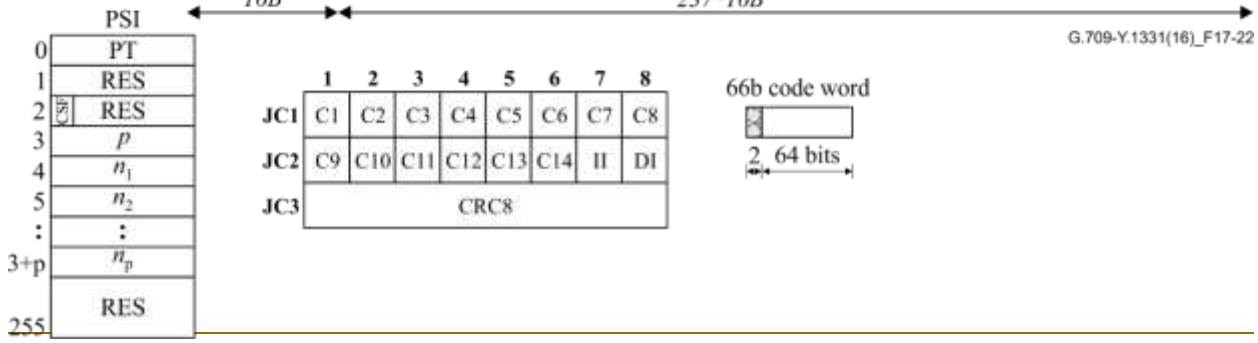
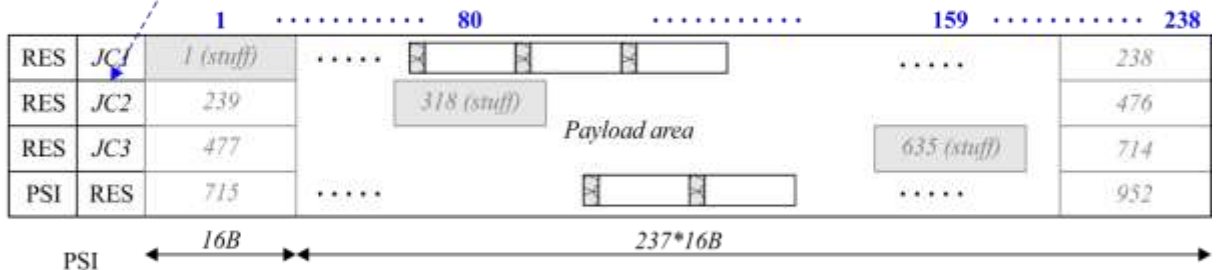
Groups of one hundred twenty-eight successive bits of the client signal are mapped into a 16-byte block of the OPUflex payload area under control of the BGMP data/stuff control mechanism. For the case of  $C_{128} = 948$ , 16 byte blocks #1, #239, #477 and #715 are carrying stuff bits and the other 16-byte blocks are carrying client bits. For the case of  $C_{128} = 949$ , 16 byte blocks #1, #318 and #635 are carrying stuff bits and the other 16-byte blocks are carrying client bits. The stuff bits are set to zero.

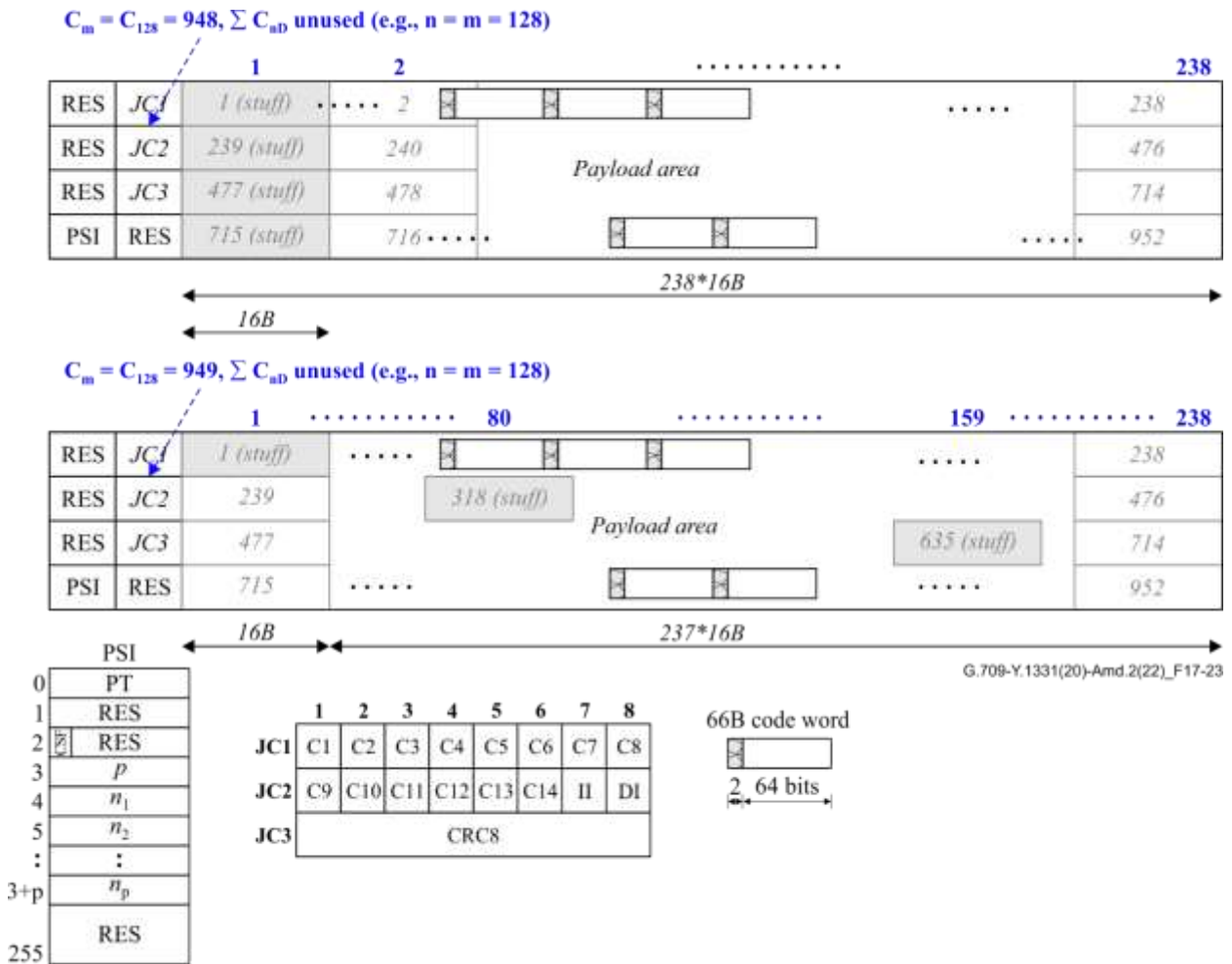
Scrambled 64B/66B blocks of the client signal are mapped into 66-bits of the OPUflex payload area skipping the 16-byte Stuff blocks under control of the BGMP control mechanism. The 66B blocks are aligned so that the first bit of the sync header appears in one of the bit positions 1, 3, 5, or 7 of a byte in the OPUflex payload.

$$C_m = C_{128} = 948, \sum C_{nd} \text{ unused (e.g., } n = m = 128)$$



$$C_m = C_{128} = 949, \sum C_{nd} \text{ unused (e.g., } n = m = 128)$$





**Figure 17-223 – Mapping of the combined FlexE stream into ODUflex via deterministic stuffing and using GMP encoding**

During a signal fail condition of an incoming equipped 100G FlexE Instance (e.g., in the case of a loss of 100G/200G/400G input PHY signal carrying this 100G FlexE Instance or FlexE local fault condition), this failed incoming 100G FlexE Instance and the p-1 other 100G FlexE Instances are not mapped into the payload of the OPUflex. Instead the OPUflex payload is filled with the stuff blocks, 66B blocks that carry a local fault sequence ordered set and the OPU CSF bit is set to "1". The OPUflex clock is derived from a local clock. The OPUflex payload signal bit rate shall be within the limits specified in Table 7-3 and the limits for the ODCb defined in [ITU-T G.8251] and no frame phase discontinuity shall be introduced in this case and when resynchronization on the incoming client signal.

During a signal fail condition of the incoming ODUflex/OPUflex signal (e.g., in the case of an ODUflex-AIS, ODUflex-LCK, ODUflex-OCI condition) or a CSF condition is present in the OPUflex overhead, a stream of 66B blocks, with each block carrying one local fault sequence ordered set is generated as a replacement signal for each of the p lost FlexE signals.

NOTE 5 – A FlexE Instance local fault sequence ordered set is a 66B control block (sync header = 10) with a block type of 0x4B, an "O" code of 0x00, a value of 0x01 to indicate a "local fault" in lane 3, and all of the other octets (before scrambling) equal to 0x00.

### 17.13 Mapping a 64B/66B PCS coded signal into OPUflex using BMP and 2-bit alignment of 66B code words

Mapping of a 64B/66B PCS coded (xGBASE-R) client signal (with up to  $\pm 100$  ppm bit-rate tolerance) into an OPUflex is performed by a bit-synchronous mapping procedure (BMP). Table 17-16 specifies the clients defined by this Recommendation.

The bit-synchronous mapping process deployed to map constant bit rate client signals into an OPUflex does not generate any justification control signals.

The 66B block stream of the xGBASE-R client signal shall be scrambled before mapping into the OPUflex. In the reverse operation, following termination of the OPUflex signal, the 66 block stream will be descrambled after demapping from the OPUflex.

A self-synchronizing scrambler with generator polynomial  $1 + x^{39} + x^{58}$  shall be used, that is identical to the scrambler specified in clause 49.2.6 of [IEEE 802.3]. 66B block stream scrambling is required to provide security against false 66B block delineation (as the two sync header bits bypass the scrambler), the 66B codewords replicating the OTU and ODU frame alignment signal and the 66B codewords combined with the OTU scrambler pattern used for the interface replicating the OTU and ODU frame alignment signal.

The OPUflex clock for the bit-synchronous mapping is derived from the client signal. During a signal fail condition of the incoming client signal (e.g., in the case of a loss of input signal), this failed incoming signal is replaced by the appropriate replacement signal as defined in Table 17-17. The OPUflex payload signal bit rate shall be within the limits specified in Table 7-3 and the limits defined in [ITU-T G.8251] and no frame phase discontinuity shall be introduced in this case and when resynchronization on the incoming client signal.

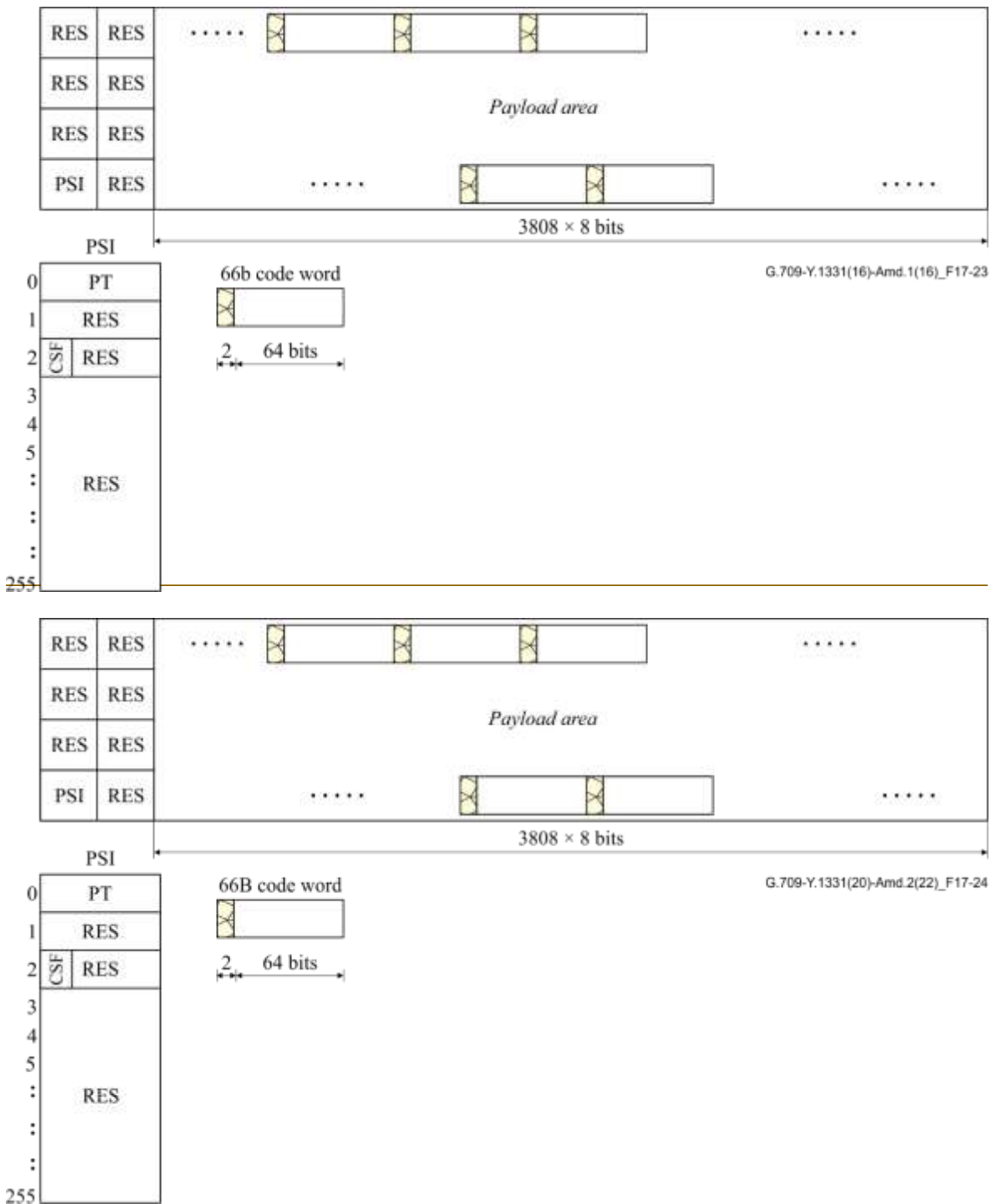
During a signal fail condition of the incoming ODUflex/OPUflex signal (e.g., in the case of an ODUflex-AIS, ODUflex-LCK, ODUflex-OCI condition), the failed client signal is replaced by the appropriate replacement signal as defined in Table 17-17.

The OPUflex overhead for this mapping consists of:

- a payload structure identifier (PSI) including the payload type (PT) as specified in Table 15-9, the client signal fail (CSF) and 254 bytes plus 7 bits reserved for future international standardization (RES);
- seven bytes reserved for future international standardization (RES).

The OPUflex payload area for this mapping consists of  $4 \times 3808$  bytes (see Figure 17-234). Scrambled 64B/66B blocks of the client signal are mapped into 66-bits of the OPUflex payload area. The 66B blocks are aligned so that the first bit of the sync header appears in one of the bit positions 1, 3, 5, or 7 of a byte in the OPUflex payload.





**Figure 17-234** – OPUflex frame structure for the mapping of a 64B/66B PCS client signal with 2-bit alignment

**Table 17-16 – Supra-2.488G CBR clients**

Client signal	Nominal bit rate (kbit/s)	Bit-rate tolerance (ppm)
<b>25GBASE-R</b>	25 781 250	±100
<b>50GBASE-R</b>	51 562 500	±100
<b>200GBASE-R</b> (Note)	206 250 000	±100
<b>400GBASE-R</b> (Note)	412 500 000	±100
NOTE – These signals represent a rate adapted 64B/66B encoded signal, which includes RC blocks.		

**Table 17-17 – Replacement signal for supra-2.488 Gbit/s clients**

Client signal	Replacement signal	Bit-rate tolerance (ppm)
<b>25GBASE-R</b>	LF (Note 1)	±100
<b>50GBASE-R</b>	LF (Note 3)	±100
<b>200GBASE-R</b>	LF (Note 2)	±100
<b>400GBASE-R</b>	LF (Note 2)	±100
NOTE 1 – The replacement signal for a 25GBASE-R signal is a continuous stream of 66B encoded and scrambled LF sequence ordered sets encoded according to Figure 49-7 of [IEEE 802.3] using control block type 0x55 (two ordered sets per 66B block) and scrambled according to clause 49.2.6 of [IEEE 802.3].		
NOTE 2 – The replacement signal for a 200GBASE-R and 400GBASE-R signal is a continuous stream of LF sequence ordered sets encoded according to Figure 82-5 of [IEEE 802.3] using control block type 0x4B. RC block insertion will be performed on the stream in the mapping direction, while 257B transcoding plus AM insertion will be performed on the stream in the demapping direction after which these signals are scrambled.		
NOTE 3 – The replacement signal for a 50GBASE-R signal is a continuous stream of 66B encoded and scrambled LF sequence ordered sets encoded according to Figure 82-5 of [IEEE 802.3] using control block type 0x4B with 4 PCS lane alignment markers inserted after each 20479 x 4 sixty-six-bit blocks and scrambled according to clause 49.2.6 of [IEEE 802.3].		

### 17.13.1 25GBASE-R

The mapped format for the signal is the 25GBASE-R PCS sublayer as defined in clause 107 of [IEEE 802.3], with a bit-stream at a signalling rate of 25.78125 Gb/s consisting of 64B/66B encoded blocks.

25GBASE-R PHYs may use one of three different operational modes: No FEC, BASE-R FEC, or RS FEC. Only the RS FEC operational mode is applicable to optical PHYs, while any of the three modes may be used for backplane and copper cable PHYs, with the operational mode selected between the endpoints of a PHY link via auto-negotiation.

The No FEC mode of operation sends bits at the physical layer using the same format as the PCS: a continuous stream of 64B/66B blocks at 25.78125 Gb/s ±100 ppm.

In the BASE-R FEC mode of operation, the signal is encoded according to clause 74 of [IEEE 802.3], using a shortened cyclical code (2112,2080). This code removes the redundant sync header bit from each of thirty-two 66B blocks and adds 32 bits of parity to produce the 2112-bit FEC codeword. The FEC is framed by the mapper using a "search and test" algorithm as described in clause 73 of [IEEE 802.3]. Errors are corrected, the FEC parity is removed, and the second sync header bit is restored to produce the stream of 66B blocks to map into OPUflex. The demapper removes the redundant sync header bit from each 66B block and adds the 32 bits of parity to each group of thirty-two, now 65B blocks. Since this process adds and removes the same number of bits in the process of encoding and decoding the FEC, this mapping is timing transparent.

In the RS FEC mode of operation, the signal is encoded according to clause 108 of [IEEE 802.3], using a Reed-Solomon (528,514) error correcting code based on 10-bit symbols. Each group of four 66B blocks from the PCS is transcoded into a 257B block. Twenty 257B blocks (5140 bits) are combined with 140 bits of FEC parity (14 FEC symbols) to produce a 5280-bit FEC codeword. To frame the bit-stream, a 257-bit codeword marker (CWM) is inserted as the first 257 bits of every 1024th FEC codeword, with sufficient idles being deleted from the PCS to make room for the CWM at the same bit-rate as the PCS. The mapper will reverse this process, finding the CWMs in the bit-stream, decoding the FEC and correcting errors, removing the CWMs, trans-decoding 257B to 64B/66B, and inserting idles to maintain the bit-rate as described in the Rx direction data flow of clause 108 of [IEEE 802.3]. The demapper will remove idles to make room for the CWM (maintaining the bit-rate), transcode to 257B, and adding the FEC parity to each group of twenty 257B blocks as described in the Tx direction data flow of clause 108 of [IEEE 802.3]. This process preserves the timing of the client signal, and this mapping is timing transparent.

### 17.13.2 200GBASE-R and 400GBASE-R

The characteristic information of the adapted and mapped 200GBASE-R or 400GBASE-R client signal consists of a scrambled sequence of 64B/66B encoded blocks with a nominal bit-rate of  $X$  kbit/s  $\pm 100$  ppm.

The mapper shall first recover the 200GBASE-R or 400GBASE-R client stream, which is referred to as the OTN reference signal, that is a sequence of 64B/66B encoded blocks as per clause 119.2.5.7 of [IEEE 802.3], with a bit rate of  $(528/544 \times 20479/20480 \times Y$  kbit/s)  $\pm 100$  ppm.

NOTE 1 –  $Y$  kbit/s is the nominal bit-rate of the aggregate 200GBASE-R or 400GBASE-R PCS signal consisting of 8 or 16 PCS lanes with 256B/257B encoding and FEC at the PMA service interface.

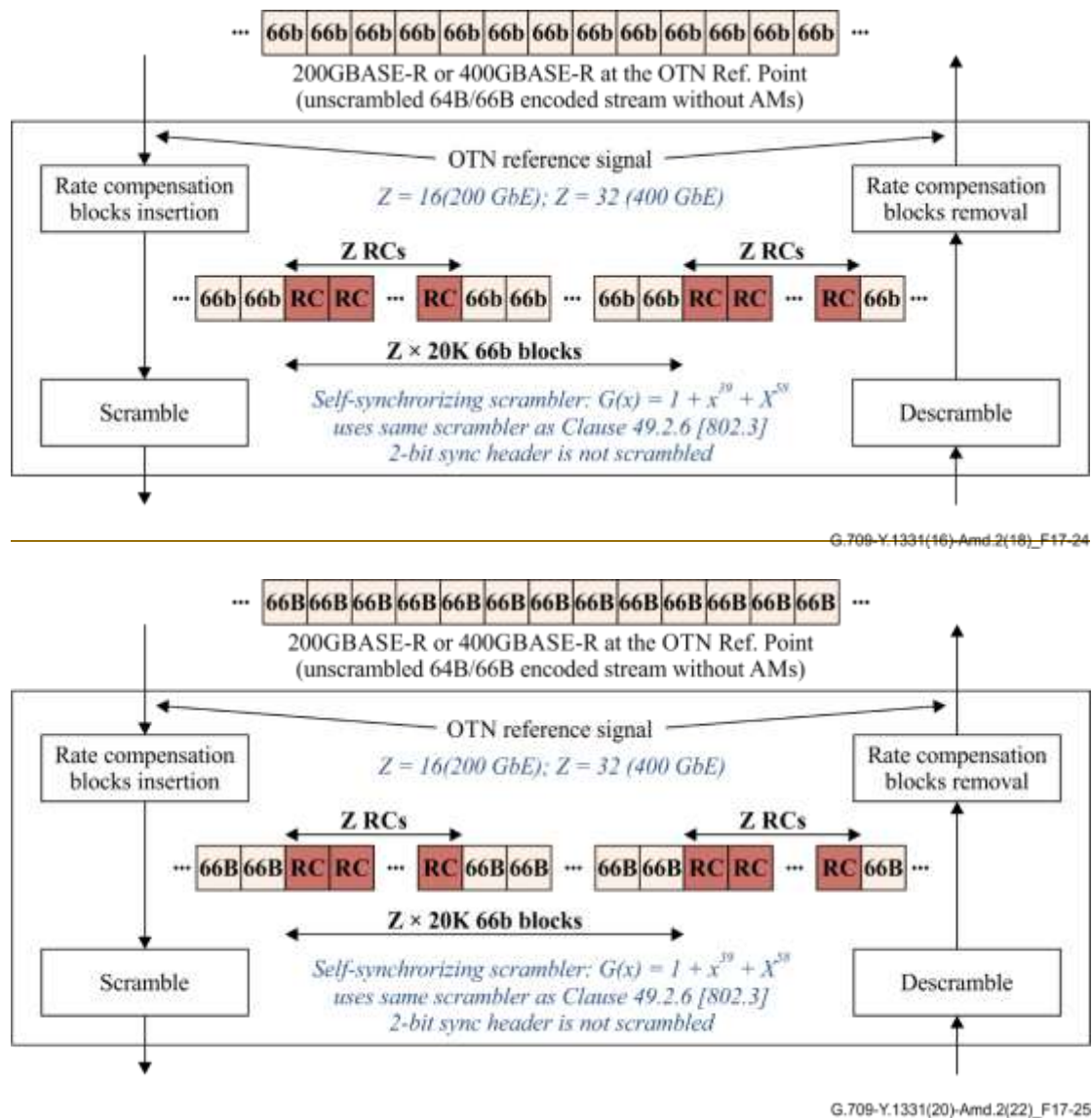
**Table 17-18 – X, Y and Z parameter values**

Parameter	200GBASE-R	400G BASE-R
X	206 250 000	412 500 000
Y	212 500 000	425 000 000
Z	16	32

The client stream for the 200GBASE-R or 400G BASE-R OTN reference signal (64B/66B encoded, un-scrambled and without alignment markers) is recovered using the process described in Annex J for parallel 256B/257B interfaces. The lane(s) of the physical interface are bit-disinterleaved, if necessary, into eight or sixteen streams of 26 562 500 kbit/s. Lane alignment marker lock is acquired on each PCS lane, allowing lane deskew and reorder, as well as de-interleave for FEC code word synchronization and error correction. The mapper shall extract the FEC parity bits and alignment markers, perform descrambling and transdecode the 256B/257B blocks to 64B/66B blocks. Uncorrectable FEC code words shall be replaced with error control blocks at the output of the transdecoder.

Then, the client stream for the 200GBASE-R or 400GBASE-R OTN reference signal (or its replacement stream upon signal failure) is rate compensated by inserting  $Z$  rate compensation (RC) blocks every  $(Z \times 20479)$  client blocks (Figure 17-245). The resulting nominal bit-rate of the compensated 64B/66B client stream is  $[528/544 \times Y$  kbit/s] =  $X$  kbit/s  $\pm 100$  ppm. The 64B/66B client stream shall be scrambled after rate compensation, and before mapping into the OPUflex.

In the reverse operation, following termination of the OPUflex signal, the demapper must recover 66B block lock from the demapped CBR signal, descramble the 64B/66B client stream, and remove the rate compensation blocks to retrieve the 200GBASE-R or 400GBASE-R client stream at the OTN reference signal as specified in clause 119.2.4.1 of [IEEE 802.3].

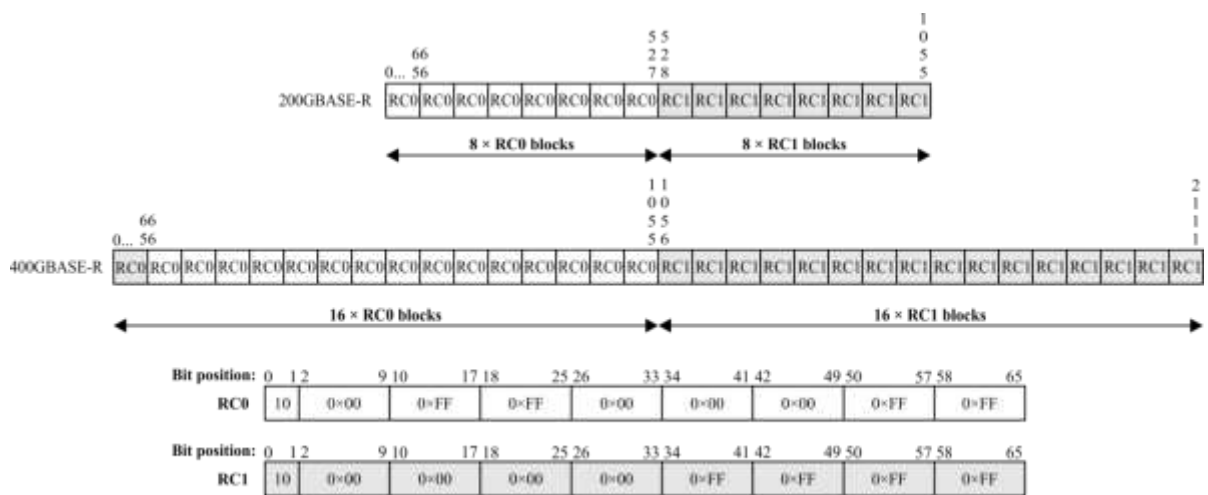


**Figure 17-245** – Adapted xGBASE-R (x = 200, 400) client signal for OPUflex mapping

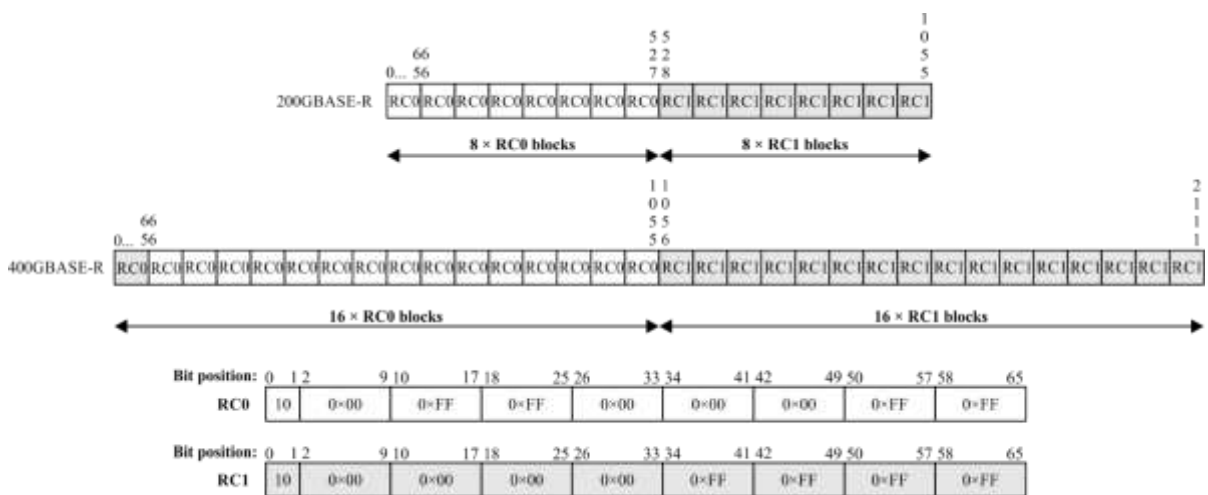
Then, 64B/66B blocks to 256B/257B blocks transcoding and scrambling can be performed, and as described in Annex J, alignment markers and FEC parity bits can be inserted prior to the 200GBASE-R or 400GBASE-R PCS lane distribution, and interleaving, if necessary, into physical lanes at the PMA interface.

The rate compensation blocks (RC) have the form of a specially defined 66-bit block with a control block sync header. The  $Z/2$  first RC blocks carry an RC0 value, and the last  $Z/2$  RC blocks carry an RC1 value as shown in Figure 17-256.

NOTE 2 – The value of the RC blocks (RC0 or RC1) has been chosen so that it does not match any defined control block. The 8b located at the same position as the block type field (bits 2 to 9 in Figure 17-256) carry the unused value 0x00, still maintaining the 4-bit hamming distance with the defined and used block types. At the sink, the RC pattern can be search on a subset of the RC0 and RC1 bits and blocks, using a simple alignment process.



G.709-Y.1331(16)-Amd.2(18)\_F17-25

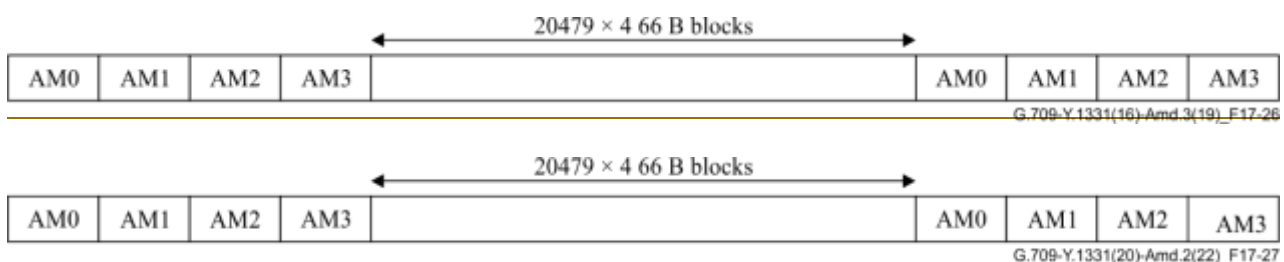


G.709-Y.1331(20)-Amd.2(22)\_F17-26

**Figure 17-256 – Rate compensation blocks format for 200GBASE-R and 400GBASE-R mapping**

### 17.13.3 50GBASE-R

The mapped format for the signal is the 50GBASE-R PCS sublayer as defined in clause 133 of [IEEE 802.3cd]. The 50GBASE-R signal (64B/66B encoded, nominal aggregate bit-rate of 51 562 500 kbit/s  $\pm$ 100 ppm, with alignment markers) is recovered using the following process: block lock and lane alignment marker lock are acquired on each of the four PCS lanes, with bit streams of 12 890 625 kbit/s, at the 50GBASE-R sublayer reference point, allowing the 66B blocks to be de-skewed and reordered. The four PCS lanes are serialized with their respective AMs occurring in sequence. Figure 17-267 illustrates the order of 66B blocks mapped into the ODUflex.



G.709-Y.1331(16)-Amd.2(19)\_F17-26

G.709-Y.1331(20)-Amd.2(22)\_F17-27

**Figure 17-267 – Order of 66B blocks mapped into ODUflex for 50GBASE-R**

The payload of the ODUflex is at a nominal rate of  $51\,562\,500\text{ kbit/s} \pm 100\text{ppm}$ , which is a precise ratio of 33/34 from the  $53\,125\,000\text{ kbit/s}$  bit-rate of the single-lane FEC encoded signal. For bit-synchronous mapping into an ODUflex, the ODUflex rate is 7887/8092 times the physical line rate of the 50G Ethernet signal; i.e.,  $7887/8092 \times 53\,125\,000\text{ kbit/s}$ .

In the mapper, the received Ethernet PCS lane BIP may be compared with the expected Ethernet PCS lane BIP as a non-intrusive monitor.

The de-mapper will pass through the PCS lane BIP from the ingress. In addition, the received Ethernet PCS lane BIP may be compared with the expected Ethernet PCS lane BIP as a non-intrusive monitor.

The de-mapper will recover from the output of the BMP processor 64B/66B block lock per the state diagram in Figure 82-10 [IEEE 802.3]. The 66B blocks are re-distributed round-robin to four PCS lanes and these four PCS lanes presented at the 50GBASE-R egress reference point of the PCS layer.

## 18 Blank clause

*This clause is intentionally left blank.*

## 19 Mapping ODUj signals into the ODTU signal and the ODTU into the OPUk tributary slots

This clause specifies the multiplexing of:

- ODU0 into OPU1, ODU1 into OPU2, ODU1 and ODU2 into OPU3 using client/server specific asynchronous mapping procedures (AMP);
- other ODUj into OPUk using a client agnostic generic mapping procedure (GMP).

This ODUj into OPUk multiplexing is performed in two steps:

- 1) asynchronous mapping of ODUj into optical data tributary unit (ODTU) using either AMP or GMP;
- 2) byte-synchronous mapping of ODTU into one or more OPUk tributary slots.

### 19.1 OPUk tributary slot definition

The OPUk is divided into a number of tributary slots (TS) and these tributary slots are interleaved within the OPUk. A tributary slot includes a part of the OPUk OH area and a part of the OPUk payload area. The bytes of the ODUj frame are mapped into the ODTU payload area and the ODTU bytes are mapped into the OPUk tributary slot or slots. The bytes of the ODTU justification overhead are mapped into the OPUk OH area.

There are two types of tributary slots:

- 1) Tributary slot with a bandwidth of approximately 2.5 Gbit/s; an OPUk is divided into n tributary slots, numbered 1 to n.
- 2) Tributary slot with a bandwidth of approximately 1.25 Gbit/s; an OPUk is divided into 2n tributary slots, numbered 1 to 2n.

OPU2 and OPU3 interface ports supporting 1.25 Gbit/s tributary slots must also support the 2.5 Gbit/s tributary slot mode for interworking with interface ports supporting only the 2.5G tributary slot mode (i.e., interface ports compliant with issues of this Recommendation: prior to the definition of 1.25G tributary slots). When operated in 2.5G tributary slot mode, 1.25G tributary slots "i" and "i+n" (i = 1 to n, n = 4 (OPU2) and n = 16 (OPU3)) function as one 2.5G tributary slot.

### 19.1.1 OPU2 tributary slot allocation

Figure 19-1 presents the OPU2 2.5G tributary slot allocation and the OPU2 1.25G tributary slot allocation. An OPU2 is divided into four 2.5G tributary slots numbered 1 to 4, or in eight 1.25G tributary slots numbered 1 to 8.

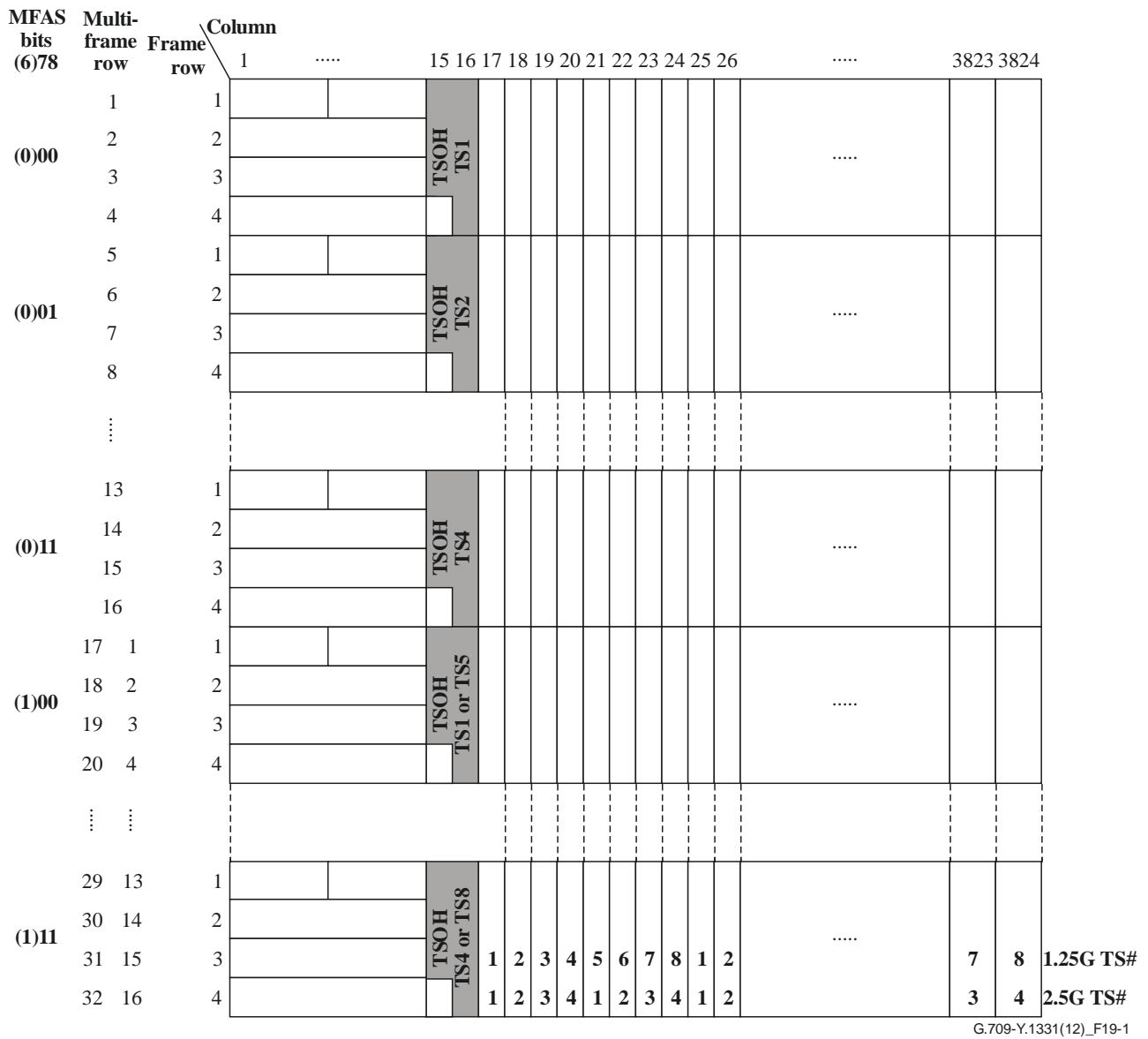
- An OPU2 2.5G tributary slot occupies 25% of the OPU2 payload area. It is a structure with 952 columns by 16 ( $4 \times 4$ ) rows (see Figures 19-1 and 19-7) plus a tributary slot overhead (TSOH). The four OPU2 TSs are byte interleaved in the OPU2 payload area and the four OPU2 TSOHs are frame interleaved in the OPU2 overhead area.
- An OPU2 1.25G tributary slot occupies 12.5% of the OPU2 payload area. It is a structure with 476 columns by 32 ( $8 \times 4$ ) rows (see Figures 19-1 and 19-7) plus a tributary slot overhead (TSOH). The eight OPU2 TSs are byte interleaved in the OPU2 payload area and the eight OPU2 TSOHs are frame interleaved in the OPU2 overhead area.

An OPU2 2.5G tributary slot "i" ( $i = 1,2,3,4$ ) is provided by two OPU2 1.25G tributary slots "i" and "i+4" as illustrated in Figure 19-1.

The tributary slot overhead (TSOH) of OPU2 tributary slots is located in column 16 plus column 15, rows 1, 2 and 3 of the OPU2 frame.

The TSOH for a 2.5G tributary slot is available once every 4 frames. A 4-frame multiframe structure is used for this assignment. This multiframe structure is locked to bits 7 and 8 of the MFAS byte as shown in Table 19-1 and Figure 19-1.

The TSOH for a 1.25G tributary slot is available once every 8 frames. An 8-frame multiframe structure is used for this assignment. This multiframe structure is locked to bits 6, 7 and 8 of the MFAS byte as shown in Table 19-1 and Figure 19-1.



G.709-Y.1331(12)\_F19-1

**Figure 19-1 – OPU2 tributary slot allocation**

**Table 19-1 – OPU2 tributary slot OH allocation**

MFAS bits 7 8	TSOH 2.5G TS	MFAS bits 6 7 8	TSOH 1.25G TS
0 0	1	0 0 0	1
0 1	2	0 0 1	2
1 0	3	0 1 0	3
1 1	4	0 1 1	4
		1 0 0	5
		1 0 1	6
		1 1 0	7
		1 1 1	8



### 19.1.2 OPU3 tributary slot allocation

Figure 19-2 presents the OPU3 2.5G tributary slot allocation and the OPU3 1.25G tributary slot allocation. An OPU3 is divided into sixteen 2.5G tributary slots numbered 1 to 16, or in thirty-two 1.25G tributary slots numbered 1 to 32.

- An OPU3 2.5G tributary slot occupies 6.25% of the OPU3 payload area. It is a structure with 238 columns by 64 ( $16 \times 4$ ) rows (see Figures 19-2 and 19-8) plus a tributary slot overhead (TSOH). The sixteen OPU3 2.5G TSs are byte interleaved in the OPU3 payload area and the sixteen OPU3 TSOHs are frame interleaved in the OPU3 overhead area.
- An OPU3 1.25G tributary slot occupies 3.125% of the OPU3 payload area. It is a structure with 119 columns by 128 ( $32 \times 4$ ) rows (see Figures 19-2 and 19-8) plus a tributary slot overhead (TSOH). The thirty-two OPU3 1.25G TSs are byte interleaved in the OPU3 payload area and the thirty-two OPU3 TSOHs are frame interleaved in the OPU3 overhead area.

An OPU3 2.5G tributary slot "i" ( $i = 1, 2, \dots, 16$ ) is provided by two OPU3 1.25G tributary slots "i" and "i+16" as illustrated in Figure 19-2.

The tributary slot overhead (TSOH) of OPU3 tributary slots is located in column 16 plus column 15, rows 1, 2 and 3 of the OPU3 frame.

The TSOH for a 2.5G tributary slot is available once every 16 frames. A 16-frame multiframe structure is used for this assignment. This multiframe structure is locked to bits 5, 6, 7 and 8 of the MFAS byte as shown in Table 19-2 and Figure 19-2.

The TSOH for a 1.25G tributary slot is available once every 32 frames. A 32-frame multiframe structure is used for this assignment. This multiframe structure is locked to bits 4, 5, 6, 7 and 8 of the MFAS byte as shown in Table 19-2 and Figure 19-2.

MFAS bits (4)5678	Multi-frame row	Frame row	Column		1		.....		15 16 17 18		.....		31 32 33 34		.....		47 48 49 50		.....		3823 3824	
			1	.....	15 16	17 18	.....	31 32	33 34	.....	47 48	49 50	.....	3823	3824							
(0)0000	1	1																				
	2	2			TSOH																	
	3	3			TS1			.....				.....						.....				
	4	4																				
(0)0001	5	1																				
	6	2			TSOH																	
	7	3			TS2			.....				.....										
	8	4																				
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
(0)1111	61	1																				
	62	2			TSOH																	
	63	3			TS16			.....				.....										
	64	4																				
(1)0000	65	1																				
	66	2			TSOH																	
	67	3			TS1 or TS17			.....				.....										
	68	4																				
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	
(1)1111	125	61																				
	126	62			TSOH																	
	127	63			TS16 or TS32			1 2	.....			15 16 17 18	.....				31 32	1 2	.....			31 32
	128	64						1 2	.....			15 16 1 2	.....				15 16	1 2	.....			15 16

G.709-Y.1331(12)\_F19-2

Figure 19-2 – OPU3 tributary slot allocation

**Table 19-2 – OPU3 tributary slot OH allocation**

MFAS bits 5 6 7 8	TSOH 2.5G TS	MFAS bits 4 5 6 7 8	TSOH 1.25G TS	MFAS bits 4 5 6 7 8	TSOH 1.25G TS
0 0 0 0	1	0 0 0 0 0	1	1 0 0 0 0	17
0 0 0 1	2	0 0 0 0 1	2	1 0 0 0 1	18
0 0 1 0	3	0 0 0 1 0	3	1 0 0 1 0	19
0 0 1 1	4	0 0 0 1 1	4	1 0 0 1 1	20
0 1 0 0	5	0 0 1 0 0	5	1 0 1 0 0	21
0 1 0 1	6	0 0 1 0 1	6	1 0 1 0 1	22
0 1 1 0	7	0 0 1 1 0	7	1 0 1 1 0	23
0 1 1 1	8	0 0 1 1 1	8	1 0 1 1 1	24
1 0 0 0	9	0 1 0 0 0	9	1 1 0 0 0	25
1 0 0 1	10	0 1 0 0 1	10	1 1 0 0 1	26
1 0 1 0	11	0 1 0 1 0	11	1 1 0 1 0	27
1 0 1 1	12	0 1 0 1 1	12	1 1 0 1 1	28
1 1 0 0	13	0 1 1 0 0	13	1 1 1 0 0	29
1 1 0 1	14	0 1 1 0 1	14	1 1 1 0 1	30
1 1 1 0	15	0 1 1 1 0	15	1 1 1 1 0	31
1 1 1 1	16	0 1 1 1 1	16	1 1 1 1 1	32

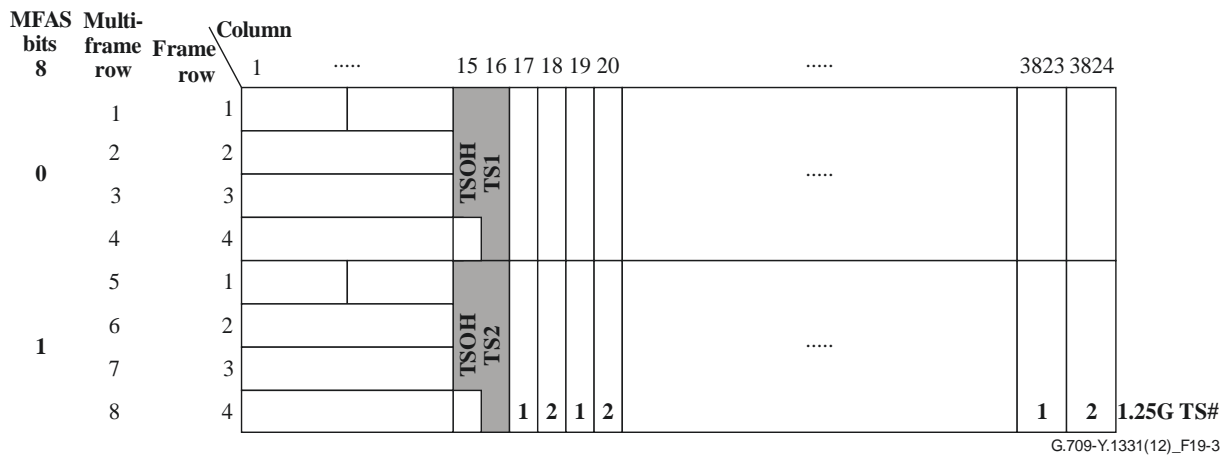
### 19.1.3 OPU1 tributary slot allocation

Figure 19-3 presents the OPU1 1.25G tributary slot allocation. An OPU1 is divided into two 1.25G tributary slots numbered 1 to 2.

- An OPU1 1.25G tributary slot occupies 50% of the OPU1 payload area. It is a structure with 1904 columns by 8 ( $2 \times 4$ ) rows (see Figure 19-3) plus a tributary slot overhead (TSOH). The two OPU1 1.25G TSs are byte interleaved in the OPU1 payload area and the two OPU1 TSOHs are frame interleaved in the OPU1 overhead area.

The tributary slot overhead (TSOH) of OPU1 tributary slots is located in column 16 plus column 15, rows 1, 2 and 3 of the OPU1 frame.

The TSOH for a 1.25G tributary slot is available once every 2 frames. A 2-frame multiframe structure is used for this assignment. This multiframe structure is locked to bit 8 of the MFAS byte as shown in Table 19-3 and Figure 19-3.



G.709-Y.1331(12)\_F19-3

**Figure 19-3 – OPU1 tributary slot allocation**

**Table 19-3 – OPU1 tributary slot OH allocation**

MFAS bit 8	TSOH 1.25G TS
0	1
1	2

#### 19.1.4 OPU4 tributary slot allocation

Figures 19-4A and 19-4B present the OPU4 1.25G tributary slot allocation. An OPU4 is divided into eighty 1.25G tributary slots (numbered 1 to 80), which are located in columns 17 to 3816, and 8 columns of fixed stuff located in columns 3817 to 3824. The OPU4 frame may be represented in a 320 row by 3810 column format (Figure 19-4A) and in a 160 row by 7620 column format (Figure 19-4B).

- An OPU4 1.25G tributary slot occupies 1.247% of the OPU4 payload area. It is a structure with 95 columns by 160 ( $80 \times 4/2$ ) rows (see Figure 19-4B) plus a tributary slot overhead (TSOH). The eighty OPU4 1.25G TSs are byte interleaved in the OPU4 payload area and the eighty OPU4 TSOHs are frame interleaved in the OPU4 overhead area.

The tributary slot overhead (TSOH) of OPU4 tributary slots is located in rows 1 to 3, columns 15 and 16 of the OPU4 frame.

The TSOH for a 1.25G tributary slot is available once every 80 frames. An 80-frame multiframe structure is used for this assignment. This multiframe structure is locked to bits 2, 3, 4, 5, 6, 7 and 8 of the OMFI byte as shown in Table 19-4.

OMFI bits 2345678	Multi-frame row	Frame row	Column																																			
			1	.....	15	16	17	18	.....	55	56	57	58	.....	95	96	97	98	.....	3815	3816	3817	3818	3819	3820	3821	3822	3823	3824									
0000000	1	1			TSOH TS1	1	2						39	40	41	42													39	40	FS	FS	FS	FS	FS	FS	FS	FS
	2	2				41	42							79	80	1	2													79	80	FS	FS	FS	FS	FS	FS	FS
	3	3			1	2							39	40	41	42													39	40	FS	FS	FS	FS	FS	FS	FS	FS
	4	4			PSI	OM FI	41	42					79	80	1	2													79	80	FS	FS	FS	FS	FS	FS	FS	FS
0000001	5	1			TSOH TS2	1	2						39	40	41	42													39	40	FS	FS	FS	FS	FS	FS	FS	FS
	6	2				41	42							79	80	1	2													79	80	FS	FS	FS	FS	FS	FS	FS
	7	3			1	2							39	40	41	42													39	40	FS	FS	FS	FS	FS	FS	FS	FS
	8	4			PSI	OM FI	41	42					79	80	1	2													79	80	FS	FS	FS	FS	FS	FS	FS	FS
⋮																																						
1001110	313	1			TSOH TS79	1	2						39	40	41	42													39	40	FS	FS	FS	FS	FS	FS	FS	FS
	314	2				41	42							79	80	1	2													79	80	FS	FS	FS	FS	FS	FS	FS
	315	3			1	2							39	40	41	42													39	40	FS	FS	FS	FS	FS	FS	FS	FS
	316	4			PSI	OM FI	41	42					79	80	1	2													79	80	FS	FS	FS	FS	FS	FS	FS	FS
1001111	317	1			TSOH TS80	1	2						39	40	41	42													39	40	FS	FS	FS	FS	FS	FS	FS	FS
	318	2				41	42							79	80	1	2													79	80	FS	FS	FS	FS	FS	FS	FS
	319	3			1	2							39	40	41	42													39	40	FS	FS	FS	FS	FS	FS	FS	FS
	320	4			PSI	OM FI	41	42					79	80	1	2													79	80	FS	FS	FS	FS	FS	FS	FS	FS

G.709-Y.1331(12)\_F19-4A

Figure 19-4A – OPU4 1.25G tributary slot allocation

OMFI bits 2345678	Multi-frame D-row	Frame row	Column																																																																							
			1	....	15	16	17	18	....	95	96	97	98	....	3815	3816	3817	3818	3819	3820	3821	3822	3823	3824	1	....	15	16	17	18	....	55	56	57	58	....	3815	3816	3817	3818	3819	3820	3821	3822	3823	3824																												
0000000	1	1+2			TS1	1	2			79	80	1	2			39	40	FS	FS	FS	FS	FS	FS	FS	FS				TS1	41	42			79	80	1	2			79	80	FS	FS	FS	FS	FS	FS	FS	FS																									
	2	3+4				1	2			79	80	1	2			39	40	FS	FS	FS	FS	FS	FS	FS	FS				PSI OM FI	41	42			79	80	1	2			79	80	FS	FS	FS	FS	FS	FS	FS	FS																									
0000001	3	1+2			TS2	1	2			79	80	1	2			39	40	FS	FS	FS	FS	FS	FS	FS	FS				TS2	41	42			79	80	1	2			79	80	FS	FS	FS	FS	FS	FS	FS	FS																									
	4	3+4				1	2			79	80	1	2			39	40	FS	FS	FS	FS	FS	FS	FS	FS				PSI OM FI	41	42			79	80	1	2			79	80	FS	FS	FS	FS	FS	FS	FS	FS																									
⋮																																																																										
1001110	157	1+2			TS79	1	2			79	80	1	2			39	40	FS	FS	FS	FS	FS	FS	FS	FS				TS79	41	42			79	80	1	2			79	80	FS	FS	FS	FS	FS	FS	FS	FS																									
	158	3+4				1	2			79	80	1	2			39	40	FS	FS	FS	FS	FS	FS	FS	FS				PSI OM FI	41	42			79	80	1	2			79	80	FS	FS	FS	FS	FS	FS	FS	FS																									
1001111	159	1+2			TS80	1	2			79	80	1	2			39	40	FS	FS	FS	FS	FS	FS	FS	FS				TS80	41	42			79	80	1	2			79	80	FS	FS	FS	FS	FS	FS	FS	FS																									
	160	3+4				1	2			79	80	1	2			39	40	FS	FS	FS	FS	FS	FS	FS	FS				PSI OM FI	41	42			79	80	1	2			79	80	FS	FS	FS	FS	FS	FS	FS	FS																									

G.709-Y.1331(12)\_F19-4B

Figure 19-4B – OPU4 tributary slots in 160 row x 7620 column format

**Table 19-4 – OPU4 tributary slot OH allocation**

OMFI bits 2 3 4 5 6 7 8	TSOH 1.25G TS	OMFI bits 2 3 4 5 6 7 8	TSOH 1.25G TS	OMFI bits 2 3 4 5 6 7 8	TSOH 1.25G TS	OMFI bits 2 3 4 5 6 7 8	TSOH 1.25G TS
0000000	1	0010100	21	0101000	41	0111100	61
0000001	2	0010101	22	0101001	42	0111101	62
0000010	3	0010110	23	0101010	43	0111110	63
0000011	4	0010111	24	0101011	44	0111111	64
0000100	5	0011000	25	0101100	45	1000000	65
0000101	6	0011001	26	0101101	46	1000001	66
0000110	7	0011010	27	0101110	47	1000010	67
0000111	8	0011011	28	0101111	48	1000011	68
0001000	9	0011100	29	0110000	49	1000100	69
0001001	10	0011101	30	0110001	50	1000101	70
0001010	11	0011110	31	0110010	51	1000110	71
0001011	12	0011111	32	0110011	52	1000111	72
0001100	13	0100000	33	0110100	53	1001000	73
0001101	14	0100001	34	0110101	54	1001001	74
0001110	15	0100010	35	0110110	55	1001010	75
0001111	16	0100011	36	0110111	56	1001011	76
0010000	17	0100100	37	0111000	57	1001100	77
0010001	18	0100101	38	0111001	58	1001101	78
0010010	19	0100110	39	0111010	59	1001110	79
0010011	20	0100111	40	0111011	60	1001111	80

**19.1.5 OPU25 tributary slot allocation**

Figures 19-5A and 19-5B present the OPU25 1.25G tributary slot allocation. An OPU25 is divided into twenty 1.25G tributary slots (numbered 1 to 20), which are located in columns 17 to 3824. The OPU25 frame may be represented in an 80 row by 3810 column format (Figure 19-5A) and in a 16 row by 19050 column format (Figure 19-5B).

- An OPU25 1.25G tributary slot occupies 5% of the OPU25 payload area. It is a structure with 952 columns by 16 (20 × 4/5) rows (see Figure 19-5B) plus a tributary slot overhead (TSOH). The twenty OPU25 1.25G TSs are byte interleaved in the OPU25 payload area and the twenty OPU25 TSOHs are frame interleaved in the OPU25 overhead area.

The tributary slot overhead (TSOH) of OPU25 tributary slots is located in rows 1 to 3, columns 15 and 16 of the OPU25 frame.

The TSOH for a 1.25G tributary slot is available once every 20 frames. A 20-frame multiframe structure is used for this assignment. This multiframe structure is locked to bits 4, 5, 6, 7 and 8 of the OMFI byte as shown in Table 19-5.

OMFI bits 45678	Multi-frame row	Frame row	Column		15	16	17	18	....	35	36	37	38	....	55	56	57	58	....	3815	3816	3817	3818	3819	3820	3821	3822	3823	3824			
			1	2																												
00000	1	1																														
		2			TSOH TS1		1	2				19	20	1	2																	
		3					9	10				7	8	9	10																	
		4					17	18				15	16	17	18																	
00001	1	1			PSI OMFI																											
		2			TSOH TS2		1	2				19	20	1	2																	
		3					9	10				7	8	9	10																	
		4					17	18				15	16	17	18																	
10010	1	1																														
		2			TSOH TS19		5	6				3	4	5	6																	
		3					13	14				11	12	13	14																	
		4					1	2				19	20	1	2																	
10011	1	1			PSI OMFI																											
		2			TSOH TS20		9	10				7	8	9	10																	
		3					17	18				15	16	17	18																	
		4					5	6				3	4	5	6																	

G.709-Y.1331(20)\_F19-5A

Figure 19-5A – OPU25 1.25G tributary slot allocation

Multi-frame row	Frame row	Column		15	16	17	18	36	37	38	3824	15	16	17	18	36	37	38	3824	15	16	17	18	36	37	38	3824																										
		1	2																																																		
1	1, 2(1 <sup>st</sup> 1/4)	1	TSOH #1	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50
		2	TSOH #2	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50
		3	TSOH #3	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50
		4	PSI OMFI	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50
		5	TSOH #6	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50
15	78(2 <sup>nd</sup> 1/2), 79(1 <sup>st</sup> 3/4)	1	PSI OMFI	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50
		2	TSOH #18	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50
		3	TSOH #19	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50
		4	TSOH #20	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50
		5	PSI OMFI	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50
16	79(4 <sup>th</sup> 1/4), 80	1	PSI OMFI	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50
		2	TSOH #20	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50
		3	PSI OMFI	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50
		4	TSOH #19	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50
		5	PSI OMFI	TS1	TS2	TS3	TS4	TS5	TS6	TS7	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50

G.709-Y.1331(20)\_F19-5B

Figure 19-5B – OPU25 tributary slots in 16 row x 19050 column format



**Table 19-5 – OPU25 tributary slot OH allocation**

OMFI bits 4 5 6 7 8	TSOH 1.25G TS
0 0 0 0 0	1
0 0 0 0 1	2
0 0 0 1 0	3
0 0 0 1 1	4
0 0 1 0 0	5
0 0 1 0 1	6
0 0 1 1 0	7
0 0 1 1 1	8
0 1 0 0 0	9
0 1 0 0 1	10
0 1 0 1 0	11
0 1 0 1 1	12
0 1 1 0 0	13
0 1 1 0 1	14
0 1 1 1 0	15
0 1 1 1 1	16
1 0 0 0 0	17
1 0 0 0 1	18
1 0 0 1 0	19
1 0 0 1 1	20

**19.1.6 OPU50 tributary slot allocation**

Figures 19-6A and 19-6B present the OPU50 1.25G tributary slot allocation. An OPU50 is divided into forty 1.25G tributary slots (numbered 1 to 40), which are located in columns 17 to 3824. The OPU50 frame may be represented in a 160 row by 3810 column format (Figure 19-6A) and in a 32 row by 19050 column format (Figure 19-6B).

- An OPU25 1.25G tributary slot occupies 2.5% of the OPU50 payload area. It is a structure with 476 columns by 32 ( $40 \times 4/5$ ) rows (see Figure 19-6B) plus a tributary slot overhead (TSOH). The forty OPU50 1.25G TSs are byte interleaved in the OPU50 payload area and the forty OPU25 TSOHs are frame interleaved in the OPU25 overhead area.

The tributary slot overhead (TSOH) of OPU50 tributary slots is located in rows 1 to 3, columns 15 and 16 of the OPU25 frame.

The TSOH for a 1.25G tributary slot is available once every 40 frames. A 40-frame multiframe structure is used for this assignment. This multiframe structure is locked to bits 3, 4, 5, 6, 7 and 8 of the OMFI byte as shown in Table 19-6.

OMFI bits 345678	Multi-frame row	Frame row	Column																																				
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32					
000000	1	1																																					
	2	2																																					
	3	3																																					
	4	4																																					
000001	1	1																																					
	2	2																																					
	3	3																																					
	4	4																																					
100110	1	1																																					
	2	2																																					
	3	3																																					
	4	4																																					
100111	1	1																																					
	2	2																																					
	3	3																																					
	4	4																																					

G.709-Y.1331(20)\_F19-6A

Figure 19-6A – OPU50 1.25G tributary slot allocation

Multi-frame row	Frame row	Column																																					
		15	16	17	18	56	57	58	3824	15	16	17	18	56	57	58	3824	15	16	17	18	56	57	58	3824	15	16	17	18	56	57	58	3824	15	16	17	18	56	57
1	1	TSOH #1	TS1	TS2	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50	TS51	TS52	TS53	TS54	TS55	TS56	TS57	TS58	TS59	TS60
	2(1 <sup>st</sup> /4)	PSI	OMFI	TS2	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50	TS51	TS52	TS53	TS54	TS55	TS56	TS57	TS58	TS59	TS60
2	2	TSOH #2	TS1	TS2	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50	TS51	TS52	TS53	TS54	TS55	TS56	TS57	TS58	TS59	TS60
	3(1 <sup>st</sup> /2)	PSI	OMFI	TS2	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50	TS51	TS52	TS53	TS54	TS55	TS56	TS57	TS58	TS59	TS60
3	3	TSOH #3	TS1	TS2	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50	TS51	TS52	TS53	TS54	TS55	TS56	TS57	TS58	TS59	TS60
	4(1 <sup>st</sup> /3/4)	PSI	OMFI	TS2	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50	TS51	TS52	TS53	TS54	TS55	TS56	TS57	TS58	TS59	TS60
5	5	TSOH #6	TS1	TS2	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50	TS51	TS52	TS53	TS54	TS55	TS56	TS57	TS58	TS59	TS60
	6	PSI	OMFI	TS2	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50	TS51	TS52	TS53	TS54	TS55	TS56	TS57	TS58	TS59	TS60
31	158(2 <sup>nd</sup> /1/2)	TSOH #38	TS1	TS2	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50	TS51	TS52	TS53	TS54	TS55	TS56	TS57	TS58	TS59	TS60
	159(1 <sup>st</sup> /3/4)	PSI	OMFI	TS2	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50	TS51	TS52	TS53	TS54	TS55	TS56	TS57	TS58	TS59	TS60
32	159(4 <sup>th</sup> /1/4)	TSOH #39	TS1	TS2	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50	TS51	TS52	TS53	TS54	TS55	TS56	TS57	TS58	TS59	TS60
	160	PSI	OMFI	TS2	TS26	TS27	TS28	TS29	TS30	TS31	TS32	TS33	TS34	TS35	TS36	TS37	TS38	TS39	TS40	TS41	TS42	TS43	TS44	TS45	TS46	TS47	TS48	TS49	TS50	TS51	TS52	TS53	TS54	TS55	TS56	TS57	TS58	TS59	TS60

G.709-Y.1331(20)\_F19-6B

Figure 19-6B – OPU50 tributary slots in 32 row x 19050 column format

**Table 19-6 – OPU50 tributary slot OH allocation**

OMFI bits 3 4 5 6 7 8	TSOH 1.25G TS	OMFI bits 3 4 5 6 7 8	TSOH 1.25G TS
0 0 0 0 0 0	1	0 1 0 1 0 0	21
0 0 0 0 0 1	2	0 1 0 1 0 1	22
0 0 0 0 1 0	3	0 1 0 1 1 0	23
0 0 0 0 1 1	4	0 1 0 1 1 1	24
0 0 0 1 0 0	5	0 1 1 0 0 0	25
0 0 0 1 0 1	6	0 1 1 0 0 1	26
0 0 0 1 1 0	7	0 1 1 0 1 0	27
0 0 0 1 1 1	8	0 1 1 0 1 1	28
0 0 1 0 0 0	9	0 1 1 1 0 0	29
0 0 1 0 0 1	10	0 1 1 1 0 1	30
0 0 1 0 1 0	11	0 1 1 1 1 0	31
0 0 1 0 1 1	12	0 1 1 1 1 1	32
0 0 1 1 0 0	13	1 0 0 0 0 0	33
0 0 1 1 0 1	14	1 0 0 0 0 1	34
0 0 1 1 1 0	15	1 0 0 0 1 0	35
0 0 1 1 1 1	16	1 0 0 0 1 1	36
0 1 0 0 0 0	17	1 0 0 1 0 0	37
0 1 0 0 0 1	18	1 0 0 1 0 1	38
0 1 0 0 1 0	19	1 0 0 1 1 0	39
0 1 0 0 1 1	20	1 0 0 1 1 1	40

## 19.2 ODTU definition

The optical data tributary unit (ODTU) carries a justified ODU signal. There are two types of ODTUs:

- 1) ODTU<sub>jk</sub> ((j,k) = {(0,1), (1,2), (1,3), (2,3)}; ODTU01, ODTU12, ODTU13 and ODTU23) in which an ODU<sub>j</sub> signal is mapped via the asynchronous mapping procedure (AMP) as defined in clause 19.5;
- 2) ODTU<sub>k.ts</sub> ((k,ts) = (2,1..8), (3,1..32), (4,1..80), (25,1..20), (50,1..40)) in which a ODU<sub>j</sub> (ODU0, ODU1, ODU2, ODU2e, ODU3, ODUflex) signal is mapped via the generic mapping procedure (GMP) defined in clause 19.6.

### Optical data tributary unit jk

The optical data tributary unit jk (ODTU<sub>jk</sub>) is a structure which consists of an ODTU<sub>jk</sub> payload area and an ODTU<sub>jk</sub> overhead area (Figure 19-7). The ODTU<sub>jk</sub> payload area has c columns and r rows (see Table 19-7) and the ODTU<sub>jk</sub> overhead area has "ts" times 4 bytes, of which "ts" times 1 byte can carry payload. The ODTU<sub>jk</sub> is carried in "ts" 1.25G or 2.5G tributary slots of an OPU<sub>k</sub>.

The location of the ODTU<sub>jk</sub> overhead depends on the OPU<sub>k</sub> tributary slot(s) used when multiplexing the ODTU<sub>jk</sub> in the OPU<sub>k</sub> (see clauses 19.1.1, 19.1.2, 19.1.3). The ts instances of the ODTU<sub>jk</sub> overhead might not be equally distributed.

The ODTU<sub>jk</sub> overhead carries the AMP justification overhead as specified in clause 19.4.

NOTE – The 1.25G and 2.5G tributary slot versions of an ODTU<sub>12</sub> are identical when the two 1.25G tributary slots carrying the ODTU<sub>12</sub> are TS<sub>a</sub> and TS<sub>a+4</sub>. The 1.25G and 2.5G tributary slot versions of an ODTU<sub>13</sub> are identical when the two 1.25G tributary slots carrying the ODTU<sub>12</sub> are TS<sub>a</sub> and TS<sub>a+16</sub>. The 1.25G and 2.5G tributary slot versions of an ODTU<sub>23</sub> are identical when the eight 1.25G tributary slots carrying the ODTU<sub>23</sub> are TS<sub>a</sub>, TS<sub>b</sub>, TS<sub>c</sub>, TS<sub>d</sub>, TS<sub>a+16</sub>, TS<sub>b+16</sub>, TS<sub>c+16</sub> and TS<sub>d+16</sub>.

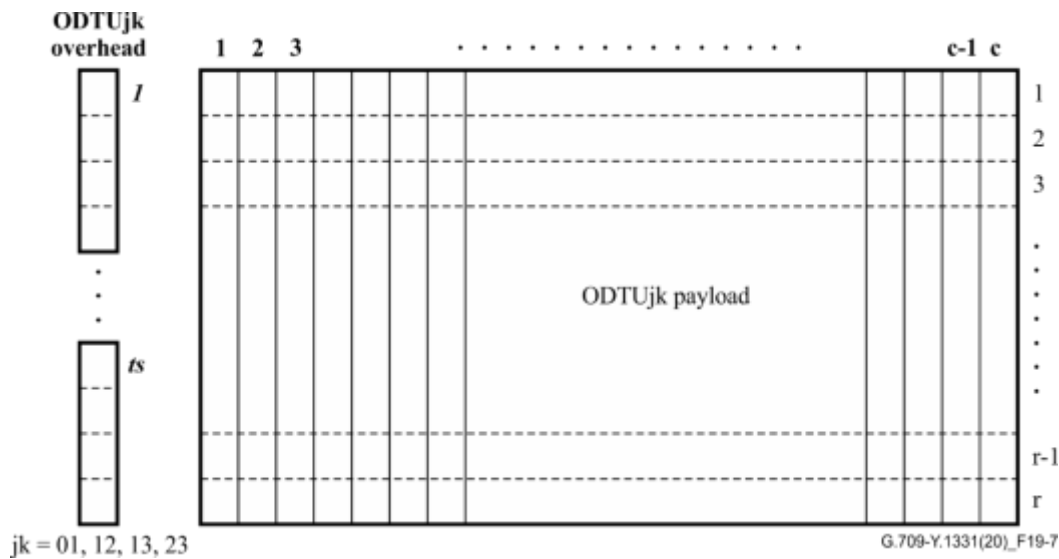


Figure 19-7 – ODTU<sub>jk</sub> frame formats

Table 19-7 – ODTU<sub>jk</sub> characteristics for 2.5G and 1.25G tributary slots

2.5G TS	c	r	ts	ODTU <sub>jk</sub> payload bytes	ODTU <sub>jk</sub> overhead bytes
ODTU <sub>12</sub>	952	16	1	15232	1 x 4
ODTU <sub>13</sub>	238	64	1	15232	1 x 4
ODTU <sub>23</sub>	952	64	4	60928	4 x 4

1.25G TS	c	r	ts	ODTU <sub>jk</sub> payload bytes	ODTU <sub>jk</sub> overhead bytes
ODTU <sub>01</sub>	1904	8	1	15232	1 x 4
ODTU <sub>12</sub>	952	32	2	30464	2 x 4
ODTU <sub>13</sub>	238	128	2	30464	2 x 4
ODTU <sub>23</sub>	952	128	8	121856	8 x 4

### Optical data tributary unit k.ts

The optical data tributary unit k.ts (ODTUK.ts) is a structure which consists of an ODTUK.ts payload area and an ODTUK.ts overhead area (Figure 19-8). The ODTUK.ts payload area has  $j \times ts$  columns and  $r$  rows (see Table 19-8) and the ODTUK.ts overhead area has one times 6 bytes. The ODTUK.ts is carried in "ts" 1.25G tributary slots of an OPUK.

The location of the ODTUK.ts overhead depends on the OPUK tributary slot used when multiplexing the ODTUK.ts in the OPUK (see clauses 19.1.1, 19.1.2, 19.1.4, 19.1.5, 19.1.6). The single instance of an ODTUK.ts overhead is located in the OPUK TSOH of the last OPUK tributary slot allocated to the ODTUK.ts.

The ODTUk.ts overhead carries the GMP justification overhead as specified in clause 19.4.

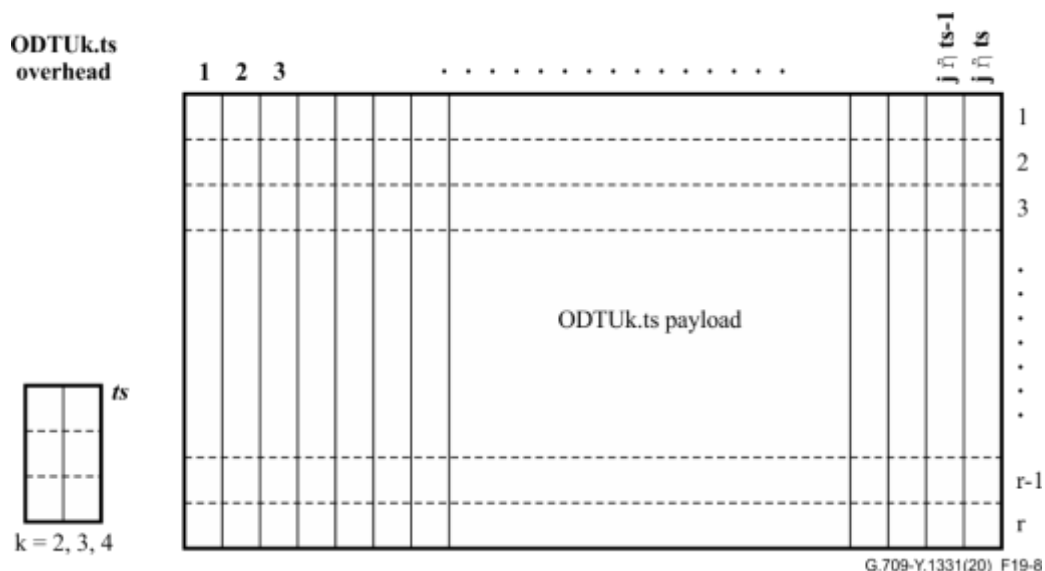


Figure 19-8 – ODTUk.ts frame formats

Table 19-8 – ODTUk.ts characteristics

	<b>j</b>	<b>r</b>	<b>ts</b>	<b>ODTUk.ts payload bytes</b>	<b>ODTUk.ts overhead bytes</b>
<b>ODTU2.ts</b>	476	32	1 to 8	$15232 \times ts$	$1 \times 6$
<b>ODTU3.ts</b>	119	128	1 to 32	$15232 \times ts$	$1 \times 6$
<b>ODTU4.ts</b>	95	160	1 to 80	$15200 \times ts$	$1 \times 6$
<b>ODTU25.ts</b>	952	16	1 to 20	$15232 \times ts$	$1 \times 6$
<b>ODTU50.ts</b>	476	32	1 to 40	$15232 \times ts$	$1 \times 6$

### 19.3 Multiplexing ODTU signals into the OPUk

Multiplexing an ODTU01 signal into an OPU1 is realized by mapping the ODTU01 signal in one of the two OPU1 1.25G tributary slots.

Multiplexing an ODTU12 signal into an OPU2 is realized by mapping the ODTU12 signal in one of the four OPU2 2.5G tributary slots or in two (of the eight) arbitrary OPU2 1.25G tributary slots: OPU2 TSa and TSb with  $1 \leq a < b \leq 8$ .

Multiplexing an ODTU13 signal into an OPU3 is realized by mapping the ODTU13 signal in one of the sixteen OPU3 2.5G tributary slots or in two (of the thirty-two) arbitrary OPU3 1.25G tributary slots: OPU3 TSa and TSb with  $1 \leq a < b \leq 32$ .

Multiplexing an ODTU23 signal into an OPU3 is realized by mapping the ODTU23 signal in four (of the sixteen) arbitrary OPU3 2.5G tributary slots: OPU3 TSa, TSb, TSc and TSd with  $1 \leq a < b < c < d \leq 16$  or in eight (of the thirty-two) arbitrary OPU3 1.25G tributary slots: OPU3 TSa, TSb, TSc, TSd, TSe, TSf, TSh and TSh with  $1 \leq a < b < c < d < e < f < g < h \leq 32$ .

NOTE – a, b, c, d, e, f, g and h do not have to be sequential ( $a = i, b = i+1, c = i+2, d = i+3, e = i+4, f = i+5, g = i+6, h = i+7$ ); the values can be arbitrarily selected to prevent bandwidth fragmentation.

Multiplexing an ODTU2.ts signal into an OPU2 is realized by mapping the ODTU2.ts signal in ts (of the eight) arbitrary OPU2 1.25G tributary slots: OPU2 TSa, TSb, .., TS<sub>p</sub> with  $1 \leq a < b < .. < p \leq 8$ .

Multiplexing an ODTU3.ts signal into an OPU3 is realized by mapping the ODTU3.ts signal in ts (of the thirty-two) arbitrary OPU3 1.25G tributary slots: OPU3 TSa, TSb, .. , TSq with  $1 \leq a < b < .. < q \leq 32$ .

Multiplexing an ODTU4.ts signal into an OPU4 is realized by mapping the ODTU4.ts signal in ts (of the eighty) arbitrary OPU4 1.25G tributary slots: OPU4 TSa, TSb, .. , TSr with  $1 \leq a < b < .. < r \leq 80$ .

Multiplexing an ODTU25.ts signal into an OPU25 is realized by mapping the ODTU25.ts signal in ts (of the twenty) arbitrary OPU25 1.25G tributary slots: OPU25 TSa, TSb, .. , TSx with  $1 \leq a < b < .. < x \leq 20$ .

Multiplexing an ODTU50.ts signal into an OPU50 is realized by mapping the ODTU50.ts signal in ts (of the forty) arbitrary OPU50 1.25G tributary slots: OPU25 TSa, TSb, .. , TSx with  $1 \leq a < b < .. < x \leq 40$ .

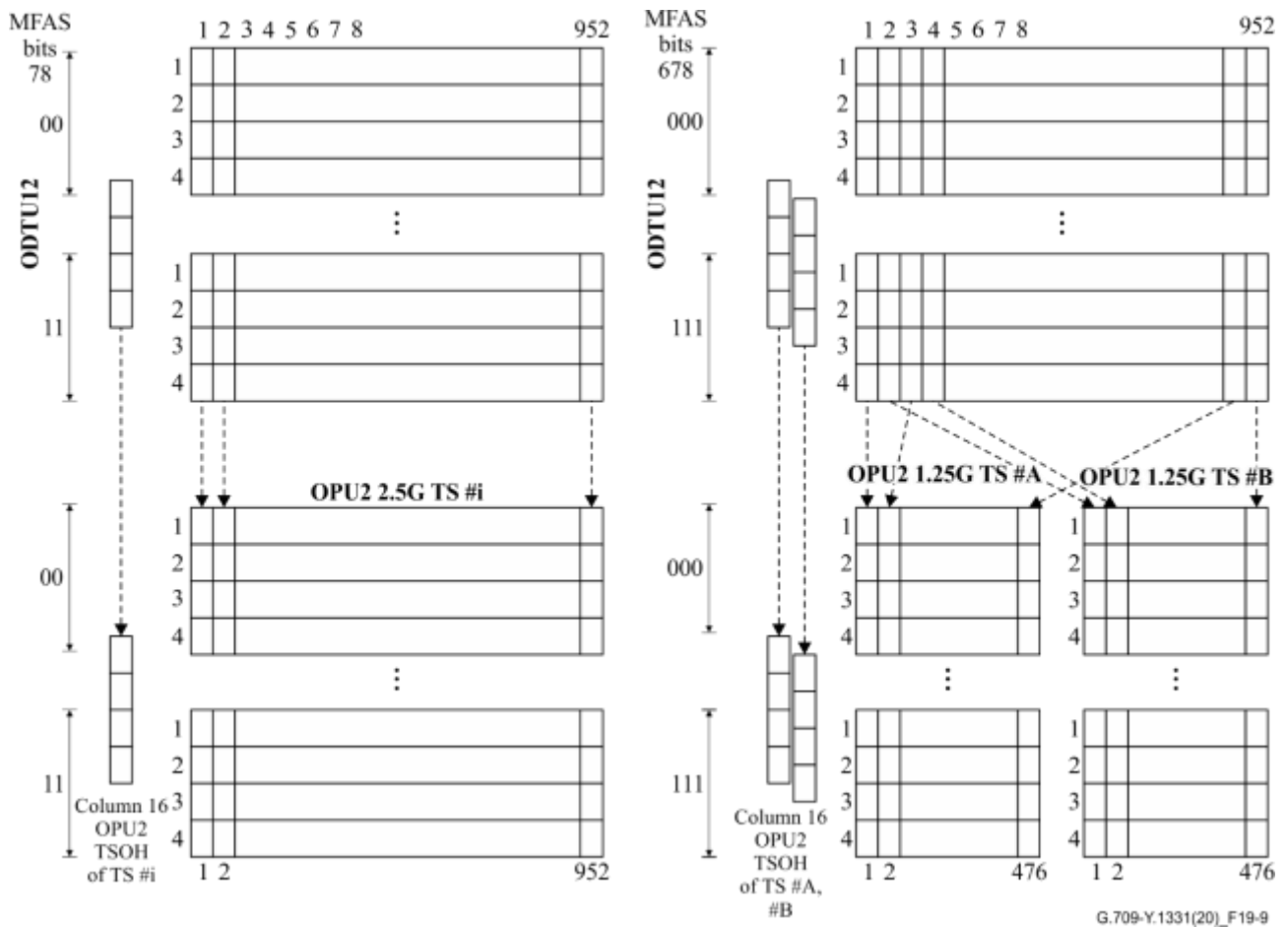
The OPUk overhead for these multiplexed signals consists of a payload type (PT), the multiplex structure identifier (MSI), the OPU4 multiframe identifier (k=4), the OPUk tributary slot overhead carrying the ODTU overhead and depending on the ODTU type one or more bytes reserved for future international standardization.

### **19.3.1 ODTU12 mapping into one OPU2 tributary slot**

A byte of the ODTU12 payload signal is mapped into a byte of an OPU2 2.5G TS #i (i = 1,2,3,4) payload area, as indicated in Figure 19-9 (left). A byte of the ODTU12 overhead is mapped into a TSOH byte within column 16 of the OPU2 2.5G TS #i.

A byte of the ODTU12 signal is mapped into a byte of one of two OPU2 1.25G TS #A,B (A,B = 1,2,...,8) payload areas, as indicated in Figure 19-9 (right). A byte of the ODTU12 overhead is mapped into a TSOH byte within column 16 of the OPU2 1.25G TS #a,b.

The remaining OPU2 TSOH bytes in column 15 are reserved for future international standardization.



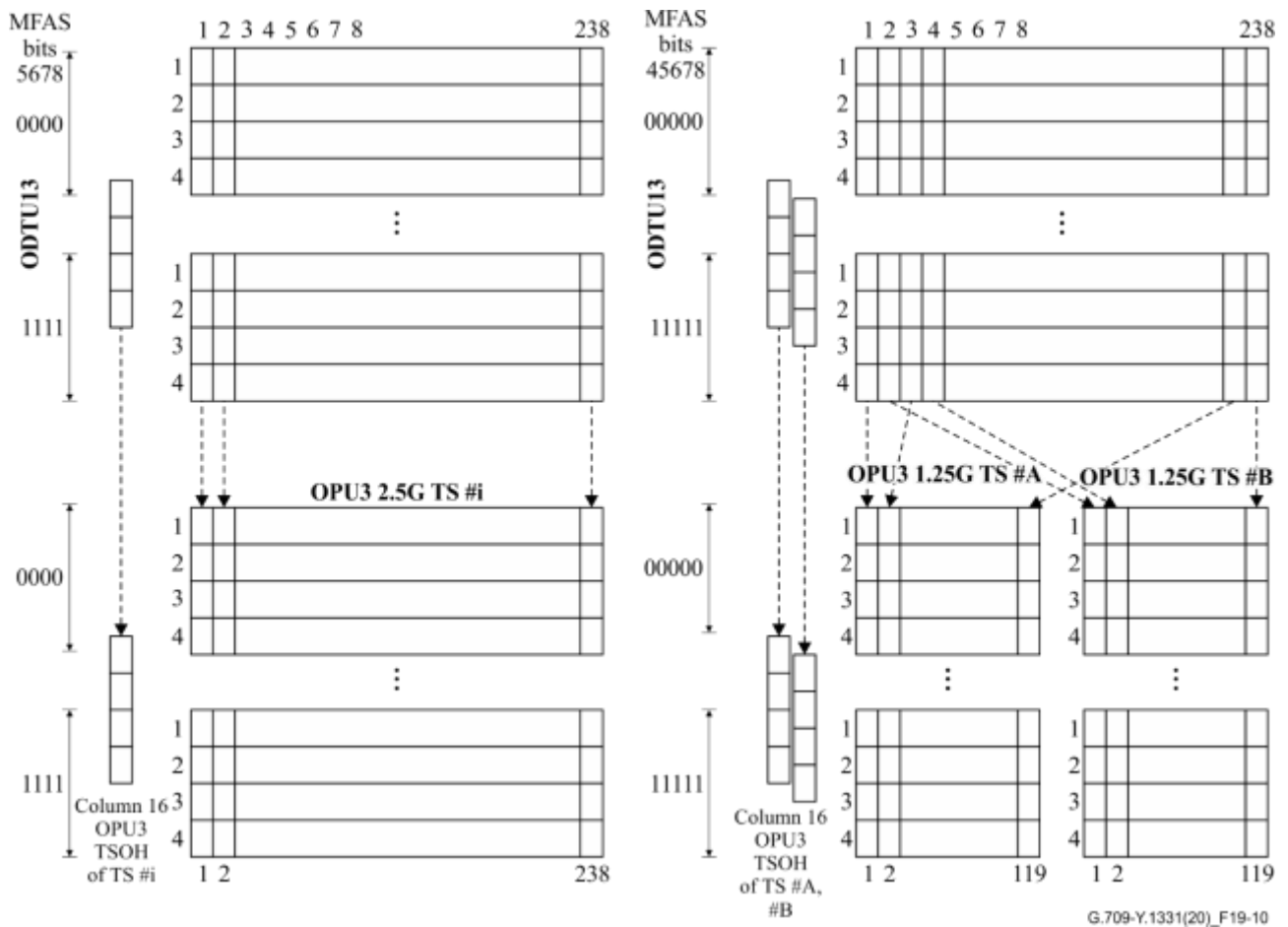
**Figure 19-9 – Mapping of ODTU12 into one OPU2 2.5G tributary slot (left) and two OPU2 1.25G tributary slots (right)**

### 19.3.2 ODTU13 mapping into one OPU3 tributary slot

A byte of the ODTU13 signal is mapped into a byte of an OPU3 2.5G TS #i (i = 1,2,...,16) payload area, as indicated in Figure 19-10 (left). A byte of the ODTU13 overhead is mapped into a TSOH byte within column 16 of the OPU3 2.5G TS #i.

A byte of the ODTU13 signal is mapped into a byte of one of two OPU3 1.25G TS #A, B (A,B = 1,2,...,32) payload areas, as indicated in Figure 19-10 (right). A byte of the ODTU13 overhead is mapped into a TSOH byte within column 16 of the OPU3 1.25G TS #a,b.

The remaining OPU3 TSOH bytes in column 15 are reserved for future international standardization.



**Figure 19-10 – Mapping of ODTU13 into one OPU3 2.5G tributary slot (left) and two OPU3 1.25G tributary slots (right)**

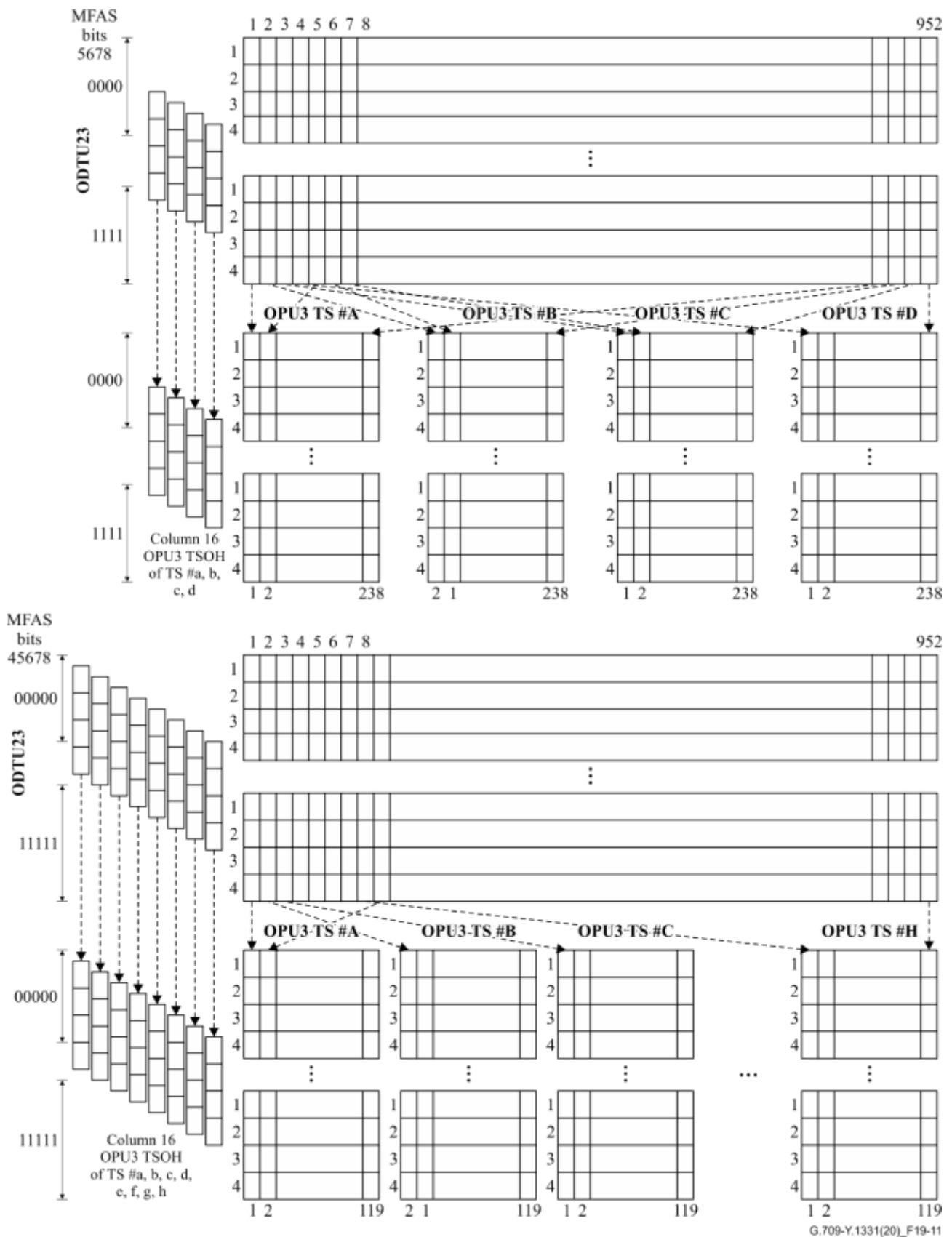
### 19.3.3 ODTU23 mapping into four OPU3 tributary slots

A byte of the ODTU23 signal is mapped into a byte of one of four OPU3 2.5G TS #A,B,C,D (A,B,C,D = 1,2,...,16) payload areas, as indicated in Figure 19-11 (top). A byte of the ODTU23 overhead is mapped into a TSOH byte within column 16 of the OPU3 TS #a,b,c,d.

A byte of the ODTU23 signal is mapped into a byte of one of eight OPU3 1.25G TS #A, B, C, D, E, F, G, H (A,B,C,D,E,F,G,H = 1,2,...,32) payload areas, as indicated in Figure 19-11 (bottom). A byte of the ODTU23 overhead is mapped into a TSOH byte within column 16 of the OPU3 1.25G TS #a,b,c,d,e,f,g,h.

The remaining OPU3 TSOH bytes in column 15 are reserved for future international standardization.





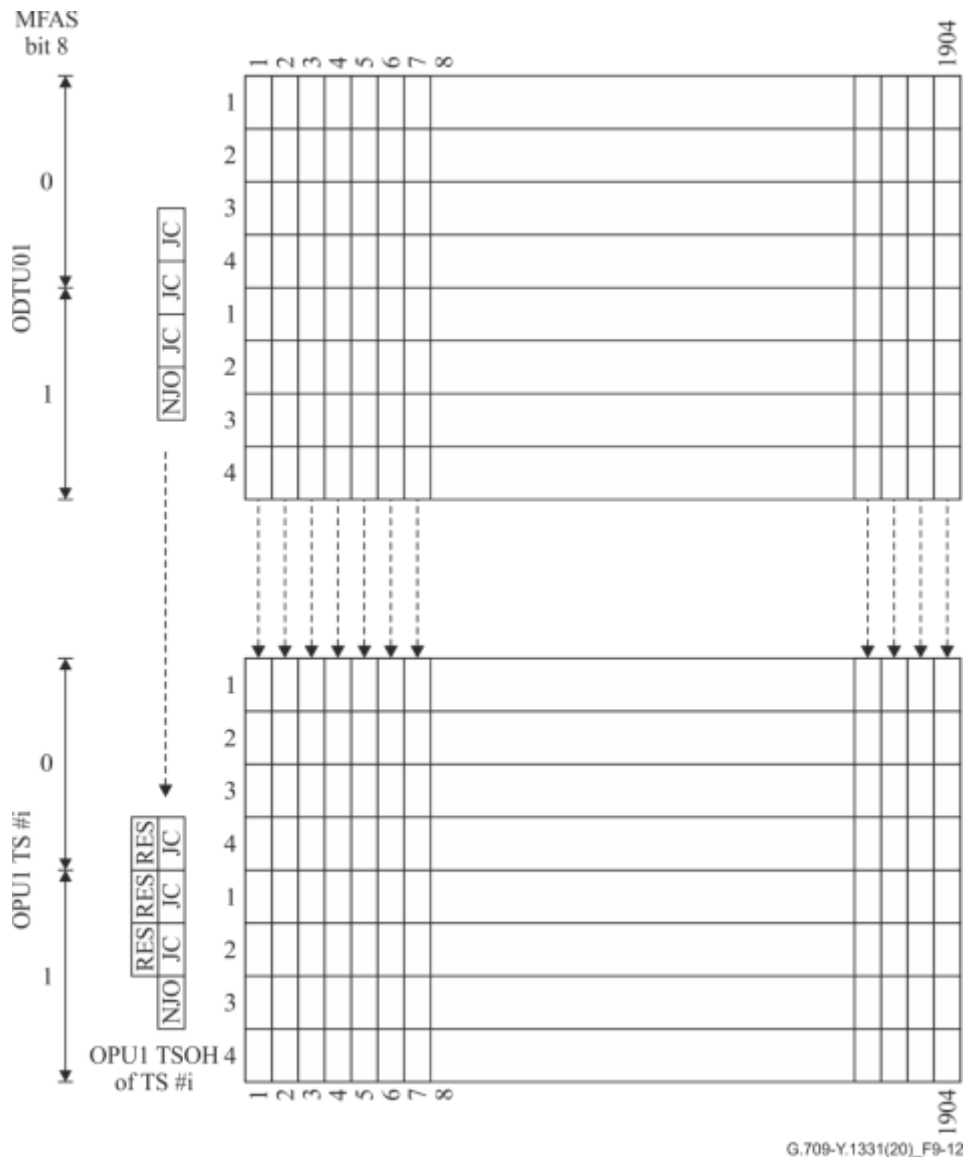
**Figure 19-11 – Mapping of ODTU23 into 4 OPU3 2.5G tributary slots (#A, #B, #C, #D with A<B<C<D) (top) and 8 OPU3 1.25G tributary slots (#A, #B, #C, #D, #E, #F, #G, #H with A<B<C<D<E<F<G<H) (bottom)**

### 19.3.4 ODTU01 mapping into one OPU1 1.25G tributary slot

A byte of the ODTU01 signal is mapped into a byte of an OPU1 1.25G TS #i (i = 1,2), as indicated in Figure 19-12 for a group of 4 rows out of the ODTU01.

A byte of the ODTU01 TSOH is mapped into a TSOH byte within column 16 of the OPU1 1.25G TS #i.

The remaining OPU1 TSOH bytes in column 15 are reserved for future international standardization.



**Figure 19-12 – Mapping of ODTU01 (excluding JOH) into OPU1 1.25G tributary slot**

### 19.3.5 ODTU2.ts mapping into ts OPU2 1.25G tributary slots

A byte of the ODTU2.ts payload signal is mapped into a byte of an OPU2 1.25G TS #i (i = 1,...,ts) payload area, as indicated in Figure 19-13.

A byte of the ODTU2.ts overhead is mapped into a TSOH byte within columns 15 and 16, rows 1 to 3 of the last OPU2 1.25G tributary slot allocated to the ODTU2.ts.

The remaining OPU2 TSOH bytes are reserved for future international standardization.

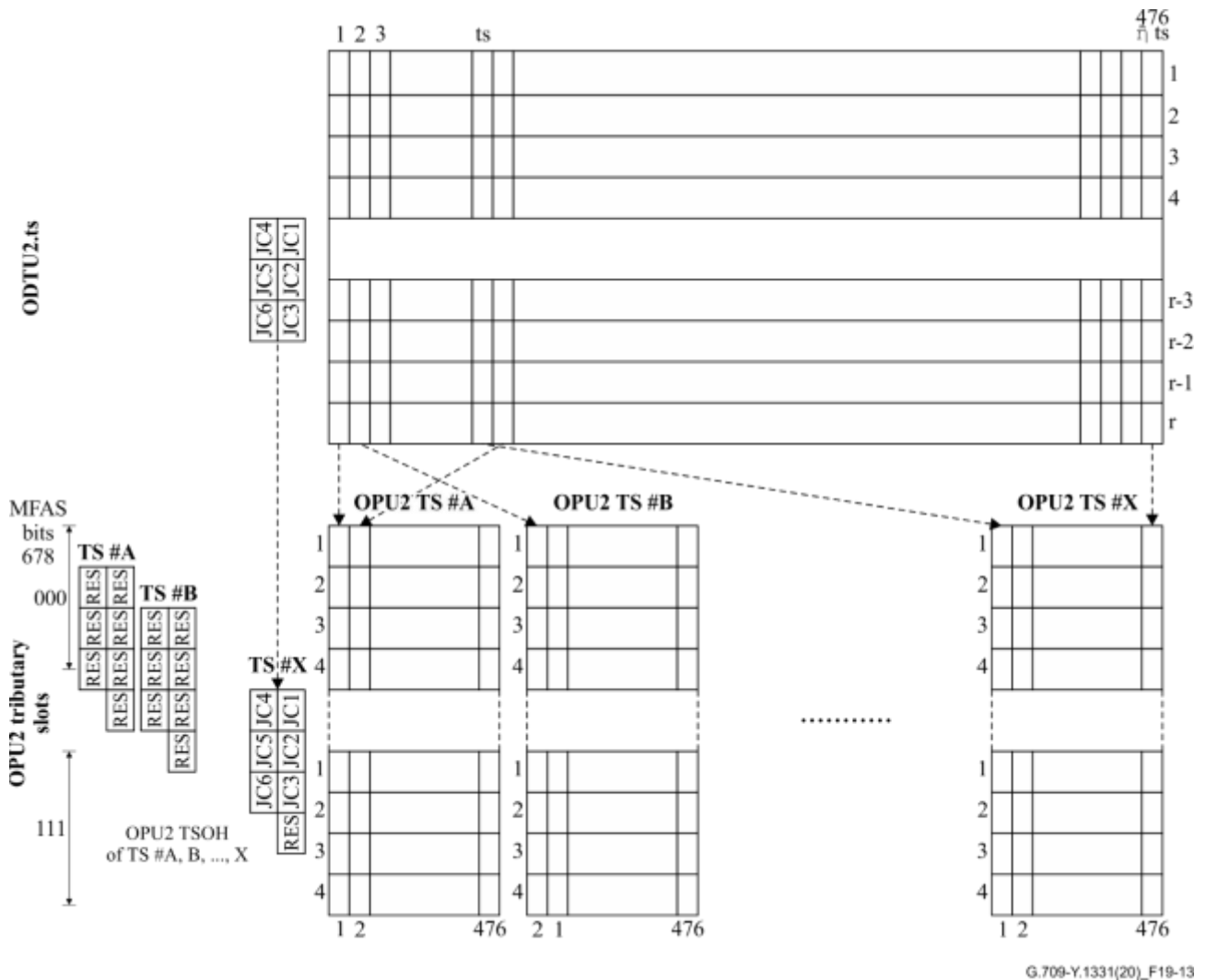


Figure 19-13 – Mapping of ODTU2.ts into 'ts' OPU2 1.25G tributary slots

### 19.3.6 ODTU3.ts mapping into ts OPU3 1.25G tributary slots

A byte of the ODTU3.ts payload signal is mapped into a byte of an OPU3 1.25G TS #i (i = 1,...,ts) payload area, as indicated in Figure 19-14.

A byte of the ODTU3.ts overhead is mapped into a TSOH byte within columns 15 and 16, rows 1 to 3 of the last OPU3 1.25G tributary slot allocated to the ODTU3.ts.

The remaining OPU3 TSOH bytes are reserved for future international standardization.

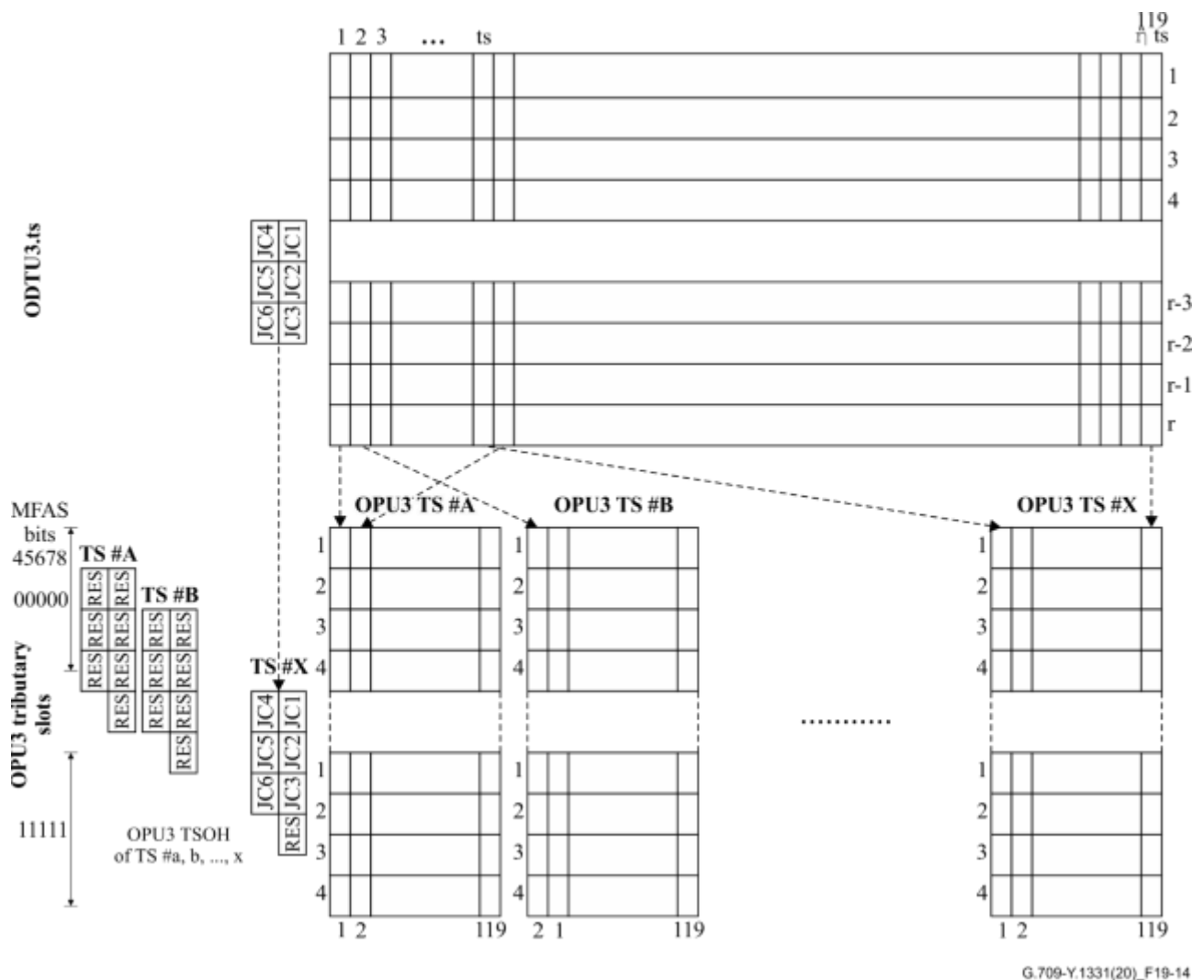


Figure 19-14 – Mapping of ODTU3.ts into 'ts' OPU3 1.25G tributary slots

### 19.3.7 ODTU4.ts mapping into ts OPU4 1.25G tributary slots

A byte of the ODTU4.ts payload signal is mapped into a byte of an OPU4 1.25G TS #i (i = 1,...,ts) payload area, as indicated in Figure 19-15.

A byte of the ODTU4.ts overhead is mapped into a TSOH byte within columns 15 and 16, rows 1 to 3 of the last OPU4 1.25G tributary slot allocated to the ODTU4.ts.

The remaining OPU4 TSOH bytes are reserved for future international standardization.

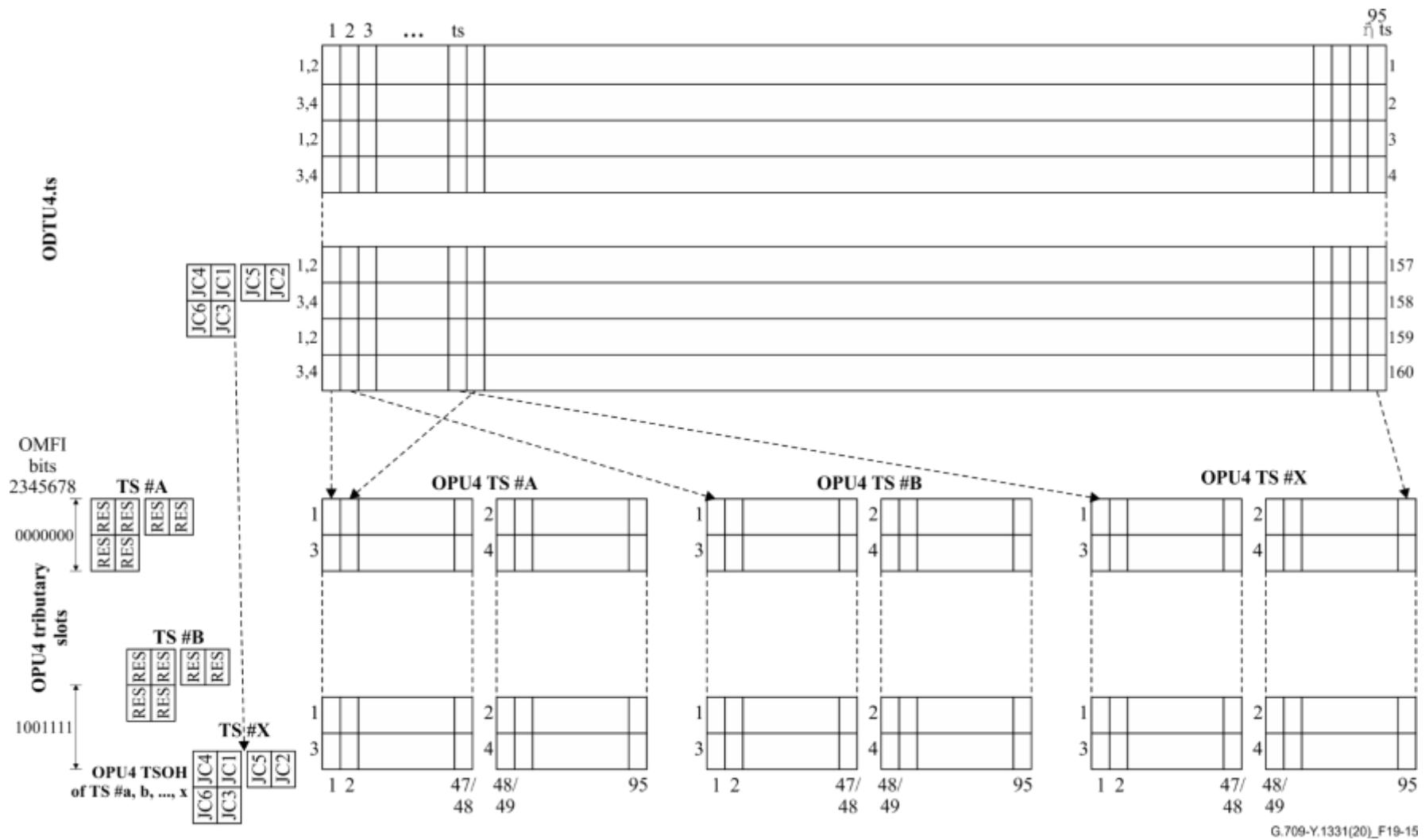


Figure 19-15 – Mapping of ODTU4.ts into 'ts' OPU4 1.25G tributary slots

### 19.3.8 ODTU25.ts mapping into ts OPU25 1.25G tributary slots

A byte of the ODTU25.ts payload signal is mapped into a byte of an OPU25 1.25G TS #i (i = 1,...,ts) payload area, as indicated in Figure 19-16.

A byte of the ODTU25.ts overhead is mapped into a TSOH byte within columns 15 and 16, rows 1 to 3 of the last OPU25 1.25G tributary slot allocated to the ODTU25.ts.

The remaining OPU25 TSOH bytes are reserved for future international standardization.

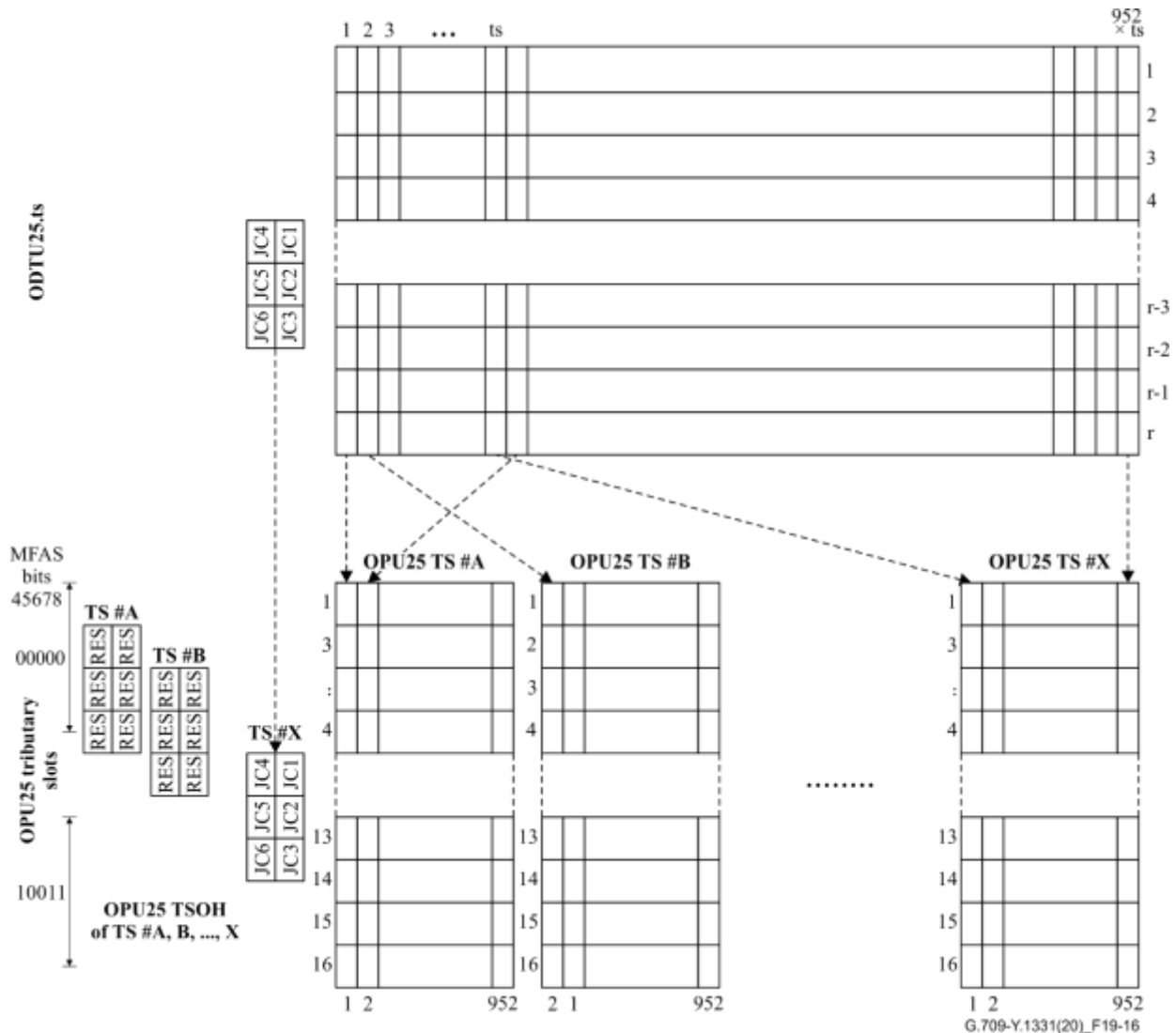


Figure 19-16 – Mapping of ODTU25.ts into 'ts' OPU25 1.25G tributary slots

### 19.3.9 ODTU50.ts mapping into ts OPU50 1.25G tributary slots

A byte of the ODTU50.ts payload signal is mapped into a byte of an OPU50 1.25G TS #i (i = 1,...,ts) payload area, as indicated in Figure 19-17.

A byte of the ODTU50.ts overhead is mapped into a TSOH byte within columns 15 and 16, rows 1 to 3 of the last OPU50 1.25G tributary slot allocated to the ODTU50.ts.

The remaining OPU50 TSOH bytes are reserved for future international standardization.



located in the second column of OPU $k$  2.5G tributary slot # $i$  (OPU2 column  $20+i$ , OPU3 column  $32+i$ ) in frame # $i$  of the four or sixteen frame multiframe.

EXAMPLE – ODU1 in OPU2 or OPU3 TS(1): PJO1 in column  $16+1=17$ , PJO2 in column  $20+1=21$  (OPU2) and  $32+1=33$  (OPU3). ODU1 in OPU2 TS(4): PJO1 in column  $16+4=20$ , PJO2 in column  $20+4=24$ . ODU1 in OPU3 TS(16): PJO1 in column  $16+16=32$ , PJO2 in column  $32+16=48$ .

The four PJO1s for an ODU2 in OPU3 2.5G tributary slots # $a$ , # $b$ , # $c$  and # $d$  are located in the first column of OPU3 2.5G tributary slot # $a$  (OPU3 column  $16+a$ ) in frames # $a$ , # $b$ , # $c$  and # $d$  of the sixteen frame multiframe. The four PJO2s for an ODU2 in OPU3 2.5G tributary slots # $a$ , # $b$ , # $c$  and # $d$  are located in the first column of OPU3 2.5G tributary slot # $b$  (OPU3 column  $16+b$ ) in frames # $a$ , # $b$ , # $c$  and # $d$  of the sixteen frame multiframe. Figure 19-18A presents an example with four ODU2s in the OPU3 mapped into 2.5G tributary slots (1,5,9,10), (2,3,11,12), (4,14,15,16) and (6,7,8,13).

EXAMPLE – ODU2 in OPU3 TS(1,2,3,4): PJO1 in column  $16+1=17$ , PJO2 in column  $16+2=18$ . ODU2 in OPU3 TS(13,14,15,16): PJO1 in column  $16+13=29$ , PJO2 in column  $16+14=30$ .

The PJO1 for an ODU0 in OPU1 1.25G tributary slot # $i$  ( $i$ : 1,2) is located in the first column of OPU1 1.25G tributary slot # $i$  (OPU1 column  $16+i$ ) and the PJO2 is located in the second column of OPU1 1.25G tributary slot # $i$  (OPU1 column  $18+i$ ) in frame # $i$  of the two frame multiframe.

The PJO1 for an ODU1 in OPU2 or OPU3 1.25G tributary slots # $a$  and # $b$  ( $a$ : 1..7 or 1..31 respectively;  $b$ : 2..8 or 2..32 respectively) is located in the first column of OPU $k$  1.25G tributary slot # $a$  (OPU $k$  column  $16+a$ ) and the PJO2 is located in the first column of OPU $k$  1.25G tributary slot # $b$  (OPU $k$  column  $16+b$ ) in frames # $a$  and # $b$  of the eight or thirty-two frame multiframe.

EXAMPLE – ODU1 in OPU2 or OPU3 TS(1,2): PJO1 in column  $16+1=17$ , PJO2 in column  $16+2=18$ . ODU1 in OPU2 TS(7,8): PJO1 in column  $16+7=23$ , PJO2 in column  $16+8=24$ . ODU1 in OPU3 TS(31,32): PJO1 in column  $16+31=47$ , PJO2 in column  $16+32=48$ .

The eight PJO1s for an ODU2 in OPU3 1.25G tributary slots # $a$ , # $b$ , # $c$ , # $d$ , # $e$ , # $f$ , # $g$  and # $h$  are located in the first column of OPU3 1.25G tributary slot # $a$  (OPU3 column  $16+a$ ) in frames # $a$ , # $b$ , # $c$ , # $d$ , # $e$ , # $f$ , # $g$  and # $h$  of the thirty-two frame multiframe. The eight PJO2s for an ODU2 in OPU3 1.25G tributary slots # $a$ , # $b$ , # $c$ , # $d$ , # $e$ , # $f$ , # $g$  and # $h$  are located in the first column of OPU3 1.25G tributary slot # $b$  (OPU3 column  $16+b$ ) in frames # $a$ , # $b$ , # $c$ , # $d$ , # $e$ , # $f$ , # $g$  and # $h$  of the thirty-two frame multiframe. Figure 19-18B presents an example with two ODU2s and two ODU1s in the OPU3 mapped into 1.25G tributary slots (1,5,9,10,17,19,20,21), (25,26,27,28,29,30,31,32), (2,3) and (4,24).

EXAMPLE – ODU2 in OPU3 TS(1,2,3,4,5,6,7,8): PJO1 in column  $16+1=17$ , PJO2 in column  $16+2=18$ . ODU2 in OPU3 TS(25,26,27,28,29,30,31,32): PJO1 in column  $16+25=41$ , PJO2 in column  $16+26=42$ .



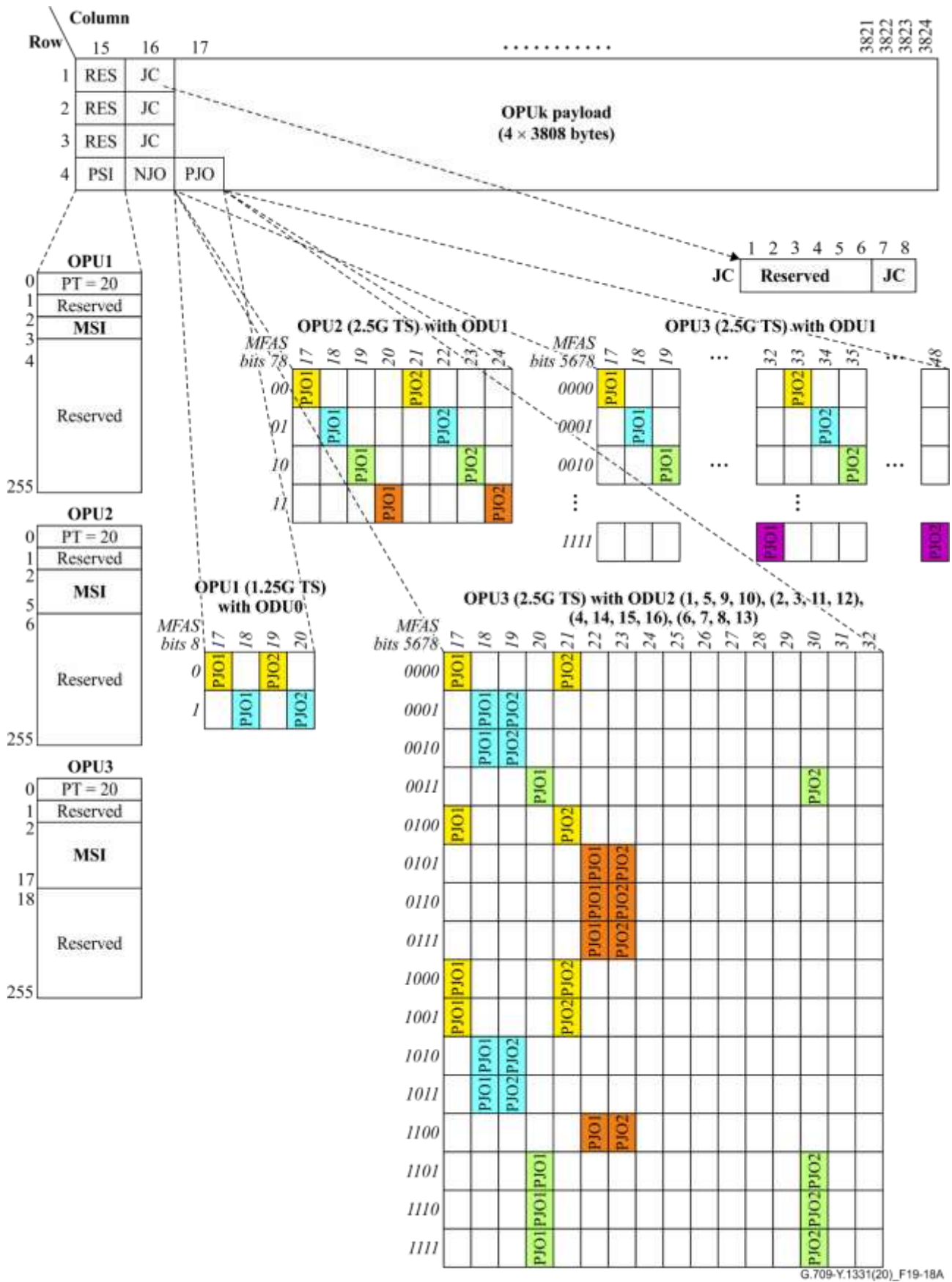


Figure 19-18A – OPUk (k=1,2,3) multiplex overhead associated with an ODTUjk only (payload type = 20)

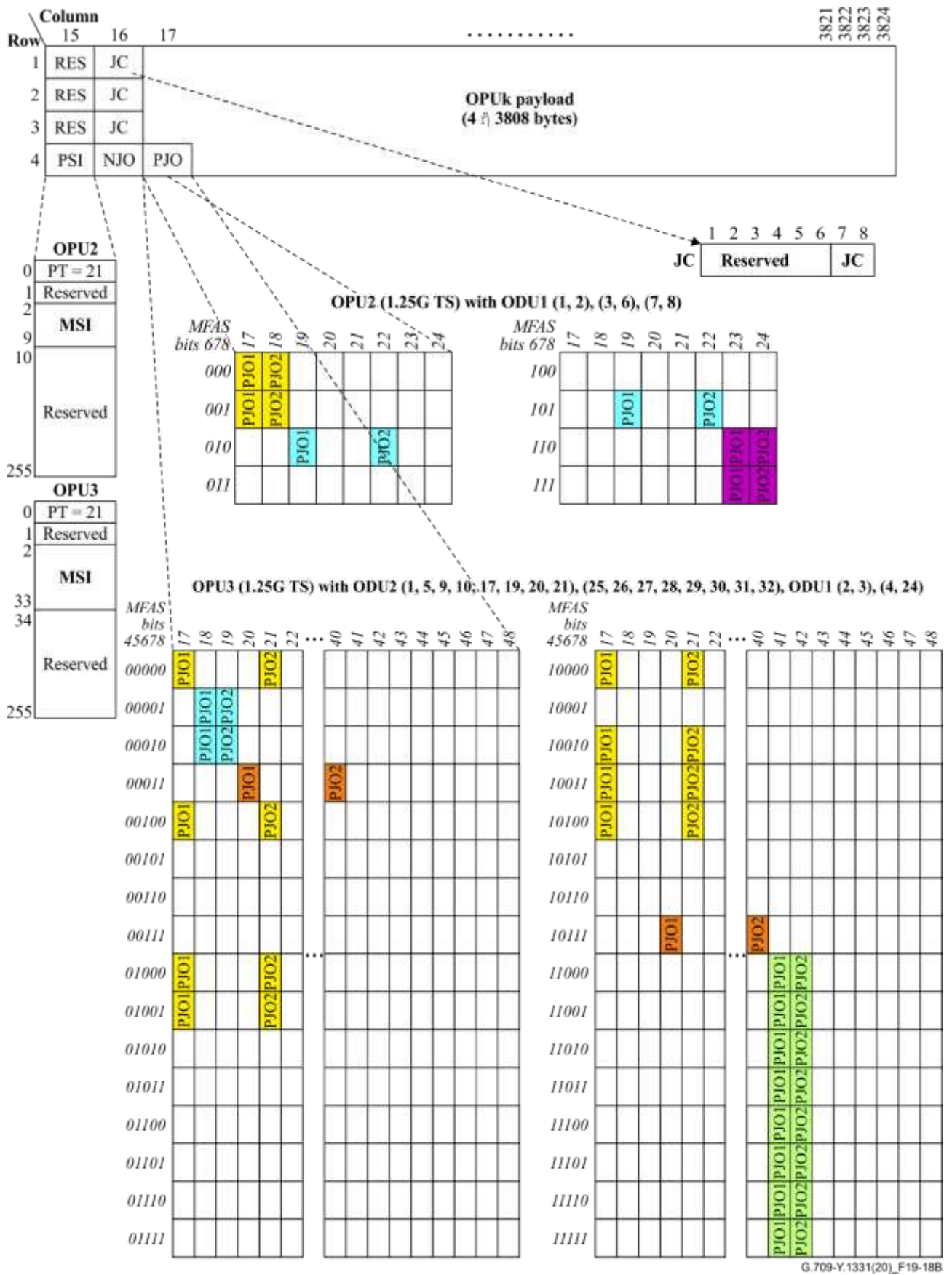
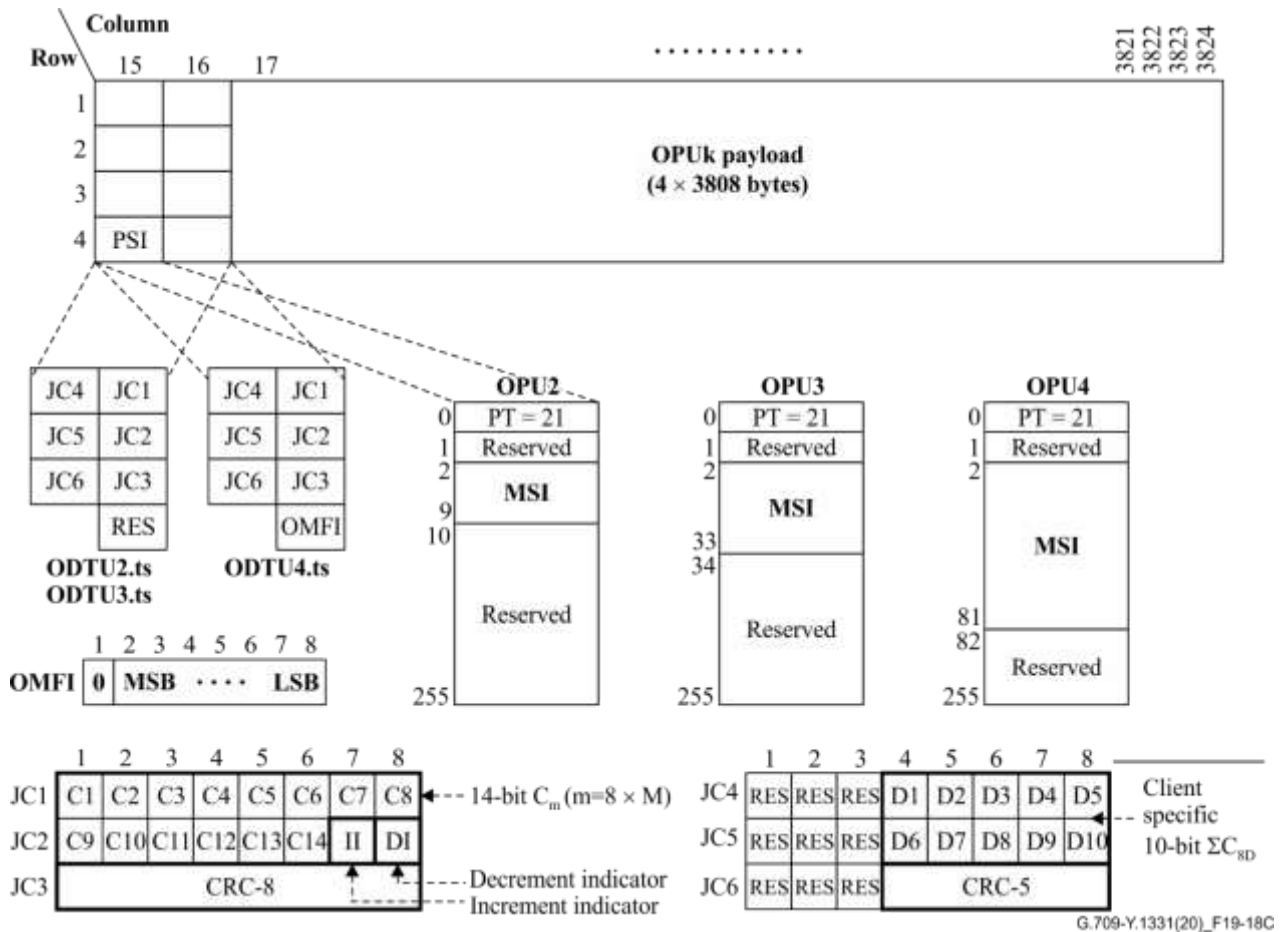


Figure 19-18B – OPUk (k=2,3) multiplex overhead associated with an ODTUjk only (payload type = 21)

## ODTUK.ts overhead

The ODTUK.ts overhead carries the GMP justification overhead consisting of 3 bytes of justification control (JC1, JC2, JC3) which carry the 14-bit GMP  $C_m$  information and client/ODU specific 3 bytes of justification control (JC4, JC5, JC6) which carry the 10-bit GMP  $\Sigma C_{8D}$  information.

The JC1, JC2, JC3, JC4, JC5 and JC6 overhead locations are shown in Figure 19-18C.



**Figure 19-18C – OPUk (k=2,3,4,25,50) multiplex overhead associated with an ODTUK.ts (payload type = 21)**

### 19.4.1 OPUk multiplex structure identifier (MSI)

The OPUk (k=1,2,3,4,25,50) multiplex structure identifier (MSI) overhead, which encodes the ODU multiplex structure in the OPU, is located in the mapping specific area of the PSI signal (refer to Figure 19-18A for the MSI location in OPUk with PT=20, refer to Figures 19-18B and 19-18C for the MSI location in OPUk with PT=21). The MSI has an OPU and tributary slot (2.5G, 1.25G) specific length (OPU1: 2 bytes, OPU2: 4 or 8 bytes, OPU3: 16 or 32 bytes, OPU4: 80 bytes, OPU25: 20 bytes, OPU50: 40 bytes) and indicates the ODTU content of each tributary slot (TS) of an OPU. One byte is used for each TS.

#### 19.4.1.1 OPU2 multiplex structure identifier (MSI) – Payload type 20

For the 4 OPU2 2.5G tributary slots four bytes of the PSI are used (PSI[2] .. PSI[5]) as MSI bytes as shown in Figures 19-18A and 19-19. The MSI indicates the ODTU content of each tributary slot of the OPU2. One byte is used for each tributary slot.

- The ODTU type in bits 1 and 2 is fixed to 00 to indicate the presence of an ODTU12.
- The tributary port # indicates the port number of the ODU1 that is being transported in this 2.5G TS; the assignment of ports to tributary slots is fixed, the port number equals the tributary slot number.

	1	2	3	4	5	6	7	8	
<i>PSI[2]</i>	00				00	0000			<i>TS1</i>
<i>PSI[3]</i>	00				00	0001			<i>TS2</i>
<i>PSI[4]</i>	00				00	0010			<i>TS3</i>
<i>PSI[5]</i>	00				00	0011			<i>TS4</i>

**Figure 19-19 – OPU2-MSI coding – Payload type 20**

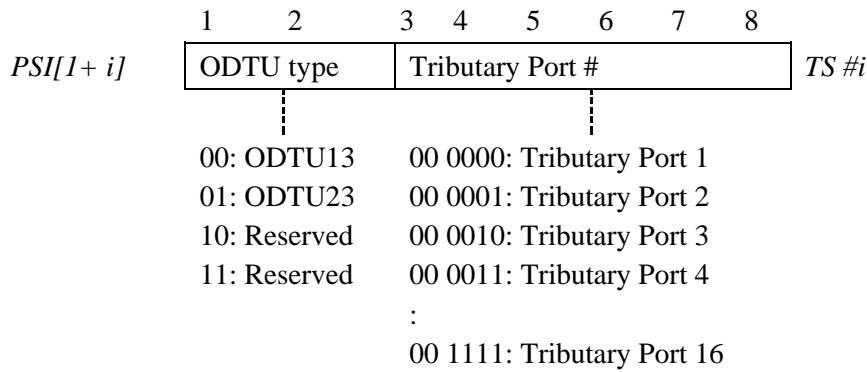
#### 19.4.1.2 OPU3 multiplex structure identifier (MSI) – Payload type 20

For the 16 OPU3 2.5G tributary slots 16 bytes of the PSI are used (*PSI[2]* .. *PSI[17]*) as MSI bytes as shown in Figures 19-18A, 19-20A and 19-20B. The MSI indicates the ODTU content of each tributary slot of the OPU3. One byte is used for each tributary slot.

- The ODTU type in bits 1 and 2 indicates if the OPU3 TS is carrying ODTU13 or ODTU23. The default ODTU type is ODTU13; it is present when either a tributary slot carries an ODTU13, or is not allocated to carry an ODTU. Refer to Appendix V for some examples.
- The tributary port # in bits 3 to 8 indicates the port number of the ODTU13/23 that is being transported in this 2.5G TS; for the case of ODTU23, a flexible assignment of tributary ports to tributary slots is possible, for the case of ODTU13, this assignment is fixed, the tributary port number equals the tributary slot number. ODTU23 tributary ports are numbered 1 to 4.

	1	2	3	4	5	6	7	8	
<i>PSI[2]</i>	ODTU type		Tributary Port #						<i>TS1</i>
<i>PSI[3]</i>	ODTU type		Tributary Port #						<i>TS2</i>
<i>PSI[4]</i>	ODTU type		Tributary Port #						<i>TS3</i>
<i>PSI[5]</i>	ODTU type		Tributary Port #						<i>TS4</i>
<i>PSI[6]</i>	ODTU type		Tributary Port #						<i>TS5</i>
<i>PSI[7]</i>	ODTU type		Tributary Port #						<i>TS6</i>
<i>PSI[8]</i>	ODTU type		Tributary Port #						<i>TS7</i>
<i>PSI[9]</i>	ODTU type		Tributary Port #						<i>TS8</i>
<i>PSI[10]</i>	ODTU type		Tributary Port #						<i>TS9</i>
<i>PSI[11]</i>	ODTU type		Tributary Port #						<i>TS10</i>
<i>PSI[12]</i>	ODTU type		Tributary Port #						<i>TS11</i>
<i>PSI[13]</i>	ODTU type		Tributary Port #						<i>TS12</i>
<i>PSI[14]</i>	ODTU type		Tributary Port #						<i>TS13</i>
<i>PSI[15]</i>	ODTU type		Tributary Port #						<i>TS14</i>
<i>PSI[16]</i>	ODTU type		Tributary Port #						<i>TS15</i>
<i>PSI[17]</i>	ODTU type		Tributary Port #						<i>TS16</i>

**Figure 19-20A – OPU3-MSI coding – Payload type 20**

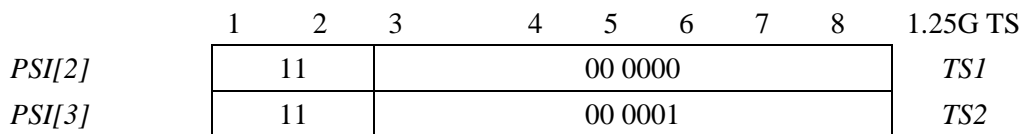


**Figure 19-20B – OPU3 MSI coding – Payload type 20**

### 19.4.1.3 OPU1 multiplex structure identifier (MSI) – Payload type 20

For the 2 OPU1 1.25G tributary slots 2 bytes of the PSI are used ( $PSI[2]$ ,  $PSI[3]$ ) as MSI bytes as shown in Figures 19-18A and 19-21. The MSI indicates the ODTU content of each tributary slot of the OPU1. One byte is used for each tributary slot.

- The ODTU type in bits 1 and 2 is fixed to 11 to indicate the presence of an ODTU01.
- The tributary port # in bits 3 to 8 indicates the port number of the ODTU01 that is being transported in this 1.25G TS; the assignment of ports to tributary slots is fixed, the port number equals the tributary slot number.



**Figure 19-21 – OPU1 MSI coding – Payload type 20**

### 19.4.1.4 OPU4 multiplex structure identifier (MSI) – Payload type 21

For the eighty OPU4 1.25G tributary slots 80 bytes of the PSI are used ( $PSI[2]$  to  $PSI[81]$ ) as MSI bytes as shown in Figures 19-18C, 19-22A and 19-22B. The MSI indicates the ODTU content of each tributary slot of an OPU. One byte is used for each tributary slot.

- The TS occupation bit 1 indicates if the tributary slot is allocated or unallocated.
- The tributary port # in bits 2 to 8 indicates the port number of the ODTU4.ts that is being transported in this TS; for the case of an ODTU4.ts carried in two or more tributary slots, a flexible assignment of tributary port to tributary slots is possible. ODTU4.ts tributary ports are numbered 1 to 80. The value is set to all-0s when the occupation bit has the value 0 (tributary slot is unallocated).

	1	2	3	4	5	6	7	8	1.25G TS
<i>PSI[2]</i>	TS occupied	Tributary Port #							<i>TS1</i>
<i>PSI[3]</i>	TS occupied	Tributary Port #							<i>TS2</i>
<i>PSI[4]</i>	TS occupied	Tributary Port #							<i>TS3</i>
<i>PSI[5]</i>	TS occupied	Tributary Port #							<i>TS4</i>
<i>PSI[6]</i>	TS occupied	Tributary Port #							<i>TS5</i>
<i>PSI[7]</i>	TS occupied	Tributary Port #							<i>TS6</i>
<i>PSI[8]</i>	TS occupied	Tributary Port #							<i>TS7</i>
<i>PSI[9]</i>	TS occupied	Tributary Port #							<i>TS8</i>
:	:	:							:
:	:	:							:
<i>PSI[81]</i>	TS occupied	Tributary Port #							<i>TS80</i>

**Figure 19-22A – OPU4 1.25G TS MSI coding – Payload type 21**

	1	2	3	4	5	6	7	8	
<i>PSI[1 + i]</i>	Occupation		Tributary Port #						<i>TS #i</i>
	0 : Unallocated		000 0000: Tributary Port 1						
	1 : Allocated		000 0001: Tributary Port 2						
			000 0010: Tributary Port 3						
			000 0011: Tributary Port 4						
			:						
			100 1111: Tributary Port 80						

**Figure 19-22B – OPU4 MSI coding – Payload type 21**

#### 19.4.1.5 OPU2 multiplex structure identifier (MSI) – Payload type 21

For the eight OPU2 1.25G tributary slots 8 bytes of the PSI (*PSI[2]* to *PSI[9]*) are used as MSI bytes as show in Figures 19-18B, 19-23A and 19-23B. The MSI indicates the ODTU content of each tributary slot of an OPU. One byte is used for each tributary slot.

- The ODTU type in bits 1 and 2 indicates if the OPU2 1.25G TS is carrying an ODTU12 or ODTU2.ts. The default ODTU type is 11 (unallocated); it is present when a tributary slot is not allocated to carry an ODTU.
- The tributary port # in bits 3 to 8 indicates the port number of the ODTU that is being transported in this TS; a flexible assignment of tributary ports to tributary slots is possible, ODTU12 tributary ports are numbered 1 to 4, and ODTU2.ts tributary ports are numbered 1 to 8. The value is set to all-0s when the ODTU type has the value 11 (tributary slot is unallocated).

	1	2	3	4	5	6	7	8	
<i>PSI[2]</i>	ODTU type		Tributary Port #						<i>TS1</i>
<i>PSI[3]</i>	ODTU type		Tributary Port #						<i>TS2</i>
<i>PSI[4]</i>	ODTU type		Tributary Port #						<i>TS3</i>
<i>PSI[5]</i>	ODTU type		Tributary Port #						<i>TS4</i>
<i>PSI[6]</i>	ODTU type		Tributary Port #						<i>TS5</i>
<i>PSI[7]</i>	ODTU type		Tributary Port #						<i>TS6</i>
<i>PSI[8]</i>	ODTU type		Tributary Port #						<i>TS7</i>
<i>PSI[9]</i>	ODTU type		Tributary Port #						<i>TS8</i>

**Figure 19-23A – OPU2 MSI coding – Payload type 21**

	1	2	3	4	5	6	7	8	
<i>PSI[1+ i]</i>	ODTU type		Tributary Port #						<i>TS #i</i>
	00: ODTU12		00 0000: Tributary Port 1						
	01: Reserved		00 0001: Tributary Port 2						
	10: ODTU2.ts		00 0010: Tributary Port 3						
	11: Unallocated		00 0011: Tributary Port 4						
			:						
			00 0111: Tributary Port 8						

**Figure 19-23B – OPU2 MSI coding – Payload type 21**

#### 19.4.1.6 OPU3 with 1.25G tributary slots (payload type 21) multiplex structure identifier (MSI)

For the thirty-two OPU3 1.25G tributary slots 32 bytes of the PSI (*PSI[2]* to *PSI[33]*) are used as MSI bytes as shown in Figures 19-18B, 19-24A and 19-24B. The MSI indicates the ODTU content of each tributary slot of an OPU. One byte is used for each tributary slot.

- The ODTU type in bits 1 and 2 indicates if the OPU3 1.25G TS is carrying an ODTU13, ODTU23 or ODTU3.ts. The default ODTU type is 11 (unallocated); it is present when a tributary slot is not allocated to carry an ODTU.
- The tributary port # in bits 3 to 8 indicates the port number of the ODTU that is being transported in this TS; a flexible assignment of tributary ports to tributary slots is possible, ODTU13 tributary ports are numbered 1 to 16, ODTU23 tributary ports are numbered 1 to 4 and ODTU3.ts tributary ports are numbered 1 to 32. The value is set to all-0s when the ODTU type has the value 11 (tributary slot is unallocated).

	1	2	3	4	5	6	7	8	
<i>PSI[2]</i>	ODTU type		Tributary Port #						<i>TS1</i>
<i>PSI[3]</i>	ODTU type		Tributary Port #						<i>TS2</i>
<i>PSI[4]</i>	ODTU type		Tributary Port #						<i>TS3</i>
<i>PSI[5]</i>	ODTU type		Tributary Port #						<i>TS4</i>
<i>PSI[6]</i>	ODTU type		Tributary Port #						<i>TS5</i>
:	:	:						:	
:	:	:						:	
<i>PSI[33]</i>	ODTU type		Tributary Port #						<i>TS32</i>

**Figure 19-24A – OPU3 MSI coding – Payload type 21**

	1	2	3	4	5	6	7	8	
<i>PSI[1+ i]</i>	ODTU type		Tributary Port #						<i>TS #i</i>
	00: ODTU13		00 0000: Tributary Port 1						
	01: ODTU23		00 0001: Tributary Port 2						
	10: ODTU3.ts		00 0010: Tributary Port 3						
	11: Unallocated		00 0011: Tributary Port 4						
			:						
			01 1111: Tributary Port 32						

**Figure 19-24B – OPU3 MSI coding – Payload type 21**

#### 19.4.1.7 OPU25 multiplex structure identifier (MSI) – Payload type 21

For the twenty OPU25 1.25G tributary slots 20 bytes of the PSI are used (*PSI[2]* to *PSI[21]*) as MSI bytes as shown in Figures 19-18C, 19-25A and 19-25B. The MSI indicates the ODTU content of each tributary slot of an OPU. One byte is used for each tributary slot.

- The TS occupation bit 1 indicates if the tributary slot is allocated or unallocated.
- The tributary port # in bits 2 to 8 indicates the port number of the ODTU25.ts that is being transported in this TS; for the case of an ODTU25.ts carried in two or more tributary slots, a flexible assignment of tributary port to tributary slots is possible. ODTU25.ts tributary ports are numbered 1 to 20. The value is set to all-0s when the occupation bit has the value 0 (tributary slot is unallocated).



	1	2	3	4	5	6	7	8	1.25G TS
<i>PSI[2]</i>	TS occupied	Tributary Port #							<i>TS1</i>
<i>PSI[3]</i>	TS occupied	Tributary Port #							<i>TS2</i>
<i>PSI[4]</i>	TS occupied	Tributary Port #							<i>TS3</i>
<i>PSI[5]</i>	TS occupied	Tributary Port #							<i>TS4</i>
<i>PSI[6]</i>	TS occupied	Tributary Port #							<i>TS5</i>
:	:	:							:
:	:	:							:
<i>PSI[21]</i>	TS occupied	Tributary Port #							<i>TS20</i>

**Figure 19-25A – OPU25 1.25G TS MSI coding – Payload type 21**

	1	2	3	4	5	6	7	8	<i>TS #i</i>
<i>PSI[1+ i]</i>	Occupation	Tributary Port #							
0 : Unallocated		000 0000: Tributary Port 1							
1 : Allocated		000 0001: Tributary Port 2							
		000 0010: Tributary Port 3							
		000 0011: Tributary Port 4							
		:							
		001 0011: Tributary Port 20							

**Figure 19-25B – OPU25 MSI coding – Payload type 21**

#### 19.4.1.8 OPU50 multiplex structure identifier (MSI) – Payload type 21

For the forty OPU50 1.25G tributary slots 40 bytes of the PSI are used (*PSI[2]* to *PSI[41]*) as MSI bytes as shown in Figures 19-18C, 19-26A and 19-26B. The MSI indicates the ODTU content of each tributary slot of an OPU. One byte is used for each tributary slot.

- The TS occupation bit 1 indicates if the tributary slot is allocated or unallocated.
- The tributary port # in bits 2 to 8 indicates the port number of the ODTU50.ts that is being transported in this TS; for the case of an ODTU50.ts carried in two or more tributary slots, a flexible assignment of tributary port to tributary slots is possible. ODTU50.ts tributary ports are numbered 1 to 40. The value is set to all-0s when the occupation bit has the value 0 (tributary slot is unallocated).

	1	2	3	4	5	6	7	8	1.25G TS
<i>PSI[2]</i>	TS occupied	Tributary Port #							<i>TS1</i>
<i>PSI[3]</i>	TS occupied	Tributary Port #							<i>TS2</i>
<i>PSI[4]</i>	TS occupied	Tributary Port #							<i>TS3</i>
<i>PSI[5]</i>	TS occupied	Tributary Port #							<i>TS4</i>
<i>PSI[6]</i>	TS occupied	Tributary Port #							<i>TS5</i>
<i>PSI[7]</i>	TS occupied	Tributary Port #							<i>TS6</i>
:	:	:							:
:	:	:							:
<i>PSI[41]</i>	TS occupied	Tributary Port #							<i>TS40</i>

**Figure 19-26A – OPU50 1.25G TS MSI coding – Payload type 21**

	1	2	3	4	5	6	7	8	
<i>PSI[1+ i]</i>	Occupation	Tributary Port #							<i>TS #i</i>
		:	:	:	:	:	:	:	
	0 : Unallocated	000 0000: Tributary Port 1							
	1 : Allocated	000 0001: Tributary Port 2							
		000 0010: Tributary Port 3							
		000 0011: Tributary Port 4							
		:							
		010 0111: Tributary Port 40							

**Figure 19-26B – OPU50 MSI coding – Payload type 21**

#### 19.4.2 OPU<sub>k</sub> payload structure identifier reserved overhead (RES)

253 (OPU1), 251 or 247 (OPU2), 239 or 223 (OPU3), 175 (OPU4), 234 (OPU25) and 214 (OPU50) bytes are reserved in the OPU<sub>k</sub> PSI for future international standardization. These bytes are located in PSI[1] and PSI[4] (OPU1), PSI[6] or PSI[10] (OPU2), PSI[18] or PSI[34] (OPU3), PSI[82] (OPU4), PSI[22] (OPU25), PSI[42] (OPU50) to PSI[255] of the OPU<sub>k</sub> overhead. These bytes are set to all-0s.

#### 19.4.3 OPU<sub>k</sub> multiplex justification overhead (JOH)

Two mapping procedures are used for the mapping of ODU<sub>j</sub>: either the asynchronous mapping procedure (AMP) or generic mapping procedure (GMP) into ODTU<sub>jk</sub> or ODTU<sub>k.ts</sub>, respectively. AMP uses ODU<sub>j</sub> and OPU<sub>k</sub> specific fixed stuff and justification opportunity definitions (ODTU<sub>jk</sub>). GMP uses ODU<sub>j</sub> and OPU<sub>k</sub> independent stuff and justification opportunity definitions (ODTU<sub>k.ts</sub>). Stuff locations within an ODTU<sub>k.ts</sub> are determined by means of a formula which is specified in clause 19.4.3.2.

##### 19.4.3.1 Asynchronous mapping procedures (AMP)

The justification overhead (JOH) located in column 16 of the OPU<sub>k</sub> (k=1,2,3) as indicated in Figures 19-18A and 19-18B consists of three justification control (JC) bytes and one negative justification opportunity (NJO) byte. The three JC bytes are located in rows 1, 2 and 3. The NJO byte is located in row 4.

Bits 7 and 8 of each JC byte are used for justification control. The other six bits are reserved for future international standardization.

### 19.4.3.2 Generic mapping procedure (GMP)

The justification overhead (JOH) for the generic mapping procedure consists of two groups of three bytes of justification control; the general (JC1, JC2, JC3) and the client to ODU mapping specific (JC4, JC5, JC6). Refer to Figure 19-18C.

The JC1, JC2 and JC3 bytes consist of a 14-bit  $C_m$  field (bits C1, C2, ..., C14), a 1-bit increment indicator (II) field, a 1-bit decrement indicator (DI) field and an 8-bit CRC-8 field which contains an error check code over the JC1, JC2 and JC3 fields.

The JC4, JC5 and JC6 bytes consist of a 10-bit  $\Sigma C_{nD}$  field (bits D1, D2, ..., D10), a 5-bit CRC-5 field which contains an error check code over bits 4 to 8 in the JC4, JC5 and JC6 fields and nine bits reserved for future international standardization (RES).

The value of 'm' in  $C_m$  is  $8 \times \text{'ts'}$  (number of tributary slots occupied by the ODTUK.ts).

The value of 'n' represents the timing granularity of the GMP  $C_n$  parameter, which is also present in  $\Sigma C_{nD}$ . The value of n is 8.

The value of  $C_m$  controls the distribution of groups of 'ts' ODU<sub>j</sub> data bytes into groups of 'ts' ODTUK.ts payload bytes. Refer to clause 19.6 and Annex D for further specification of this process.

The value of  $\Sigma C_{nD}$  provides additional 'n'-bit timing information, which is necessary to control the jitter and wander performance experienced by the ODU<sub>j</sub> signal.

The value of  $C_n$  (i.e., number of client n-bit data entities per OPUC<sub>n</sub> multiframe) is computed as follows:  $C_n(t) = m \times C_m(t) + (\Sigma C_{nD}(t) - \Sigma C_{nD}(t-1))$ . Note that the value  $C_{nD}$  is effectively an indication of the amount of data in the mapper's virtual queue that it could not send during that multiframe due to it being less than an M-byte word. For the case where the value of  $\Sigma C_{nD}$  in a multiframe 't' is corrupted, it is possible to recover from such error in the next multiframe 't+1'.

### 19.4.4 OPU multiframe identifier overhead (OMFI)

An OPU4 multiframe identifier (OMFI) byte is defined in row 4, column 16 of the OPU4 overhead (Figure 19-27). The value of bits 2 to 8 of the OMFI byte will be incremented each OPU4 frame to provide an 80 frame multiframe for the multiplexing of ODU<sub>j</sub> signals into the OPU4.

NOTE 1 – It is an option to align the OMFI = 0 position with MFAS = 0 position every 1280 (the least common multiple of 80 and 256) frame periods.

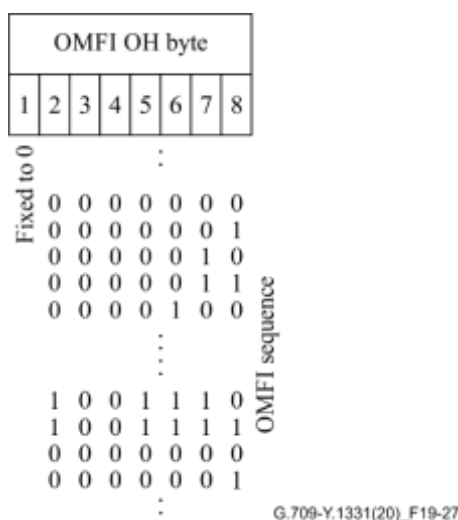


Figure 19-27 – OPU4 multiframe identifier (OMFI) overhead

An OPU25 multiframe identifier (OMFI) byte is defined in row 4, column 16 of the OPU25 overhead (Figure 19-28). The value of bits 4 to 8 of the OMFI byte will be incremented each OPU25 frame to provide a 20 frame multiframe for the multiplexing of ODUj signals into the OPU25.

NOTE 2 – It is an option to align the OMFI = 0 position with MFAS = 0 position every 1280 (the least common multiple of 20 and 256) frame periods.

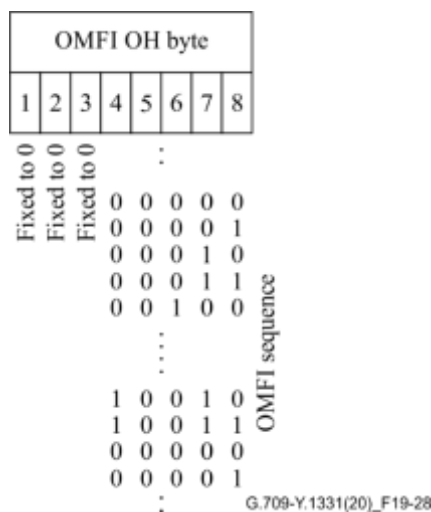


Figure 19-28 – OPU25 multiframe identifier (OMFI) overhead

An OPU50 multiframe identifier (OMFI) byte is defined in row 4, column 16 of the OPU50 overhead (Figure 19-29). The value of bits 3 to 8 of the OMFI byte will be incremented each OPU50 frame to provide a 40 frame multiframe for the multiplexing of ODUj signals into the OPU4.

NOTE 3 – It is an option to align the OMFI = 0 position with MFAS = 0 position every 1280 (the least common multiple of 40 and 256) frame periods.

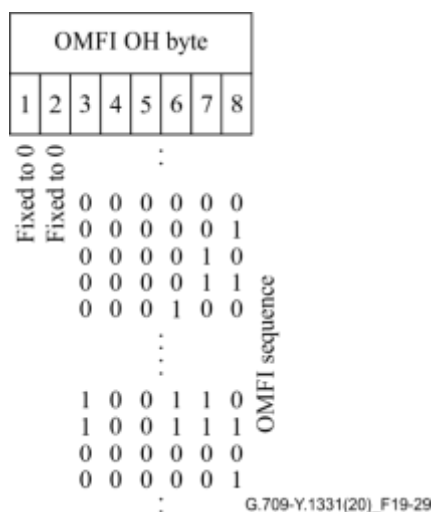


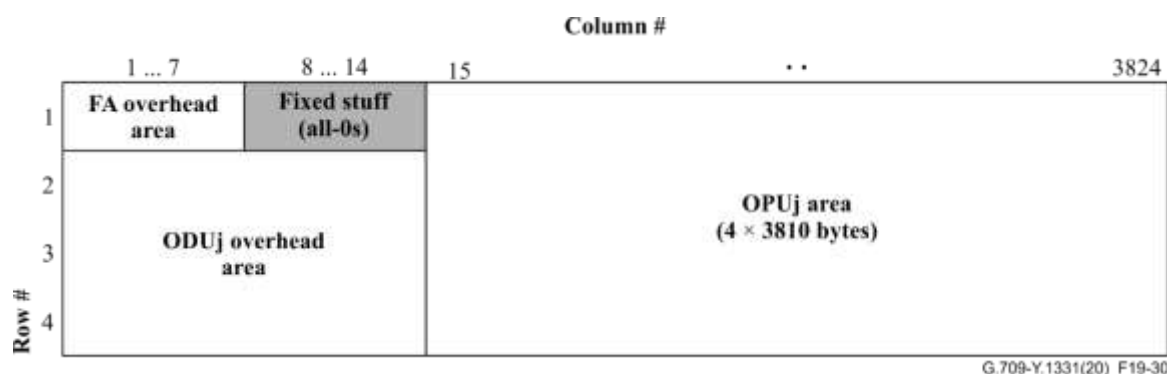
Figure 19-29 – OPU50 multiframe identifier (OMFI) overhead

### 19.5 Mapping ODUj into ODTUjk

The mapping of ODUj signals (with up to ±20 ppm bit-rate tolerance) into the ODTUjk signal ((j,k) = {(0,1), (1,2); (1,3), (2,3)}) is performed as an asynchronous mapping.

NOTE 1 – The maximum bit-rate tolerance between OPUk and the ODUj signal clock, which can be accommodated by this mapping scheme is –130 to +65 ppm (ODU0 into OPU1), –113 to +83 ppm (ODU1 into OPU2), –96 to +101 ppm (ODU1 into OPU3) and –95 to +101 ppm (ODU2 into OPU3).

The ODU<sub>j</sub> signal is extended with a frame alignment overhead as specified in clauses 15.6.2.1 and 15.6.2.2 and an all-0s pattern in the OTU<sub>j</sub> overhead field (see Figure 19-30).



**Figure 19-30 – Extended ODU<sub>j</sub> frame structure  
(FA OH included, OTU<sub>j</sub> OH area contains fixed stuff)**

The OPU<sub>k</sub> signal and therefore the ODTU<sub>jk</sub> ( $k = 1,2,3$ ) signals are created from a locally generated clock (within the limits specified in Table 7-3), which is independent of the ODU<sub>j</sub> ( $j = 0,1,2$ ) client signals.

The extended ODU<sub>j</sub> ( $j = 0,1,2$ ) signal is mapped into the ODTU<sub>jk</sub> ( $k = 1,2,3$ ) using an asynchronous mapping with  $-1/0/+1/+2$  positive/negative/zero (pnz) justification scheme.

An extended ODU<sub>j</sub> byte is mapped into an ODTU<sub>jk</sub> byte.

The asynchronous mapping process generates the JC, NJO, PJO1 and PJO2 according to Table 19-9. The de-mapping process interprets JC, NJO, PJO1 and PJO2 according to Table 19-9. Majority vote (two out of three) shall be used to make the justification decision in the de-mapping process to protect against an error in one of the three JC signals.

**Table 19-9 – JC, NJO, PJO1 and PJO2 generation and interpretation**

JC 7 8	NJO	PJO1	PJO2	Interpretation
0 0	justification byte	data byte	data byte	no justification (0)
0 1	data byte	data byte	data byte	negative justification (-1)
1 0 (Note)	justification byte	justification byte	justification byte	double positive justification (+2)
1 1	justification byte	justification byte	data byte	positive justification (+1)

NOTE – Note that this code is not used for the case of ODU0 into OPU1.

The value contained in NJO, PJO1 and PJO2 when they are used as justification bytes is all-0s. The receiver is required to ignore the value contained in these bytes whenever they are used as justification bytes.

During a signal fail condition of the incoming ODU<sub>j</sub> client signal (e.g., OTU<sub>j</sub>-LOF), this failed incoming signal will contain the ODU<sub>j</sub>-AIS signal as specified in clause 16.5.1. This ODU<sub>j</sub>-AIS is then mapped into the ODTU<sub>jk</sub>.

For the case where the ODU<sub>j</sub> is received from the output of a fabric (ODU connection function), the incoming signal may contain (in the case of an open matrix connection), the ODU<sub>j</sub>-OCI signal as specified in clause 16.5.2. This ODU<sub>j</sub>-OCI signal is then mapped into the ODTU<sub>jk</sub>.

NOTE 2 – Not all equipment will have a real connection function (i.e., switch fabric) implemented; instead, the presence/absence of tributary interface port units represents the presence/absence of a matrix connection. If such a unit is intentionally absent (i.e., not installed), the associated ODTU<sub>jk</sub> signals should carry an ODU<sub>j</sub>-OCI signal. If such a unit is installed but temporarily removed as part of a repair action, the associated ODTU<sub>jk</sub> signal should carry an ODU<sub>j</sub>-AIS signal.

The de-mapping of ODU<sub>j</sub> signals from the ODTU<sub>jk</sub> signal ( $j = 0,1,2$ ;  $k = 1,2,3$ ) is performed by extracting the extended ODU<sub>j</sub> signal from the OPU<sub>k</sub> under control of its justification overhead (JC, NJO, PJO1, PJO2).

NOTE 3 – For the case where the ODU<sub>j</sub> signal is output as an OTU<sub>j</sub> signal, frame alignment of the extracted extended ODU<sub>j</sub> signal is to be recovered to allow frame synchronous mapping of the ODU<sub>j</sub> into the OTU<sub>j</sub> signal.

During a signal fail condition of the incoming ODU<sub>k</sub>/OPU<sub>k</sub> signal (e.g., in the case of an ODU<sub>k</sub>-AIS, ODU<sub>k</sub>-LCK, ODU<sub>k</sub>-OCI condition) the ODU<sub>j</sub>-AIS pattern as specified in clause 16.5.1 is generated as a replacement signal for the lost ODU<sub>j</sub> signal.

### **19.5.1 Mapping ODU1 into ODTU12**

A byte of the ODU1 signal is mapped into an information byte of the ODTU12 (see Figure 19-31A). Once per 4 OPU2 frames, it is possible to perform either a positive or a negative justification action. The frame in which justification can be performed is related to the TSOH of the OPU2 2.5G TS in which the ODTU12 is mapped (Figure 19-1). Figure 19-31A shows the case with mapping in OPU2 2.5G TS1.

A byte of the ODU1 signal is mapped into an information byte of the ODTU12 (see Figure 19-31B). Twice per 8 OPU2 frames, it is possible to perform either a positive or a negative justification action. The frames in which justification can be performed are related to the TSOH of the OPU2 1.25G TSs in which the ODTU12 is mapped (Figure 19-1). Figure 19-31B shows the case with mapping in OPU2 1.25G TS1 and TS4.

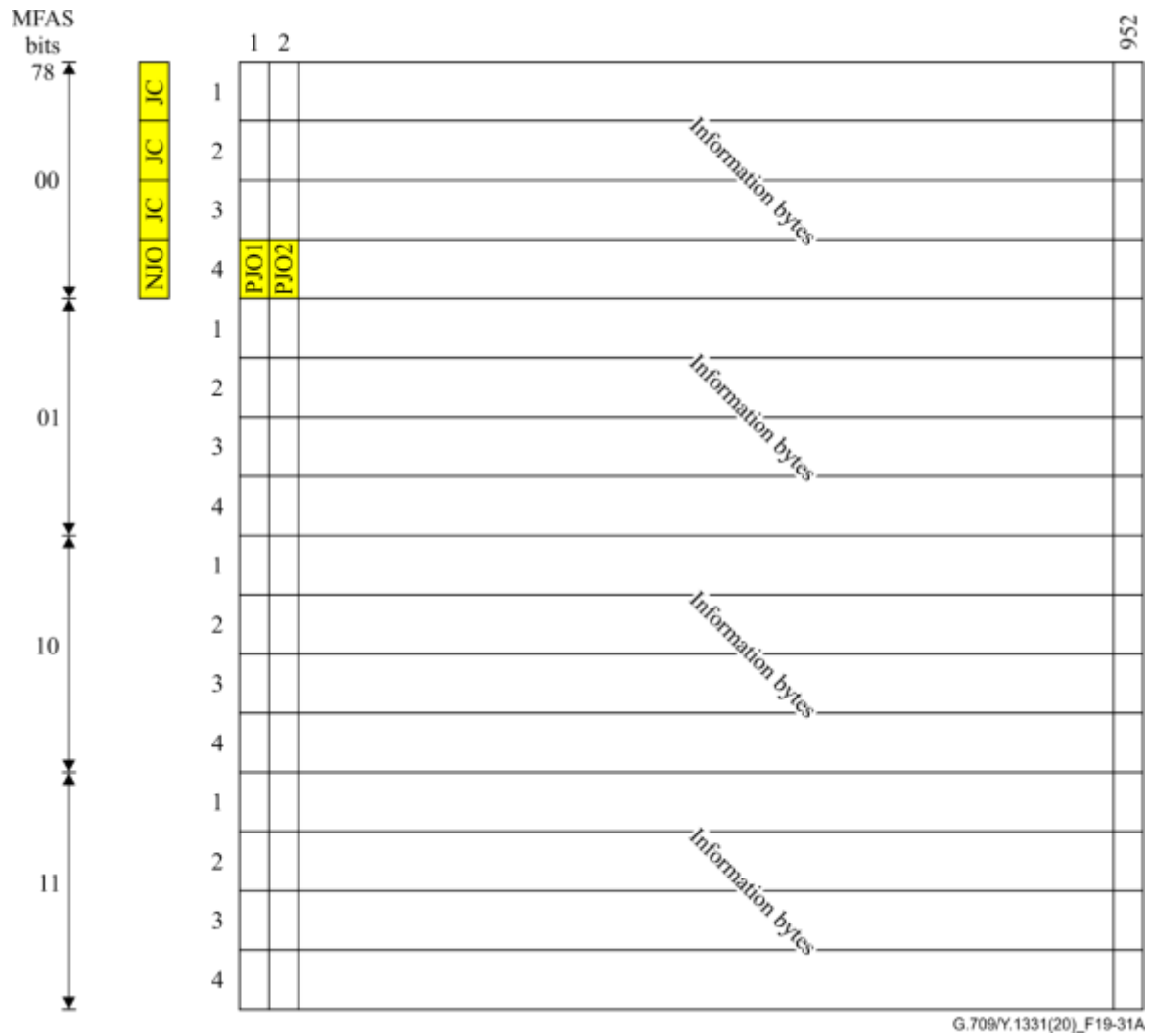
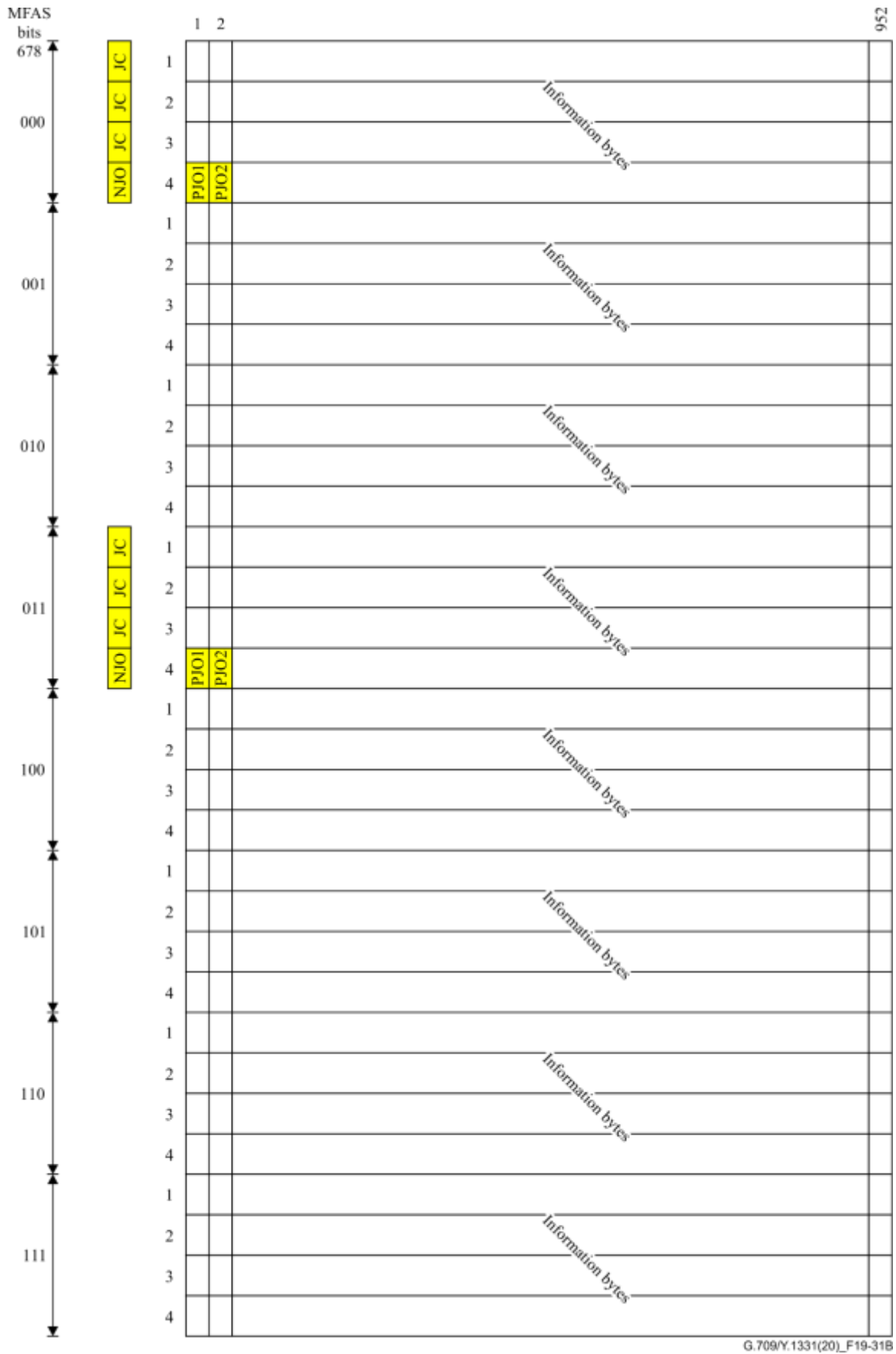


Figure 19-31A – ODTU12 frame format and mapping of ODU1 (mapping in 2.5G TS1)



G.709/Y.1331(20)\_F19-31B

**Figure 19-31B – ODTU12 frame format and mapping of ODU1  
(mapping in 1.25G TS1 and TS4)**



### 19.5.2 Mapping ODU1 into ODTU13

A byte of the ODU1 signal is mapped into an information byte of the ODTU13 (Figure 19-32A). Column 119 of the ODTU13 is fixed stuff. An all-0s pattern is inserted in the fixed stuff bytes. Once per 16 OPU3 frames, it is possible to perform either a positive or a negative justification action. The frame in which justification can be performed is related to the TSOH of the OPU3 2.5G TS in which the ODTU13 is mapped (Figure 19-2). Figure 19-32A shows the case with mapping in OPU3 2.5G TS3.

A byte of the ODU1 signal is mapped into an information byte of the ODTU13 (see Figure 19-32B). Column 119 of the ODTU13 is fixed stuff. An all-0s pattern is inserted in the fixed stuff bytes. Twice per 32 OPU3 frames, it is possible to perform either a positive or a negative justification action. The frames in which justification can be performed are related to the TSOH of the OPU3 1.25G TSs in which the ODTU13 is mapped (Figure 19-2). Figure 19-32B shows the case with mapping in OPU3 1.25G TS2 and TS25.

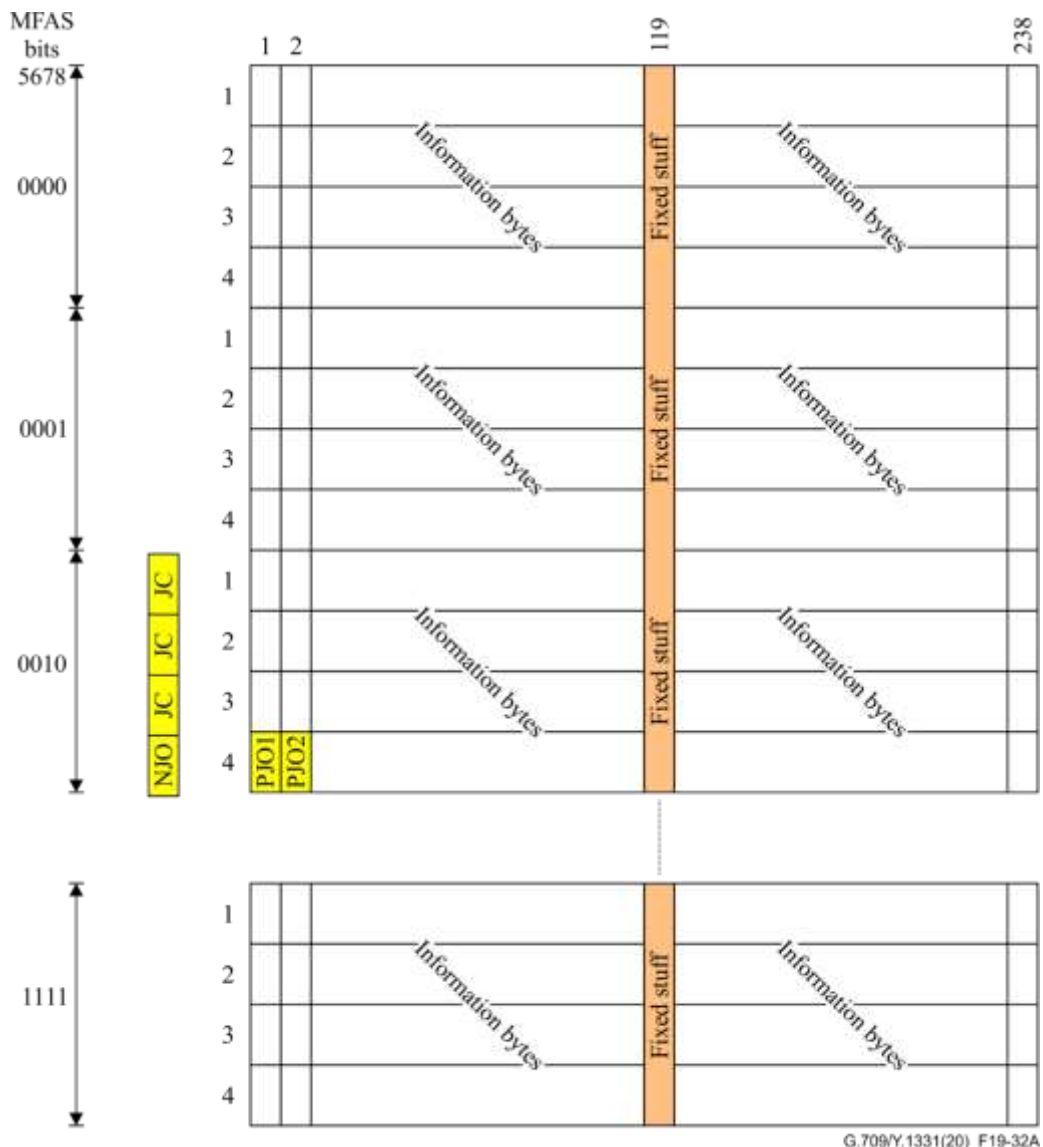
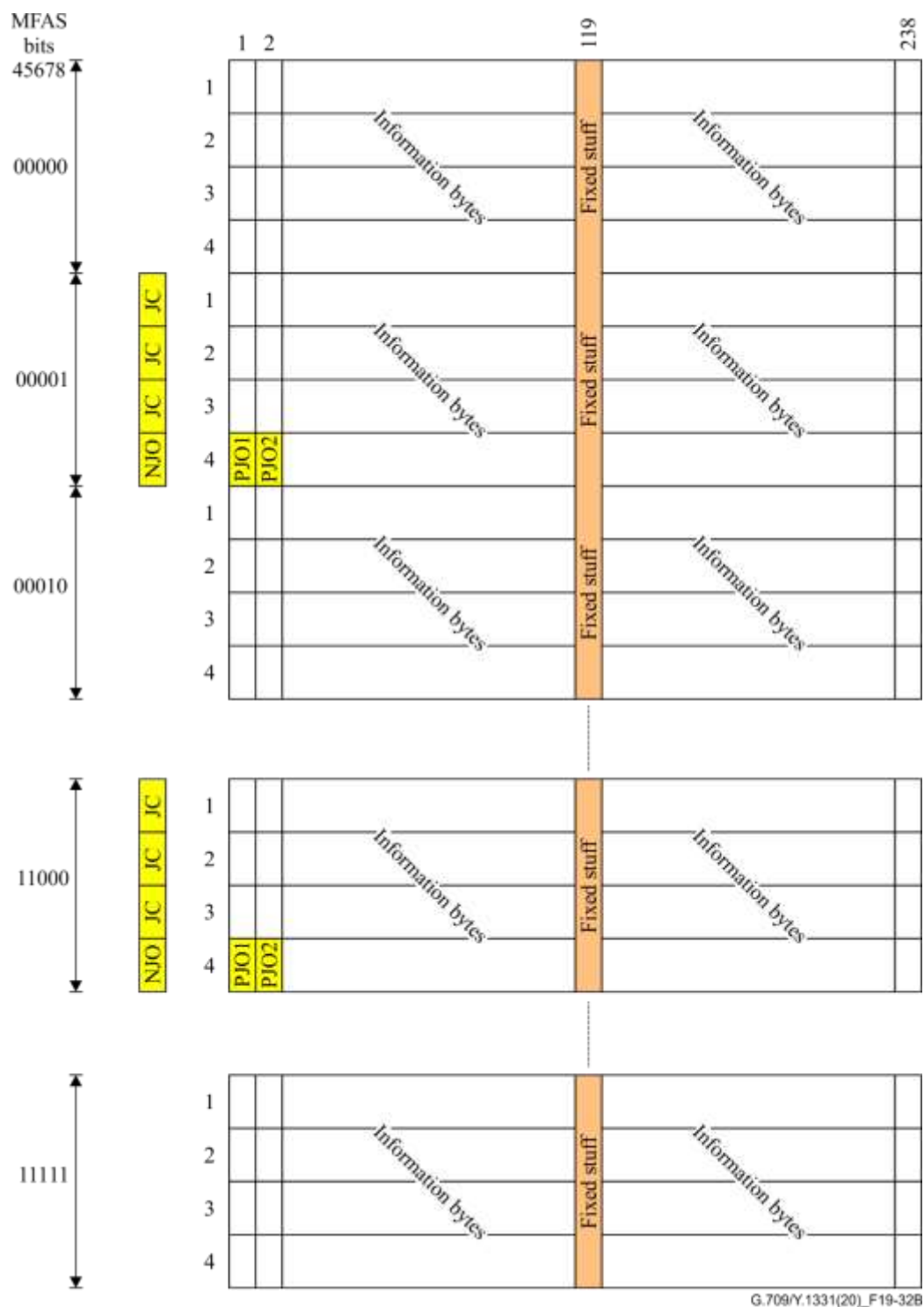


Figure 19-32A – ODTU13 frame format and mapping of ODU1 (mapping in 2.5G TS3)



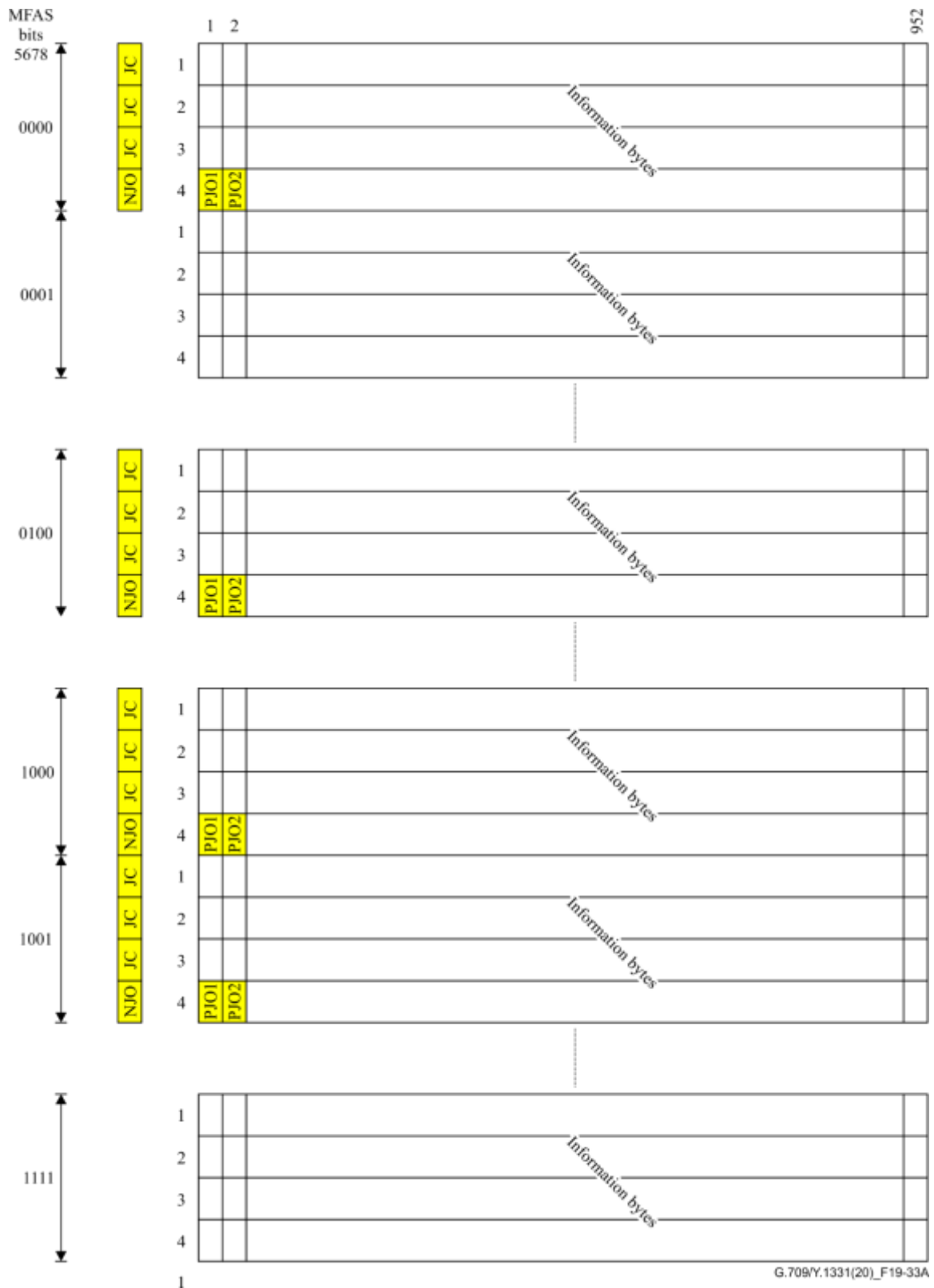
G.709/Y.1331(20)\_F19-32B

**Figure 19-32B – ODTU13 frame format and mapping of ODU1 (mapping in 1.25G TS2 and TS25)**

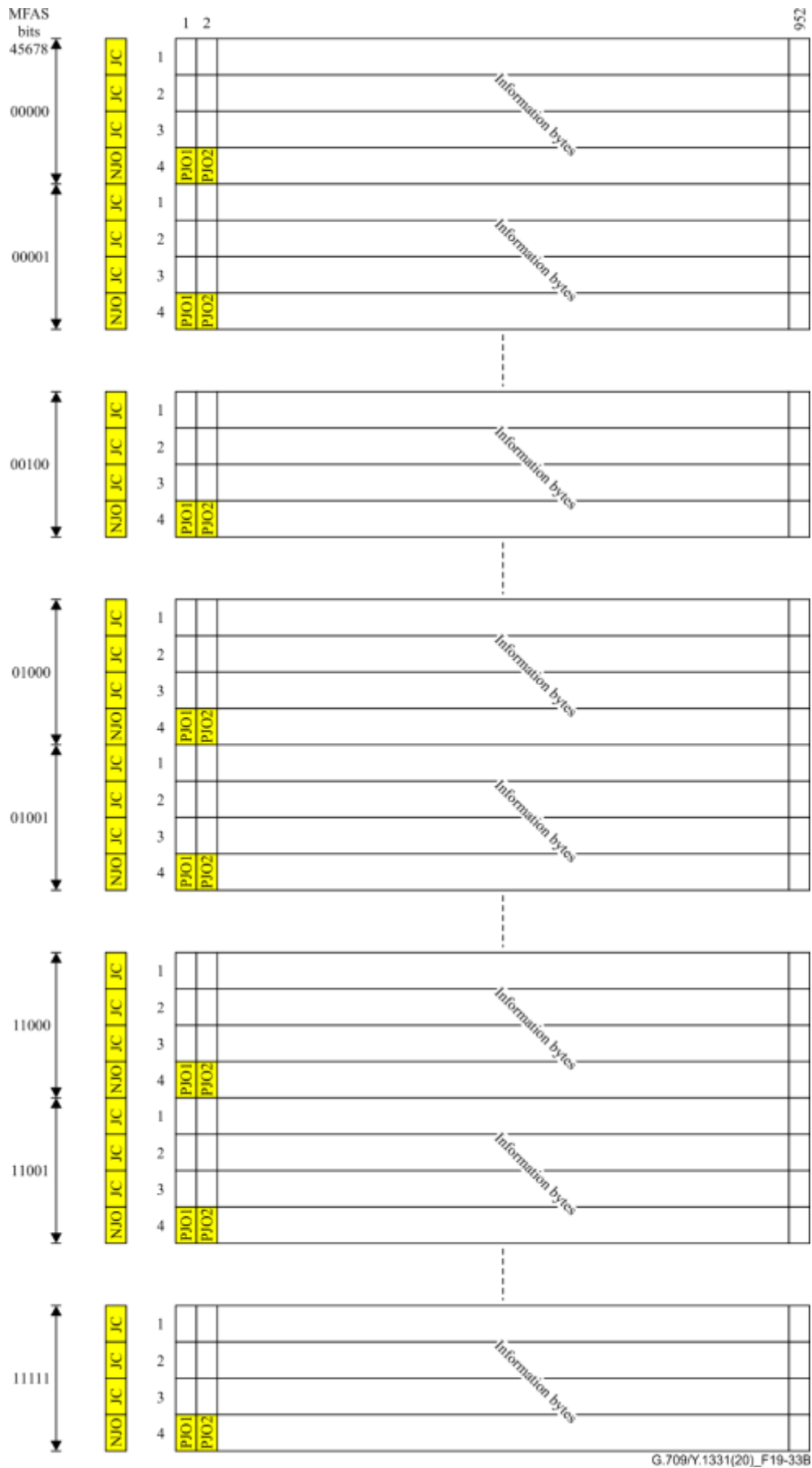
### 19.5.3 Mapping ODU2 into ODTU23

A byte of the ODU2 signal is mapped into an information byte of the ODTU23 (Figure 19-33A). Four times per sixteen OPU3 frames, it is possible to perform either a positive or a negative justification action. The four frames in which justification can be performed are related to the TSOH of the OPU3 2.5G TSs in which the ODTU23 is mapped (Figure 19-2). Figure 19-33A shows the case with mapping in OPU3 2.5G TS1, TS5, TS9 and TS10.

A byte of the ODU2 signal is mapped into an information byte of the ODTU23 (see Figure 19-33B). Eight times per 32 OPU3 frames, it is possible to perform either a positive or a negative justification action. The frames in which justification can be performed are related to the TSOH of the OPU3 1.25G TSs in which the ODTU23 is mapped (Figure 19-2). Figure 19-33B shows the case with mapping in OPU3 1.25G TS 1, 2, 5, 9, 10, 25, 26 and 32.



**Figure 19-33A – ODTU23 frame format and mapping of ODU2 (mapping in 2.5G TS 1,5,9,10)**



G.709/Y.1331(20)\_F19-33B

**Figure 19-33B – ODTU23 frame format and mapping of ODU2  
(mapping in 1.25G TS 1,2,5,9,10,25,26,32)**

### 19.5.4 Mapping ODU0 into ODTU01

A byte of the ODU0 signal is mapped into an information byte of the ODTU01 (see Figure 19-34). Once per 2 OPU1 frames, it is possible to perform either a positive or a negative justification action.

The frame in which justification can be performed is related to the TSOH of the OPU1 TS in which the ODTU01 is mapped (Figure 19-3). Figure 19-34 shows the case with mapping in OPU1 TS1.

NOTE – The PJO2 field will always carry an information byte.

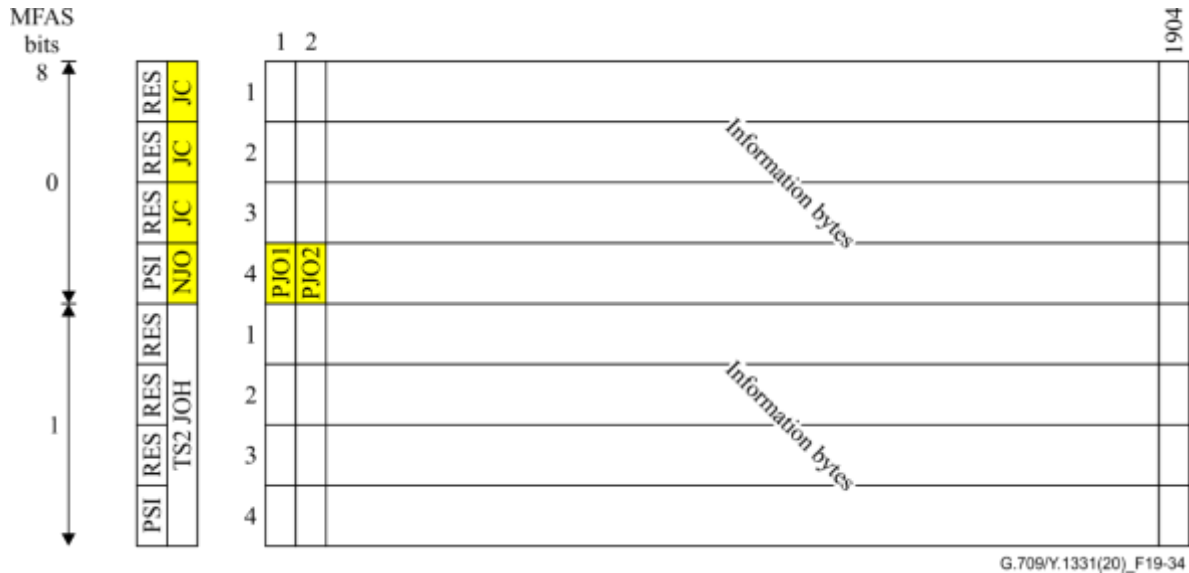


Figure 19-34 – Mapping of ODU0 in OPU1 TS1

### 19.6 Mapping of ODUj into ODTUk.ts

The mapping of ODUj (j = 0, 1, 2, 2e, 3, flex) signals (with up to ±100 ppm bit-rate tolerance) into the ODTUk.ts (k = 2,3,4,25,50; ts = M) signal is performed by means of a generic mapping procedure as specified in Annex D.

The OPUk and therefore the ODTUk.ts (k = 2,3,4,25,50) signals are created from a locally generated clock (within the limits specified in Table 7-3), which is independent of the ODUj client signal.

The ODUj signal is extended with a frame alignment overhead as specified in clauses 15.6.2.1 and 15.6.2.2 and an all-0s pattern in the OTUj overhead field (see Figure 19-30).

The extended ODUj signal is adapted to the locally generated OPUk/ODTUk.ts clock by means of a generic mapping procedure (GMP) as specified in Annex D. The value of n in  $c_n$  and  $C_n(t)$  and  $C_{nD}(t)$  is specified in Annex D. The value of M is the number of tributary slots occupied by the ODUj;  $ODTUk.ts = ODTUk.M$ .

A group of 'M' successive extended ODUj bytes is mapped into a group of 'M' successive ODTUk.M bytes.

The generic mapping process generates for the case of ODUj (j = 0,1,2,2e,3,flex) signals once per ODTUk.M multiframe the  $C_m(t)$  and  $C_{nD}(t)$  information according to Annex D and encodes this information in the ODTUk.ts justification control overhead JC1/JC2/JC3 and JC4/JC5/JC6. The de-mapping process decodes  $C_m(t)$  and  $C_{nD}(t)$  from JC1/JC2/JC3 and JC4/JC5/JC6 and interprets  $C_m(t)$  and  $C_{nD}(t)$  according to Annex D. CRC-8 shall be used to protect against an error in JC1,JC2,JC3 signals. CRC-5 shall be used to protect against an error in JC4,JC5,JC6 signals.

During a signal fail condition of the incoming ODUj signal, this failed incoming signal will contain the ODUj-AIS signal as specified in clause 16.5.1. This ODUj-AIS is then mapped into the ODTUk.M.

For the case where the ODU<sub>j</sub> is received from the output of a fabric (ODU connection function), the incoming signal may contain (in the case of an open matrix connection) the ODU<sub>j</sub>-OCI signal as specified in clause 16.5.2. This ODU<sub>j</sub>-OCI signal is then mapped into the ODTU<sub>k</sub>.M.

NOTE 1 – Not all equipment will have a real connection function (i.e., switch fabric) implemented; instead, the presence/absence of tributary interface port units represents the presence/absence of a matrix connection. If such a unit is intentionally absent (i.e., not installed), the associated ODTU<sub>k</sub>.M signals should carry an ODU<sub>j</sub>-OCI signal. If such a unit is installed but temporarily removed as part of a repair action, the associated ODTU<sub>k</sub>.M signal should carry an ODU<sub>j</sub>-AIS signal.

A group of 'M' successive extended ODU<sub>j</sub> bytes is de-mapped from a group of 'M' successive ODTU<sub>k</sub>.M bytes.

NOTE 2 – For the case where the ODU<sub>j</sub> signal is output as an OTU<sub>j</sub> signal, frame alignment of the extracted extended ODU<sub>j</sub> signal is to be recovered to allow frame synchronous mapping of the ODU<sub>j</sub> into the OTU<sub>j</sub> signal.

During a signal fail condition of the incoming ODU<sub>k</sub>/OPU<sub>k</sub> signal (e.g., in the case of an ODU<sub>k</sub>-AIS, ODU<sub>k</sub>-LCK, ODU<sub>k</sub>-OCI condition) the ODU<sub>j</sub>-AIS pattern as specified in clause 16.5.1 is generated as a replacement signal for the lost ODU<sub>j</sub> signal.

The values of M, m, C<sub>m,min</sub>, C<sub>m,max</sub>, n, C<sub>n,min</sub> and C<sub>n,max</sub> for ODU<sub>j</sub> into ODTU<sub>k</sub>.ts are as follows:

$$M = \text{ceiling} \left( \frac{ODUj\_nom\_bit\_rate \times (1 + ODUj\_bit\_rate\_tolerance + 0.00006)}{(ODTuk.1\_nom\_bit\_rate \times (1 - ODTuk.ts\_bit\_rate\_tolerance))} \right) \text{ for ODU}_j \text{ with } j \neq \text{flex(GFP,n,k')} \quad (19-1a)$$

$$M = \left( \frac{ODUj\_nom\_bit\_rate}{ODUk'.ts} \right) = n \text{ for ODU}_j \text{ with } j = \text{flex(GFP,n,k')} \text{ and } k' \leq k \text{ with } k' \in \{2,3,4\} \quad (19-1b)$$

$$m = 8 \times M \quad (19-2)$$

$$c_{m,nom} = \left( \frac{ODUj\_nom\_bit\_rate \times \text{Number\_of\_GMP\_blocks\_in\_ODTuk.ts}}{ODTuk.1\_nom\_bit\_rate \times M} \right) \quad (19-3)$$

$$c_{m,min} = c_{m,nom} \times \left( \frac{1 - ODUj\_bit\_rate\_tolerance}{1 + ODTuk.1\_bit\_rate\_tolerance} \right) \quad (19-4)$$

$$c_{m,max} = c_{m,nom} \times \left( \frac{1 + ODUj\_bit\_rate\_tolerance}{1 - ODTuk.1\_bit\_rate\_tolerance} \right) \quad (19-5)$$

$$C_{m,min} = \text{floor}(c_{m,min}) \quad (19-6)$$

$$C_{m,max} = \text{ceiling}(c_{m,max}) \quad (19-7)$$

$$n = 8 \quad (19-8)$$

$$c_{n,nom} = \left( \frac{ODUj\_nom\_bit\_rate \times \text{Number\_of\_GMP\_blocks\_in\_ODTuk.ts}}{ODTuk.1\_nom\_bit\_rate} \right) \quad (19-9)$$

$$c_{n,min} = c_{n,nom} \times \left( \frac{1 - ODUj\_bit\_rate\_tolerance}{1 + ODTuk.1\_bit\_rate\_tolerance} \right) \quad (19-10)$$

$$c_{n,max} = c_{n,nom} \times \left( \frac{1 + ODUj\_bit\_rate\_tolerance}{1 - ODTuk.1\_bit\_rate\_tolerance} \right) \quad (19-11)$$

$$C_{n,min} = \text{floor}(c_{n,min}) \quad (19-12)$$

$$C_{n,max} = \text{ceiling}(c_{n,max}) \quad (19-13)$$

$C_{m,min}$ ,  $C_{n,min}$  ( $n=8$ ),  $C_{m,max}$  and  $C_{n,max}$  ( $n=8$ ) values represent the boundaries of ODU $_j$ /ODTU $_k.M$  ppm offset combinations (i.e., min. ODU $_j$ /max. ODTU $_k.M$  and max. ODU $_j$ /min. ODTU $_k.M$ ). In steady state, given instances of ODU $_k$ /ODTU $_k.M$  offset combinations should not result in generated  $C_n$  and  $C_m$  values throughout this range but rather should be within as small a range as possible.

NOTE 3 – Under transient ppm offset conditions (e.g., AIS to normal signal), it is possible that  $C_n$  and  $C_m$  values outside the range  $C_{n,min}$  to  $C_{n,max}$  and  $C_{m,min}$  to  $C_{m,max}$  may be generated and a GMP de-mapper should be tolerant of such occurrences. Refer to Annex D for a general description of the GMP principles.

### 19.6.1 Mapping ODU $_j$ into ODTU2.M

Groups of  $M$  successive bytes of the extended ODU $_j$  ( $j = 0$ , flex) signal are mapped into a group of  $M$  successive bytes of the ODTU2.M payload area under control of the GMP data/stuff control mechanism. Each group of  $M$  bytes in the ODTU2.M payload area may either carry  $M$  ODU bytes, or carry  $M$  stuff bytes. The value of the stuff bytes is set to all-0s.

The groups of  $M$  bytes in the ODTU2.M payload area are numbered from 1 to 15232.

The ODTU2.M payload byte numbering for GMP  $M$ -byte ( $m$ -bit) blocks is illustrated in Figure 19-35. In row 1 of the ODTU2.M multiframe the first  $M$ -bytes will be labelled 1, the next  $M$ -bytes will be labelled 2, etc.

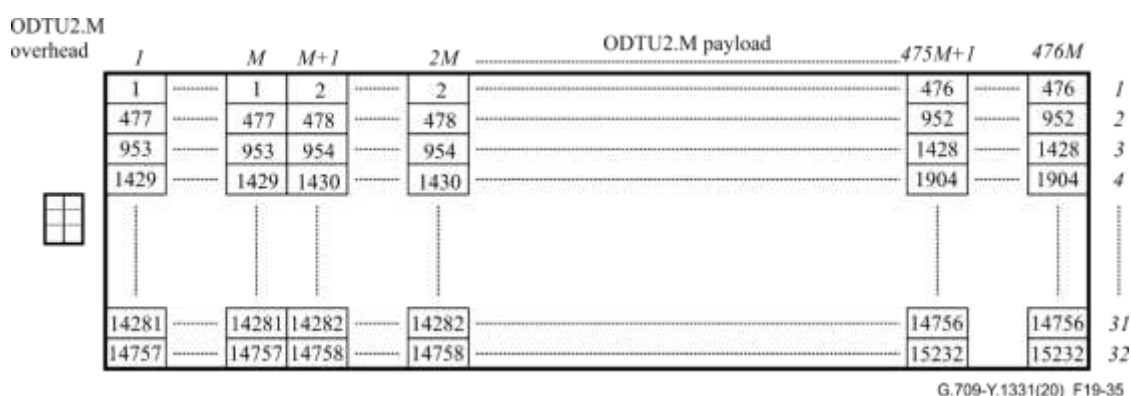


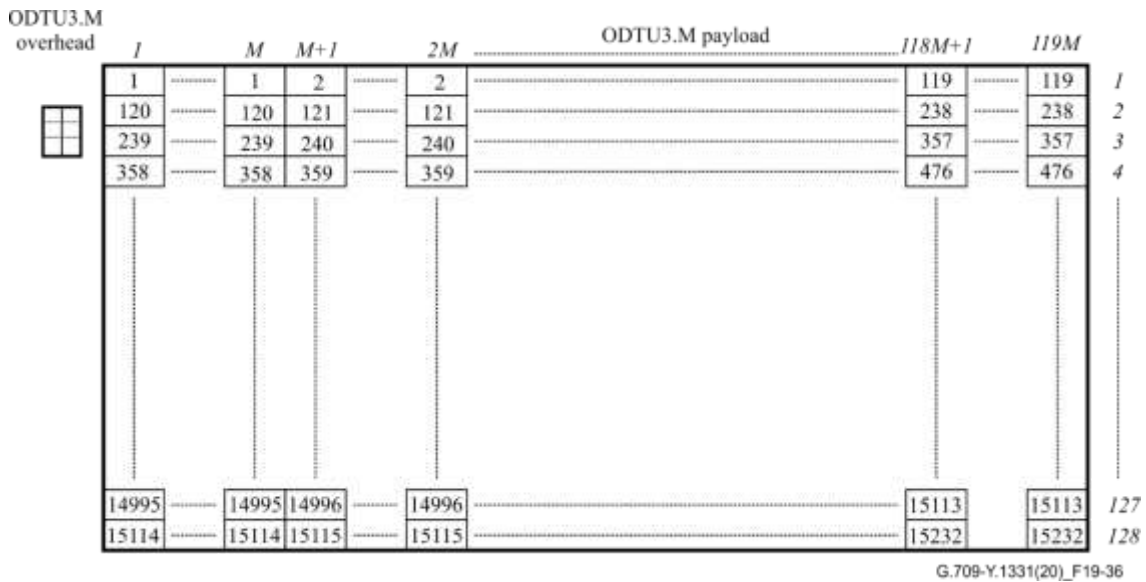
Figure 19-35 – ODTU2.M GMP byte numbering

### 19.6.2 Mapping ODU $_j$ into ODTU3.M

Groups of  $M$  successive bytes of the extended ODU $_j$  ( $j = 0, 2e$ , flex) signal are mapped into a group of  $M$  successive bytes of the ODTU3.M payload area under control of the GMP data/stuff control mechanism. Each group of  $M$  bytes in the ODTU3.M payload area may either carry  $M$  ODU bytes, or carry  $M$  stuff bytes. The value of the stuff bytes is set to all-0s.

The groups of  $M$  bytes in the ODTU3.M payload area are numbered from 1 to 15232.

The ODTU3.M payload byte numbering for GMP  $M$ -byte ( $m$ -bit) blocks is illustrated in Figure 19-36. In row 1 of the ODTU3.M multiframe the first  $M$ -bytes will be labelled 1, the next  $M$ -bytes will be labelled 2, etc.



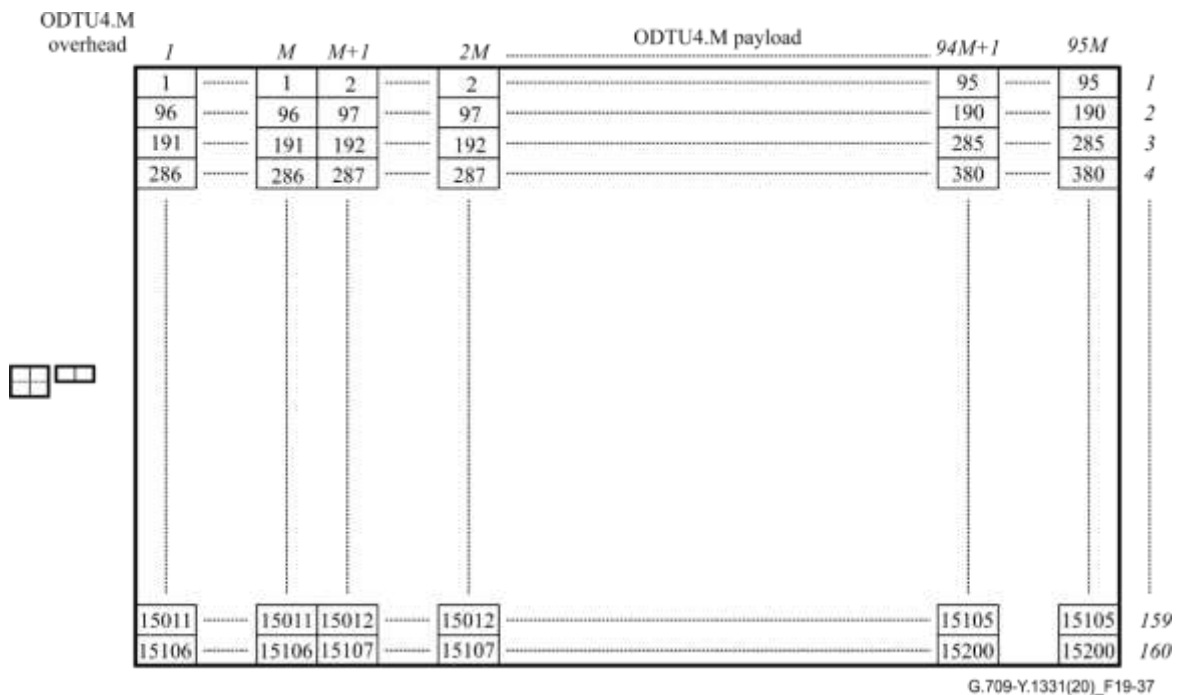
**Figure 19-36 – ODTU3.M GMP byte numbering**

### 19.6.3 Mapping ODU<sub>j</sub> into ODTU4.M

Groups of  $M$  successive bytes of the extended ODU <sub>$j$</sub>  ( $j = 0, 1, 2, 2e, 3, \text{flex}$ ) signal are mapped into a group of  $M$  successive bytes of the ODTU4.M payload area under control of the GMP data/stuff control mechanism. Each group of  $M$  bytes in the ODTU4.M payload area may either carry  $M$  ODU bytes, or carry  $M$  stuff bytes. The value of the stuff bytes is set to all-0s.

The groups of  $M$  bytes in the ODTU4.M payload area are numbered from 1 to 15200.

The ODTU4.M payload byte numbering for GMP  $M$ -byte ( $m$ -bit) blocks is illustrated in Figure 19-37. In row 1 of the ODTU4.M multiframe the first  $M$ -bytes will be labelled 1, the next  $M$ -bytes will be labelled 2, etc.



**Figure 19-37 – ODTU4.M GMP byte numbering**



### 19.6.4 Mapping ODU<sub>j</sub> into ODTU25.M

Groups of M successive bytes of the extended ODU<sub>j</sub> ( $j = 0, 1, 2, 2e, \text{flex}$ ) signal are mapped into a group of M successive bytes of the ODTU25.M payload area under control of the GMP data/stuff control mechanism. Each group of M bytes in the ODTU25.M payload area may either carry M ODU bytes, or carry M stuff bytes. The value of the stuff bytes is set to all-0s.

The groups of M bytes in the ODTU25.M payload area are numbered from 1 to 15232.

The ODTU25.M payload byte numbering for GMP M-byte (m-bit) blocks is illustrated in Figure 19-38. In row 1 of the ODTU25.M multiframe the first M-bytes will be labelled 1, the next M-bytes will be labelled 2, etc.

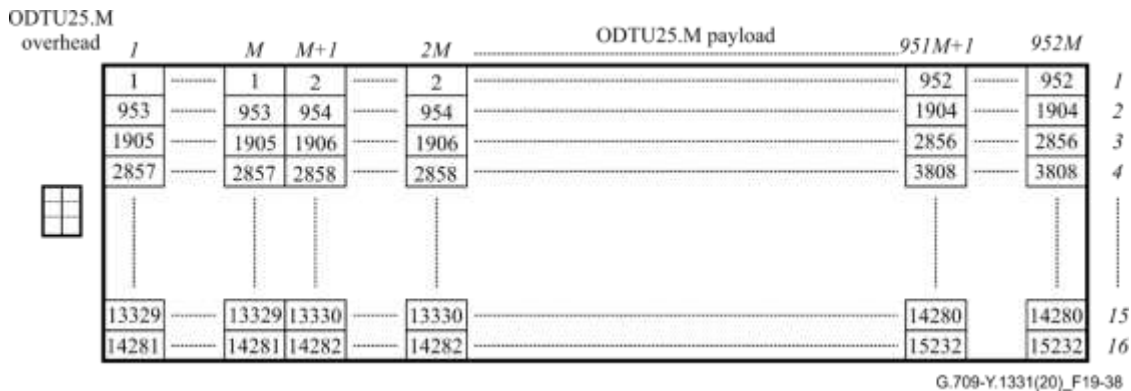


Figure 19-38 – ODTU25.M GMP byte numbering

### 19.6.5 Mapping ODU<sub>j</sub> into ODTU50.M

Groups of M successive bytes of the extended ODU<sub>j</sub> ( $j = 0, 1, 2, 2e, 3, \text{flex}$ ) signal are mapped into a group of M successive bytes of the ODTU50.M payload area under control of the GMP data/stuff control mechanism. Each group of M bytes in the ODTU50.M payload area may either carry M ODU bytes, or carry M stuff bytes. The value of the stuff bytes is set to all-0s.

The groups of M bytes in the ODTU50.M payload area are numbered from 1 to 15232.

The ODTU50.M payload byte numbering for GMP M-byte (m-bit) blocks is illustrated in Figure 19-39. In row 1 of the ODTU50.M multiframe the first M-bytes will be labelled 1, the next M-bytes will be labelled 2, etc.

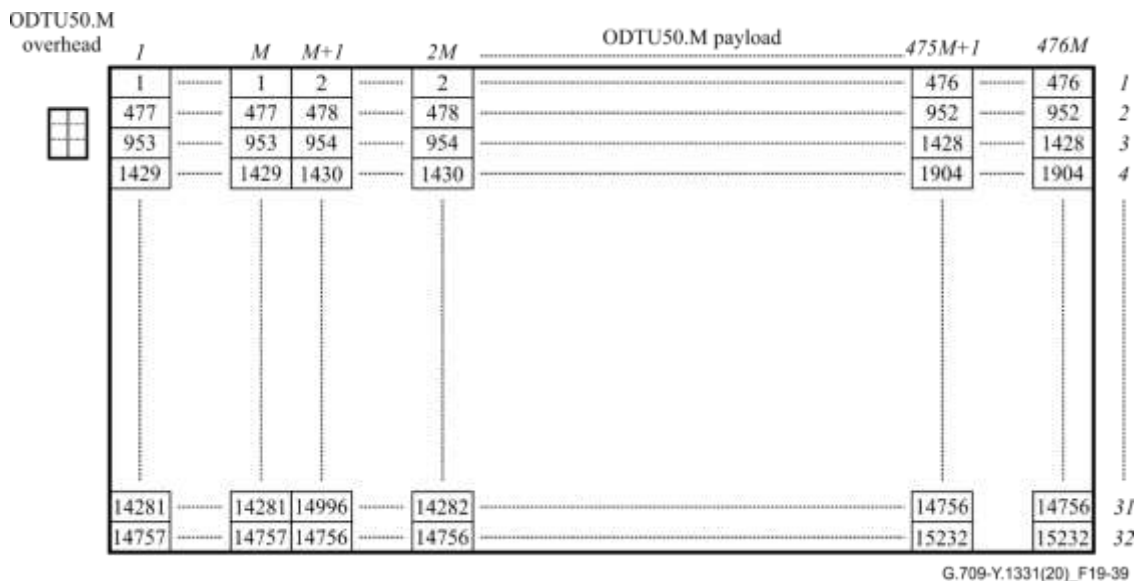


Figure 19-39 – ODTU50.M GMP byte numbering

## 20 Mapping ODUk signals into the ODTUCn signal and the ODTUCn into the OPUCn tributary slots

This clause specifies the multiplexing of:

- ODUk into OPUCn using a client agnostic generic mapping procedure (GMP).

This ODUk into OPUCn multiplexing is performed in two steps:

- 1) asynchronous mapping of ODUk into optical data tributary unit (ODTUCn) using GMP;
- 2) byte-synchronous mapping of ODTUCn into one or more OPUCn tributary slots.

The OPUCn supports up to 10n different ODUk signals.

### 20.1 OPUCn tributary slot definition

The OPUCn consists of n OPUC. Each OPUC is divided into 20 tributary slots (TS) and these tributary slots are 16-byte interleaved within the OPUC payload area. A tributary slot includes a part of the OPUC OH area and a part of the OPUC payload area. The bytes of the ODUk frame are mapped into the ODTUCn payload area and the ODTUCn bytes are mapped into the OPUCn tributary slot or slots. The bytes of the ODTUCn justification overhead are mapped into the OPUCn OH area.

There is *only* one type of tributary slot:

- 1) Tributary slot with a bandwidth of approximately 5 Gbit/s; an OPUCn is divided into 20n tributary slots, numbered 1.1 to n.20.

#### 20.1.1 OPUCn tributary slot allocation

Figures 20-1 and 20-2 present the OPUC 5G tributary slot allocation. An OPUC is divided into 20 5G tributary slots (named TS #A.B where A = 1...n which denotes the number of the OPUC within the OPUCn and B = 1...20 which denotes the number of the TS within the OPUC), which are located in columns 17 to 3824. The OPUC multi-frame may be represented in an 80 row by 3810 column format (Figure 20-1) and in a 8 row by 38100 column format (Figure 20-2).

An OPUC 5G tributary slot occupies 5% of the OPUC payload area. It is a structure with 119 16-byte columns by  $8(20 \times 4/10)$  rows (see Figure 20-2) plus a tributary slot overhead (TSOH). The 20 OPUC 5G TSs are 16-byte interleaved in the OPUC payload area and the 20 OPUC TSOHs are frame interleaved in the OPUC overhead area.

The tributary slot overhead (TSOH) of OPUC tributary slots is located in rows 1 to 3, columns 15 and 16 of the OPUC frame.

The TSOH for a 5G tributary slot is available once every 20 frames. A 20-frame multiframe structure is used for this assignment. This multiframe structure is locked to bits 4, 5, 6, 7 and 8 of the OMFI byte as shown in Table 20-1 and Figure 20-1.

Figure 20-3 presents the 5G tributary slots in the OPUCn for the case of 16-byte interleaving of the OPUC instances. This interleaving presents the tributary slot order within the OPUCn.

OMFI bits	Row	Column	15~16	17~32	33~48	49~320	321~336	337~352	353~368	369~3807	3808~3824
45678	1	TSOH TS #A.1		TSA.1	TSA.2	⋮	TSA.20	TSA.1	TSA.2	⋮	TSA.18
	2			TSA.19	TSA.20	⋮	TSA.18	TSA.19	TSA.20	⋮	TSA.16
	3			TSA.17	TSA.18	⋮	TSA.16	TSA.17	TSA.18		⋮
	4	PSI	OMFI	TSA.15	TSA.16	⋮	TSA.14	TSA.15	TSA.16	⋮	TSA.12
00000	1	TSOH TS #A.2		TSA.13	TSA.14	⋮	TSA.12	TSA.13	TSA.14	⋮	TSA.10
	2			TSA.11	TSA.12	⋮	TSA.10	TSA.11	TSA.12	⋮	TSA.8
	3			TSA.9	TSA.10	⋮	TSA.8	TSA.9	TSA.10		⋮
	4	PSI	OMFI	TSA.7	TSA.8	⋮	TSA.6	TSA.7	TSA.8	⋮	TSA.4
00001	1	TSOH TS #A.3		TSA.5	TSA.6	⋮	TSA.4	TSA.5	TSA.6	⋮	TSA.2
	2			TSA.3	TSA.4	⋮	TSA.2	TSA.3	TSA.4	⋮	TSA.20
	3			TSA.1	TSA.2	⋮	TSA.20	TSA.1	TSA.2		⋮
	4	PSI	OMFI	TSA.19	TSA.20	⋮	TSA.18	TSA.19	TSA.20	⋮	TSA.16
00010	1	TSOH TS #A.20		TSA.9	TSA.10	⋮	TSA.8	TSA.9	TSA.10	⋮	TSA.6
	2			TSA.7	TSA.8	⋮	TSA.6	TSA.7	TSA.8	⋮	TSA.4
	3			TSA.5	TSA.6	⋮	TSA.4	TSA.5	TSA.6		⋮
	4	PSI	OMFI	TSA.3	TSA.4	⋮	TSA.2	TSA.3	TSA.4	⋮	TSA.20
10011	1	TSOH TS #A.20		TSA.9	TSA.10	⋮	TSA.8	TSA.9	TSA.10	⋮	TSA.6
	2			TSA.7	TSA.8	⋮	TSA.6	TSA.7	TSA.8	⋮	TSA.4
	3			TSA.5	TSA.6	⋮	TSA.4	TSA.5	TSA.6		⋮
	4	PSI	OMFI	TSA.3	TSA.4	⋮	TSA.2	TSA.3	TSA.4	⋮	TSA.20

Figure 20-1 – OPUC tributary slot allocation in 80 row x 3810 column format

Multi-frame Row	Column Frame		
		TS OH	TS OH
1	1,2,3(1 <sup>st</sup> 1/2)	#A.16	#A.6
		TS OH	TS OH
2	3(2 <sup>nd</sup> 1/2), 4,5	#A.18	#A.3
		TS OH	TS OH
3	6,7,8(1 <sup>st</sup> 1/2)	#A.16	#A.6
		TS OH	TS OH
4	8(2 <sup>nd</sup> 1/2), 9,10	#A.18	#A.3
		TS OH	TS OH
5	11,12,13(1 <sup>st</sup> 1/2)	#A.16	#A.6
		TS OH	TS OH
6	13(2 <sup>nd</sup> 1/2), 14,15	#A.18	#A.3
		TS OH	TS OH
7	16,17,18(1 <sup>st</sup> 1/2)	#A.16	#A.6
		TS OH	TS OH
8	18(2 <sup>nd</sup> 1/2), 19,20	#A.18	#A.3
		TS OH	TS OH

Figure 20-2 – OPUC tributary slot allocation in 8 row x 38100 column format



**Table 20-1 – OPUCn tributary slot OH allocation**

OMFI bits 4 5 6 7 8	TSOH 5G TS
0 0 0 0 0	A.1
0 0 0 0 1	A.2
0 0 0 1 0	A.3
0 0 0 1 1	A.4
0 0 1 0 0	A.5
0 0 1 0 1	A.6
0 0 1 1 0	A.7
0 0 1 1 1	A.8
0 1 0 0 0	A.9
0 1 0 0 1	A.10
0 1 0 1 0	A.11
0 1 0 1 1	A.12
0 1 1 0 0	A.13
0 1 1 0 1	A.14
0 1 1 1 0	A.15
0 1 1 1 1	A.16
1 0 0 0 0	A.17
1 0 0 0 1	A.18
1 0 0 1 0	A.19
1 0 0 1 1	A.20

## 20.2 ODTUCn definition

The optical data tributary unit  $C_n$  (ODTUC $n$ ) carries a justified ODU $k$  signal. There is one type of ODTUC $n$ :

- ODTUC $n.ts$  ( $ts = 1$  to  $20n$ ) in which a ODU $k$  ( $k = 0,1,2,e,3,4,flex$ ) signal is mapped via the generic mapping procedure (GMP) defined in clause 20.5.

### Optical data tributary unit $C_n.ts$ (ODTUC $n.ts$ )

The optical data tributary unit  $C_n.ts$  (ODTUC $n.ts$ ) is a structure which consists of an ODTUC $n.ts$  payload area and an ODTUC $n.ts$  overhead area (Figure 20-4). The ODTUC $n.ts$  payload area has  $119 \times ts$  ( $ts=1$  to  $20n$ ) 16-byte-columns and 8 rows ( $15232 \times ts$  bytes) and the ODTUC $n.ts$  overhead area has one times 6 bytes. The ODTUC $n.ts$  is carried in "ts" 5G tributary slots of an OPUC $n$ .

The location of the ODTUC $n.ts$  overhead depends on the OPUC $n$  tributary slot used when multiplexing the ODTUC $n.ts$  in the OPUC $n$  (see clause 20.1.1). The single instance of an ODTUC $n.ts$  overhead is located in the OPUC $n$  TSOH of the last OPUC $n$  tributary slot allocated to the ODTUC $n.ts$ .

The ODTUC $n.ts$  overhead carries the GMP justification overhead as specified in clause 20.4.

The ODTUC $n.ts$  overhead carries the GMP justification overhead consisting of 6 bytes of justification control (JC1, JC2, JC3, JC4, JC5, JC6) which carry the GMP  $C_m$  and  $\Sigma C_{8D}$  information.

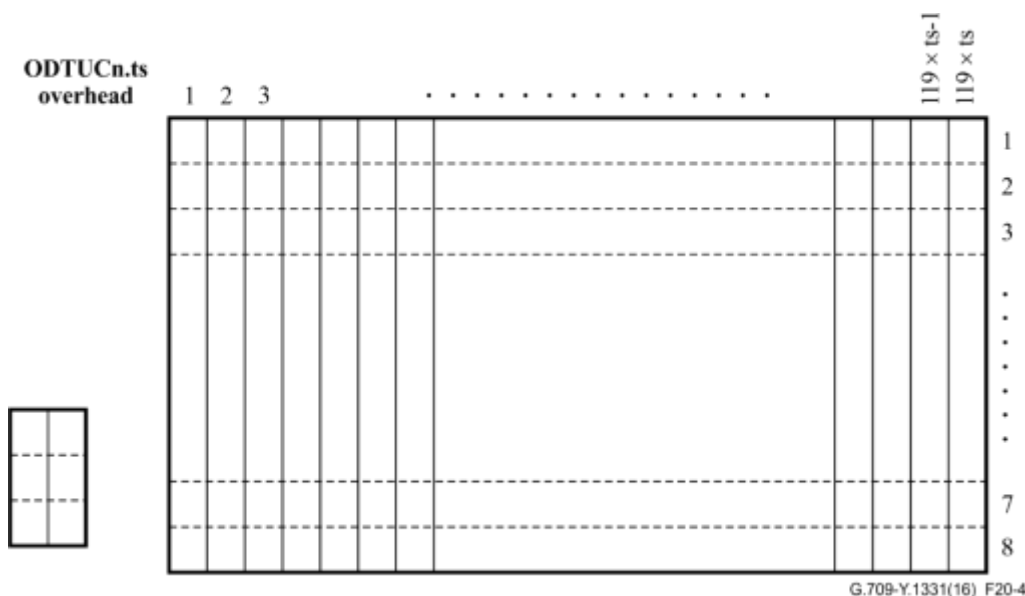


Figure 20-4 – ODTUCn.ts frame formats

### 20.3 Multiplexing ODTUCn signals into the OPUCn

Multiplexing an ODTUCn.ts signal into an OPUCn is realized by mapping the ODTUCn.ts signal into ts (of 20n) arbitrary OPUCn 5G tributary slots: OPUCn TS #A<sub>1</sub>.B<sub>1</sub>, TS #A<sub>2</sub>.B<sub>2</sub>, .. , TS #A<sub>ts</sub>.B<sub>ts</sub> with  $1 \leq n \times (B_1 - 1) + A_1 < n \times (B_2 - 1) + A_2 < \dots < n \times (B_{ts} - 1) + A_{ts} \leq 20n$ .

NOTE 1 – TS #A<sub>1</sub>.B<sub>1</sub>, TS #A<sub>2</sub>.B<sub>2</sub>, ..., TS #A<sub>ts</sub>.B<sub>ts</sub> do not have to be sequential in the OPUCn TS sequence; the TSs can be arbitrarily selected to prevent bandwidth fragmentation.

NOTE 2 – TS order is illustrated in Figure 20-5.

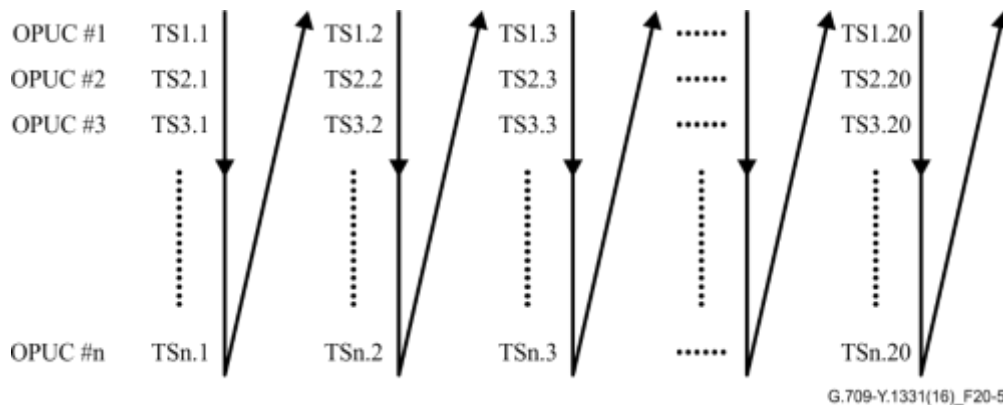


Figure 20-5 – OPUCn TS order

The OPUCn overhead for these multiplexed signals consists of a payload type (PT), the multiplex structure identifier (MSI), the OPUCn multiframe identifier, the OPUCn tributary slot overhead carrying the ODTUCn overhead and depending on the ODTU type one or more bytes reserved for future international standardization.

#### 20.3.1 ODTUCn.ts mapping into ts OPUCn 5G tributary slots

A 16-byte of the ODTUCn.ts payload signal is mapped into a 16-byte of an OPUCn 5G TS #A<sub>i</sub>.B<sub>i</sub> (i = 1,...,ts) payload area, as indicated in Figure 20-6.

A byte of the ODTUCn.ts overhead is mapped into a TSOH byte of TS #A<sub>ts</sub>.B<sub>ts</sub> within columns 15 and 16, rows 1 to 3 of the last OPUCn 5G tributary slot allocated to the ODTUCn.ts.

The remaining OPUC<sub>n</sub> TSOH bytes are reserved for future international standardization.

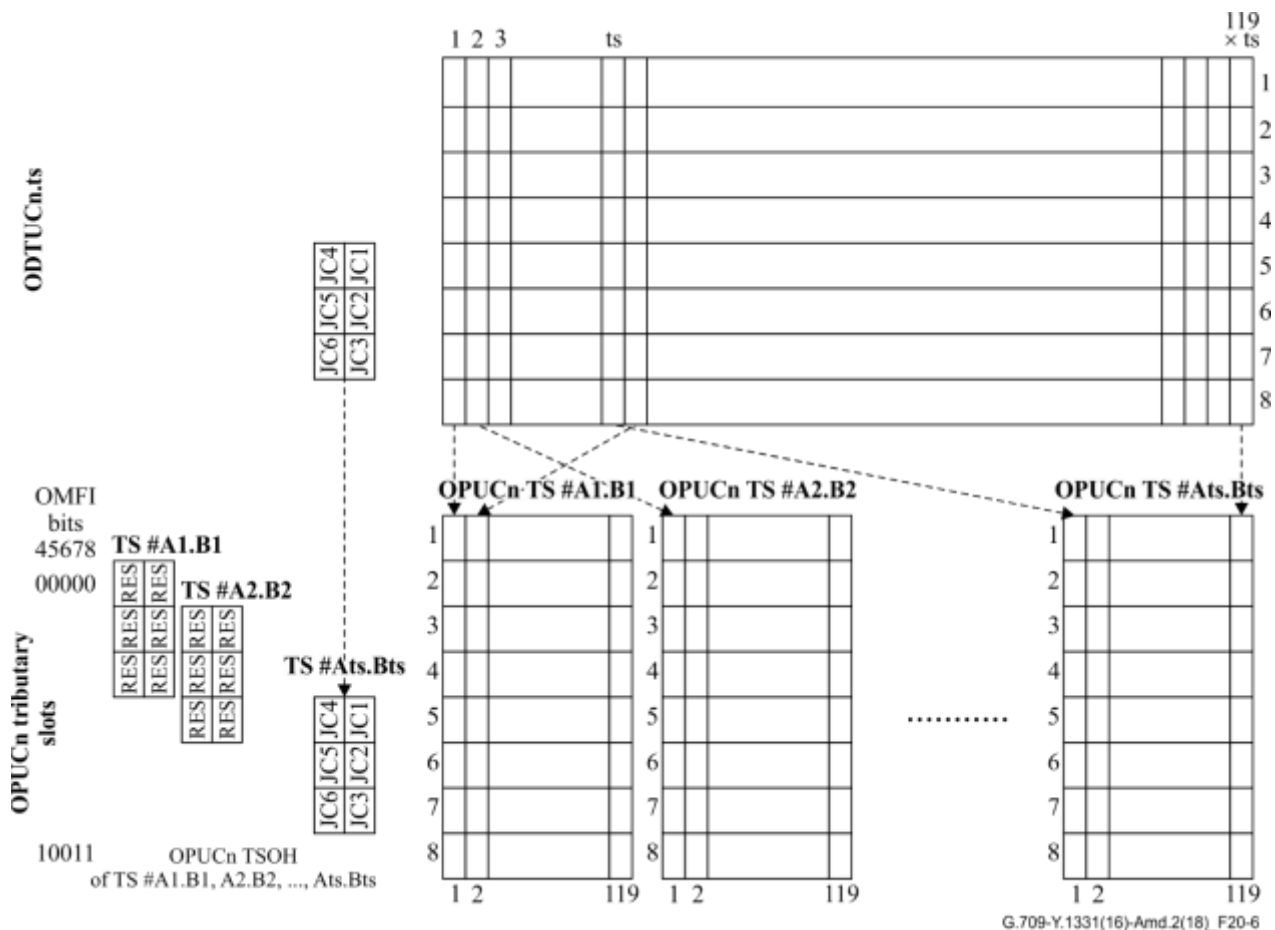


Figure 20-6 – Mapping of ODTUC<sub>n</sub>.ts into 'ts' OPUC<sub>n</sub> 5G tributary slots

#### 20.4 OPUC<sub>n</sub> multiplex overhead and ODTU justification overhead

The OPUC<sub>n</sub> multiplex overhead consists of a multiplex structure identifier (MSI), an OPU multiframe identifier (OMFI), an ODTU overhead and bytes reserved for future international standardization.

The OPUC<sub>n</sub> MSI, OMFI and RES overhead locations are shown in Figure 20-7.

##### ODTUC<sub>n</sub>.ts overhead

The ODTUC<sub>n</sub>.ts overhead carries the GMP justification overhead consisting of 18 bits of justification control (JC1[3-8], JC2[3-8], JC3[3-8]) which carry the 10-bit GMP C<sub>m</sub> information and ODU<sub>k</sub> (k=0,1,2,2e,3,4,flex) specific 30 bits of justification control (JC1[1-2], JC2[1-2], JC3[1-2], JC4, JC5, JC6) which carry the 18-bit GMP ΣC<sub>8D</sub> information.

The JC1, JC2, JC3, JC4, JC5 and JC6 overhead locations are shown in Figure 20-7.



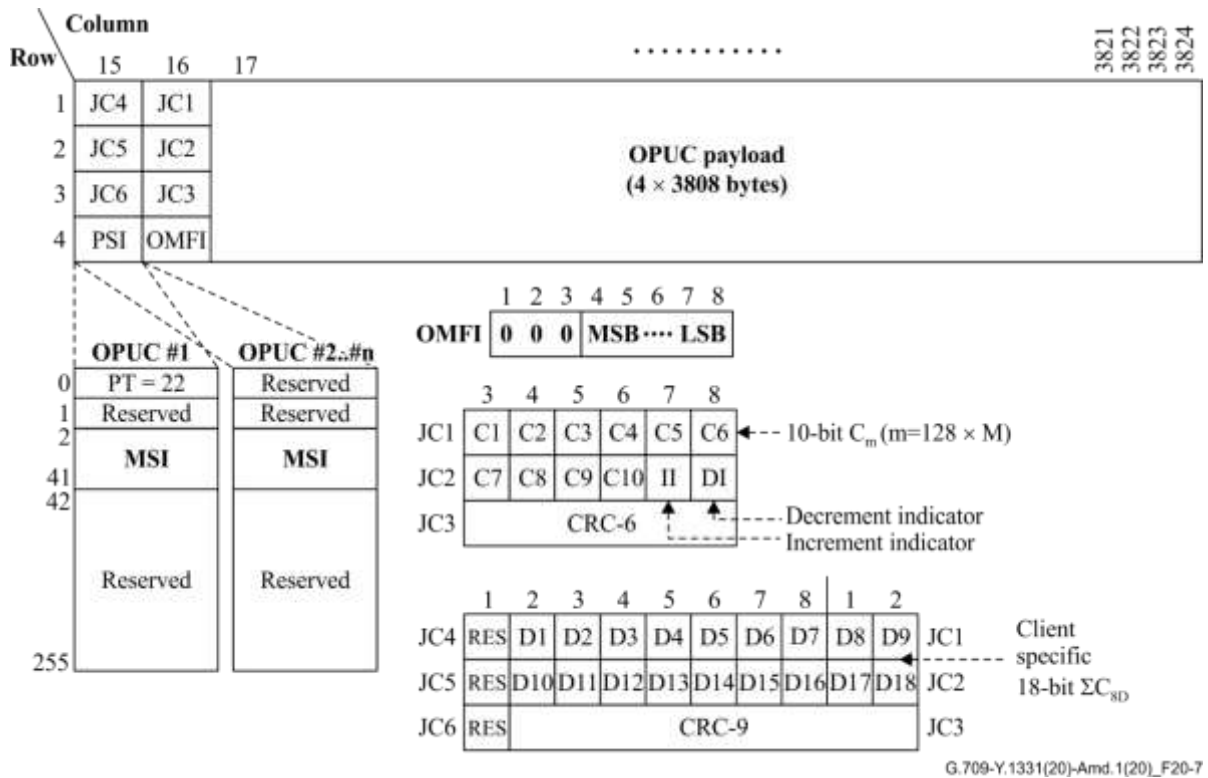


Figure 20-7 – OPUC<sub>n</sub> multiplex overhead (payload type = 22)

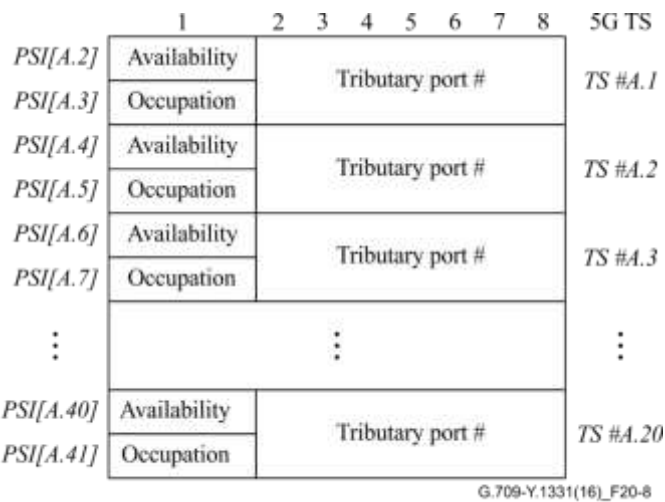
#### 20.4.1 OPUC<sub>n</sub> multiplex structure identifier (MSI)

The OPUC<sub>n</sub> multiplex structure identifier (MSI) overhead, which encodes the ODU multiplex structure in the OPU, is located in the mapping specific area of the PSI signal (refer to Figure 20-7 for the MSI location in OPUC<sub>n</sub> with PT=22). The MSI has a fixed length of 40n bytes and indicates the ODTU content of each tributary slot (TS) of an OPUC<sub>n</sub>. Two bytes are used for each TS.

##### 20.4.1.1 OPUC<sub>n</sub> multiplex structure identifier (MSI) – Payload type 22

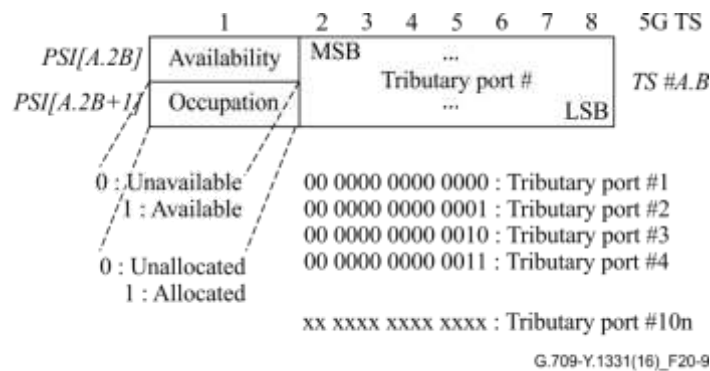
For the 20n OPUC<sub>n</sub> 5G tributary slots n times 40 bytes of the PSI are used (named PSI[x.y] where x = 1...n and y = 2...41, that is PSI[1.2], PSI[1.3],...PSI[1.41], PSI[2.2], PSI[2.3],..., PSI[2.41], PSI[3.2],...,PSI[n-1.41], PSI[n.2]..., PSI[n.41]) as MSI bytes as shown in Figure 20-7. The MSI indicates the ODTU content of each tributary slot of an OPU. Two bytes are used for each tributary slot as illustrated in Figure 20-8 and the encoding of the fields of each MSI instance is illustrated in Figure 20-9.

- The TS availability bit 1 indicates if the tributary slot is available or unavailable.
- The TS occupation bit 9 indicates if the tributary slot is allocated or unallocated.
- The tributary port # in bits 2 to 8 and 10 to 16 indicates the port number of the ODTUC<sub>n</sub>.ts that is being transported in this TS; a flexible assignment of tributary port to tributary slots is possible. ODTUC<sub>n</sub>.ts tributary ports are numbered 1 to 10n. The value is set to all-0s when the occupation bit has the value 0 (tributary slot is unallocated).



NOTE –  $A = 1 \dots n$

**Figure 20-8 – OPUCn 5G TS MSI coding – Payload type 22**



NOTE –  $A = 1 \dots n, B = 1 \dots 20$

**Figure 20-9 – OPUCn MSI coding – Payload type 22**

### 20.4.2 OPUCn payload structure identifier reserved overhead (RES)

216×n-1 (OPUCn) bytes are reserved in the OPUCn PSI for future international standardization. These bytes are located in PSI[x.1] and PSI[x.42] to PSI[x.255] of the OPUCn overhead where  $x = 1 \dots n$  and PSI[x.0],  $x=2$  to  $n$ . These bytes are set to all-0s.

### 20.4.3 OPUCn multiplex justification overhead (JOH)

The generic mapping procedure (GMP) is used for the mapping of an ODU<sub>k</sub> into ODTUC<sub>n.ts</sub>. GMP uses ODU<sub>k</sub> and OPUC<sub>n</sub> independent stuff and justification opportunity definitions (ODTUC<sub>n.ts</sub>). Stuff locations within an ODTUC<sub>n.ts</sub> are determined by means of a formula which is specified in clause 20.4.3.1.

#### 20.4.3.1 Generic mapping procedure (GMP)

The justification overhead (JOH) for the generic mapping procedure consists of two groups of three bytes of justification control; JC1, JC2, JC3 and JC4, JC5, JC6. Refer to Figure 20-7.

The bits 3 to 8 of the JC1, JC2 and JC3 bytes consist of a 10-bit C<sub>m</sub> field (bits C1, C2, ..., C10), a 1-bit increment indicator (II) field, a 1-bit decrement indicator (DI) field and a 6-bit CRC-6 field which contains an error check code over the JC1, JC2 and JC3 bits 3 to 8 fields.

The bits 1 and 2 of the JC1, JC2, JC3 bytes and bits 2 to 8 of the JC4, JC5 and JC6 bytes consist of a 18-bit ΣC<sub>nD</sub> field (bits D1, D2, ..., D18), a 9-bit CRC-9 field which contains an error check code over

bits 2 to 8 in the JC4, JC5 and JC6 fields plus bits 1 and 2 in the JC1, JC2 and JC3 fields and three reserved bits.

The value of 'm' in  $C_m$  is  $128 \times 'ts'$  (number of tributary slots occupied by the ODTUCn.ts).

The value of 'n' represents the timing granularity of the GMP  $C_n$  parameter, which is also present in  $\Sigma C_{nD}$ . The value of n is 8.

The value of  $C_m$  controls the distribution of groups of '16ts' ODUk data bytes into groups of '16ts' ODTUCn.ts payload bytes. Refer to clause 20.5 and Annex D for further specification of this process.

The value of  $\Sigma C_{nD}$  provides additional 'n'-bit timing information, which is necessary to control the jitter and wander performance experienced by the ODUk signal.

The value of  $C_n$  (i.e., number of client n-bit data entities per OPUCn multiframe) is computed as follows:  $C_n(t) = m \times C_m(t) + (\Sigma C_{nD}(t) - \Sigma C_{nD}(t-1))$ . Note that the value  $C_{nD}$  is effectively an indication of the amount of data in the mapper's virtual queue that it could not send during that multiframe due to it being less than a 16M-byte word. For the case where the value of  $\Sigma C_{nD}$  in a multiframe 't' is corrupted, it is possible to recover from such error in the next multiframe 't+1'.

#### 20.4.4 OPUCn multiframe identifier overhead (OMFI)

An OPUCn multiframe identifier (OMFI) byte is defined in row 4, column 16 of the OPUC #1 to #n overhead (Figure 20-10). The value of bits 4 to 8 of the OMFI byte will be incremented each OPUCn frame to provide a 20 frame multiframe for the multiplexing of ODUk signals into the OPUCn.

NOTE 1 – It is an option to align the OMFI = 0 position with MFAS = 0 position every 1280 (the least common multiple of 20 and 256) frame periods.

NOTE 2 – OMFI must be copied in all n OPUC instances at the source, and only 1 need to be processed at the sink.

OMFI OH byte							
1	2	3	4	5	6	7	8
Fixed to 0	Fixed to 0	Fixed to 0	0	0	0	0	0
			0	0	0	0	1
			0	0	0	1	0
			0	0	0	1	1
			0	0	1	0	0
			0	0	1	0	1
			0	0	1	1	0
			0	0	1	1	1
			0	1	0	0	0
			0	1	0	0	1
			0	1	0	1	0
			0	1	0	1	1
			0	1	1	0	0
			0	1	1	0	1
			0	1	1	1	0
			0	1	1	1	1
			1	0	0	0	0
			1	0	0	0	1
			1	0	0	1	0
			1	0	0	1	1
			0	0	0	0	0
			0	0	0	0	1

G.709-Y.1331(20)\_F20-10

Figure 20-10 – OPUCn multiframe identifier (OMFI) overhead

## 20.5 Mapping ODUk into ODTUCn.ts

The mapping of ODU $k$  ( $k = 0, 1, 2, 2e, 3, 4, \text{flex}$ ) signals (with up to  $\pm 100$  ppm bit-rate tolerance) into the ODTUC $n.ts$  ( $ts = M$ ) signal is performed by means of a generic mapping procedure as specified in Annex D.

The OPU $Cn$  and therefore the ODTUC $n.ts$  signals are created from a locally generated clock (within the limits specified in Table 7-3), which is independent of the ODU $k$  signal.

The ODU $k$  signal is extended with a frame alignment overhead as specified in clauses 15.6.2.1 and 15.6.2.2 and an all-0s pattern in the OTU $k$  overhead field (see Figure 19-30, read "j" by "k").

The extended ODU $k$  signal is adapted to the locally generated OPU $Cn$ /ODTUC $n.ts$  clock by means of a generic mapping procedure (GMP) as specified in Annex D. The value of  $n$  in  $c_n$  and  $C_n(t)$  and  $C_{nD}(t)$  is specified in Annex D. The value of  $M$  is the number of tributary slots occupied by the ODU $k$ ; ODTUC $n.ts = ODTUCn.M$ .

A group of  $M$  successive extended ODU $k$  16-byte (128-bit) words is mapped into a group of  $M$  successive ODTUC $n.M$  16-byte (128-bit) words.

NOTE 1 – The 16-byte word alignment of the extended ODU $k$  is preserved through the mapping procedure; e.g., the position of the first 16 OH bytes of the ODU $k$  is always located after an integer number of 16-byte words from the start of the ODTUC $n.M$  structure.

The generic mapping process generates for the case of ODU $k$  signals once per ODTUC $n.M$  multiframe the  $C_m(t)$  and  $C_{nD}(t)$  information according to Annex D and encodes this information in the ODTUC $n.ts$  justification control overhead JC1/JC2/JC3 and JC4/JC5/JC6. The de-mapping process decodes  $C_m(t)$  and  $C_{nD}(t)$  from JC1/JC2/JC3 and JC4/JC5/JC6 and interprets  $C_m(t)$  and  $C_{nD}(t)$  according to Annex D. CRC-6 shall be used to protect against an error in bits 3 to 8 of the JC1, JC2, JC3 signals. CRC-9 shall be used to protect against an error in bits 1 and 2 of JC1, JC2, JC3 and bits 2 to 8 of JC4, JC5, JC6 signals.

During a signal fail condition of the incoming ODU $k$  signal, this failed incoming signal will contain the ODU $k$ -AIS signal as specified in clause 16.5.1. This ODU $k$ -AIS is then mapped into the ODTUC $n.M$ .

For the case where the ODU $k$  is received from the output of a fabric (ODU connection function), the incoming signal may contain (in the case of an open matrix connection) the ODU $k$ -OCI signal as specified in clause 16.5.2. This ODU $k$ -OCI signal is then mapped into the ODTUC $n.M$ .

NOTE 2 – Not all equipment will have a real connection function (i.e., switch fabric) implemented; instead, the presence/absence of tributary interface port units represents the presence/absence of a matrix connection. If such a unit is intentionally absent (i.e., not installed), the associated ODTUC $n.M$  signals should carry an ODU $k$ -OCI signal. If such a unit is installed but temporarily removed as part of a repair action, the associated ODTUC $n.M$  signal should carry an ODU $k$ -AIS signal.

A group of  $M$  successive extended ODU $k$  16-byte words is de-mapped from a group of  $M$  successive ODTUC $n.M$  16-byte blocks.

NOTE 3 – For the case where the ODU $k$  signal is output as an OTU $k$  signal, frame alignment of the extracted extended ODU $k$  signal is to be recovered to allow frame synchronous mapping of the ODU $k$  into the OTU $k$  signal.

During a signal fail condition of the incoming ODU $Cn$ /OPU $Cn$  signal (e.g., in the case of an ODU $Cn$ -AIS condition) the ODU $k$ -AIS pattern as specified in clause 16.5.1 is generated as a replacement signal for the lost ODU $k$  signal.

The values of  $M$ ,  $m$ ,  $C_{m,\min}$ ,  $C_{m,\max}$ ,  $n$ ,  $C_{n,\min}$  and  $C_{n,\max}$  for ODU $k$  into ODTUC $n.ts$  are as follows:

$$M = \text{ceiling} \left( \frac{\text{ODUk\_nom\_bit\_rate} \times (1 + \text{ODUk\_bit\_rate\_tolerance} + 0.00006)}{(\text{ODTUCn.1\_nom\_bit\_rate} \times (1 - \text{ODTUCn.ts\_bit\_rate\_tolerance}))} \right) \text{ for ODUk with } k \neq \text{flex(GFP,n,k')} \quad (20-1a)$$

$$M = \text{ceiling} \left( \frac{\text{ODUk}_{nom\_bit\_rate}}{\text{ODUk}'_{ts} \times 4} \right) = \text{ceiling} \left( \frac{n}{4} \right) \text{ for ODUk with } k = \text{flex}(\text{GFP}, n, k') \text{ and } k' \in \{2, 3, 4\} \quad (20-1b)$$

$$m = 128 \times M \quad (20-2)$$

$$c_{m,nom} = \left( \frac{\text{ODUk}_{nom\_bit\_rate} \times \text{Number\_of\_GMP\_blocks\_in\_ODTUCnts}}{\text{ODTUCn.1}_{nom\_bit\_rate} \times M} \right) \quad (20-3)$$

$$c_{m,min} = c_{m,nom} \times \left( \frac{1 - \text{ODUk}_{bit\_rate\_tolerance}}{1 + \text{ODTUCn.1}_{bit\_rate\_tolerance}} \right) \quad (20-4)$$

$$c_{m,max} = c_{m,nom} \times \left( \frac{1 + \text{ODUk}_{bit\_rate\_tolerance}}{1 - \text{ODTUCn.1}_{bit\_rate\_tolerance}} \right) \quad (20-5)$$

$$C_{m,min} = \text{floor}(c_{m,min}) \quad (20-6)$$

$$C_{m,max} = \text{ceiling}(c_{m,max}) \quad (20-7)$$

$$n = 8 \quad (20-8)$$

$$c_{n,nom} = \left( \frac{\text{ODUk}_{nom\_bit\_rate} \times \text{Number\_of\_GMP\_blocks\_in\_ODTUCnts} \times 16}{\text{ODTUCn.1}_{nom\_bit\_rate}} \right) \quad (20-9)$$

$$c_{n,min} = c_{n,nom} \times \left( \frac{1 - \text{ODUk}_{bit\_rate\_tolerance}}{1 + \text{ODTUCn.1}_{bit\_rate\_tolerance}} \right) \quad (20-10)$$

$$c_{n,max} = c_{n,nom} \times \left( \frac{1 + \text{ODUk}_{bit\_rate\_tolerance}}{1 - \text{ODTUCn.1}_{bit\_rate\_tolerance}} \right) \quad (20-11)$$

$$C_{n,min} = \text{floor}(c_{n,min}) \quad (20-12)$$

$$C_{n,max} = \text{ceiling}(c_{n,max}) \quad (20-13)$$

$C_{m,min}$ ,  $C_{n,min}$  ( $n=8$ ),  $C_{m,max}$  and  $C_{n,max}$  ( $n=8$ ) values represent the boundaries of ODUk/ODTUCn.M ppm offset combinations (i.e., min. ODUk/max. ODTUCn.M and max. ODUk/min. ODTUCn.M). In steady state, given instances of ODUk/ODTUCn.M offset combinations should not result in generated  $C_n$  and  $C_m$  values throughout this range but rather should be within as small a range as possible.

NOTE 4 – Under transient ppm offset conditions (e.g., AIS to normal signal), it is possible that  $C_n$  and  $C_m$  values outside the range  $C_{n,min}$  to  $C_{n,max}$  and  $C_{m,min}$  to  $C_{m,max}$  may be generated and a GMP de-mapper should be tolerant of such occurrences. Refer to Annex D for a general description of the GMP principles.

### 20.5.1 Mapping ODUk into ODTUCn.M

Groups of  $M$  successive 16-byte words of the extended ODUk ( $k = 0, 1, 2, 2e, 3, 4, \text{flex}$ ) signal are mapped into a group of  $M$  successive 16-byte blocks of the ODTUCn.M payload area under control of the GMP data/stuff control mechanism. Each group of  $M$  16-byte blocks in the ODTUCn.M payload area may either carry  $M$  ODUk 16-byte words, or carry  $M$  stuff 16-byte words. The value of the stuff bytes is set to all-0s.

The groups of  $M$  16-byte blocks in the ODTUCn.M payload area are numbered from 1 to 952.

The ODTUCn.M payload 16-byte numbering for GMP  $M$  16-byte ( $m$ -bit) blocks is illustrated in Figure 20-11. In row 1 of the ODTUCn.M multiframe the first  $M$  16-byte blocks will be labeled 1, the next  $M$  16-byte blocks will be labeled 2, etc.

		<i>I</i>	<i>M</i>	<i>M+1</i>	<i>2M</i>	.....	<i>118*M+1</i>	<i>119*M</i>						
<table border="1"> <tr><td>JC4</td><td>JC1</td></tr> <tr><td>JC5</td><td>JC2</td></tr> <tr><td>JC6</td><td>JC3</td></tr> </table>	JC4	JC1	JC5	JC2	JC6	JC3	1	1	2	2	.....	119	119	<i>I</i>
	JC4	JC1												
	JC5	JC2												
	JC6	JC3												
	120	120	121	121	.....	238	238	2						
	239	239	240	240	.....	357	357	3						
	358	358	359	359	.....	476	476	4						
	477	477	478	478	.....	595	595	5						
596	596	597	597	.....	714	714	6							
715	715	716	716	.....	833	833	7							
834	834	835	835	.....	952	952	8							

G.709-Y.1331(16)-Amd.1\_F20-11

Figure 20-11 – ODTUC $n.M$  GMP 16-byte block numbering

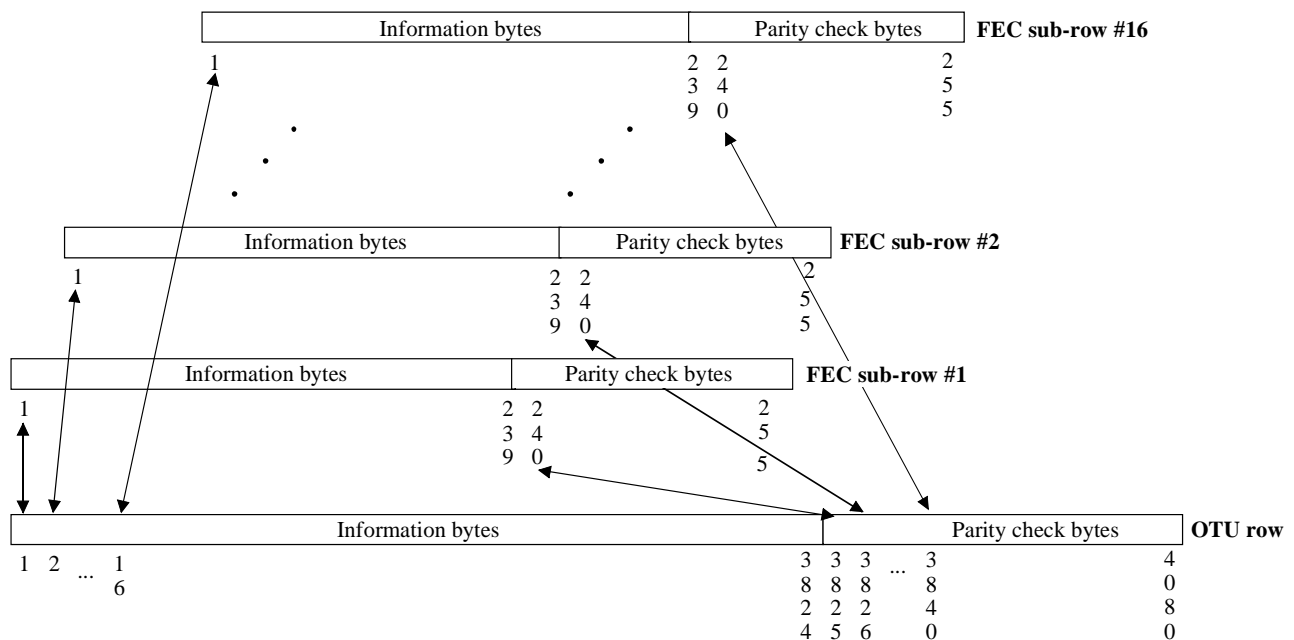
## Annex A

### Forward error correction using 16-byte interleaved RS(255,239) codecs

(This annex forms an integral part of this Recommendation.)

The forward error correction for the OTU-k uses 16-byte interleaved codecs using a Reed-Solomon RS(255,239) code. The RS(255,239) code is a non-binary code (the FEC algorithm operates on byte symbols) and belongs to the family of systematic linear cyclic block codes.

For FEC processing, an OTU row is separated into 16 sub-rows using byte-interleaving as shown in Figure A.1. Each FEC encoder/decoder processes one of these sub-rows. The FEC parity check bytes are calculated over the information bytes 1 to 239 of each sub-row and transmitted in bytes 240 to 255 of the same sub-row.



G.709/Y.1331\_FA.1

**Figure A.1 – FEC sub-rows**

The bytes in an OTU row belonging to FEC sub-row X are defined by:  $X + 16 \times (i - 1)$  (for  $i = 1 \dots 255$ ).

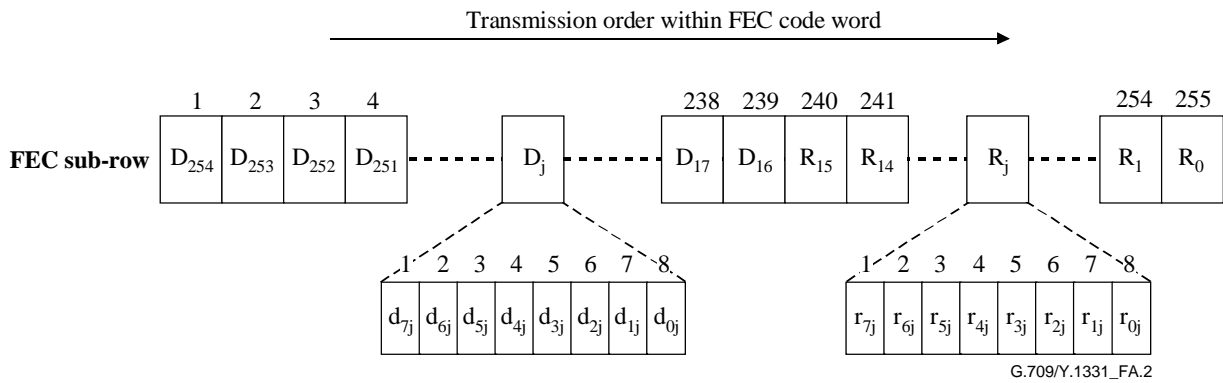
The generator polynomial of the code is given by:

$$G(z) = \prod_{i=0}^{15} (z - \alpha^i)$$

where  $\alpha$  is a root of the binary primitive polynomial  $x^8 + x^4 + x^3 + x^2 + 1$ .

The FEC code word (see Figure A.2) consists of information bytes and parity bytes (FEC redundancy) and is represented by the polynomial:

$$C(z) = I(z) + R(z)$$



**Figure A.2 – FEC code word**

Information bytes are represented by:

$$I(z) = D_{254} \cdot z^{254} + D_{253} \cdot z^{253} + \dots + D_{16} \cdot z^{16}$$

Where  $D_j$  ( $j = 16$  to  $254$ ) is the information byte represented by an element out of GF(256) and:

$$D_j = d_{7j} \cdot \alpha^7 + d_{6j} \cdot \alpha^6 + \dots + d_{1j} \cdot \alpha^1 + d_{0j}$$

Bit  $d_{7j}$  is the MSB and  $d_{0j}$  the LSB of the information byte.

$D_{254}$  corresponds to byte 1 in the FEC sub-row and  $D_{16}$  to byte 239.

Parity bytes are represented by:

$$R(z) = R_{15} \cdot z^{15} + R_{14} \cdot z^{14} + \dots + R_1 \cdot z^1 + R_0$$

Where  $R_j$  ( $j = 0$  to  $15$ ) is the parity byte represented by an element out of GF(256) and:

$$R_j = r_{7j} \cdot \alpha^7 + r_{6j} \cdot \alpha^6 + \dots + r_{1j} \cdot \alpha^1 + r_{0j}$$

Bit  $r_{7j}$  is the MSB and  $r_{0j}$  the LSB of the parity byte.

$R_{15}$  corresponds to the byte 240 in the FEC sub-row and  $R_0$  to byte 255.

$R(z)$  is calculated by:

$$R(z) = I(z) \bmod G(z)$$

where "mod" is the modulo calculation over the code generator polynomial  $G(z)$  with elements out of the GF(256). Each element in GF(256) is defined by the binary primitive polynomial

$$x^8 + x^4 + x^3 + x^2 + 1.$$

The Hamming distance of the RS(255,239) code is  $d_{\min} = 17$ . The code can correct up to 8 symbol errors in the FEC code word when it is used for error correction. The FEC can detect up to 16 symbol errors in the FEC code word when it is used for error detection capability only.



## Annex B

### Adapting 64B/66B encoded clients via transcoding into 513B code blocks

(This annex forms an integral part of this Recommendation.)

Clients using 64B/66B coding can be adapted in a codeword and timing transparent mapping via transcoding into 513B code blocks to reduce the bit rate that is required to transport the signal. The resulting 513B blocks can be mapped in one of several ways depending on the requirements of the client and the available bandwidth of the container into which the client is mapped. This mapping can be applied to serial or parallel client interfaces.

#### B.1 Transmission order

The order of transmission of information in all the diagrams in this annex is first from left to right and then from top to bottom.

#### B.2 Client frame recovery

For 40GBASE-R and 100GBASE-R clients, framing recovery consists of the recovering 64B/66B block lock per the state diagram in Figure 82-10 of [IEEE 802.3]. For other 64B/66B encoded clients, block lock is achieved as per the state diagram in Figure 49-12 of [IEEE 802.3]. Descrambling is performed as per the process shown in Figure 49-10 of [IEEE 802.3].

Each 66B codeword (after block lock) is one of the following:

- a set of eight data bytes with a sync header of "01";
- a control block (possibly including seven or fewer data octets) beginning with a sync header of "10".

The 64 bits following the sync header are scrambled as a continuous bit-stream (skipping sync headers and PCS lane markers) according to the polynomial  $G(x) = 1 + x^{39} + x^{58}$ . The 64B/66B PCS receive process will descramble the bits other than (1) the sync header of 66B data and control blocks, and (2) the PCS lane markers.

Figure B.1 illustrates the ordering of 64B/66B code blocks after the completion of the recovering process for an interface.

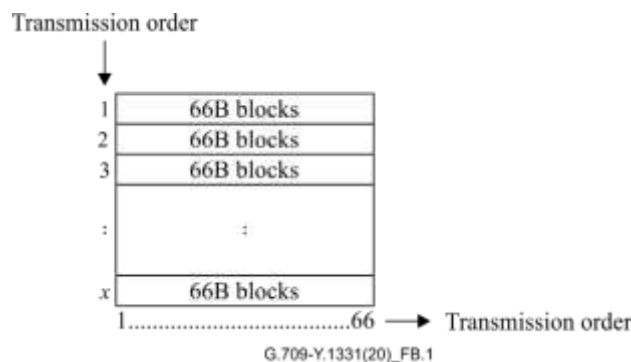


Figure B.1 – Stream of 64B/66B code blocks for transcoding

### **B.3 Transcoding from 66B blocks to 513B blocks**

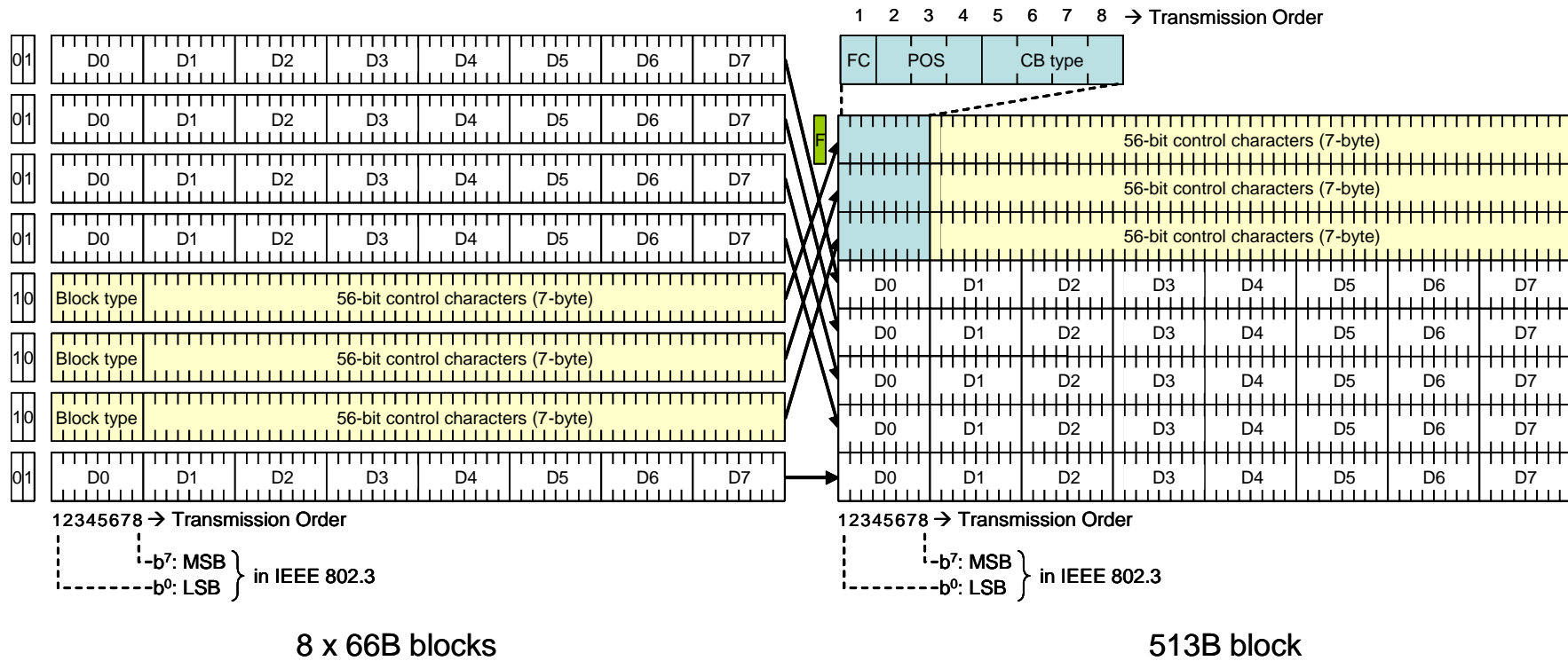
The transcoding process at the encoder operates on an input sequence of 66B code blocks.

66B control blocks (after descrambling) follow the format shown in Figure B.2.

A group of eight 66B blocks is encoded into a single 513B block. The format is illustrated in Figure B.3.

Input Data		S Y N C	Block Payload																																																														
Data Block Format	Bit Position	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65																																																															
		D0D1D2D3D4D5D6D7	0 1	D0							D1							D2							D3							D4							D5							D6							D7												
Control block formats			Block type field																																																												4-bit code		
C0C1C2C3C4C5C6C7	1 0	0x1e	C0							C1							C2							C3							C4							C5							C6							C7							0001						
C0C1C2C3O4D5D6D7	1 0	0x2d	C0							C1							C2							C3							O4			D5							D6							D7							0010										
C0C1C2C3S4D5D6D7	1 0	0x33	C0							C1							C2							C3										D5							D6							D7							0111										
O0D1D2D3S4D5D6D7	1 0	0x66	D1							D2							D3							O0			D5							D6							D7							1011																	
O0D1D2D3O4D5D6D7	1 0	0x55	D1							D2							D3							O0			O4			D5							D6							D7							1101														
S0D1D2D3D4D5D6D7	1 0	0x78	D1							D2							D3							D4							D5							D6							D7							1110													
O0D1D2D3C4C5C6C7	1 0	0x4b	D1							D2							D3							O0			C4							C5							C6							C7							1000										
T0C1C2C3C4C5C6C7	1 0	0x87								C1							C2							C3							C4							C5							C6							C7							0011						
D0T1C2C3C4C5C6C7	1 0	0x99	D0														C2							C3							C4							C5							C6							C7							0101						
D0D1T2C3C4C5C6C7	1 0	0xaa	D0							D1														C3							C4							C5							C6							C7							1001						
D0D1D2T3C4C5C6C7	1 0	0xb4	D0							D1							D2														C4							C5							C6							C7							1010						
D0D1D2D3T4C5C6C7	1 0	0xcc	D0							D1							D2							D3														C5							C6							C7							1100						
D0D1D2D3D4T5C6C7	1 0	0xd2	D0							D1							D2							D3							D4														C6							C7							0110						
D0D1D2D3D4D5T6C7	1 0	0xe1	D0							D1							D2							D3							D4							D5														C7							0000						
D0D1D2D3D4D5D6T7	1 0	0xff	D0							D1							D2							D3							D4							D5							D6														1111						

Figure B.2 – 66B Block coding



**Figure B.3 – 513B block code format**

Each of the 66B blocks is encoded into a row of the 8-byte by 8-row structure. Any 66B control blocks (CBi) are placed into the uppermost rows of the structure in the order received, while any all-data 66B blocks (DBi) are placed into the lowermost rows of the structure in the order received.

The flag bit "F" is 1 if the 513B structure contains at least one 66B control block, and 0 if the 513B structure contains eight all-data 66B blocks. Because the 66B control blocks are placed into the uppermost rows of the 513B block, if the flag bit "F" is 1, then the first row will contain a mapping of a 66B control block.

A 66B control block is encoded into a row of the structure shown in Figure B.3 as follows: the sync header of "10" is removed. The byte representing the block type field (see Figure B.2) is replaced by the structure shown in Figure B.4:



**Figure B.4 – 513B block's control block header**

The byte indicating the control block type (one of 15 legal values) is translated into a 4-bit code according to the rightmost column of Figure B.2. The 3-bit POS field is used to encode the position in which this control block was received in the sequence of eight 66B blocks. The flag continuation bit "FC" will be set to a 0 if this is the final 66B control block or PCS lane alignment marker encoded in this 513B block, or to a 1 if one or more 66B control blocks or PCS lane alignment markers follow this one. At the decoder, the flag bit for the 513B block as a whole, plus the flag continuation bits in each row containing the mapping of a 66B control block or PCS lane alignment marker will allow identification of those rows, which can then be restored to their original position amongst any all-data 66B blocks at the egress according to the POS field. The remaining 7 bytes of the row are filled with the last 7 bytes of the 66B control block.

An all-data 66B block is encoded into a row of the 513B block by dropping the sync header and copying the remaining eight bytes into the row. If all eight rows of the 513B block are placements of 66B all-data blocks, the flag bit "F" will be 0. If fewer than eight rows of the 513B block are placements of 66B all-data blocks, they will appear at the end, and the row containing the placement of the final 66B control block will have a flag continuation bit "FC" value of 0.

The decoder operates in the reverse of the encoder to reconstruct the original sequence of 66B blocks. If flag bit "F" is 1, then 66B control blocks starting from the first row of the block are reconstructed and placed in the position indicated by the POS field. This process continues through all of the control blocks working downward from the top row. The final 66B control block placed within the 513B block will be identified when the flag continuation bit "FC" is zero.

The structure of the 512B/513B code block is shown in Figure B.5. For example, if there is a single 64B/66B control block CB1 in a 512B/513B code block and it was originally located between 64B/66B data blocks DB2 and DB3, the first octet of the 64B character will contain 0.010.1101.CB1; the leading bit in the control octet of 0 indicates the flag continuation "FC" that this 64B control block is the last one in the 512B/513B code block, the value of 010 indicates CB1's position "POS" between DB2 and DB3, and the value of 1101 is a four-bit representation of the control code's block type "CB TYPE" (of which the eight-bit original block type is 0x55).

Input client characters	Flag bit	512-bit (64-Octet) field							
All data block	0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8
7 data block 1 control block	1	0 AAA aaaa CB1	DB1	DB2	DB3	DB4	DB5	DB6	DB7
6 data block 2 control block	1	1 AAA aaaa CB1	0 BBB bbbb CB2	DB1	DB2	DB3	DB4	DB5	DB6
5 data block 3 control block	1	1 AAA aaaa CB1	1 BBB bbbb CB2	0 CCC cccc CB3	DB1	DB2	DB3	DB4	DB5
4 data block 4 control block	1	1 AAA aaaa CB1	1 BBB bbbb CB2	1 CCC cccc CB3	0 DDD dddd CB4	DB1	DB2	DB3	DB4
3 data block 5 control block	1	1 AAA aaaa CB1	1 BBB bbbb CB2	1 CCC cccc CB3	1 DDD dddd CB4	0 EEE eeee CB5	DB1	DB2	DB3
2 data block 6 control block	1	1 AAA aaaa CB1	1 BBB bbbb CB2	1 CCC cccc CB3	1 DDD dddd CB4	1 EEE eeee CB5	0 FFF ffff CB6	DB1	DB2
1 data block 7 control block	1	1 AAA aaaa CB1	1 BBB bbbb CB2	1 CCC cccc CB3	1 DDD dddd CB4	1 EEE eeee CB5	1 FFF ffff CB6	0 GGG gggg CB7	DB1
8 control block	1	1 AAA aaaa CB1	1 BBB bbbb CB2	1 CCC cccc CB3	1 DDD dddd CB4	1 EEE eeee CB5	1 FFF ffff CB6	1 GGG gggg CB7	0 HHH hhhh CB8

- Leading bit in a 66B control block FC = 1 if there are more than 66B control block and = 0 if this payload contains the last control block in that 513B block  
- AAA = 3-bit representation of the first control code's original position (First control code locator: POS)  
- BBB = 3-bit representation of the second control code's original position (Second control code locator: POS)  
.....  
- HHH = 3-bit representation of the eighth control code's original position (Eighth control code locator: POS)  
- aaa = 4-bit representation of the first control code's type (first control block type: CB TYPE)  
- bbb = 4-bit representation of the second control code's type (Second control block type: CB TYPE)  
.....  
- hhh = 4-bit representation of the eighth control code's type (Eighth control block type: CB TYPE)  
- CBi = 56-bit representation of the i-th control code characters  
- DBi = 64-bit representation of the i-th data value in order of transmission

G.709-Y.1331(12)\_FB.5

**Figure B.5 – 513B code block components**

### B.3.1 Errors detected before 512B/513B encoder

A set of errors might be detected at the 64B/66B PCS receive process which, in addition to appropriate alarming, needs to send the appropriate signal downstream.

Errors encountered before the encoder, such as loss of client signal, will result in the insertion of an Ethernet LF sequence ordered set prior to this process, which will be transcoded as any other control block. The same action should be taken as a result of failure to achieve 66B block lock on an input signal.

An invalid 66B block will be converted to an error control block before transcoding and the OTN BIP-8 calculation as described in clause E.4.1. An invalid 66B block is one which does not have a sync header of "01" or "10", or one which has a sync header of "10" and a control block type field which does not appear in Figure B.2. An error control block has sync bits of "10", a block type code of 0x1E, and 8 seven-bit/E/error control characters. This will prevent the Ethernet receiver from interpreting a sequence of bits containing this error as a valid packet.

### B.3.2 Errors detected by 512B/513B decoder

Several mechanisms will be employed to reduce the probability that the decoder constructs erroneous 64B/66B encoded data at the egress if bit errors have corrupted. Since detectable corruption normally means that the proper order of 66B blocks to construct at the decoder cannot be reliably determined, if any of these checks fail, the decoder will transmit eight 66B error control blocks (sync="10", control block type=0x1e, and eight 7-bit/E/control characters).

Mechanisms for improving the robustness and for 513B block lock are discussed in Annex F.

#### **B.4 Link fault signalling**

In-band link fault signalling in the client 64B/66B code (e.g., if a local fault or remote fault sequence ordered set is being transmitted between Ethernet equipments) is carried transparently according to this transcoding.

## Annex C

### Adaptation of OTU3 and OTU4 over multichannel parallel interfaces

(This annex forms an integral part of this Recommendation.)

NOTE 1 – This mechanism is designed to allow the use of the optical modules being developed for IEEE 40GBASE-R and 100GBASE-R signals for short-reach client-side OTU3 and OTU4 interfaces respectively. The corresponding physical layer specifications are being added to [ITU-T G.695] and [ITU-T G.959.1].

OTU3 signals may be carried over parallel interfaces consisting of four lanes. This four-lane format is referred to as the OTL3.4 format.

OTU4 signals may be carried over parallel interfaces consisting of four or ten lanes, which are formed by bit multiplexing of 20 logical lanes. The four-lane format is referred to as the OTL4.4 signal format and the ten-lane format is referred to as the OTL4.10 signal format.

NOTE 2 – Ten lane IEEE 100GBASE-R interfaces have no corresponding ITU-T physical layer interface specification.

The OTU3 and OTU4 frames are inversely multiplexed over physical/logical lanes on a 16-byte boundary aligned with the OTUk frame as illustrated in Figure C.1. The OTUk frame is divided into 1020 groups of 16-bytes.

<i>l</i>					<i>4080</i>
1	1:16 (FAS)	17:32	33:48	49:64	4065:4080
2	4081:4096	4097:5012	5013:5028	5029:5044	9145:9160
3	9161:9176	9177:9192	9193:9208	9209:9224	12225:12240
4	12241:12256	12257:12272	12273:12288	12289:13304	16305:16320
			.....		

G.709-Y.1331(20)\_FC.1

**Figure C.1 – OTU3 and OTU4 frames divided on 16-byte boundary**

#### OTU3 16-byte increment distribution

Each 16-byte increment of an OTU3 frame is distributed round robin, to each of the four physical lanes. On each OTU3 frame boundary the lane assignments are rotated.

For OTU3, the lane rotation and assignment is determined by the two LSBs of the MFAS as described in Table C.1 and Figure C.2, which indicates the starting group of bytes of the OTU3 frame that are sent on each lane.

NOTE 3 – MFAS is scrambled as defined in clause 11.2.

The pattern repeats every 64 bytes until the end of the OTU3 frame. The following OTU3 frame will use different lane assignments according to the MFAS.

**Table C.1 – Lane rotation assignments for OTU3**

MFAS 7-8	Lane 0	Lane 1	Lane 2	Lane 3
*00	1:16	17:32	33:48	49:64
*01	49:64	1:16	17:32	33:48
*10	33:48	49:64	1:16	17:32
*11	17:32	33:48	49:64	1:16



The distribution of 16-byte blocks from the sequence of OTU3 frames is illustrated in Figure C.2:

The parallel lanes can be reassembled at the sink by first recovering framing on each of the parallel lanes, then recovering the lane identifiers and then performing lane de-skewing. Frame alignment, lane identifier recovery and multi-lane alignment should operate under  $10^{-3}$  bit error rate conditions before error correction. Refer to [ITU-T G.798] for the specific processing details.

The lane rotation mechanism will place the first 16 bytes of the OTU3 frame on each lane once per  $4080 \times 4$  (i.e., 16320) bytes (the same as an OTU3 itself). The two LSBs of the MFAS will be the same in each FAS on a particular lane, which allows the lane to be identified. Since the MFAS cycles through 256 distinct values, the lanes can be de-skewed and reassembled by the receiver as long as the total skew does not exceed 127 OTU3 frame periods (approximately 385  $\mu$ s). The receiver must use the MFAS to identify each received lane, as lane positions may not be preserved by the optical modules to be used for this application.

**OTU4 16-byte increment distribution**

Each 16-byte increment of an OTU4 frame is distributed, round robin, to each of the 20 logical lanes. On each OTU4 frame boundary the lane assignments are rotated.

For distribution of OTU4 to twenty logical lanes, since the MFAS is not a multiple of 20, a different marking mechanism must be used. Since the frame alignment signal is 6 bytes (48 bits) and as per [ITU-T G.798] only 32 bits must be checked for frame alignment, the third OA2 byte position will be borrowed as a logical lane marker (LLM). For maximum skew detection range, the lane marker value will increment on successive frames from 0-239 (240 values being the largest multiple of 20 that can be represented in 8-bits). LLM = 0 position shall be aligned with MFAS = 0 position every 3840 (the least common multiple of 240 and 256) frame periods. The logical lane number can be recovered from this value by a modulo 20 operation. Table C.2 and Figure C.3 illustrate how bytes of the OTU4 are distributed in 16-byte increments across the 20 logical lanes.

The pattern repeats every 320 bytes until the end of the OTU4 frame.

The following OTU4 frame will use different lane assignment according to the LLM MOD 20.

**Table C.2 – Lane rotation assignments for OTU4**

LLM MOD 20	Lane 0	Lane 1	.....	Lane 18	Lane 19
0	1:16	17:32		289:304	305:320
1	305:320	1:16		273:288	289:304
:					
18	33:48	49:64		1:16	17:32
19	17:32	33:48		305:320	1:16

The distribution of 16-byte blocks from the sequence of OTU4 frames is illustrated in Figure C.3.

The parallel lanes can be reassembled at the sink by first recovering framing on each of the parallel lanes, then recovering the lane identifiers and then performing de-skewing of the lanes. Frame alignment, lane identifier recovery and multi-lane alignment should operate under  $10^{-3}$  bit error rate conditions before error correction. Refer to [ITU-T G.798] for specific processing details.

The lane rotation mechanism will place the first 16 bytes of the OTU4 frame on each lane once per  $4080 \times 4$  (i.e., 16320) bytes (the same as an OTU4 itself). The "LLM MOD 20" will be the same in each FAS on a particular lane, which allows the lane to be identified. Since the LLM cycles through 240 distinct values, the lanes can be de-skewed and reassembled by the receiver as long as the total skew does not exceed 119 OTU4 frame periods (approximately 139  $\mu$ s). The receiver must use the

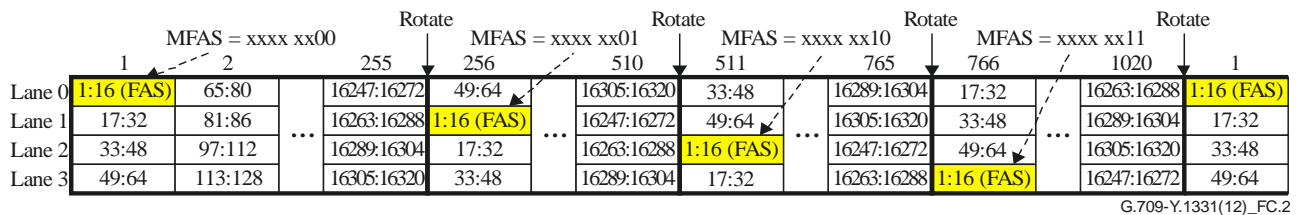
"LLM MOD 20" to identify each received lane, as lane positions may not be preserved by the optical modules to be used for this application.

The lanes are identified, de-skewed, and reassembled into the original OTU4 frame according to the lane marker. The MFAS can be combined with the lane marker to provide additional skew detection range, the maximum being up to the least common multiple "LCM(240, 256)/2 – 1" or 1919 OTU4 frame periods (approximately 2.241 ms). In mapping from lanes back to the OTU4 frame, the sixth byte of each OTU4 frame which was borrowed for lane marking is restored to the value OA2.

Each physical lane of an OTL4.4 carried over a multi-lane interface is formed by simple bit multiplexing of five logical lanes. At the sink, the bits are disinterleaved into five logical lanes from each physical lane. The sink will identify each logical lane according to the lane marker in the LLM byte. The sink must be able to accept the logical lanes in any position as the ordering of bit multiplexing on each physical lane is arbitrary; the optical module hardware to be used for this application is permitted full flexibility concerning which physical lane will be used for output of each logical lane, and the order of bit multiplexing of logical lanes on each physical output lane.

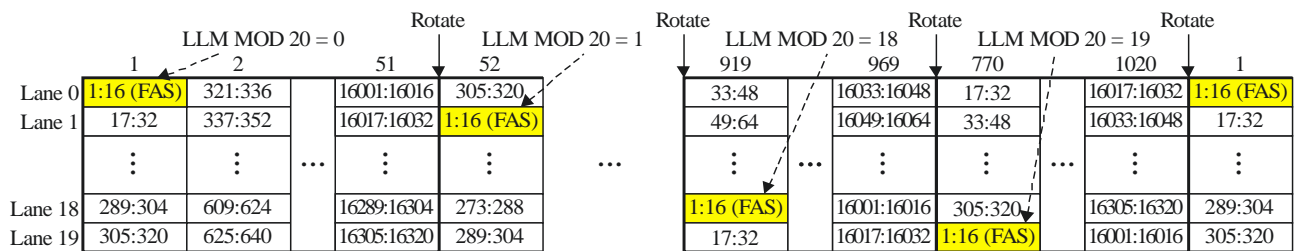
NOTE 4 – Ten-lane IEEE 100GBASE-R interfaces are specified, although not with ITU-T physical layer specifications. These interfaces may be compatible with a 10-lane interface for OTU4 (OTL4.10), each lane consisting of two bit-multiplexed logical lanes. Refer to [ITU-T G-Sup.58].

This mechanism handles any normally framed OTU3 or OTU4 sequence.



G.709-Y.1331(12)\_FC.2

**Figure C.2 – Distribution of bytes from OTU3 to parallel lanes**



G.709-Y.1331(12)\_FC.3

**Figure C.3 – Distribution of bytes from OTU4 to parallel lanes**

## Annex D

### Generic mapping procedure principles

(This annex forms an integral part of this Recommendation.)

#### D.1 Basic principle

For any given CBR client signal, the number of n-bit (e.g., n = 1/8, 1, 8) data entities that arrive during one server frame or server multiframe period is defined by:

$$c_n = \left( \frac{f_{client}}{n} \times T_{server} \right) \quad (D-1)$$

$f_{client}$ : client bit rate

$T_{server}$ : frame period of the server frame or server multiframe

$c_n$ : number of client n-bit data entities per server frame or server multiframe

As only an integer number of n-bit data entities can be transported per server frame or multiframe, the integer value  $C_n(t)$  of  $c_n$  has to be used. Since it is required that no client information is lost, the rounding process to the integer value has to take care of the truncated part, e.g., a  $c_n$  with a value of 10.25 has to be represented by the integer sequence 10,10,10,11.

$$C_n(t) = \text{int} \left( \frac{f_{client}}{n} \times T_{server} \right) \quad (D-2)$$

$C_n(t)$ : number of client n-bit data entities per server frame t or server multiframe t (integer)

For the case  $c_n$  is not an integer,  $C_n(t)$  will vary between:

$$C_n(t) = \text{floor} \left( \frac{f_{client}}{n} \times T_{server} \right) \quad (D-3)$$

and

$$C_n(t) = \text{ceiling} \left( \frac{f_{client}}{n} \times T_{server} \right) = 1 + \text{floor} \left( \frac{f_{client}}{n} \times T_{server} \right) \quad (D-4)$$

The server frame or multiframe rate is defined by the server bit rate and the number of bits per server frame or multiframe:

$$T_{server} = \frac{B_{server}}{f_{server}} \quad (D-5)$$

$f_{server}$ : server bit rate

$B_{server}$ : bits per server frame or multiframe

Combining (D-5) with (D-1) and (D-2) results in:

$$c_n = \left( \frac{f_{client}}{f_{server}} \times \frac{B_{server}}{n} \right) \quad (D-6)$$

and

$$C_n(t) = \text{int} \left( \frac{f_{client}}{f_{server}} \times \frac{B_{server}}{n} \right) \quad (\text{D-7})$$

As the client data has to fit into the payload area of the server signal, the maximum value of  $C_n$  and as such the maximum client bit rate is limited by the size of the server payload area.

$$C_n(t) \leq P_{server} \quad (\text{D-8})$$

$$f_{client} \leq f_{server} \times \frac{P_{server}}{B_{server}} \times n \quad (\text{D-9})$$

$P_{server}$ : maximum number of (n bits) data entities in the server payload area

The client and server bit rate are independent. This allows specifying the server bit rate independently from the client bit rates. Furthermore, client clock impairments are not seen at the server clock.

If the client or server bit rate changes due to client or server frequency tolerances,  $c_n$  and  $C_n(t)$  change accordingly. A special procedure has to take care that  $C_n(t)$  is changed fast enough to the correct value during start-up or during a step in the client bit rate (e.g., when the client signal is replaced by its AIS signal or the AIS signal is replaced by the client signal). This procedure may be designed to prevent buffer over-/underflow, or an additional buffer over-/underflow prevention method has to be deployed.

A transparent mapping has to determine  $C_n(t)$  on a server (multi)frame per (multi)frame base.

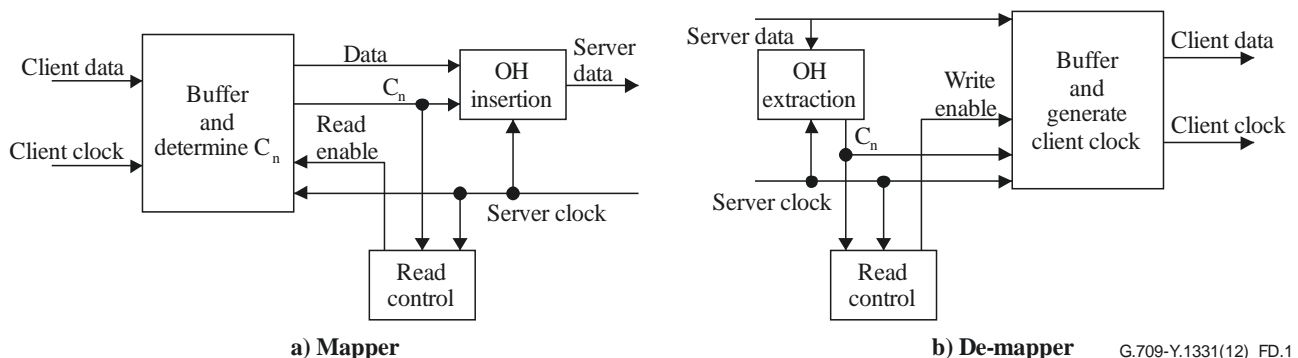
In order to extract the correct number of client information entities at the de-mapper,  $C_n(t)$  has to be transported in the overhead area of the server frame or multiframe from the mapper to the de-mapper.

Figure D.1 shows the generic functionality of the mapper and de-mapper circuit.

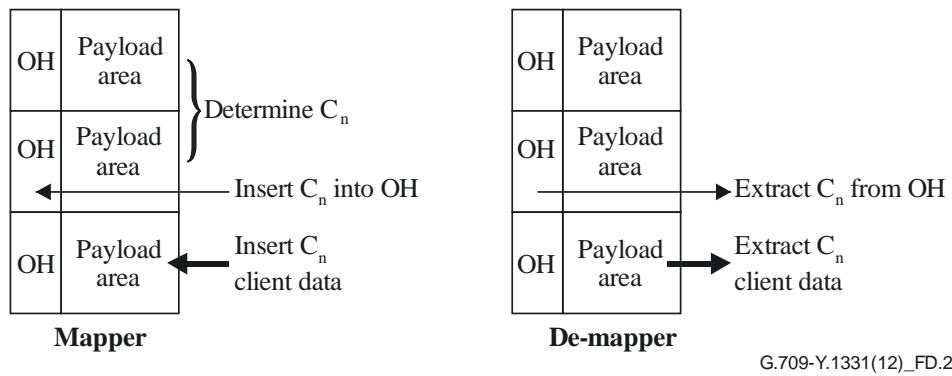
At the mapper,  $C_n(t)$  is determined based on the client and server clocks. The client data is constantly written into the buffer memory. The read out is controlled by the value of  $C_n(t)$ .

At the de-mapper,  $C_n(t)$  is extracted from the overhead.  $C_n(t)$  controls the write enable signal for the buffer. The client clock is generated based on the server clock and the value of  $C_n(t)$ .

$C_n(t)$  has to be determined first, then it has to be inserted into the overhead and afterwards  $C_n(t)$  client data entities have to be inserted into the payload area of the server as shown in Figure D.2.



**Figure D.1 – Generic functionality of a mapper/de-mapper circuit**

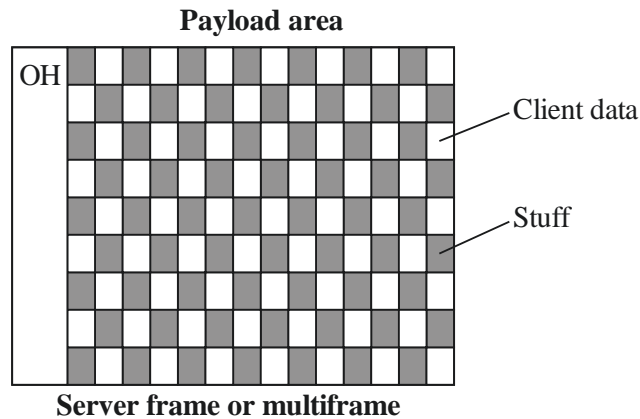


**Figure D.2 – Processing flow**

$C_n(t)$  client data entities are mapped into the payload area of the server frame or multiframe using a sigma-delta data/stuff mapping distribution. It provides a distributed mapping as shown in Figure D.3. Payload field  $j$  ( $j = 1 .. P_{server}$ ) carries:

– client data (D)                    if  $(j \times C_n(t)) \bmod P_{server} < C_n(t)$                     (D-10)

– stuff (S)                            if  $(j \times C_n(t)) \bmod P_{server} \geq C_n(t)$ .                    (D-11)

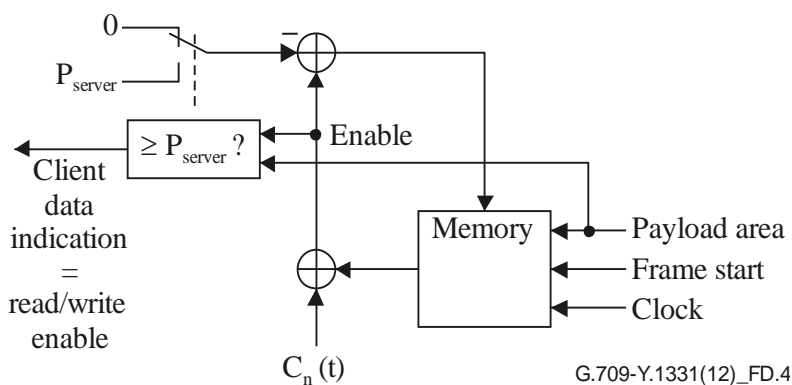


G.709-Y.1331(12)\_FD.3

**Figure D.3 – Sigma-delta based mapping**

$C_n(t)$  client data entities have to be distributed over  $P_{server}$  locations. A client data entity has therefore to be inserted with a spacing of  $\frac{P_{server}}{C_n(t)}$ . This is normally not an integer value, however it can be emulated by an integer calculation using the sigma-delta method based on an overflow accumulator as shown in Figure D.4.

The accumulator memory is reset to 0 at every frame start of the server frame. At every location of the payload area,  $C_n(t)$  is added to the memory and the result is compared with  $P_{server}$ . If the result is lower than  $P_{server}$ , it is stored back into the memory and no client data is indicated for this payload position. If it is equal or greater than  $P_{server}$ ,  $P_{server}$  is subtracted from the result and the new result is stored back in the memory. In addition, client data is indicated for the client position.



**Figure D.4 – Sigma-delta accumulator**

As the same start value and  $C_n(t)$  are used at the mapper and de-mapper the same results are obtained and interworking is achieved.

## D.2 Applying GMP in OTN

Clauses 17.7, 19.6 and 20.5 specify GMP as the asynchronous generic mapping method for the mapping of CBR client signals into OPUk, the mapping of ODUk signals into a server OPUk (via the ODTUk.ts) and the mapping of ODUk signals into an OPUCn (via ODTUCn.ts).

NOTE – GMP complements the traditional asynchronous client/server specific mapping method specified in clauses 17.6 and 19.5. GMP is intended to provide the justification of new CBR type client signals into OPUk.

Asynchronous mappings in the OTN have a default 8-bit timing granularity. Such 8-bit timing granularity is supported in GMP by means of a  $c_n$  with  $n=8$  ( $c_8$ ). The jitter/wander requirements for some of the OTN client signals are such that for those signals an 8-bit timing granularity may not be sufficient. For such a case, a 1-bit timing granularity is supported in GMP by means of  $c_n$  with  $n=1$  ( $c_1$ ).

### M-byte granularity mapping

Clauses 17.7 and 19.6 specify that the mapping of CBR client bits into the payload of an OPUk and the mapping of ODUj bits into the payload of an ODTUk.ts is performed with  $8 \times M$ -bit ( $M$ -byte) granularity.

The insertion of CBR client data into the payload area of the OPUk frame and the insertion of ODUj data into the payload area of the ODTUk.ts multiframe at the mapper is performed in  $M$ -byte (or  $m$ -bit,  $m = 8 \times M$ ) data entities, denoted as  $C_m(t)$ . The remaining  $C_{nD}(t)$  data entities are signalled in the justification overhead as additional timing/phase information.

$$c_m = \left( \frac{n \times c_n}{m} \right) = \left( \frac{f_{client}}{f_{server}} \times \frac{B_{server}}{m} \right) = \left( \frac{f_{client}}{f_{server}} \times \frac{B_{server}}{8 \times M} \right) = \left( \frac{f_{client}}{f_{server}} \times \frac{B_{server}/8}{M} \right) \quad (D-12)$$

As only an integer number of  $m$ -bit data entities can be transported per server frame or multiframe, the integer value  $C_m(t)$  of  $c_m$  has to be used. Since it is required that no information is lost, the rounding process to the integer value has to take care of the truncated part, e.g., a  $c_m$  with a value of 10.25 has to be represented by the integer sequence 10,10,10,11.

$$C_m(t) = \text{int}(c_m) = \text{int} \left( \frac{f_{client}}{f_{server}} \times \frac{B_{server}/8}{M} \right) \quad (D-13)$$

For the case  $c_m$  is not an integer,  $C_m(t)$  will vary between:

$$C_m(t) = \text{floor}\left(\frac{f_{client}}{f_{server}} \times \frac{B_{server}/8}{M}\right) \text{ and } C_m(t) = \text{ceiling}\left(\frac{f_{client}}{f_{server}} \times \frac{B_{server}/8}{M}\right) \quad (\text{D-14})$$

The remainder of  $c_n$  and  $C_m(t)$  is:

$$c_{nD} = c_n - \left(\frac{8 \times M}{n} \times C_m(t)\right) \quad (\text{D-15})$$

As only an integer number of  $c_{nD}$  n-bit data entities can be signalled per server frame or multiframe, the integer value  $C_{nD}(t)$  of  $c_{nD}$  has to be used.

$$C_{nD}(t) = \text{int}(c_n) - \left(\frac{8 \times M}{n} \times C_m(t)\right) = C_n(t) - \left(\frac{8 \times M}{n} \times C_m(t)\right) \quad (\text{D-16})$$

$C_{nD}(t)$  is a number between  $1 - \frac{8 \times M}{n}$  and  $\frac{8 \times M}{n} - 1$ .

### 16M-byte granularity mapping

Clause 20.5 specifies that the mapping of ODUk bits into the payload of an ODTUCn.ts is performed with  $128 \times M$ -bit (16M-byte) granularity.

The insertion of ODUk data into the payload area of the ODTUCn.ts multiframe at the mapper is performed in 16M-byte (or m-bit,  $m = 128 \times M$ ) data entities, denoted as  $C_m(t)$ . The remaining  $C_{nD}(t)$  data entities are signalled in the justification overhead as additional timing/phase information.

$$c_m = \left(\frac{n \times c_n}{m}\right) = \left(\frac{f_{client}}{f_{server}} \times \frac{B_{server}}{m}\right) = \left(\frac{f_{client}}{f_{server}} \times \frac{B_{server}}{128 \times M}\right) = \left(\frac{f_{client}}{f_{server}} \times \frac{B_{server}/128}{M}\right) \quad (\text{D-17})$$

As only an integer number of m-bit data entities can be transported per server frame or multiframe, the integer value  $C_m(t)$  of  $c_m$  has to be used. Since it is required that no information is lost, the rounding process to the integer value has to take care of the truncated part, e.g., a  $c_m$  with a value of 10.25 has to be represented by the integer sequence 10,10,10,11.

$$C_m(t) = \text{int}(c_m) = \text{int}\left(\frac{f_{client}}{f_{server}} \times \frac{B_{server}/128}{M}\right) \quad (\text{D-18})$$

For the case  $c_m$  is not an integer,  $C_m(t)$  will vary between:

$$C_m(t) = \text{floor}\left(\frac{f_{client}}{f_{server}} \times \frac{B_{server}/128}{M}\right) \text{ and } C_m(t) = \text{ceiling}\left(\frac{f_{client}}{f_{server}} \times \frac{B_{server}/128}{M}\right) \quad (\text{D-19})$$

The remainder of  $c_n$  and  $C_m(t)$  is:

$$c_{nD} = c_n - \left(\frac{128 \times M}{n} \times C_m(t)\right) \quad (\text{D-20})$$

As only an integer number of  $c_{nD}$  n-bit data entities can be signalled per server frame or multiframe, the integer value  $C_{nD}(t)$  of  $c_{nD}$  has to be used.

$$C_{nD}(t) = \text{int}(c_n) - \left(\frac{128 \times M}{n} \times C_m(t)\right) = C_n(t) - \left(\frac{128 \times M}{n} \times C_m(t)\right) \quad (\text{D-21})$$

$C_{nD}(t)$  is a number between  $1 - \frac{128 \times M}{n}$  and  $\frac{128 \times M}{n} - 1$ .

As the client data has to fit into the payload area of the server signal, the maximum value of  $C_m$  and as such the maximum client bit rate is limited by the size of the server payload area.

$$C_m(t) \leq P_{m,server} \quad (D-22)$$

$P_{m,server}$ : maximum number of (m bits) data entities in the server payload area

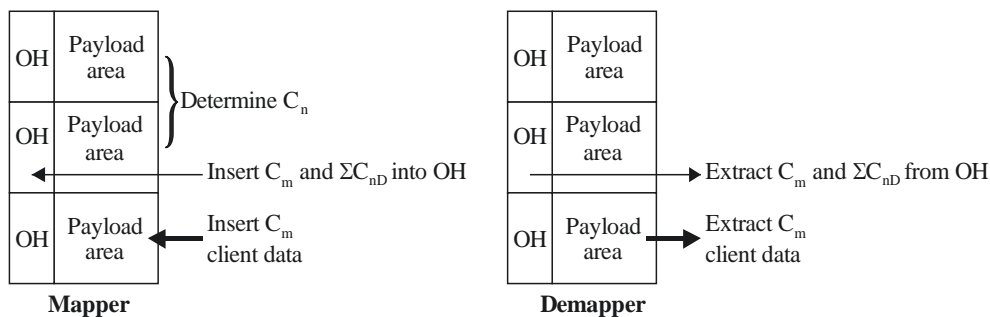
In order to extract the correct number of client information entities at the de-mapper,  $C_m(t)$  has to be transported in the overhead area of the server frame or multiframe from the mapper to the de-mapper.

At the mapper,  $C_n(t)$  is determined based on the client and server clocks. The client data is constantly written into the buffer memory. The read out is controlled by the value of  $C_m(t)$ .

At the de-mapper,  $C_m(t)$  and  $C_{nD}(t)$  are extracted from the overhead and used to compute  $C_n(t)$ .  $C_m(t)$  controls the write enable signal for the buffer. The client clock is generated based on the server clock and the value of  $C_n(t)$ .

$C_n(t)$  has to be determined first, then it has to be inserted into the overhead as  $C_m(t)$  and  $\Sigma C_{nD}(t)$  and afterwards  $C_m(t)$  client data entities have to be inserted into the payload area of the server as shown in Figure D.5.

The  $C_n(t)$  value determines the  $C_m(t)$  and  $C_{nD}(t)$  values;  $C_m(t) = \text{floor}(n/m \times C_n(t))$  and  $C_{nD}(t) = C_n(t) - (m/n \times C_m(t))$ . The values of  $C_{nD}(t)$  are accumulated and if  $\Sigma C_{nD}(t) \geq m/n$  then  $m/n$  is subtracted from  $\Sigma C_{nD}(t)$  and  $C_m(t)$  is incremented with +1. These latter two values are then encoded in the overhead bytes. This  $C_m(t)$  value is applied as input to the sigma-delta process.



G.709-Y.1331(12)\_FD.5

**Figure D.5 – Processing flow for GMP in OTN**

During start-up or during a step in the client bit rate, the value of  $C_n(t)$  will not match the actual number of n-bit client data entities arriving at the mapper buffer and the  $C_n(t)$  determination process has to adjust its value to the actual number of n-bit client data entities arriving. This adjustment method is implementation specific. During the mismatch period, the mapper buffer fill level may increase if more n-bit client data entities arrive per multiframe than there are transmitted, or decrease if less n-bit client data entities arrive per multiframe than there are transmitted.

To prevent overflow or underflow of the mapper buffer and thus data loss, the fill level of the mapper buffer has to be monitored. For the case where too many m-bit client data entities are in the buffer, it is necessary to insert temporarily more m-bit client data entities in the server (multi)frame(s) than required by  $C_n(t)$ . For the case too few m-bit client data entities are in the buffer, it is necessary to insert temporarily fewer m-bit client data entities in the server (multi)frame(s) than required by  $C_n(t)$ . This behaviour is similar to the behaviour of AMP under these conditions.

The OTN supports a number of client signal types for which transfer delay (latency) and transfer delay variation are critical parameters. Those client signal types require that the transfer delay introduced by the mapper plus de-mapper buffers is minimized and that the delay variation introduced by the mapper plus de-mapper buffers is minimized.



In steady state periods,  $C_n(t)$  is a value in the range  $C_{n,\min}$  to  $C_{n,\max}$ . A value outside this range indicates that there is a misalignment of the expected client bit rate and the actual client bit rate. During transient periods after e.g., a frequency step,  $C_n(t)$  may be temporarily outside the range  $C_{n,\min}$  to  $C_{n,\max}$ .

$C_m(t)$  client data entities are mapped into the payload area of the server frame or multiframe using a sigma-delta data/stuff mapping distribution. It provides a distributed mapping as shown in Figure D.3. Payload field  $j$  ( $j = 1 \dots P_{m,\text{server}}$ ) carries

$$- \quad \text{client data (D)} \quad \text{if } (j \times C_m(t)) \bmod P_{m,\text{server}} < C_m(t); \quad (\text{D-23})$$

$$- \quad \text{stuff (S)} \quad \text{if } (j \times C_m(t)) \bmod P_{m,\text{server}} \geq C_m(t). \quad (\text{D-24})$$

### Values of $n$ , $m$ , $M$ , $f_{\text{client}}$ , $f_{\text{server}}$ , $T_{\text{server}}$ , $B_{\text{server}}$ , and $P_{m,\text{server}}$ for OPUk and ODTUk.ts

The values for  $n$ ,  $m$ ,  $M$ ,  $f_{\text{client}}$ ,  $f_{\text{server}}$ ,  $T_{\text{server}}$ ,  $B_{\text{server}}$ , and  $P_{m,\text{server}}$  are specified in Table D.1.

**Table D.1 – OPUk, ODTUk.ts and ODTUCn.ts GMP parameter values**

GMP parameter	CBR client into OPUk	ODUj into OPUk (ODTUK.ts)	ODUk into OPUCn (ODTUCn.ts)
$n$	8 (default) 1 (client specific)	8	8
$m$	$m = 8 \times M$ OPU0: $8 \times 1 = 8$ OPU1: $8 \times 2 = 16$ OPU2: $8 \times 8 = 64$ OPU3: $8 \times 32 = 256$ OPU4: $8 \times 80 = 640$	$m = 8 \times M$ ODTU2.ts: $8 \times \text{ts}$ ODTU3.ts: $8 \times \text{ts}$ ODTU4.ts: $8 \times \text{ts}$ ODTU25.ts: $8 \times \text{ts}$ ODTU50.ts: $8 \times \text{ts}$	$m = 128 \times M$ ODTUCn.ts: $128 \times \text{ts}$
$f_{\text{client}}$	CBR client bit rate and tolerance	ODUj bit rate and tolerance (Table 7-2)	ODUk bit rate and tolerance (Table 7-2)
$f_{\text{server}}$	OPUk Payload bit rate and tolerance (Table 7-3)	ODTUK.ts Payload bit rate and tolerance (Table 7-7)	ODTUCn.ts Payload bit rate and tolerance (Table 7-7)
$T_{\text{server}}$	ODUk/OPUk frame period (Table 7-4)	OPUk multiframe period (Table 7-6)	OPUCn multiframe period (Table 7-6)
$B_{\text{server}}$	OPU0: $8 \times 15232$ OPU1: $8 \times 15232$ OPU2: $8 \times 15232$ OPU3: $8 \times 15232$ OPU4: $8 \times 15200$	ODTU2.ts: $8 \times \text{ts} \times 15232$ ODTU3.ts: $8 \times \text{ts} \times 15232$ ODTU4.ts: $8 \times \text{ts} \times 15200$ ODTU25.ts: $8 \times \text{ts} \times 15232$ ODTU50.ts: $8 \times \text{ts} \times 15232$	ODTUCn.ts: $128 \times \text{ts} \times 952$
$P_{m,\text{server}}$	OPU0: 15232 OPU1: 7616 OPU2: 1904 OPU3: 476 OPU4: 190	ODTU2.ts: 15232 ODTU3.ts: 15232 ODTU4.ts: 15200 ODTU25.ts: 15232 ODTU50.ts: 15232	ODTUCn.ts: 952
$\Sigma C_{8D}$ range	OPU0: N/A OPU1: 0 to +1 OPU2: 0 to +7 OPU3: 0 to +31 OPU4: 0 to +79	ODTUK.1: N/A ODTUK.2: 0 to +1 ODTUK.3: 0 to +2 ODTUK.4: 0 to +3 : ODTUK.8: 0 to +7 : ODTUK.32: 0 to +31 :	ODTUCn.1: 0 to +15 ODTUCn.2: 0 to +31 ODTUCn.3: 0 to +47 ODTUCn.4: 0 to +59 : ODTUCn.20n-1: 0 to +320n-1 ODTUCn.20n: 0 to +320n

**Table D.1 – OPUk, ODTUk.ts and ODTUCn.ts GMP parameter values**

GMP parameter	CBR client into OPUk	ODUj into OPUk (ODTUk.ts)	ODUk into OPUCn (ODTUCn.ts)
		ODTUk.79: 0 to +78 ODTUk.80: 0 to +79	
$\Sigma C_{ID}$ range (for selected clients)	OPU0: 0 to +7 OPU1: 0 to +15 OPU2: 0 to +63 OPU3: 0 to +255 OPU4: 0 to +639	Not applicable	Not applicable

### D.3 $C_m(t)$ encoding and decoding

$C_m(t)$  is encoded in the ODTUk.ts justification control bytes JC1, JC2 and JC3 specified in clause 19.4 for the 14-bit count and clause 20.4 for the 10-bit count field.

$C_m(t)$  is an L-bit binary count of the number of groups of m OPU payload bits that carry m client bits; it has values between  $\text{Floor}(C_{m,\min})$  and  $\text{Ceiling}(C_{m,\max})$ , which are client specific. The  $C_i$  ( $i=1..L$ ) bits that comprise  $C_m(t)$  are used to indicate whether the  $C_m(t)$  value is incremented or decremented from the value in the previous frame, that is indicated by  $C_m(t-1)$ . Tables D.2 and D.3 show the inversion patterns for the  $C_i$  bits of  $C_m(t-1)$  that are inverted to indicate an increment or decrement of the  $C_m(t)$  value. Table D.2 shows the inversion patterns for the 14-bit count and Table D.3 shows the inversion patterns for the 10-bit count. An "I" entry in the table indicates an inversion of that bit.

The bit inversion patterns apply to the  $C_m(t-1)$  value, prior to the increment or decrement operation that is signalled by the inversion pattern when  $|C_m(t) - C_m(t-1)| \leq 2$  (except  $C_m(t) - C_m(t-1) = 0$ ). The incremented or decremented  $C_m(t)$  value becomes the base value for the next GMP overhead transmission.

- When  $0 < C_m(t) - C_m(t-1) \leq 2$ , indicating an increment of +1 or +2, a subset of the  $C_i$  bits containing  $C_m(t-1)$  is inverted as specified in Table D.2 or Table D.3 and the increment indicator (II) bit is set to 1.
- When  $0 > C_m(t) - C_m(t-1) \geq -2$ , indicating a decrement of -1 or -2, a subset of  $C_i$  bits containing  $C_m(t-1)$  is inverted as specified in Table D.2 or Table D.3 and the decrement indicator (DI) bit is set to 1.
- When the value of  $C_m(t)$  is changed with a value larger than +2 or –2 from the value of  $C_m(t-1)$ , both the II and DI bits are set to 1 and the  $C_i$  bits contain the new  $C_m(t)$  value. The associated CRC in JC3 verifies whether the  $C_m(t)$  value has been received correctly.
- When the value of  $C_m(t)$  is unchanged from the value of  $C_m(t-1)$ , both the II and DI bits are set to 0.

The above encoding process is illustrated in Figure D.6.

**Table D.2 – 14-bit  $C_m(t)$  increment and decrement indicator patterns**

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	II	DI	Change
U	U	U	U	U	U	U	U	U	U	U	U	U	U	0	0	0
I	U	I	U	I	U	I	U	I	U	I	U	I	U	1	0	+1
U	I	U	I	U	I	U	I	U	I	U	I	U	I	0	1	-1
U	I	I	U	U	I	I	U	U	I	I	U	U	I	1	0	+2
I	U	U	I	I	U	U	I	I	U	U	I	I	U	0	1	-2
binary value														1	1	More than +2/-2
NOTE																
– I indicates inverted $C_i$ bit																
– U indicates unchanged $C_i$ bit																

The CRC-8 located in JC3 is calculated over the JC1 and JC2 bits. The CRC-8 uses the  $g(x) = x^8 + x^3 + x^2 + 1$  generator polynomial, and is calculated as follows:

- 1) The JC1 and JC2 octets are taken in network octet order, most significant bit first, to form a 16-bit pattern representing the coefficients of a polynomial  $M(x)$  of degree 15.
- 2)  $M(x)$  is multiplied by  $x^8$  and divided (modulo 2) by  $G(x)$ , producing a remainder  $R(x)$  of degree 7 or less.
- 3) The coefficients of  $R(x)$  are considered to be an 8-bit sequence, where  $x^7$  is the most significant bit.
- 4) This 8-bit sequence is the CRC-8 where the first bit of the CRC-8 to be transmitted is the coefficient of  $x^7$  and the last bit transmitted is the coefficient of  $x^0$ .

The de-mapper process performs steps 1-3 in the same manner as the mapper process, except that here, the  $M(x)$  polynomial of step 1 includes the CRC bits of JC3, resulting in  $M(x)$  having degree 23. In the absence of bit errors, the remainder shall be 0000 0000.

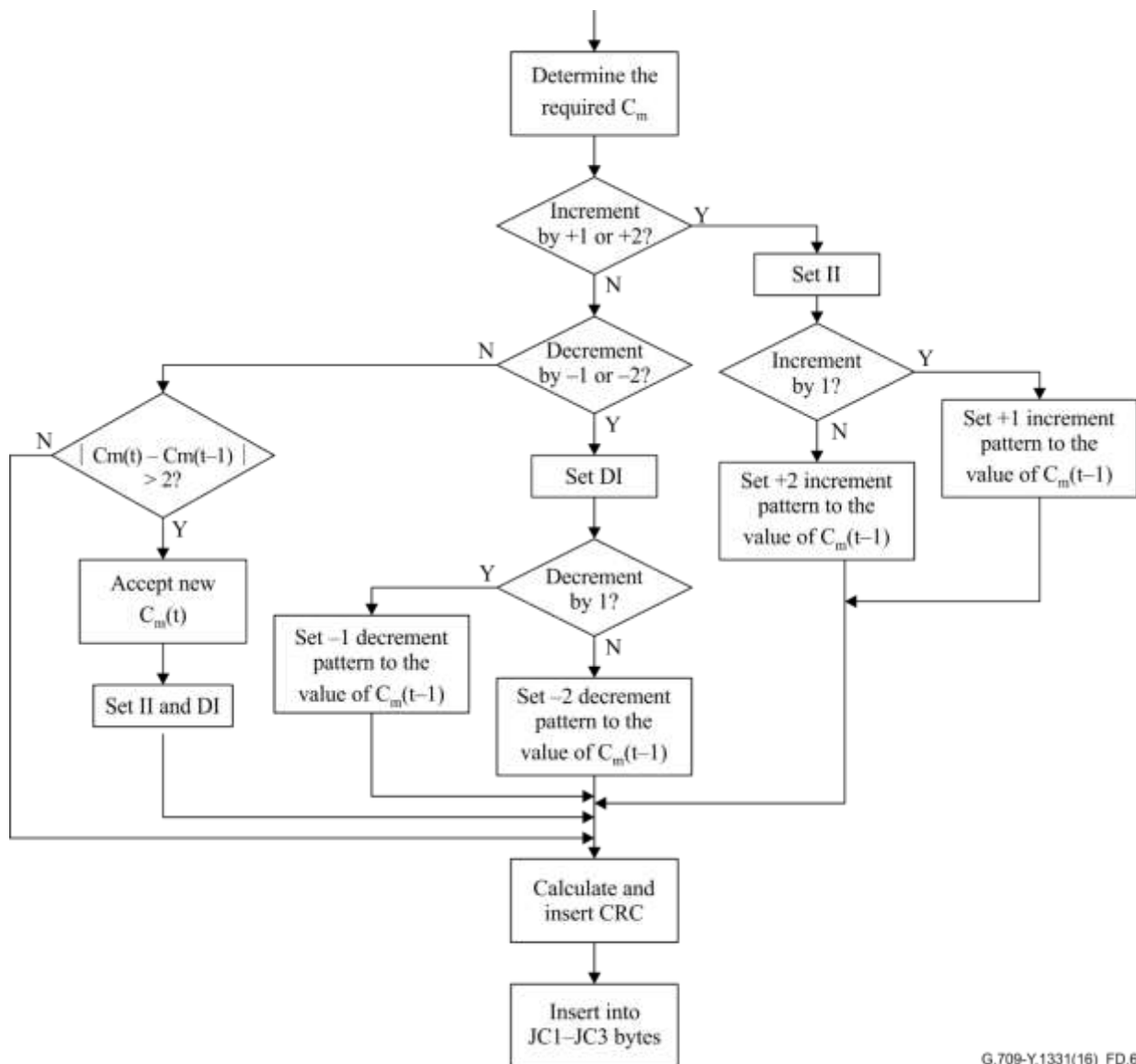
**Table D.3 – 10-bit  $C_m(t)$  increment and decrement indicator patterns**

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	II	DI	Change	
U	U	U	U	U	U	U	U	U	U	0	0	0	
I	U	I	U	I	U	I	U	I	U	1	0	+1	
I	U	U	I	U	I	I	U	U	I	0	1	-1	
U	I	U	I	I	U	U	I	U	I	1	0	+2	
U	I	I	U	U	I	U	I	I	U	0	1	-2	
binary value											1	1	More than +2/-2
NOTE													
– I indicates inverted $C_i$ bit													
– U indicates unchanged $C_i$ bit													

The CRC-6 located in JC3 is calculated over bits 3-8 of JC1 and JC2 (i.e., the bits containing the GMP overhead value shown in Table D.3). The CRC-6 uses the  $g(x) = x^6 + x^3 + x^2 + 1$  generator polynomial, and is calculated as follows:

- 1) The JC1 and JC2 octets are taken in network octet order, most significant bit first, such that bit 3 of JC1 through bit 8 of JC2 form a 12-bit pattern representing the coefficients of a polynomial  $M(x)$  of degree 11.
- 2)  $M(x)$  is multiplied by  $x^6$  and divided (modulo 2) by  $G(x)$ , producing a remainder  $R(x)$  of degree 5 or less.
- 3) The coefficients of  $R(x)$  are considered to be a 6-bit sequence, where  $x^5$  is the most significant bit.
- 4) This 6-bit sequence is the CRC-6 where the first bit of the CRC-6 to be transmitted is the coefficient of  $x^5$  and the last bit transmitted is the coefficient of  $x^0$ .

The de-mapper process performs steps 1-3 in the same manner as the mapper process, except that here, the  $M(x)$  polynomial of step 1 includes the CRC bits of JC3, resulting in  $M(x)$  having degree 17. In the absence of bit errors, the remainder shall be 000000.



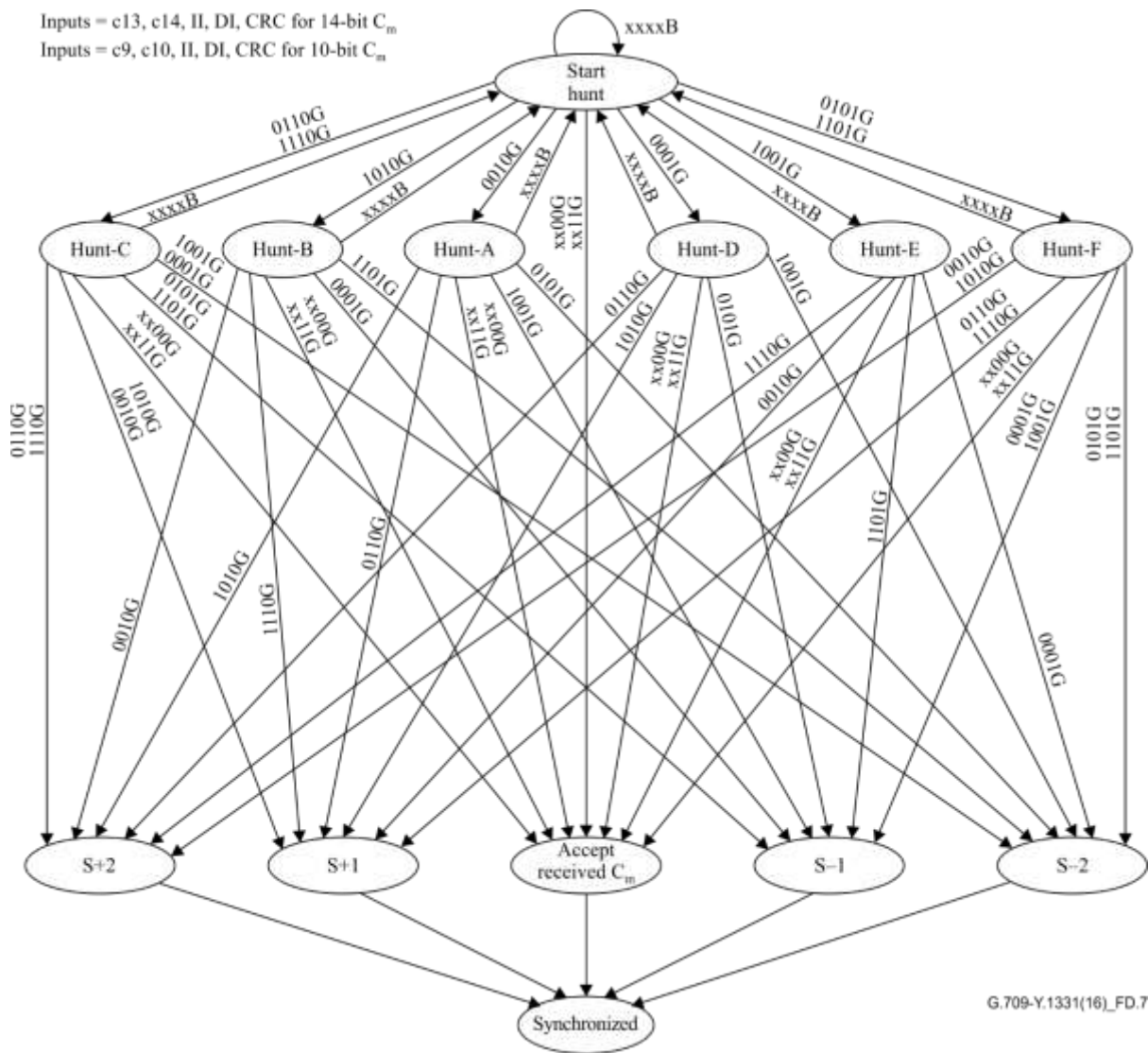
G.709-Y.1331(16)\_FD.6

Figure D.6 – JC1, JC2 and JC3 generation

A parallel logic implementation of the source CRC-8 and CRC-6 are illustrated in Appendix VI.

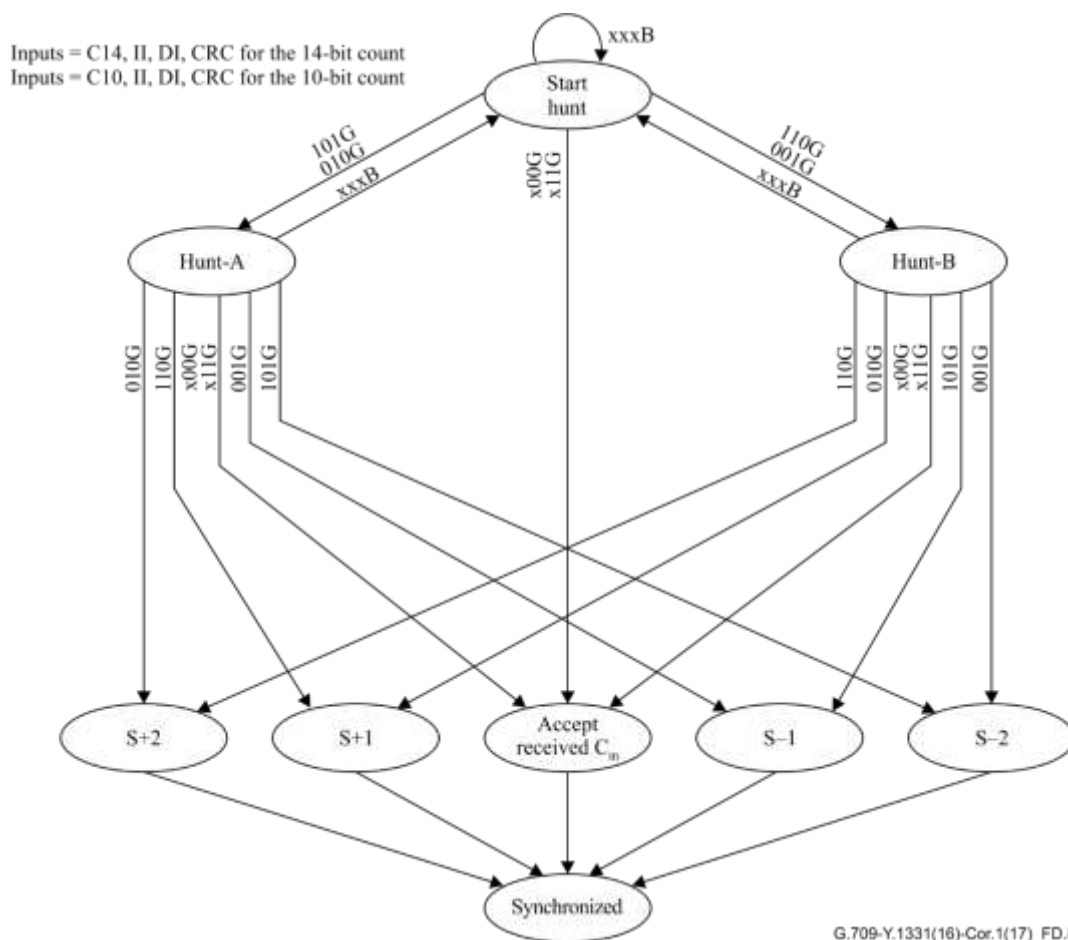
The GMP sink synchronizes its  $C_m(t)$  value to the GMP source through the following process, which is illustrated in Figure D.7 and the equivalent process in Figure D.8.

When the received JC octets contain  $II = DI$  and a valid CRC-8, the GMP sink accepts the received C1-CL as its  $C_m(t)$  value for the next frame. At this point the GMP sink is synchronized to the GMP source. When  $II \neq DI$  with a valid CRC in the current received frame (frame  $i$ ), the GMP sink must examine the received JC octets in the next frame (frame  $i+1$ ) in order to obtain  $C_m(t)$  synchronization.  $II \neq DI$  in frame  $i$  indicates that the source is performing a count increment or decrement operation that will modify the  $C_m(t)$  value it sends in frame  $i+1$ . Since this modification to the  $C_m(t)$  will affect the count LSBs, the GMP sink uses the LSBs, II, and DI in frame  $i$  to determine its synchronization hunt state when it receives frame  $i+1$ . Specifically, in Figure D.7, the Hunt state (A-F) is determined using C13, C14, II and DI for the 14-bit count and C9, C10, II and DI for the 10-bit count. Equivalently, in Figure D.8, the Hunt state (A or B) is determined using C14, II, and DI for the 14-bit count and C10, II, and DI for the 10-bit count. If  $II = DI$  with a valid CRC in frame  $i+1$ ,  $C_m(t)$  synchronization is achieved by directly accepting the received C1-CL as the new  $C_m(t)$ . If  $II \neq DI$  with a valid CRC in frame  $i+1$ , the sink uses the new LSBs, II and DI values to determine whether the source is communicating an increment or decrement operation and the magnitude of the increment/decrement step. This corresponds to the transition to the lower row of states (the "S" states) in Figure D.7 and Figure D.8. At this point, the GMP sink has identified the type of increment or decrement operation that is being signalled in frame  $i+1$ . As shown in Figure D.9, the sink then applies the appropriate bit inversion pattern from Table D.2 to the received C1-C14 field or the bit inversion pattern from Table D.3 to the received C1-C10 field to determine the transmitted  $C_m(t)$  value. Synchronization has now been achieved since the GMP sink has determined the current  $C_m(t)$  and knows the expected  $C_m(t)$  change in frame  $i+2$ .



**Figure D.7 – GMP sink count synchronization process representation using the two least significant bits of the count as inputs**

Optimization has shown that Figure D.8 provides the same function. Either one can be chosen. For historical reasons both are kept.



**Figure D.8 – GMP sink count synchronization process diagram**

14-bit count		10-bit count	
S state	Interpretation/Action	S state	Interpretation/Action
S+2	Count = C1-C14 after inverting C2, C3, C6, C7, C10, C11, & C14; Increment +2 for the next frame	S+2	Count = C1-C10 after inverting C2, C4, C5, C8 & C10; Increment +2 for the next frame
S+1	Count = C1-C14 after inverting C1, C3, C5, C7, C9, C11, & C13; Increment +1 for the next frame	S+1	Count = C1-C10 after inverting C1, C3, C5, C7 & C9; Increment +1 for the next frame
S-1	Count = C1-C14 after inverting C2, C4, C6, C8, C10, C12, & C14; Decrement -1 for next frame	S-1	Count = C1-C10 after inverting C1, C4, C6, C7 & C10; Decrement -1 for next frame
S-2	Count = C1-C14 after inverting C1, C4, C5, C8, C9, C12, C13; Decrement -2 for next frame	S-2	Count = C1-C10 after inverting C2, C3, C6, C8 & C9; Decrement -2 for next frame

**Figure D.9 – "S"-state interpretation for Figures D.7 and D.8**

Note that the state machine of Figure D.7 or Figure D.8 can also be used for off-line synchronization checking.

When the GMP sink has synchronized its  $C_m(t)$  value to the GMP source, it interprets the received JC octets according to the following principles:

- When the CRC is good and  $II = DI$ , the GMP sink accepts the received  $C_m(t)$  value.
- When the CRC is good and  $II \neq DI$ , the GMP sink compares the received  $C_m(t)$  value to its expected  $C_m(t)$  value to determine the difference between these values. This difference is compared to the bit inversion patterns of Table D.2 or Table D.3 to determine the increment or decrement operation sent by the source and updates its  $C_m(t)$  accordingly. Since the CRC is good, the sink can use either JC1 or JC2 for this comparison.
- When the CRC is bad, the GMP sink compares the received  $C_m(t)$  value to its expected  $C_m(t)$  value. The sink then compares the difference between these values, per Table D.2 or Table D.3, to the valid bit inversion patterns in JC1, and the bit inversion, II and DI pattern in JC2.
  - If JC1 contains a valid pattern and JC2 does not, the sink accepts the corresponding increment or decrement indication from JC1 and updates its  $C_m(t)$  accordingly.
  - If JC2 contains a valid pattern and JC1 does not, the sink accepts the corresponding increment or decrement indication from JC2 and updates its  $C_m(t)$  accordingly.
  - If both JC1 and JC2 contain valid patterns indicating the same increment or decrement operation, this indication is accepted and the sink updates its  $C_m(t)$  accordingly.
  - If neither JC1 nor JC2 contain valid patterns, the sink shall keep its current count value and begin the search for synchronization.

NOTE – If JC1 and JC2 each contain valid patterns that are different from each other, the receiver can either keep the current  $C_m(t)$  value and begin a synchronization search, or it can use the CRC to determine whether JC1 or JC2 contains the correct pattern.

The GMP sink uses the updated  $C_m(t)$  value to extract the client data from the next OPU frame or ODTUk.ts multiframe.

## D.4 $\Sigma C_{nD}(t)$ encoding and decoding

### D.4.1 $\Sigma C_{nD}(t)$ encoding and decoding for OPUk

The cumulative value of  $C_{nD}(t)$  ( $\Sigma C_{nD}(t)$ ) is encoded in bits 4-8 of the OPUk and ODTUk.ts justification control bytes JC4, JC5 and JC6. Bits D1 to D10 in JC4 and JC5 carry the value of  $\Sigma C_{nD}(t)$ . Bit D1 carries the most significant bit and bit D10 carries the least significant bit.

The CRC-5 located in JC6 is calculated over the D1-D10 bits in JC4 and JC5. The CRC-5 uses the  $g(x) = x^5 + x + 1$  generator polynomial, and is calculated as follows:

- 1) The JC4 bits 4-8 and JC5 bits 4-8 octets are taken in network transmission order, most significant bit first, to form a 10-bit pattern representing the coefficients of a polynomial  $M(x)$  of degree 9.
- 2)  $M(x)$  is multiplied by  $x^5$  and divided (modulo 2) by  $G(x)$ , producing a remainder  $R(x)$  of degree 4 or less.
- 3) The coefficients of  $R(x)$  are considered to be a 5-bit sequence, where  $x^4$  is the most significant bit.
- 4) This 5-bit sequence is the CRC-5 where the first bit of the CRC-5 to be transmitted is the coefficient of  $x^4$  and the last bit transmitted is the coefficient of  $x^0$ .

The de-mapper process performs steps 1-3 in the same manner as the mapper process, except that here, the  $M(x)$  polynomial of step 1 includes the CRC bits of JC6, resulting in  $M(x)$  having degree 14. In the absence of bit errors, the remainder shall be 00000.

A parallel logic implementation of the source CRC-5 is illustrated in Appendix VI.



#### D.4.2 $\Sigma C_{nD}(t)$ encoding and decoding for OPUCn

The cumulative value of  $C_{nD}(t)$  ( $\Sigma C_{nD}(t)$ ) is encoded in the ODTUCn.ts justification control bytes JC1, JC2, JC3, JC4, JC5 and JC6. Bits D1 to D18 carry the value of  $\Sigma C_{nD}(t)$ . Bit D1 carries the most significant bit and bit D18 carries the least significant bit. As shown in Figure 20-7, bits D1 to D7 are located in bits 2-8 of JC4, bits D8 to D9 are located in bits 1-2 of JC1, bits D10 to D16 are located in JC5, and bits D17 to D18 are located in bits 1-2 of JC2.

The CRC-9 located in bits 2-8 of JC6 and bits 1-2 of JC3 is calculated over the D1-D18 bits in JC4, JC1, JC5 and JC2. The CRC-9 uses the  $g(x) = x^9 + x^3 + x^2 + 1$  generator polynomial, and is calculated as follows:

- 1) The JC4 bits 2-8, JC1 bits 1-2, JC5 bits 2-8, and JC2 bits 1-2 are taken in network transmission order, most significant bit first, to form an 18-bit pattern representing the coefficients of a polynomial  $M(x)$  of degree 17.
- 2)  $M(x)$  is multiplied by  $x^9$  and divided (modulo 2) by  $G(x)$ , producing a remainder  $R(x)$  of degree 8 or less.
- 3) The coefficients of  $R(x)$  are considered to be a 9-bit sequence, where  $x^8$  is the most significant bit.
- 4) This 9-bit sequence is the CRC-9 where the first bit of the CRC-9 to be transmitted is the coefficient of  $x^8$  and the last bit transmitted is the coefficient of  $x^0$ .

The de-mapper process performs steps 1-3 in the same manner as the mapper process, except that here, the  $M(x)$  polynomial of step 1 includes the CRC bits of JC6 and JC3, resulting in  $M(x)$  having degree 26. In the absence of bit errors, the remainder shall be 000000000.

A parallel logic implementation of the source CRC-9 is illustrated in Appendix VI.

## Annex E

### Adaptation of parallel 64B/66B encoded clients

(This annex forms an integral part of this Recommendation.)

#### E.1 Introduction

IEEE 40GBASE-R and 100GBASE-R interfaces specified in [IEEE 802.3] are parallel interfaces intended for short-reach (up to 40 km) interconnection of Ethernet equipment. This annex describes the process of converting the parallel format of these interfaces into a serial bit stream to be carried over the OTN.

The order of transmission of information in all the diagrams in this annex is first from left to right and then from top to bottom.

#### E.2 Clients signal format

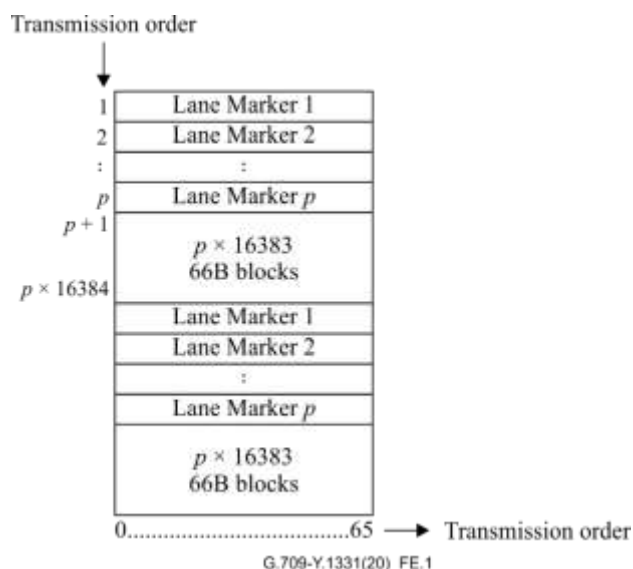
40GBASE-R and 100GBASE-R clients are initially parallel interfaces, but in the future they may be serial interfaces. Independent of whether these interfaces are parallel or serial, or what the parallel interface lane count is, 40GBASE-R signals are comprised of four PCS lanes, and 100GBASE-R signals are comprised of twenty PCS lanes. If the number of physical lanes on the interface is fewer than the number of PCS lanes, the appropriate number of PCS lanes is bit-multiplexed onto each physical lane of the interface. Each PCS lane consists of 64B/66B encoded data with a PCS lane alignment marker inserted on each lane once per 16384 66-bit blocks. The PCS lane alignment marker itself is a special format 66B codeword.

The use of this adaptation for 40GBASE-R into OPU3 also applies the transcoding method that appears in Annex B and the framing method of Annex F. The adaptation described in this annex alone can be used for the adaptation of 100GBASE-R into OPU4.

#### E.3 Client frame recovery

Client framing recovery consists of the following:

- bit-disinterleave the PCS lanes, if necessary. This is necessary whenever the number of PCS lanes and the number of physical lanes is not equal, and is not necessary when they are equal (e.g., a 4-lane 40GBASE-R interface);
- recover 64B/66B block lock as per the state diagram in Figure 82-10 of [IEEE 802.3];
- recover lane alignment marker framing on each PCS lane as per the state diagram in Figure 82-11 of [IEEE 802.3];
- reorder and de-skew the PCS lanes into a serialized stream of 66B blocks (including lane alignment markers). Figure E.1 illustrates the ordering of 66B blocks after the completion of this process for an interface with  $p$  PCS lanes.



**Figure E.1 – De-skewed/serialized stream of 66B blocks**

Each 66B codeword is one of the following:

- a set of eight data bytes with a sync header of "01";
- a control block (possibly including seven or fewer data octets) beginning with a sync header of "10";
- a PCS lane alignment marker, also encoded with a sync header of "10". Of the 8 octets following the sync header, 6 octets have fixed values allowing the PCS lane alignment markers to be recognized (see Tables E.1 and E.2). The fourth octet following the sync header is a BIP-8 calculated over the data from one alignment marker to the next as defined in Table 82-4 of [IEEE 802.3]. The eighth octet is the complement of this BIP-8 value to maintain DC balance. Note that the intended operation is to pass these BIP-8 values transparently as they are used for monitoring the error ratio of the Ethernet link between Ethernet PCS sublayers. For the case of 100GBASE-R, the BIP-8 values are not manipulated by the mapping or de-mapping procedure. For the case of 40GBASE-R, a BIP-8 compensation is done as described in clause E.4.1.

For all-data blocks and control blocks, the 64 bits following the sync header are scrambled as a continuous bit-stream (skipping sync headers and PCS lane alignment markers) according to the polynomial  $G(x) = 1 + x^{39} + x^{58}$ .

After 64B/66B block lock recovery as per the state diagram in Figure 82-10 of [IEEE 802.3] to the single-lane received aggregate signal, these 66B blocks are re-distributed to PCS lanes at the egress interface. The 66B blocks (including PCS lane alignment markers) resulting from the decoding process are distributed round-robin to PCS lanes. If the number of PCS lanes is greater than the number of physical lanes of the egress interface, the appropriate numbers of PCS lanes are bit-multiplexed onto the physical lanes of the egress interface.

### E.3.1 40GBASE-R client frame recovery

PCS lane alignment markers have the values shown in Table E.1 for 40GBASE-R signals which use PCS lane numbers 0-3.

**Table E.1 – PCS lane alignment marker format for 40GBASE-R**

Lane Number	SH	Encoding { <u>M<sub>0</sub>, M<sub>1</sub>, M<sub>2</sub>, BIP<sub>3</sub>, M<sub>4</sub>, M<sub>5</sub>, M<sub>6</sub>, BIP<sub>7</sub></u> }
0	10	0x90, 0x76, 0x47, BIP <sub>3</sub> , 0x6f, 0x89, 0xb8, BIP <sub>7</sub>
1	10	0xf0, 0xc4, 0xe6, BIP <sub>3</sub> , 0x0f, 0x3b, 0x19, BIP <sub>7</sub>
2	10	0xc5, 0x65, 0x9b, BIP <sub>3</sub> , 0x3a, 0x9a, 0x64, BIP <sub>7</sub>
3	10	0xa2, 0x79, 0x3d, BIP <sub>3</sub> , 0x5d, 0x86, 0xc2, BIP <sub>7</sub>

Since a 40GBASE-R client signal must be transcoded into 1024B/1027B for rate reduction, the 64B/66B PCS receive process at the ingress interface further descrambles the bit-stream skipping sync headers and PCS lane alignment markers, and the 64B/66B PCS transmit process at the egress interface scrambles the bit-stream again skipping sync headers and PCS lane alignment markers, as shown in Figure E.1.

### E.3.2 100GBASE-R client frame recovery

PCS lane alignment markers have the values shown in Table E.2 for 100GBASE-R signals which use PCS lane numbers 0-19.

The lane alignment markers transported over the OPU4 are distributed unchanged to the PCS lanes.

**Table E.2 – PCS lane alignment marker format for 100GBASE-R**

Lane Number	SH	Encoding { <u>M<sub>0</sub>, M<sub>1</sub>, M<sub>2</sub>, BIP<sub>3</sub>, M<sub>4</sub>, M<sub>5</sub>, M<sub>6</sub>, BIP<sub>7</sub></u> }	Lane Number	SH	Encoding { <u>M<sub>0</sub>, M<sub>1</sub>, M<sub>2</sub>, BIP<sub>3</sub>, M<sub>4</sub>, M<sub>5</sub>, M<sub>6</sub>, BIP<sub>7</sub></u> }
0	10	0xc1, 0x68, 0x21, BIP <sub>3</sub> , 0x3e, 0x97, 0xde, BIP <sub>7</sub>	10	10	0xfd, 0x6c, 0x99, BIP <sub>3</sub> , 0x02, 0x93, 0x66, BIP <sub>7</sub>
1	10	0x9d, 0x71, 0x8e, BIP <sub>3</sub> , 0x62, 0x8e, 0x71, BIP <sub>7</sub>	11	10	0xb9, 0x91, 0x55, BIP <sub>3</sub> , 0x46, 0x6e, 0xaa, BIP <sub>7</sub>
2	10	0x59, 0x4b, 0xe8, BIP <sub>3</sub> , 0xa6, 0xb4, 0x17, BIP <sub>7</sub>	12	10	0x5c, 0xb9, 0xb2, BIP <sub>3</sub> , 0xa3, 0x46, 0x4d, BIP <sub>7</sub>
3	10	0x4d, 0x95, 0x7b, BIP <sub>3</sub> , 0xb2, 0x6a, 0x84, BIP <sub>7</sub>	13	10	0x1a, 0xf8, 0xbd, BIP <sub>3</sub> , 0xe5, 0x07, 0x42, BIP <sub>7</sub>
4	10	0xf5, 0x07, 0x09, BIP <sub>3</sub> , 0x0a, 0xf8, 0xf6, BIP <sub>7</sub>	14	10	0x83, 0xc7, 0xca, BIP <sub>3</sub> , 0x7c, 0x38, 0x35, BIP <sub>7</sub>
5	10	0xdd, 0x14, 0xc2, BIP <sub>3</sub> , 0x22, 0xeb, 0x3d, BIP <sub>7</sub>	15	10	0x35, 0x36, 0xcd, BIP <sub>3</sub> , 0xca, 0xc9, 0x32, BIP <sub>7</sub>
6	10	0x9a, 0x4a, 0x26, BIP <sub>3</sub> , 0x65, 0xb5, 0xd9, BIP <sub>7</sub>	16	10	0xc4, 0x31, 0x4c, BIP <sub>3</sub> , 0x3b, 0xce, 0xb3, BIP <sub>7</sub>
7	10	0x7b, 0x45, 0x66, BIP <sub>3</sub> , 0x84, 0xba, 0x99, BIP <sub>7</sub>	17	10	0xad, 0xd6, 0xb7, BIP <sub>3</sub> , 0x52, 0x29, 0x48, BIP <sub>7</sub>
8	10	0xa0, 0x24, 0x76, BIP <sub>3</sub> , 0x5f, 0xdb, 0x89, BIP <sub>7</sub>	18	10	0x5f, 0x66, 0x2a, BIP <sub>3</sub> , 0xa0, 0x99, 0xd5, BIP <sub>7</sub>
9	10	0x68, 0xc9, 0xfb, BIP <sub>3</sub> , 0x97, 0x36, 0x04, BIP <sub>7</sub>	19	10	0xc0, 0xf0, 0xe5, BIP <sub>3</sub> , 0x3f, 0x0f, 0x1a, BIP <sub>7</sub>

#### E.4 Additions to Annex B transcoding for parallel 40GBASE-R clients

Mapping 40GBASE-R clients into OPU3 requires the transcoding into 513B code blocks described in Annex B. This clause describes the additions to the Annex B transcoding process for transport of PCS lane alignment markers.

Ethernet path monitoring is the kind of behaviour that is desirable in the case where the Ethernet equipment and the OTN equipment are in different domains (e.g., customer and service provider) and from the standpoint of the Ethernet equipment. It is also the default behaviour which would result from the current mapping of 100GBASE-R where the 66B blocks would be mapped into the OPU4 container after management of skew. It may also be perceived as a transparency requirement that BIP-8 work end-to-end. Additional functionality as described below has to be built in to allow BIP-8 transparency for 40GBASE-R client signals.

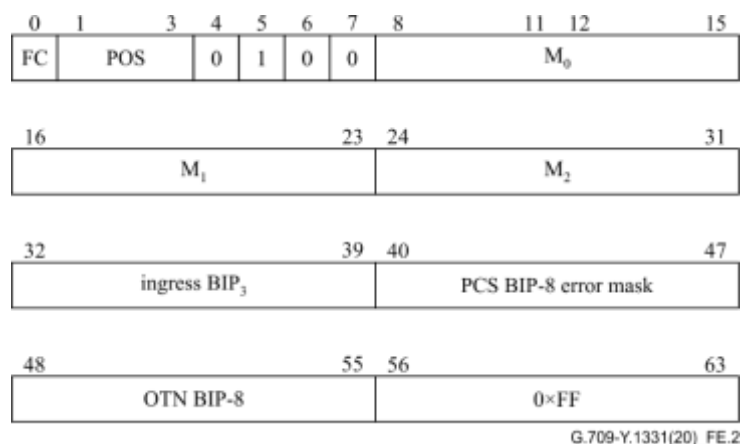
PCS lane alignment markers are encoded together with 66B control blocks into the uppermost rows of the 513B code block shown in Figure B.3. The flag bit "F" of the 513B structure is 1 if the 513B structure contains at least one 66B control block or PCS lane alignment marker, and 0 if the 513B structure contains eight all-data 66B blocks.

The transcoding into 512B/513B must encode PCS lane alignment marker into a row of the structure shown in Figure B.3 as follows: The sync header of "10" is removed. The received  $M_0$ ,  $M_1$  and  $M_2$  bytes of the PCS alignment marker encodings as shown in Table E.1 are used to forward the lane number information. The first byte of the row will contain the structure shown in Figure B.4, with a CB-TYPE field of "0100". The POS field will indicate the position where the PCS lane alignment marker was received among the group of eight 66B codewords being encoded into this 513B block. The flag continuation bit "FC" will indicate whether any other 66B control blocks or PCS lane alignment markers are encoded into rows below this one in the 513B block. Beyond this first byte, the next four bytes of the row are populated with the received  $M_0$ ,  $M_1$ ,  $M_2$  and ingress BIP<sub>3</sub> bytes of the PCS alignment marker encodings at the encoder. At the decoder, a PCS lane alignment marker will be generated in the position indicated by the POS field among any 66B all-data blocks contained in this 513B block, the sync header of "10" is generated followed by the received  $M_0$ ,  $M_1$  and  $M_2$  bytes, the egress BIP<sub>3</sub> byte, the bytes  $M_4$ ,  $M_5$  and  $M_6$  which are the bit-wise inverted  $M_0$ ,  $M_1$  and  $M_2$  bytes received at the decoder, and the egress BIP<sub>7</sub> byte which is the bit-wise inverted egress BIP<sub>3</sub> byte.

It will then be up to the Ethernet receiver to handle bit errors within the OTN section that might have altered the PCS alignment marker encodings (for details refer to clause 82.2.18.3 and Figure 82-11 in [IEEE 802.3]).

The egress BIP<sub>3</sub> and the egress BIP<sub>7</sub> bytes are calculated as described in clause E.4.1.

Figure E.2 below shows the transcoded lane marker format.



**Figure E.2 – Transcoded lane marker format**

#### E.4.1 40GBASE-R BIP-8 transparency

The transcoding method used for 40GBASE-R is timing and PCS codeword transparent. In normal operation, the only aspects of the PCS encoded bitstream that are not preserved given the mapping described in annexes B, E and F are for one the scrambling, since the scrambler does not begin with a known state and multiple different encoded bitstreams can represent the same PCS encoded content, and secondly the BIP-8 value in the Ethernet path or more precisely, the bit errors that occur between the Ethernet transmitter and the ingress point of the OTN domain and within the OTN domain. The BIP-8 values can be preserved with the scheme described below. As the scrambling itself does not contain any information that has to be preserved, no effort has been made to synchronize the scrambler states between OTN ingress and OTN egress.

Unfortunately, since the BIP-8 is calculated on the scrambled bitstream, a simple transport of the BIP-8 across the OTN domain in the transcoded lane marker will not result in a BIP-8 value that is meaningful for detecting errors in the received, descrambled, transcoded, trans-decoded, and then rescrambled bit stream.

To preserve the bit errors between the Ethernet transmitter and the egress side of the OTN domain, the bit-error handling is divided into two processes, one that takes place at the OTN ingress side, or encoder, and one on the OTN egress side, or decoder.

At the OTN ingress an 8-bit error mask is calculated by generating the expected BIP-8 for each PCS lane and XORing this value with the received BIP-8. This error mask will have a "1" for each bit of the BIP-8 which is wrong, and a "0" for each bit which is correct. This value is shown as a PCS BIP-8 error mask in Figure E.2.

In the event no errors are introduced across the OTN (as an FEC protected network can be an essentially zero error environment), the PCS BIP-8 error mask can be used to adjust the newly calculated PCS BIP-8 at the egress providing a reliable indication of the number of errors that are introduced across the full Ethernet path. If errors are introduced across the OTN, this particular BIP-8 calculation algorithm will not see these errors.

To overcome this situation, a new BIP-8 per lane for the OTN section is introduced. In the following this new BIP-8 will be identified as OTN BIP-8 in order to distinguish it from the PCS BIP-8.

It should be noted that the term OTN BIP-8 does not refer to and should not be confused with the BIP-8 defined in the OTUk overhead (byte SM[2]).

The OTN BIP-8 is calculated similarly to the PCS BIP-8 as described in clause 82.2.8 of [IEEE 802.3] with the exception that the calculation will be done over unscrambled PCS lane data, the original received lane alignment marker, after error control block insertion and before transcoding. Figure E.2 shows the byte location of the OTN BIP-8 in the transcoded lane marker.

The transcoded lane marker is transmitted together with the transcoded data blocks over the OTN section as defined in Annex B. At the OTN egress after trans-decoding and before scrambling, the ingress alignment marker is recreated using  $M_0$ ,  $M_1$ ,  $M_2$  and ingress  $BIP_3$  of the transcoded alignment marker followed by the bit-wise inversion of these bytes. This recreated alignment marker together with the trans-decoded and unscrambled data blocks is used to calculate the expected OTN BIP-8 for each PCS lane (refer to clause 82.2.8 of [IEEE 802.3]). The expected value will be XORed with the received OTN BIP-8. This error mask will have a "1" for each bit of the OTN BIP-8 which is wrong, and a "0" for each bit which is correct.

The egress  $BIP_3$  for each PCS lane is calculated over the trans-decoded and scrambled data blocks including the trans-decoded alignment marker (refer to clause E.4) following the process depicted in clause 82.2.8 of [IEEE 802.3].

The egress BIP<sub>3</sub> is then adjusted for the errors that occurred up to the OTN egress by first XORing with the PCS BIP-8 error mask and then XORing with the OTN BIP-8 error mask. This combined error mask will be used to compute the number of BIP errors when used for non-intrusive monitoring.

The BIP<sub>7</sub> is created by bit-wise inversion of the adjusted BIP<sub>3</sub>.

#### **E.4.2 Errors detected by 40GBASE-R to OPU3 mapper**

An invalid 66B block will be converted to an error control block before transcoding. An invalid 66B block is one which does not have a sync header of "01" or "10", or one which has a sync header of "10", is not a valid PCS lane alignment marker and has a control block type field which does not appear in Figure B.2 or has one of the values 0x2d, 0x33, 0x66, or 0x55 which are not used for 40GBASE-R. An error control block has sync bits of "10", a block type code of 0x1e, and 8 seven-bit/E/error control characters. This will prevent the Ethernet receiver from interpreting a sequence of bits containing this error as a valid packet.

#### **E.4.3 Errors detected by 40GBASE-R to OPU3 de-mapper**

Several mechanisms will be employed to reduce the probability that the 40GBASE-R to OPU3 de-mapper constructs erroneous parallel 64B/66B encoded data at the egress if bit errors have corrupted. Since detectable corruption normally means that the proper order of 66B blocks to construct at the de-mapper cannot be reliably determined, if any of these checks fail, the de-mapper will transmit eight 66B error control blocks (sync="10", control block type=0x1e, and eight 7-bit/E/control characters).

Mechanisms for improving the robustness and for 513B block lock including PCS lane alignment markers are discussed in Annex F.

## Annex F

### Improved robustness for mapping of 40GBASE-R into OPU3 using 1027B code blocks

(This annex forms an integral part of this Recommendation.)

#### F.1 Introduction

When a parallel 40GBASE-R signal is transcoded as per Annexes B and E and directly mapped into OPU3 without GFP framing, another method is needed to locate the start of 513B blocks and to provide protection to prevent bit errors creating an unacceptable increase in mean time to false packet acceptance (MTTFPA).

#### F.2 513B code block framing and flag bit protection

The mapping of 513B code blocks into OPU3 requires a mechanism for locating the start of the code blocks. A mechanism is also needed to protect the flag bit, whose corruption could cause data to be erroneously interpreted as control and vice versa.

Both of these requirements can be addressed by providing parity across the flag bits of two 513B blocks produced from the transcoding of Annex B.

Figure F.1 illustrates the flag parity bit across two 513B blocks. This creates a minimum two-bit Hamming distance between valid combinations of flag bits.

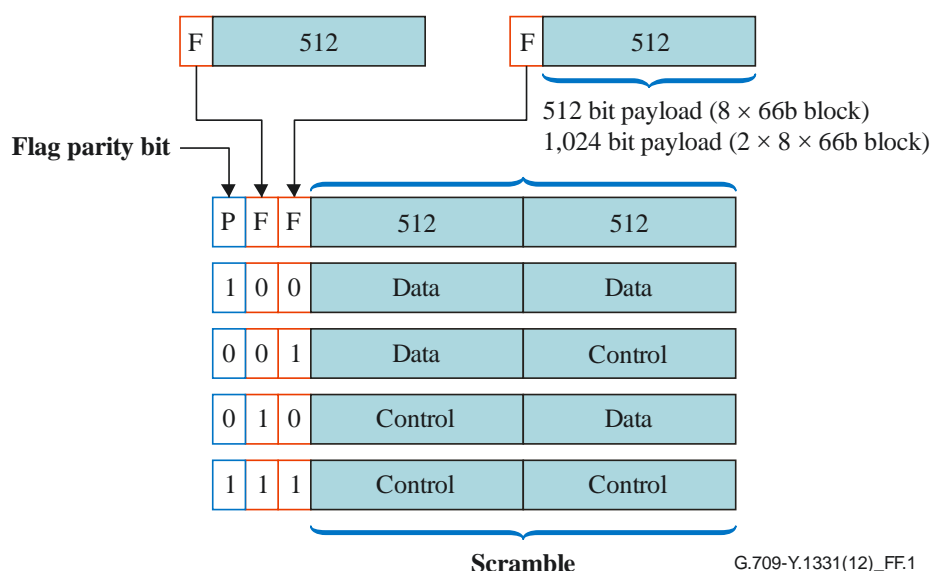


Figure F.1 – Flag parity bit on two 513B blocks (1027B code)

The flag parity bit creates a sequence that can be used for framing to locate the 513B blocks in a stream of bits. The state diagram of Figure 49-12 of [IEEE 802.3] is applied to locate a 3-bit pattern appearing once per 1027 bits (rather than a 2-bit pattern appearing once per 66 bits) where four out of eight 3-bit sequences (rather than two out of four two-bit values as used in IEEE 802.3) match the pattern. The additional step required is to scramble the non-flag bits so that the legal sequences of these bits are not systematically mimicked in the data itself. The scrambler to be used for this purpose is the Ethernet self-synchronous scrambler using the polynomial  $G(x) = 1 + x^{39} + x^{58}$ .

At the de-mapper, invalid flag bit parity will cause both of the 513B blocks across which the flag bit parity applies to be decoded as  $8 \times 2$  66B error control blocks ("10" sync header, control block type 0x1e, followed by eight 7-bit/E/control characters).



### F.3 66B block sequence check

Bit error corruption of the position or flag continuation bits could cause 66B blocks to be de-mapped from 513B code blocks in the incorrect order. Additional checks are performed to prevent that this results in incorrect packet delineation. Since detectable corruption normally means that the proper order of 66B blocks to construct at the decoder cannot be reliably determined, if any of these checks fail, the decoder will transmit eight 66B error control blocks (sync="10", control block type=0x1e, and eight 7-bit/E/control characters).

Other checks are performed to reduce the probability that invalid data is delivered at the egress in the event that bit errors have corrupted any of the POS fields or flag continuation bits "FC".

If flag bit "F" is 1 (i.e., the 513B block includes at least one 64B/66B control block), for the rows of the table up until the first one with a flag continuation bit of zero (the last one in the block), it is verified that no two 66B control blocks or lane alignment markers within that 513B block have the same value in the POS field, and further, that the POS field values for multiple control or lane alignment rows are in ascending order, which will always be the case for a properly constructed 513B block. If this check fails, the 513B block is decoded into eight 66B error control blocks.

The next check is to ensure that the block sequence corresponds to well-formed packets, which can be done according to the state diagram in Figures F.2 and F.3. This check will determine if 66B blocks are in an order that does not correspond to well-formed packets, e.g., if during an IPG an all-data 66B block is detected without first seeing a control block representing packet start, or if during a packet a control/idle block is detected without first seeing a control block representing packet termination, control blocks have likely been misordered by corruption of either the POS bits or a flag continuation bit. Failure of this check will cause the 513B block to be decoded as eight 66B error control blocks. Note that PCS lane alignment markers are accepted in either state and do not change state as shown in Figure F.3.

The sequence of PCS lane alignment markers is also checked at the decoder. For an interface with  $p$  PCS lanes, the PCS lane alignment markers for lanes 0 to  $p-1$  will appear in a sequence, followed by  $16383 \times p$  non-lane-marker 66B blocks, followed by another group of PCS lane alignment markers. A counter is maintained at the decoder to keep track of when the next group of lane alignment markers is expected. If, in the process of decoding lane alignment markers from a 513B block, a lane alignment marker is found in a position where it is not expected, or a lane alignment marker is missing in a position where it would have been expected, the entire 513B block is decoded as eight 66B error control blocks as shown in Figures F.2, F.3, and F.4.

#### F.3.1 State diagram conventions

The body of this clause is comprised of state diagrams, including the associated definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of clause 21.5 of [IEEE 802.3]. State diagram timers follow the conventions of clause 14.2.3.2 of [IEEE 802.3]. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

#### F.3.2 State variables

##### F.3.2.1 Constants

EBLOCK\_T<65:0>

66-bit vector to be sent to the PCS containing /E/ in all the eight character locations.

Mi<65:0>

66-bit vector containing the trans-decoded alignment marker of i-th PCS lane ( $0 < i \leq p$ ). ( $p=4$  for 40GBASE-R).

### F.3.2.2 Variables

1027B\_block\_lock

Indicates the state of the block\_lock variable when the state diagram of Figure 49-12 of [IEEE 802.3] is applied to locate a 3-bit pattern appearing once per 1027 bits (rather than a 2-bit pattern appearing once per 66 bits) as described in clause F.2. Set true when sixty-four contiguous 1027-bit blocks are received with valid 3-bit patterns, set false when sixteen 1027-bit blocks with invalid 3-bit patterns are received before sixty-four valid blocks.

1027B\_high\_ber

Indicates a Boolean variable when the state diagram of Figure 49-13 of [IEEE 802.3] is applied to count invalid 3-bit sync headers of 1027-bit blocks (rather than 2-bit sync headers of 66-bit blocks) within the current 250  $\mu$ s (rather than 125  $\mu$ s). Set true when the ber\_cnt exceeds 8 (rather than 16) indicating a bit error ratio  $>10^{-4}$ .

Mseq\_violation

Indicates a Boolean variable that is set and latched in each rx513\_raw<527:0> PCS lane alignment marker cycle based on the PCS lane marker position and order. It is true if the unexpected marker sequence is detected and false if not.

POS\_violation

A Boolean variable that is set in each rx513\_raw<527:0> based on the POS field values for rx\_tcd<65:0>. It is true if the two or more have the same POS values or if they are not in ascending order, and false if their POS values are in ascending order.

reset

A Boolean variable that controls the resetting of the PCS. It is true whenever a reset is necessary including when reset is initiated from the MDIO, during power on, and when the MDIO has put the PCS into low-power mode.

Rx513\_coded<512:0>

A vector containing the input to the 512B/513B decoder.

rx513\_raw<527:0>

A vector containing eight successive 66-bit vectors (tx\_coded).

rx\_tcd<65:0>

A 66-bit vector transcode-decoded from a 513-bit block following the rules shown in Figure B.5.

seq\_violation

A Boolean variable that is set in each rx513\_raw<527:0> based on the sequence check on an rx\_tcd<65:0> stream. It is true if the unexpected sequence is detected and false if not.

### F.3.2.3 Functions

DECODE(rx513\_coded<512:0>)

Decodes the 513-bit vector returning rx513\_raw<527:0> which is sent to the client interface. The DECODE function shall decode the block as specified in Figure F.2.

R\_BLOCK\_TYPE = {C, S, T, D, E, M}

This function classifies each 66-bit rx\_tcd vector as belonging to one of the six types depending on its contents.

Values: C, S, T, and D are defined in clause 49.2.13.2.3 of [IEEE 802.3].

M: the vector contains a sync header of 10 and is recognized as a valid PCS lane alignment marker by using the state machine shown in Figure F.3.

E: the vector does not meet the criteria for any other value.

R\_TYPE(rx\_tcd<65:0>)

Returns the R\_BLOCK\_TYPE of the rx\_tcd<65:0> bit vector.

R\_TYPE\_NEXT

Prescient end of packet check function. It returns the R\_BLOCK\_TYPE of the rx\_tcd vector immediately following the current rx\_tcd vector.

### F.3.2.4 Counters

cnt

Count up to a maximum of  $p$  of the number of PCS lanes.

### F.3.3 State diagrams

The receive state machine for a series of 513-bit blocks shown in Figure F.2 determines whether the 513-bit block contains valid eight 66-bit blocks or not.

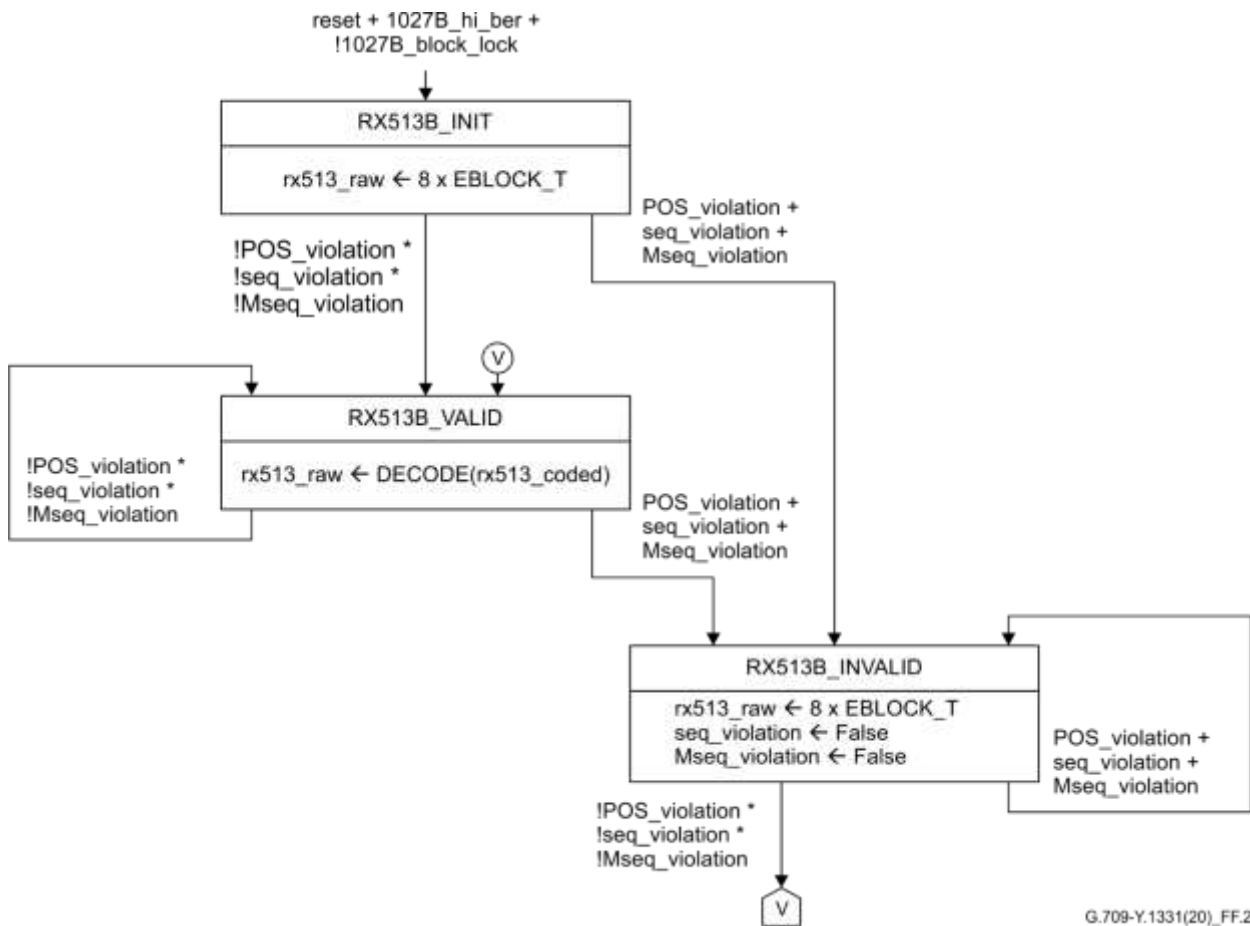
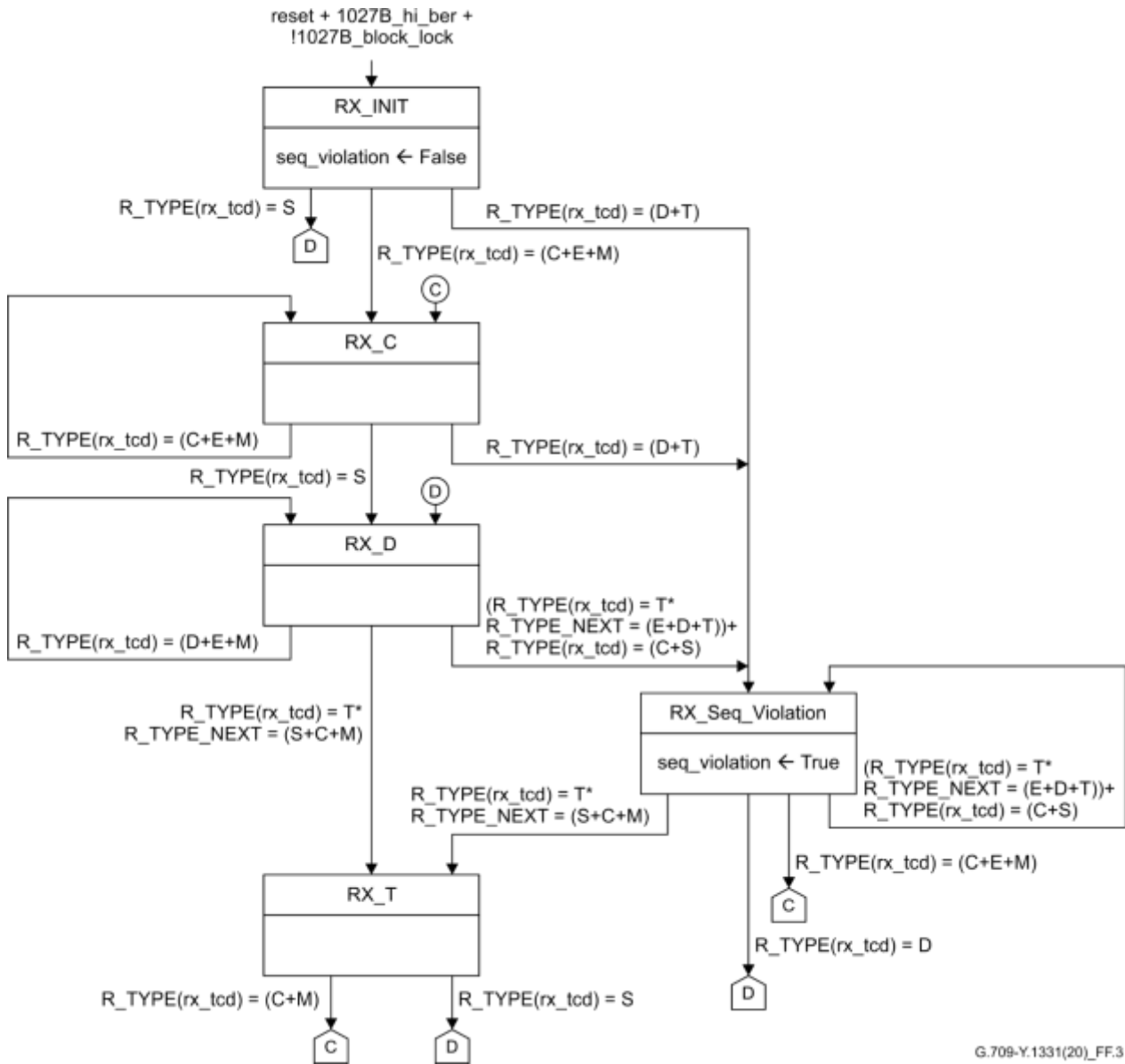


Figure F.2 – Receive state machine for the 512B/513B code blocks including lane alignment markers

The trans-decode state machine for a series of 66-bit blocks shown in Figure F.3 checks the block type sequence of recovered 66-bit blocks.

The PCS lane alignment marker state machine for a series of 66-bit blocks shown in Figure F.4 detects the alignment markers every  $p \times 16384$  blocks and checks whether the marker is in ascendant order or not.



**Figure F.3 – Trans-decode state machine for the 64B/66B code blocks including the lane alignment markers**

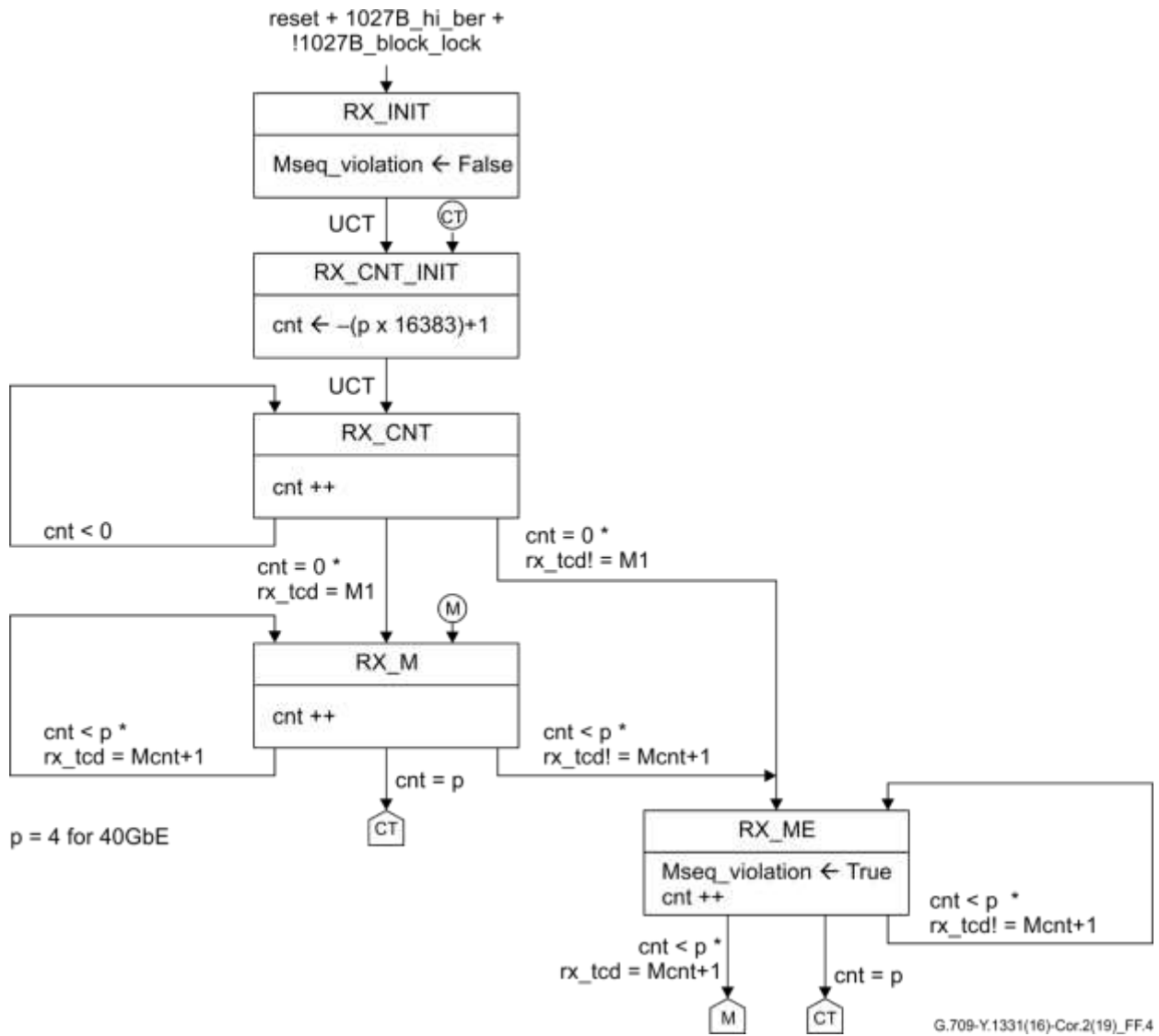


Figure F.4 – Receive state machine for the lane alignment markers

## Annex G

### Mapping ODU0 into a low latency OTU0 (OTU0LL)

(This annex forms an integral part of this Recommendation.)

#### G.1 Introduction

Within the optical transport network client signals with a bit rate up to 1.25 Gbit/s are transported within an ODU0 and the ODU0 is transported within a server ODUk and OTUk ( $k = 1,2,3,4$ ). This annex specifies a low latency 1.25G OTU0 (OTU0LL) frame format in which one ODU0 is transported which carries a client (e.g., 1G Ethernet) signal using an [ITU-T G.698.3] application code. This OTU0LL may be used at the edge of the optical transport network.

#### G.2 Optical transport unit 0 low latency (OTU0LL)

The OTU0LL conditions the ODU0 for transport over a multi-vendor optical network interface at the edge of the optical transport network. The OTU0LL frame structure, including the OTU0LL FEC is completely standardized. The optical aspects of the multi-vendor optical network interface at the edge of the optical transport network are outside the scope of this Recommendation.

NOTE 1 – Transport of the OTU0LL over the interfaces specified in this Recommendation is not supported.

NOTE 2 – An ODU0 which is transported within an OTU0LL may be passed through the OTN and terminated at the far end edge of the OTN.

##### G.2.1 OTUk frame structure

The OTU0LL frame structure is based on the ODU0 frame structure and extends it with a distributed forward error correction (FEC) as shown in Figure G.1. Sixteen times 16 columns are added to the ODU0 frame for the FEC and the reserved overhead bytes in row 1, columns 8 to 14 of the ODU0 overhead are used for an OTU0LL specific overhead, resulting in an octet-based block frame structure with four rows and 4080 columns. The MSB in each octet is bit 1, the LSB is bit 8.

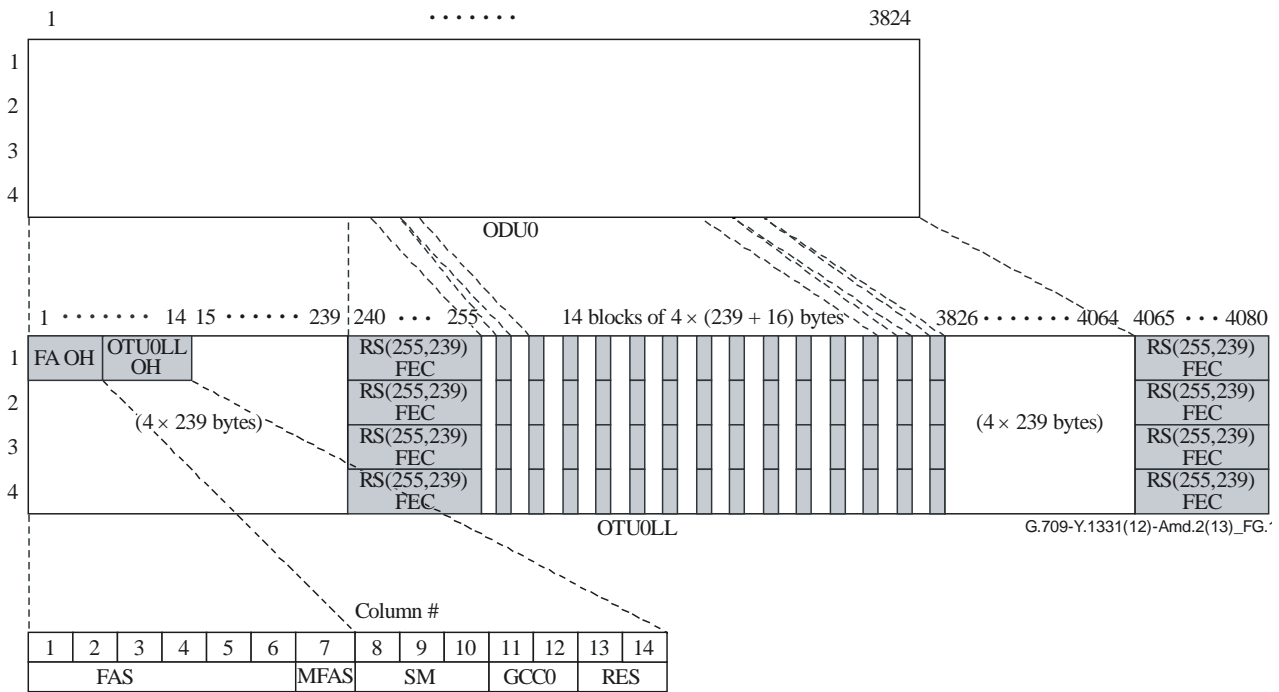
The OTU0LL overhead is the same as the OTUk overhead.

The bit rate of the OTU0LL signal is  $255/239 \times 1\,244\,160$  kbit/s ( $\sim 1\,327\,451.046$  kbit/s). The frame period of the OTU0LL signal is approximately 98.354  $\mu$ s.

The sixty-four 16-byte RS(255,239) FEC fields in the OTU0LL frame contain the Reed-Solomon RS(255,239) FEC code. Each RS(255,239) FEC is computed over the previous 239 OTU0LL bytes. Transmission of the OTU0LL FEC is mandatory.

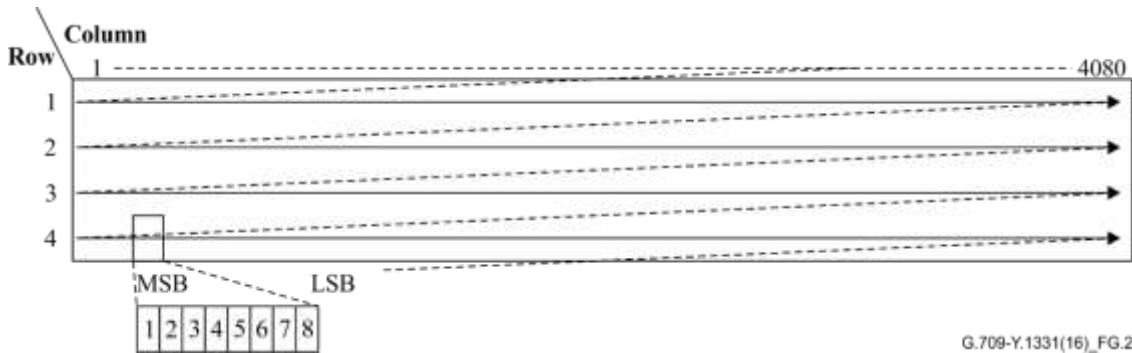
NOTE – The distribution of the RS(255,239) FEC fields over the OTU0LL frame minimizes the transfer delay introduced by the processing of this FEC and the number of codecs to compute this FEC.

The RS(255,239) FEC code shall be computed as specified in Annex A with the notion that each FEC is computed over the previous 239 OTU0LL bytes instead of over a sub-row as described in this annex for the case of an OTUk ( $k=0,1,2,3,4$ ).



**Figure G.1 – OTU0LL frame structure, overhead and ODU0 mapping**

The transmission order of the bits in the OTU0LL frame is left to right, top to bottom, and MSB to LSB (see Figure G.2).



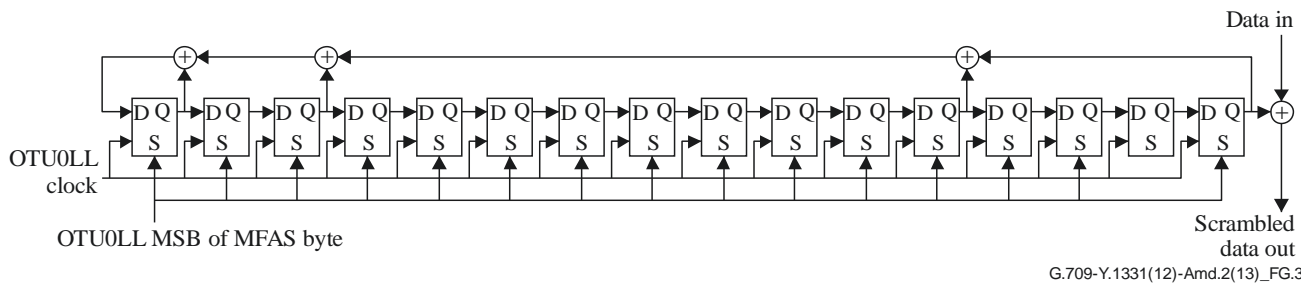
**Figure G.2 – Transmission order of the OTU0LL frame bits**

### G.2.2 Scrambling

The OTU0LL signal must have sufficient bit timing content at the NNI. A suitable bit pattern, which prevents a long sequence of "1"s or "0"s, is provided by using a scrambler.

The operation of the scrambler shall be functionally identical to that of a frame synchronous scrambler of sequence length 65535 operating at the OTU0LL rate.

The generating polynomial shall be  $1 + x + x^3 + x^{12} + x^{16}$ . Figure G.3 shows a functional diagram of the frame synchronous scrambler.



**Figure G.3 – Frame synchronous scrambler**

The scrambler shall be reset to "FFFF" (HEX) on the most significant bit of the byte following the last framing byte in the OTU0LL frame, i.e., the MSB of the MFAS byte. This bit, and all subsequent bits to be scrambled shall be added modulo 2 to the output from the  $x^{16}$  position of the scrambler. The scrambler shall run continuously throughout the complete OTU0LL frame. The framing bytes (FAS) of the OTU0LL overhead shall not be scrambled.

Scrambling is performed after FEC computation and insertion into the OTU0LL signal.



## Annex H

### OTUCn sub rates (OTUCn-M)

(This annex forms an integral part of this Recommendation.)

#### H.1 Introduction

This annex defines a subrate OTUCn, note that subrates are not defined for the OPUCn and ODUCn. Additional descriptive text, examples and applications are provided in Appendix XIII.

The OPUCn, ODUCn and OTUCn are defined in terms of  $n \times 100$  Gbit/s signals. For the OTN optical networking interface it may be advantageous to carry an OTUCn with a bit rate that is not constrained to be an integer multiple of 100 Gbit/s. This OTU is described as an OTUCn-M.

#### H.2 OTUCn-M frame format

The OTUCn-M frame is a type of OTUCn frame which contains  $n$  instances of OTUC, ODUc and OPUC overhead and  $M \times 5$  Gbit/s OPUCn tributary slots. If a particular value of  $M$  is not indicated, the frame contains  $20 \times n$  tributary slots. See Appendix XIII for examples.

An OTUCn-M framed signal can be carried over OTN optical networking interfaces. Values of  $M$  supported and the subset of the  $20n \times 5$  Gbit/s OPUCn tributary slots that are included in the OTUCn-M on such an OTN optical networking interface are vendor specific and outside the scope of this Recommendation.

The OPU tributary slots that are included in the OTUCn-M structure will have their availability bit in the OPUCn MSI overhead set to "available" (see 20.4.1.1). The OPU tributary slots which might not be carried transparently by the OTUCn-M structure will have their availability bit in the OPUCn MSI overhead set to "unavailable" (see 20.4.1.1). The data in tributary slots marked as unavailable must be set to "all 0".

During a signal fail condition of the OTUCn or ODUCn signal at the input port of the OTUCn-M section, OTUCn-AIS or ODUCn-AIS is applied at the OTUCn to OTUCn-M adaptation. Such AIS signals have their OPUCn MSI and OMFI overhead and data in their tributary slots set to "all 1". Presence of such condition can be detected via the ODUCn PM STAT field.

## **Annex I**

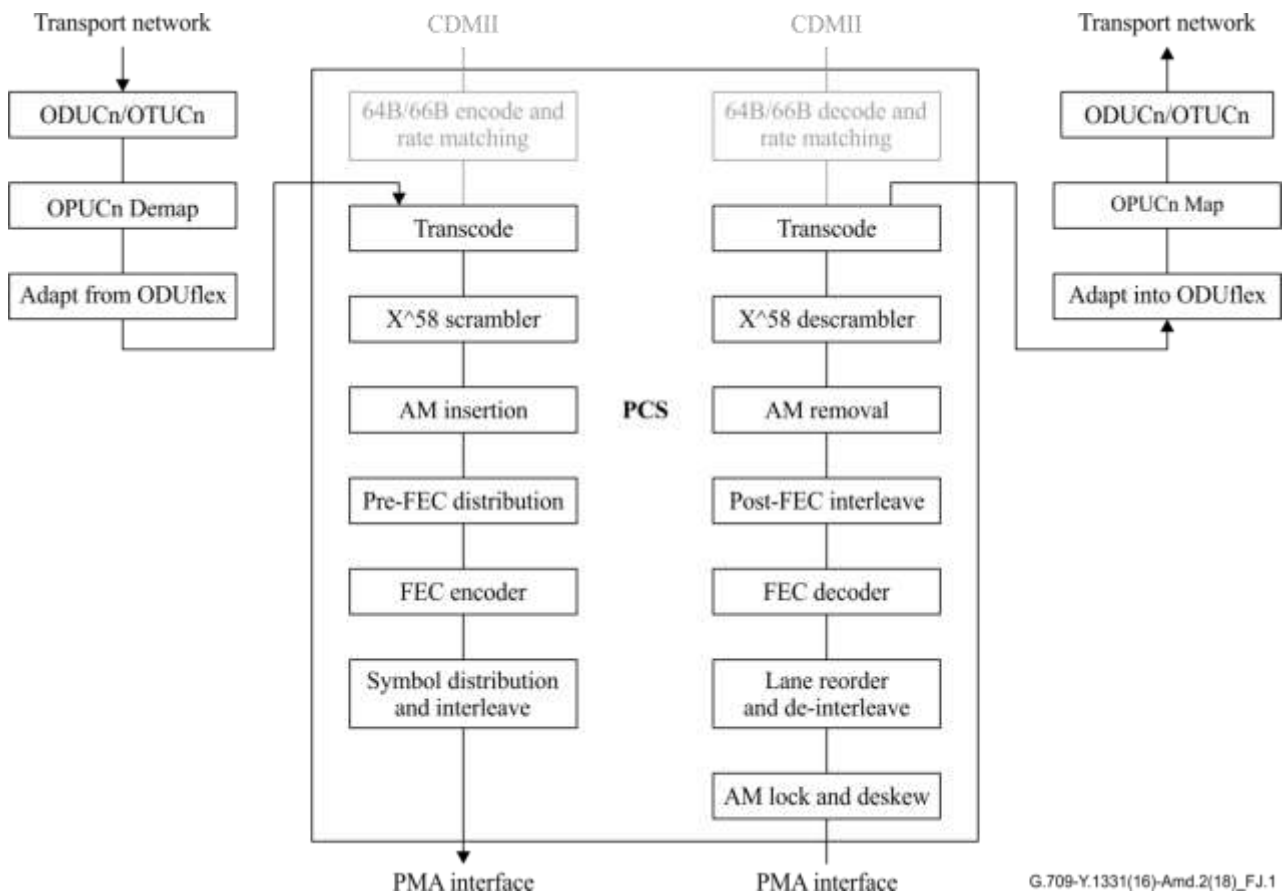
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## Annex J

### Recovery of 64B/66B encoded clients from parallel 256B/257B interfaces

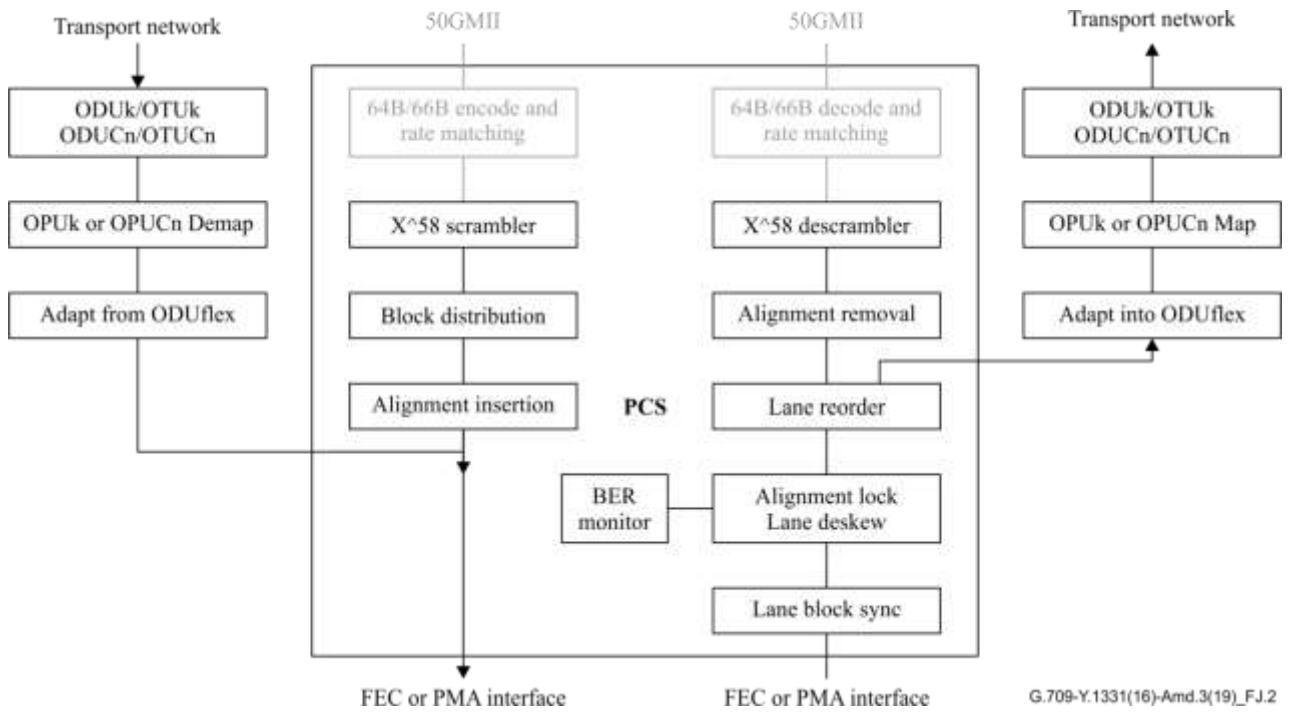
(This annex forms an integral part of this Recommendation.)

Figure J.1 illustrates the processing performed on the 200 and 400 GbE signal between the physical Ethernet interface and the point where the Ethernet signal is connected with the ODUflex to 200/400GbE adaptation function. In the receive direction (Figure J.1, right) the 200 or 400 GbE signal presented at the PMA interface passes through the AM lock and deskew, lane reorder and de-interleave, FEC decoder, post-FEC interleave, AM removal,  $x^{58}$  descrambler and 256b/257b to 64B/66B transcode processes that are specified in clause 119 of [IEEE 802.3]. The 64B/66B encoded signal is then adapted into the ODUflex and mapped into the OPUCn.



**Figure J.1 – Processing of 200/400GbE signal**

Figure J.2 illustrates the processing performed on the 50 GbE signal between the physical Ethernet interface and the point where the Ethernet signal is connected with the ODUflex to 50GbE adaptation function. In the receive direction (Figure J.2, right) the 50 GbE signal presented at the FEC or PMA interface passes through the Lane block sync, AM lock and deskew, lane reorder processes that are specified in clause 133 of [IEEE 802.3cd]. The 64B/66B encoded signal is then adapted into the ODUflex and mapped into the OPUCn or OPUCk.



G.709-Y.1331(16)-Amd.3(19)\_FJ.2

**Figure J.2 – Processing of 50GbE signal**

## Annex K

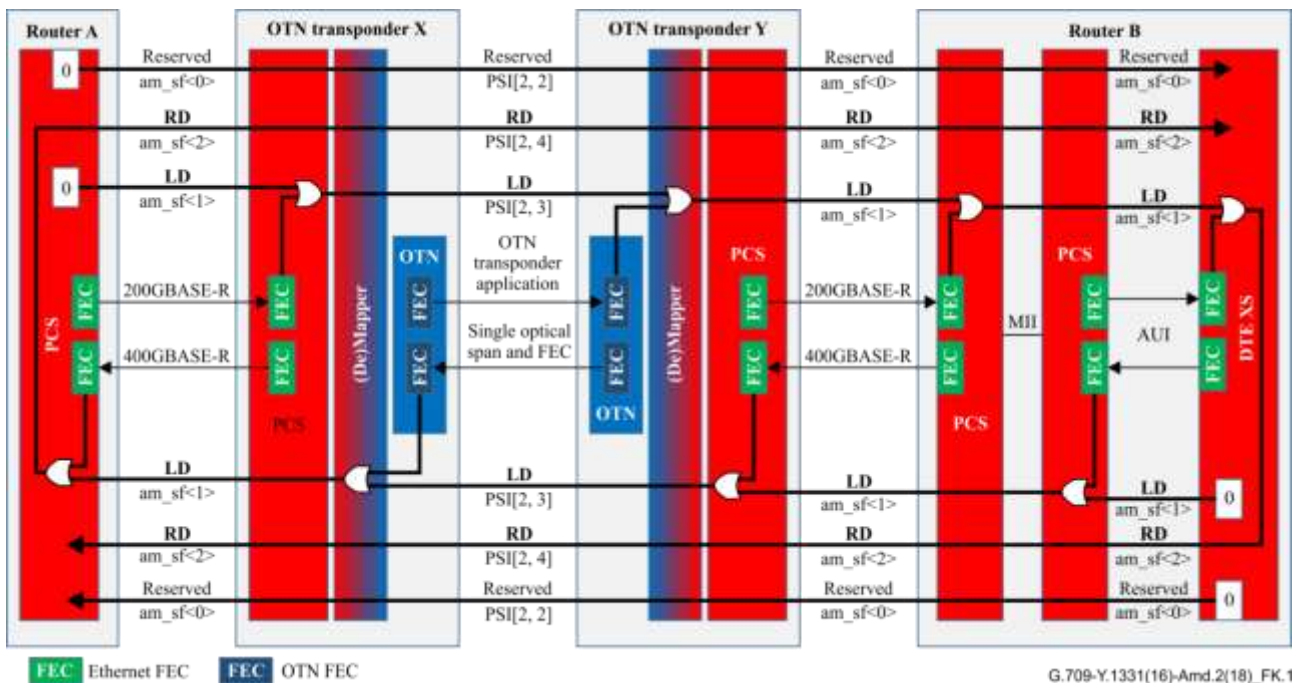
### Transporting 200GbE and 400GbE am\_sf<2:0> information through a single optical link between two Ethernet/OTN transponder entities in the OTN

(This annex forms an integral part of this Recommendation.)

#### K.1 Introduction

IP routers may support a "soft reroute" feature, which will direct IP traffic away from an optical link that experiences an increased number of FEC errors on that optical link. 200 and 400 Gbit/s Ethernet interfaces that are compliant with [IEEE 802.3] will be able to support this feature. Router vendors would like to see this feature also supported for cases in which two routers are interconnected via an OTN network. The Ethernet interfaces between router and OTN network could be equipped with (Router B in Figure K.1) or without (Router A) a clause 118 extender sublayer. In general such support is not feasible, because a 200G or 400 Gbit/s Ethernet service can be transported over more than one optical link in the OTN passing through intermediate 3R regeneration functions and ODU cross connects. Nonetheless, support for this feature is possible for the case that such service is carried over a single optical link (supported by one OTSiA trail) in the OTN, with Ethernet to OTN transponders at the two end points as illustrated in Figure K.1. For such case the Ethernet to OTN mapper and demapper processes and the OTN FEC processes are within the same transponder and the FEC status information can be exchanged between these processes.

[IEEE 802.3] has specified three bits in the AM field (am\_sf<2:0>) to carry link status information to support this feature. Bit am\_sf<2> is defined as a Remote Degrade (RD) signal, bit am\_sf<1> is defined as a Local Degrade (LD) signal and bit am\_sf<0> is reserved.



**Figure K.1 – Local/Remote degrade interworking between router and OTN transponders**

For the special case described above (illustrated in Figure K.1), the OTN transponders X and Y can forward the information in the Reserved (am\_sf<0>) and RD (am\_sf<2>) bits between ingress and egress transponder. The information in am\_sf<0> can be carried in OPUflex PSI overhead byte 2, bit 2. The status information in am\_sf<2> can be carried in OPUflex PSI overhead byte 2, bit 4. The status information in the LD (am\_sf<1>) bit can be carried after some additional processing in

OPUflex PSI overhead byte 2, bit 3 as illustrated in Figure K.1. The additional processing comprises the OR'ing of the LD status in the am\_sf<1> bit of a 200G or 400G Ethernet signal with the local Ethernet FEC degrade status in the ingress transponder (X). In the egress transponder (Y), additional processing comprises the OR'ing of the LD status in the PSI[2,3] overhead bit of the OPUflex signal with the local OTN FEC degrade status in the transponder (details defined by [ITU-T G.798]). The resulting LD status is then carried in the am\_sf<1> bit of the 200 or 400 Gbit/s Ethernet signal.

## **K.2 Client Degrade Indication (CDI) overhead**

A 3-bit Client Defect Indication is defined in bits 2, 3 and 4 of the PSI[2] byte of the payload structure identifier to indicate the client degrade status of a 200 and 400 Gbit/s Ethernet client signal which is transferred via one OTSiA trail.

OPU PSI[2,2] is used to transfer the status information present in the 200 Gbit/s or 400 Gbit/s Ethernet client's am\_sf<0> bit.

OPU PSI[2,3] is used to transfer the Local Degrade status information, which is determined by OR'ing the value present in the 200 or 400 Gbit/s Ethernet client's am\_sf<1> bit with the 200 or 400 Gbit/s Ethernet FEC Degrade status as specified in [IEEE 802.3].

OPU PSI[2,4] is used to transfer the Remote Degrade status information present in the 200 Gbit/s or 400 Gbit/s Ethernet client's am\_sf<2> bit.

## Annex L

### OTU25u and OTU50u interfaces

(This annex forms an integral part of this Recommendation.)

#### L.1 Introduction

In network applications that do not require support of all client signals, the OTU25 and OTU50 interfaces with FEC as specified in [ITU-T G.709.4] may be operated at a 5.2% lower rate that is within the  $\pm 100$  ppm clock tolerance of the associated Ethernet 25GBASE-R and 50GBASE-R with RS-FEC rates. The bit rates of ~~such~~ the corresponding "under-clocked" OTU25u and OTU50u are specified in this annex. All other OTU25 and OTU50 interface related specifications apply for the OTU25u and OTU50u.

Figure L.1 shows the relationship between various information structure elements and illustrates the multiplexing structure and mappings for the OTU25u and OTU50u. Figure L.1 shows that an ODU<sub>k</sub> ( $k = 0, 1, 2, 2e, \text{flex}$ ) signal is mapped into an OPU25u and an ODU<sub>k</sub> ( $k = 0, 1, 2, 2e, 3, \text{flex}$ ) signal is mapped into an OPU50u. This OPU25u or OPU50u signal is mapped into the associated ODU25u or ODU50u. This ODU25u or ODU50u signal is mapped into the associated OTU25u or OTU50u signal.

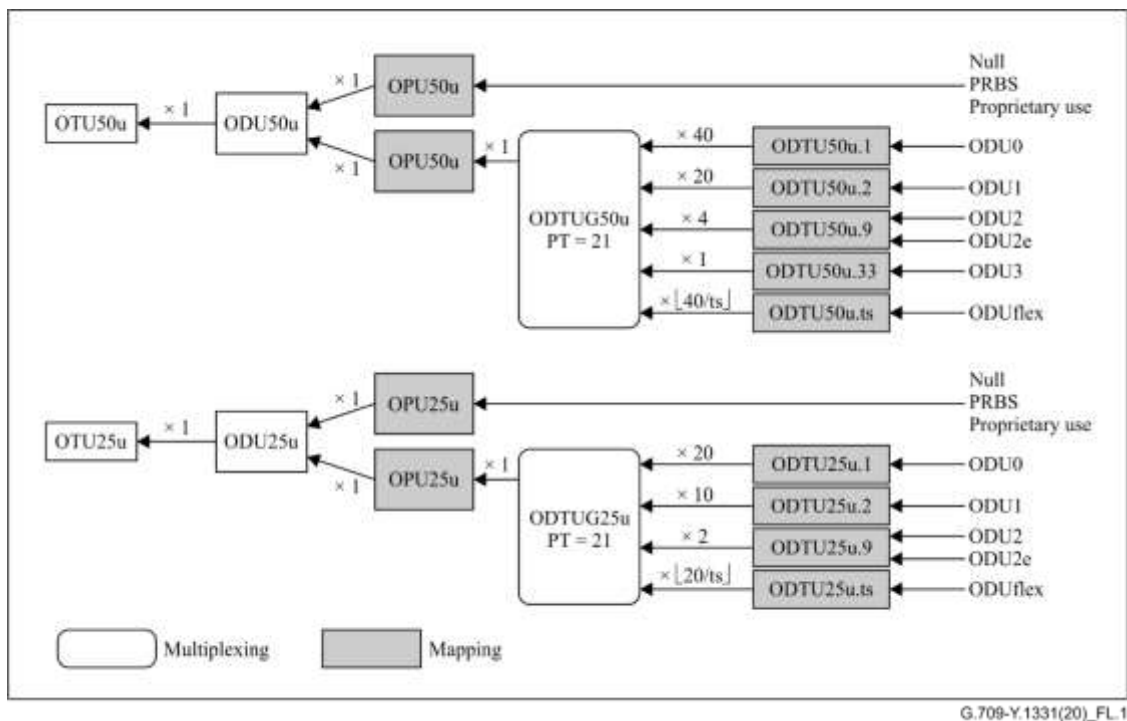


Figure L.1 – OTN multiplexing and mapping structures for OTU25u and OTU50u

#### L.2 Bit rates

The bit rates and tolerance of the OTU25u and OTU50u signals are defined in Table L.1.

The bit rates and tolerance of the ODU25u and ODU50u signals are defined in Table L.2.

The bit rates and tolerance of the OPU25u and OPU50u payload are defined in Table L.3.

The OTU25u, OTU50u, ODU25u, ODU50u, OPU25u and OPU50u frame periods are defined in Table L.4.

The 1.25G tributary slot related OPU25u and OPU50u multiframe periods are defined in Table L.5.

The ODTU payload area bandwidths are defined in Table L.6.

The number of OPU25u and OPU50u tributary slots required by a client ODU are summarized in Table L.7. Note that the value of n for ODUflex(GFP,n,2) is not restricted to the range  $1 \leq n \leq 8$  as specified in Table 7-8.

The bit rates and tolerance of the OTU25u/ODU25u and OTU50u/ODU25u GCC signals are defined in Table L.8.

**Table L.1 – OTU types and bit rates**

OTU type	OTU nominal bit rate	OTU bit-rate tolerance
OTU25u	$2937/2912 \times 24\,883\,200$ kbit/s	±20 ppm
OTU50u	$2937/2912 \times 49\,766\,400$ kbit/s	
NOTE 1 – The nominal OTU rates are approximately: 25 096 826.374 kbit/s (OTU25u), 50 193 652.747 kbit/s (OTU50u).		
NOTE 2 – The OTU25u and OTU50u signal bit rates do not include a FEC overhead area.		
NOTE 3 – The OTU25u bit rate can be based on the OTU25u-RS bit rate as follows: $514/528 \times 41118/41120 \times$ OTU25u-RS bit rate = $514/528 \times 41118/41120 \times 660/637 \times 24\,883\,200$ kbit/s.		
NOTE 4 – The OTU50u bit rate can be based on the OTU50u-RS bit rate as follows: $514/544 \times 41118/41120 \times$ OTU50u-RS bit rate = $514/544 \times 41118/41120 \times 680/637 \times 49\,766\,400$ kbit/s.		

**Table L.2 – ODU types and bit rates**

ODU type	ODU nominal bit rate	ODU bit-rate tolerance
ODU25u	$2937/2912 \times 24\,883\,200$ kbit/s	±20 ppm
ODU50u	$2937/2912 \times 49\,766\,400$ kbit/s	
NOTE – The nominal ODU rates are approximately: 25 096 826.374 kbit/s (ODU25u), 50 193 652.747 kbit/s (ODU50u).		

**Table L.3 – OPU types and bit rates**

OPU type	OPU payload nominal bit rate	OPU payload bit-rate tolerance
OPU25u	$49929/49712 \times 24\,883\,200$ kbit/s	±20 ppm
OPU50u	$49929/49712 \times 49\,766\,400$ kbit/s	
NOTE 1 – The nominal OPU payload rates are approximately: 24 991 818.732 kbit/s (OPU25u Payload), 49 983 637.464 kbit/s (OPU50u Payload).		
NOTE 2 – The OPU25u bit rate can be based on the OTU25u-RS bit rate as follows: $238/239 \times 514/528 \times 41118/41120 \times$ OTU25u-RS bit rate = $238/239 \times 514/528 \times 41118/41120 \times 660/637 \times 24\,883\,200$ kbit/s.		
NOTE 3 – The OPU50u bit rate can be based on the OTU50u-RS bit rate as follows: $238/239 \times 514/544 \times 41118/41120 \times$ OTU50u-RS bit rate = $238/239 \times 514/544 \times 41118/41120 \times 680/637 \times 49\,766\,400$ kbit/s.		



**Table L.4 – OTU/ODU/OPU frame periods**

<b>OTU/ODU/OPU type</b>	<b>Period (Note)</b>
OTU25u/ODU25u/OPU25u	4.876 $\mu$ s
OTU50u/ODU50u/OPU50u	2.483 $\mu$ s
NOTE – The period is an approximated value, rounded to 3 decimal places.	

**Table L.5 – OPUk multiframe periods for 1.25G tributary slots**

<b>OPU type</b>	<b>1.25G tributary slot multiframe period (Note)</b>
OPU25u	97.517 $\mu$ s
OPU50u	97.517 $\mu$ s
NOTE – The period is an approximated value, rounded to 3 decimal places.	

**Table L.6 – ODTU payload bandwidth (kbit/s)**

<b>ODTU type</b>	<b>ODTU payload nominal bandwidth</b>		<b>ODTU payload bit-rate tolerance</b>
<b>ODTU25u.ts</b>	ts $\times$ 190.4/3824 $\times$ ODU25u bit rate		$\pm$ 20 ppm
<b>ODTU50u.ts</b>	ts $\times$ 95.2/3824 $\times$ ODU50u bit rate		
	<b>Minimum</b>	<b>Nominal</b>	<b>Maximum</b>
<b>ODTU25u.ts, ODTU50u.ts</b>	ts $\times$ 1 249 565.945	ts $\times$ 1 249 590.937	ts $\times$ 1 249 615.928
NOTE – The bandwidth is an approximated value, rounded to 3 decimal places.			

**Table L.7 – Number of tributary slots required for ODU<sub>j</sub> into OPU25u and OPU50u**

	# 1.25G tributary slots	
	OPU25u	OPU50u
ODU0	1	1
ODU1	2	2
ODU2	9	9
ODU2e	9	9
ODU3	–	33
ODUflex(CBR)		
– ODUflex(25GBase-R)	–	21
– ODUflex(50GBase-R)	–	–
ODUflex(GFP)	Note	Note
– ODUflex(GFP,8,2) for 10GBASE-R	8	8
– ODUflex(GFP,20,2) for 25GBASE-R	20	20
– ODUflex(GFP,40,2) for 50GBASE-R	40	40
– ODUflex(GFP,n,2), $1 \leq n \leq 20$ (OPU25u) and $1 \leq n \leq 40$ (OPU50u)	n	n
– ODUflex(GFP,n,3), $9 \leq n \leq 19$ (OPU25u) and $9 \leq n \leq 32$ (OPU50u)	n+1	n+1
– ODUflex(GFP,n,4), $33 \leq n \leq 38$ (OPU50u)	–	n+2
ODUflex(IMP)	Note	Note
– ODUflex(IMP,s)	Note	Note

NOTE – Refer to equations 19-1a and 19-1b in clauses 19.6.

**Table L.8 – GCC types and bit rates (kbit/s)**

OTU/ODU type	Nominal bit rate GCC0	Nominal bit rate GCC <sub>i</sub> (i = 1,2)	Nominal bit rate GCC1+GCC2	Bit-rate tolerance
OTU25u/ODU25u	3 281.489	3 281.489	6 562.978	±20 ppm
OTU50u/ODU50u	6 562.978	6 562.978	13 125.955	

NOTE – The bandwidth is an approximated value, rounded to 3 decimal places.

## Appendix I

### **Range of stuff ratios for asynchronous mappings of CBR2G5, CBR10G, and CBR40G clients with $\pm 20$ ppm bit-rate tolerance into OPUk, and for asynchronous multiplexing of ODUj into ODUk ( $k > j$ )**

(This appendix does not form an integral part of this Recommendation.)

Clause 17.2 describes asynchronous and bit-synchronous mappings of CBR2G5, CBR10G, and CBR40G clients with  $\pm 20$  ppm bit-rate tolerance into ODU1, 2, and 3, respectively. Clause 19 describes asynchronous mapping (multiplexing) of ODUj into ODUk ( $k > j$ ). For asynchronous CBR client mappings, any frequency difference between the client and local OPUk server clocks is accommodated by the +1/0/-1 justification scheme. For asynchronous multiplexing of ODUj into ODUk ( $k > j$ ), any frequency difference between the client ODUj and local OPUk server clocks is accommodated by the +2/+1/0/-1 justification scheme. The OPUk payload, ODUk, and OTUk bit rates and tolerances are given in clause 7.3. The ODU1, ODU2, and ODU3 rates are 239/238, 239/237, and 239/236 times 2 488 320 kbit/s, 9 953 280 kbit/s, and 39 813 120 kbit/s, respectively. The ODUk bit-rate tolerances are  $\pm 20$  ppm. This appendix shows that each justification scheme can accommodate these bit rates and tolerances for the respective mappings, and also derives the range of justification (stuff) ratio for each mapping.

The +1/0/-1 mapping in clause 17.2 provides for one positive justification opportunity (PJO) and one negative justification opportunity (NJO) in each ODUk frame. The +2/+1/0/-1 mapping in clause 19 provides for 2 PJOs and one NJO in each ODUk frame. For the case of ODU multiplexing (i.e., the latter case), the ODUj being mapped will get only a fraction of the full payload capacity of the ODUk. There can be, in general, a number of fixed stuff bytes per ODUj or CBR client. Note that in both mapping cases, there is one stuff opportunity in every ODUk frame. For mapping of a CBR client into ODUk, the CBR client is allowed to use all the stuff opportunities (because only one CBR client signal is mapped into an ODUk). However, for mapping ODUj into ODUk ( $k > j$ ), the ODUj can only use 1/2 (ODU0 into ODU1), 1/4 (ODU1 into ODU2 or ODU2 into ODU3) or 1/16 (ODU1 into ODU3) of the stuff opportunities. The other stuff opportunities are needed for the other clients being multiplexed into the ODUk.

Traditionally, the justification ratio (stuff ratio) for purely positive justification schemes is defined as the long-run average fraction of justification opportunities for which a justification is done (i.e., for a very large number of frames, the ratio of the number of justifications to the total number of justification opportunities). In the +1/0/-1 scheme, positive and negative justifications must be distinguished. This is done by using different algebraic signs for positive and negative justifications. With this convention, the justification ratio can vary at most (for sufficiently large frequency offsets) from -1 to +1 (in contrast to a purely positive justification scheme, where the justification ratio can vary at most from 0 to 1). In the case of ODUk multiplexing, the justification ratio is defined relative to the stuff opportunities available for the client in question. Then, the justification ratio can vary (for sufficiently large frequency offsets) from -1 to +2. (If the justification ratio were defined relative to all the stuff opportunities for all the clients, the range would be -1/2 to +1 for multiplexing ODU0 into ODU1, -1/4 to +1/2 for multiplexing ODU1 into ODU2 and ODU2 into ODU3, and -1/16 to +1/8 for multiplexing ODU1 into ODU3.)

Let  $\alpha$  represent the justification ratio ( $-1 \leq \alpha \leq 1$  for CBR client into ODUk mapping;  $-2 \leq \alpha \leq 1$  for ODUj into ODUk mapping ( $k > j$ )), and use the further convention that positive  $\alpha$  will correspond to negative justification and negative  $\alpha$  to positive justification (the reason for this convention is explained below).

Define the following notation (the index  $j$  refers to the possible ODU $_j$  client being mapped, and the index  $k$  refers to the ODU $_k$  server layer into which the ODU $_j$  or CBR client is mapped):

- $N$  = number of fixed stuff bytes in the OPU $_k$  payload area associated with the client in question (note that this is not the total number of fixed stuff bytes if multiple clients are being multiplexed)
- $S$  = nominal STM-N or ODU $_j$  client rate (bytes/s)
- $T$  = nominal ODU $_k$  frame period(s)
- $y_c$  = client frequency offset (fraction)
- $y_s$  = server frequency offset (fraction)
- $p$  = fraction of OPU $_k$  payload area available to this client
- $N_f$  = average number of client bytes mapped into an ODU $_k$  frame, for the particular frequency offsets (averaged over a large number of frames)

Then  $N_f$  is given by:

$$N_f = ST \frac{1 + y_c}{1 + y_s} \quad (\text{I-1})$$

For frequency offsets small compared to 1, this may be approximated:

$$N_f = ST(1 + y_c - y_s) \equiv ST\beta \quad (\text{I-2})$$

The quantity  $\beta - 1$  is the net frequency offset due to client and server frequency offset.

Now, the average number of client bytes mapped into an ODU $_k$  frame is also equal to the total number of bytes in the payload area available to this client (which is  $(4)(3808)p = 15232p$ ), minus the number of fixed stuff bytes for this client ( $N$ ), plus the average number of bytes stuffed for this client over a very large number of frames. The latter is equal to the justification ratio  $\alpha$  multiplied by the fraction of frames  $p$  corresponding to justification opportunities for this client. Combining this with equation I-1 produces:

$$ST\beta + \alpha p + 15232p - N \quad (\text{I-3})$$

In equation I-3, a positive  $\alpha$  corresponds to more client bytes mapped into the ODU $_k$ , on average. As indicated above, this corresponds to negative justification. This sign convention is used so that  $\alpha$  enters in equation I-3 with a positive sign (for convenience).

Equation I-3 is the main result. For mapping STM-N (CBR clients) into ODU $_k$ , the quantity  $p$  is 1.

The range of stuff ratio may now be determined for mapping STM-N or ODU $_j$  clients into ODU $_k$ , using equation I-3. In what follows, let  $R_{16}$  be the STM-16 rate, i.e., 2.48832 Gbit/s =  $3.1104 \times 10^8$  bytes/s.

### Asynchronous mapping of CBR2G5 (2 488 320 kbit/s) signal into ODU1

The nominal client rate is  $S = R_{16}$ . The nominal ODU1 rate is  $(239/238)S$  (see clause 7.3). But the nominal ODU1 rate is also equal to  $(4)(3824)/T$ . Then:

$$ST = (4)(3824) \frac{238}{239} = 15232 \quad (\text{I-4})$$

Inserting this into equation I-3, and using the fact that  $N = 0$  (no fixed stuff bytes) for this mapping produces:

$$\alpha = 15232(\beta - 1) \quad (\text{I-5})$$

Since the ODUk and client frequency tolerances are each  $\pm 20$  ppm,  $\beta$  ranges from 0.99996 to 1.00004. Using this in equation I-5 gives as the range of  $\alpha$ :

$$-0.60928 \leq \alpha \leq +0.60928 \quad (\text{I-6})$$

### Asynchronous mapping of CBR10G (9 953 280 kbit/s) signal into ODU2

The nominal client rate is  $S = 4R_{16}$ . The nominal ODU2 rate is  $(239/237)S$  (see clause 7.3). But the nominal ODU2 rate is also equal to  $(4)(3824)/T$ . Then:

$$ST = (4)(3824) \frac{237}{239} = 15168 \quad (\text{I-7})$$

Inserting this into equation I-3, and using the fact that  $N = 64$  (number of fixed stuff bytes) for this mapping produces:

$$\alpha = 15168\beta + 64 - 15232 = 15168(\beta - 1) \quad (\text{I-8})$$

As before, the ODUk and client frequency tolerances are  $\pm 20$  ppm, and  $\beta$  ranges from 0.99996 to 1.00004. Using this in equation I-8 gives as the range of  $\alpha$ :

$$-0.60672 \leq \alpha \leq +0.60672 \quad (\text{I-9})$$

### Asynchronous mapping of CBR40G (39 813 120 kbit/s) signal into ODU3

The nominal client rate is  $S = 16R_{16}$ . The nominal ODU3 rate is  $(239/236)S$  (see clause 7.3). But the nominal ODU3 rate is also equal to  $(4)(3824)/T$ . Then:

$$ST = (4)(3824) \frac{236}{239} = 15104 \quad (\text{I-10})$$

Inserting this into equation I-3, and using the fact that  $N = 128$  (number of fixed stuff bytes) for this mapping produces:

$$\alpha = 15104\beta + 128 - 15232 = 15104(\beta - 1) \quad (\text{I-11})$$

As before, the ODUk and client frequency tolerances are  $\pm 20$  ppm, and  $\beta$  ranges from 0.99996 to 1.00004. Using this in equation I-11 gives as the range of  $\alpha$ :

$$-0.60416 \leq \alpha \leq +0.60416 \quad (\text{I-12})$$

### ODU1 into ODU2 multiplexing

The ODU1 nominal client rate is (see clause 7.3):

$$S = \frac{239}{238} R_{16} \quad (\text{I-13})$$

The ODU2 nominal frame time is:

$$T = \frac{(3824)(4)}{\frac{239}{237}(4R_{16})} \quad (\text{I-14})$$

The fraction  $p$  is 0.25. Inserting into equation I-3 produces:

$$\frac{239}{238} R_{16} \frac{(3824)(4)}{\frac{239}{237}(4R_{16})} \beta = \frac{\alpha}{4} + 3808 - N \quad (\text{I-15})$$

Simplifying and solving for  $\alpha$  produces:

$$\alpha = \frac{237}{238}(15296)\beta + 4N - 15232 \quad (\text{I-16})$$

Now let  $\beta = 1 + y$ , where  $y$  is the net frequency offset (and is very nearly equal to  $y_c - y_s$  for client and server frequency offset small compared to 1). Then:

$$\begin{aligned} \alpha &= \frac{237}{238}(15296) - 15232 + 4N + \frac{237}{238}(15296)y \\ &= 4N - 0.2689076 + 15231.731092y \end{aligned} \quad (\text{I-17})$$

The number of fixed stuff bytes  $N$  is zero, as given in clause 19.5.1. The client and mapper frequency offsets are in the range  $\pm 20$  ppm, as given in clause 7.3. Then, the net frequency offset  $y$  is in the range  $\pm 40$  ppm. Inserting these values into equation I-17 gives for the range for  $\alpha$ :

$$\begin{aligned} \alpha &= 0.340362 && \text{for } y = +40 \text{ ppm} \\ \alpha &= -0.268908 && \text{for } y = 0 \text{ ppm} \\ \alpha &= -0.878177 && \text{for } y = -40 \text{ ppm} \end{aligned} \quad (\text{I-18})$$

In addition, stuff ratios of  $-2$  and  $+1$  are obtained for frequency offsets of  $-113.65$  ppm and  $83.30$  ppm, respectively. The range of frequency offset that can be accommodated is approximately  $197$  ppm. This is  $50\%$  larger than the range that can be accommodated by a  $+1/0/-1$  justification scheme (see above), and is due to the additional positive stuff byte.

### ODU2 into ODU3 multiplexing

The ODU2 nominal client rate is (see clause 7.3):

$$S = \frac{239}{237}(4R_{16}) \quad (\text{I-19})$$

The ODU3 nominal frame time is:

$$T = \frac{(3824)(4)}{\frac{239}{236}(16R_{16})} \quad (\text{I-20})$$

The fraction  $p$  is  $0.25$ . Inserting into equation I-3 produces:

$$\frac{239}{237}4R_{16} \frac{(3824)(4)}{\frac{239}{236}(16R_{16})} \beta = \frac{\alpha}{4} + 3808 - N \quad (\text{I-21})$$

Simplifying and solving for  $\alpha$  produces:

$$\alpha = \frac{236}{237}(15296)\beta + 4N - 15232 \quad (\text{I-22})$$

As before, let  $\beta = 1 + y$ , where  $y$  is the net frequency offset (and is very nearly equal to  $y_c - y_s$  for client and server frequency offset small compared to 1). Then:

$$\begin{aligned} \alpha &= \frac{236}{237}(15296) - 15232 + 4N + \frac{236}{237}(15296)y \\ &= 4N - 0.5400844 + 15231.459916y \end{aligned} \quad (\text{I-23})$$

The number of fixed stuff bytes  $N$  is zero, as given in clause 19.5.3. The client and mapper frequency offsets are in the range  $\pm 20$  ppm, as given in clause 7.3. Then, the net frequency offset  $y$  is in the range  $\pm 40$  ppm. Inserting these values into equation I-23 gives for the range for  $\alpha$ :

$$\begin{aligned} \alpha &= 0.0691740 && \text{for } y = +40 \text{ ppm} \\ \alpha &= -0.5400844 && \text{for } y = 0 \text{ ppm} \\ \alpha &= -1.149343 && \text{for } y = -40 \text{ ppm} \end{aligned} \quad (\text{I-24})$$

In addition, stuff ratios of  $-2$  and  $+1$  are obtained for frequency offsets of  $-95.85$  ppm and  $101.11$  ppm, respectively. As above, the range of frequency offset that can be accommodated is approximately 197 ppm, which is 50% larger than the range that can be accommodated by a  $+1/0/-1$  justification scheme (see above) due to the additional positive stuff byte.

### ODU1 into ODU3 multiplexing

The ODU1 nominal client rate is (see clause 7.3):

$$S = \frac{239}{238} R_{16} \quad (\text{I-25})$$

The ODU3 nominal frame time is:

$$T = \frac{(3824)(4)}{\frac{239}{236} (16R_{16})} \quad (\text{I-26})$$

The fraction  $p$  is 0.0625. Inserting into equation I-3 produces:

$$\frac{239}{238} R_{16} \frac{(3824)(4)}{\frac{239}{236} (16R_{16})} \beta = \frac{\alpha}{16} + 952 - N \quad (\text{I-27})$$

Simplifying and solving for  $\alpha$  produces:

$$\alpha = \frac{236}{238} (15296)\beta + 16N - 15232 \quad (\text{I-28})$$

As before, let  $\beta = 1 + y$ , where  $y$  is the net frequency offset (and is very nearly equal to  $y_c - y_s$  for client and server frequency offset small compared to 1). Then:

$$\begin{aligned} \alpha &= \frac{236}{238} (15296) - 15232 + 16N + \frac{236}{238} (15296)y \\ &= 16N - 64.5378151 + 15167.462185y \end{aligned} \quad (\text{I-29})$$

The total number of fixed stuff bytes in the ODU3 payload is 64, as given in clause 19.5.2; the number for one ODU1 client,  $N$ , is therefore 4. The client and mapper frequency offsets are in the range  $\pm 20$  ppm, as given in clause 7.3. Then, the net frequency offset  $y$  is in the range  $\pm 40$  ppm. Inserting these values into equation I-29 gives for the range for  $\alpha$ :

$$\begin{aligned} \alpha &= 0.0688834 && \text{for } y = +40 \text{ ppm} \\ \alpha &= -0.5378151 && \text{for } y = 0 \text{ ppm} \\ \alpha &= -1.144514 && \text{for } y = -40 \text{ ppm} \end{aligned} \quad (\text{I-30})$$

In addition, stuff ratios of  $-2$  and  $+1$  are obtained for frequency offsets of  $-96.40$  ppm and  $101.39$  ppm, respectively. As above, the range of frequency offset that can be accommodated is approximately  $197$  ppm, which is  $50\%$  larger than the range that can be accommodated by a  $+1/0/-1$  justification scheme (see above) due to the additional positive stuff byte.

### ODU0 into ODU1 multiplexing

The ODU0 nominal client rate is (see clause 7.3):

$$S = \frac{1}{2}(R_{16}) \quad (\text{I-31})$$

The ODU1 nominal frame time is:

$$T = \frac{(3824)(4)}{\frac{239}{238}(R_{16})} \quad (\text{I-32})$$

The fraction  $p$  is  $0.5$ . Inserting into equation I-3 produces:

$$\frac{1}{2}R_{16} \frac{(3824)(4)}{\frac{239}{238}(R_{16})} \beta = \frac{\alpha}{2} + 7616 - N \quad (\text{I-33})$$

Simplifying and solving for  $\alpha$  produces:

$$\alpha = \frac{238}{239}(15296)\beta + 2N - 15232 \quad (\text{I-34})$$

As before, let  $\beta = 1 + y$ , where  $y$  is the net frequency offset (and is very nearly equal to  $y_c - y_s$  for client and server frequency offset small compared to  $1$ ). Then:

$$\begin{aligned} \alpha &= \frac{238}{239}(15296) - 15232 + 2N + \frac{238}{239}(15296)y \\ &= 2N + 15232y \end{aligned} \quad (\text{I-35})$$

The total number of fixed stuff bytes  $N$  is zero, as given in clause 19.5.4. The client and mapper frequency offsets are in the range  $\pm 20$  ppm, as given in clause 7.3. Then, the net frequency offset  $y$  is in the range  $\pm 40$  ppm. Inserting these values into equation I-35 gives for the range for  $\alpha$ :

$$\begin{aligned} \alpha &= 0.6092800 && \text{for } y = +40 \text{ ppm} \\ \alpha &= 0.0000000 && \text{for } y = 0 \text{ ppm} \\ \alpha &= -0.6092800 && \text{for } y = -40 \text{ ppm} \end{aligned} \quad (\text{I-36})$$

In addition, stuff ratios of  $-2$  and  $+1$  are obtained for frequency offsets of  $-130$  ppm and  $65$  ppm, respectively. As above, the range of frequency offset that can be accommodated is approximately  $195$  ppm.



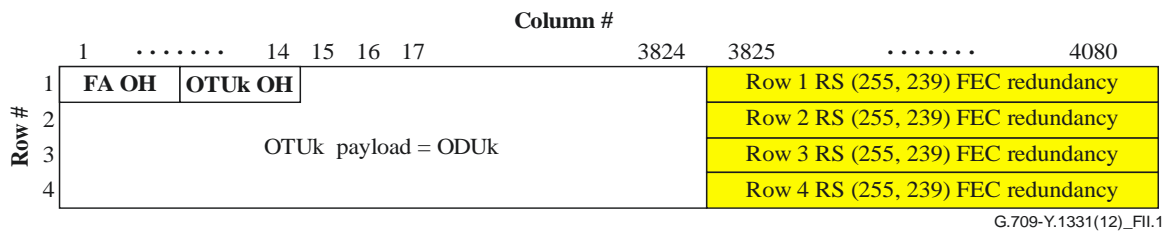
## Appendix II

### Examples of functionally standardized OTU frame structures

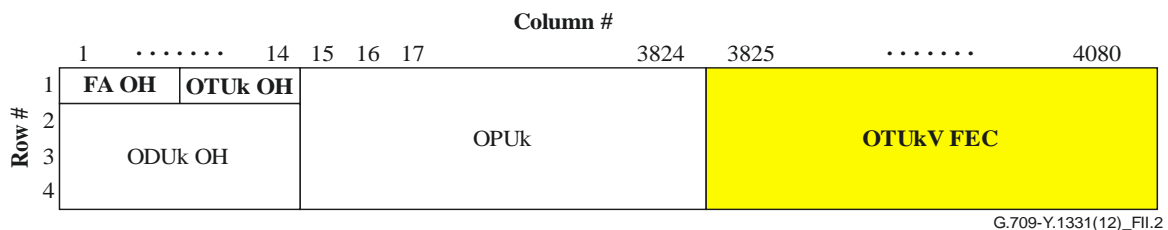
(This appendix does not form an integral part of this Recommendation.)

This appendix provides examples of functionally standardized OTU frame structures. These examples are for illustrative purposes and by no means imply a definition of such structures. The completely standardized OTUk frame structure as defined in this Recommendation is shown in Figure II.1. Functionally standardized OTUkV frame structures will be needed to support, e.g., alternative FEC. Examples of OTUkV frame structures are:

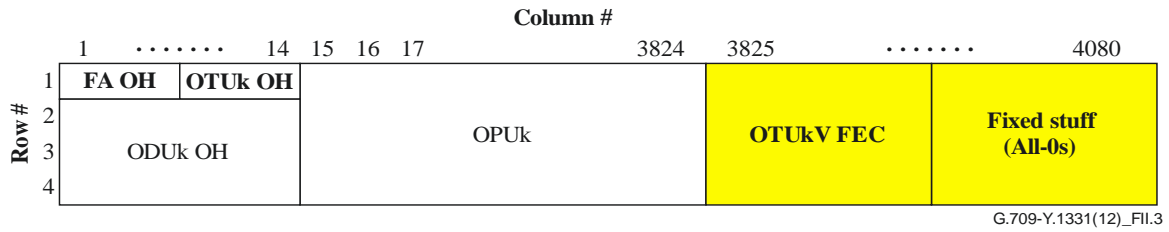
- OTUkV with the same overhead byte allocation as the OTUk, but use of an alternative FEC as shown in Figure II.2;
- OTUkV with the same overhead byte allocation as the OTUk, but use of a smaller, alternative FEC code and the remainder of the OTUkV FEC overhead area filled with fixed stuff as shown in Figure II.3;
- OTUkV with a larger FEC overhead byte allocation as the OTUk, and use of an alternative FEC as shown in Figure II.4;
- OTUkV with no overhead byte allocation for FEC as shown in Figure II.5;
- OTUkV with a different frame structure than the OTUk frame structure, supporting a different OTU overhead (OTUkV overhead and OTUkV FEC) as shown in Figure II.6;
- OTUkV with a different frame structure than the OTUk frame structure, supporting a different OTU overhead (OTUkV overhead) and with no overhead byte allocation for FEC as shown in Figure II.7.



**Figure II.1 – OTUk (with RS(255,239) FEC)**

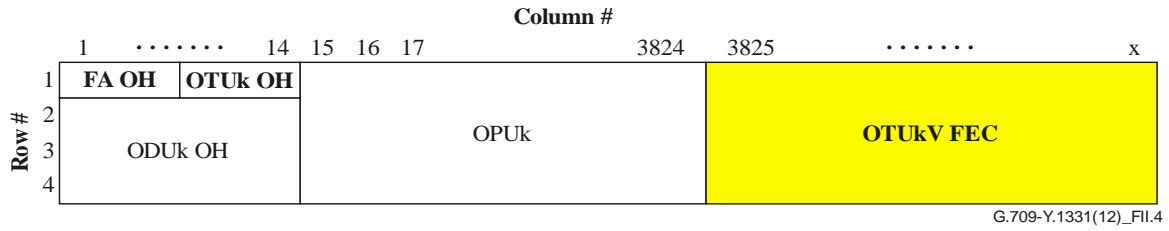


**Figure II.2 – OTUk with alternative OTUkV FEC (OTUk-v)**



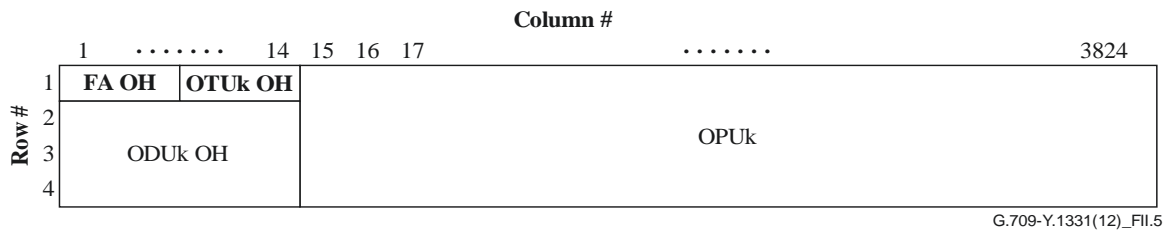
G.709-Y.1331(12)\_FI.3

**Figure II.3 – OTUk with a smaller OTUkV FEC and the remainder of an FEC area filled with fixed stuff**



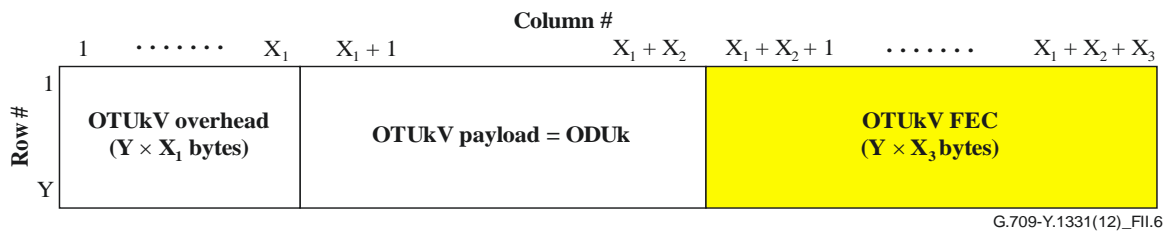
G.709-Y.1331(12)\_FI.4

**Figure II.4 – OTUk with a larger OTUkV FEC**



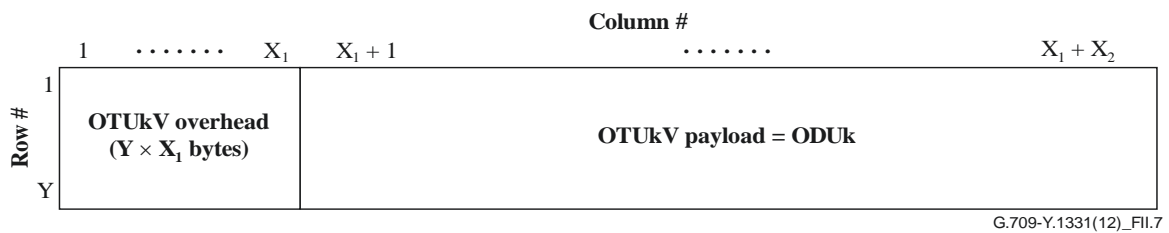
G.709-Y.1331(12)\_FI.5

**Figure II.5 – OTUk without an OTUkV FEC area**



G.709-Y.1331(12)\_FI.6

**Figure II.6 – OTUkV with a different frame structure**



G.709-Y.1331(12)\_FI.7

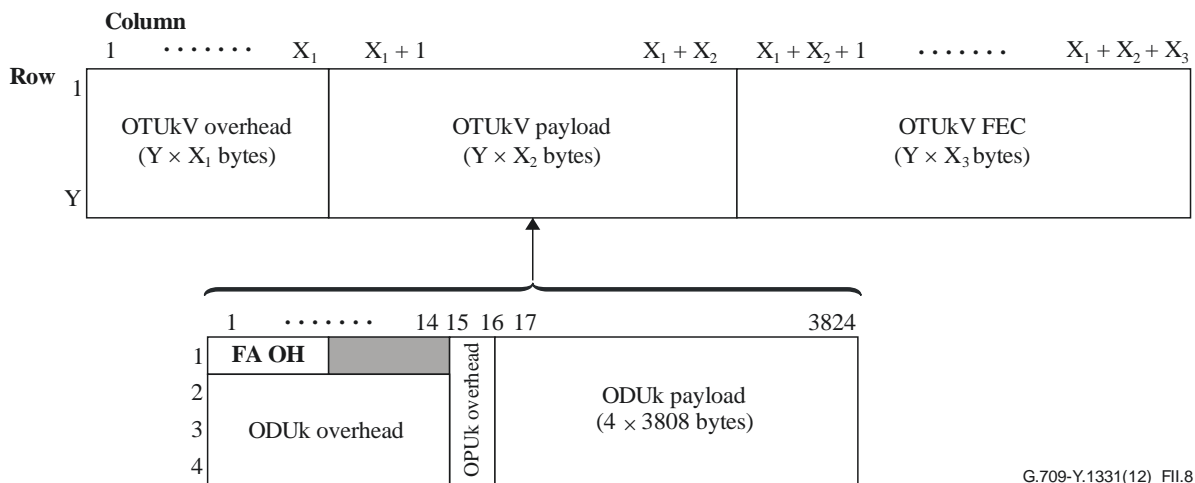
**Figure II.7 – OTUkV with a different frame structure and without FEC area**

For the case of Figures II.6 and II.7, the mapping of the ODUk signal can be either asynchronous, bit-synchronous, or frame synchronous.

For the case of asynchronous mapping, the ODUk and OTUkV bit rates can be asynchronous. The ODUk signal is mapped as a bit stream into the OTUkV payload area using a stuffing technique.

For the case of bit-synchronous mapping, the ODUk and OTUkV bit rates are synchronous. The ODUk signal is mapped into the OTUkV payload area without stuffing. The ODUk frame is not related to the OTUkV frame.

For the case of a frame synchronous mapping, the ODUk and OTUkV bit rates are synchronous and the frame structures are aligned. The ODUk signal is mapped into the OTUkV payload area without stuffing and with a fixed position of the ODUk frame within the OTUkV frame. (See Figure II.8.)



G.709-Y.1331(12)\_FII.8

**Figure II.8 – Asynchronous (or bit-synchronous) mapping of ODUk into OTUkV**

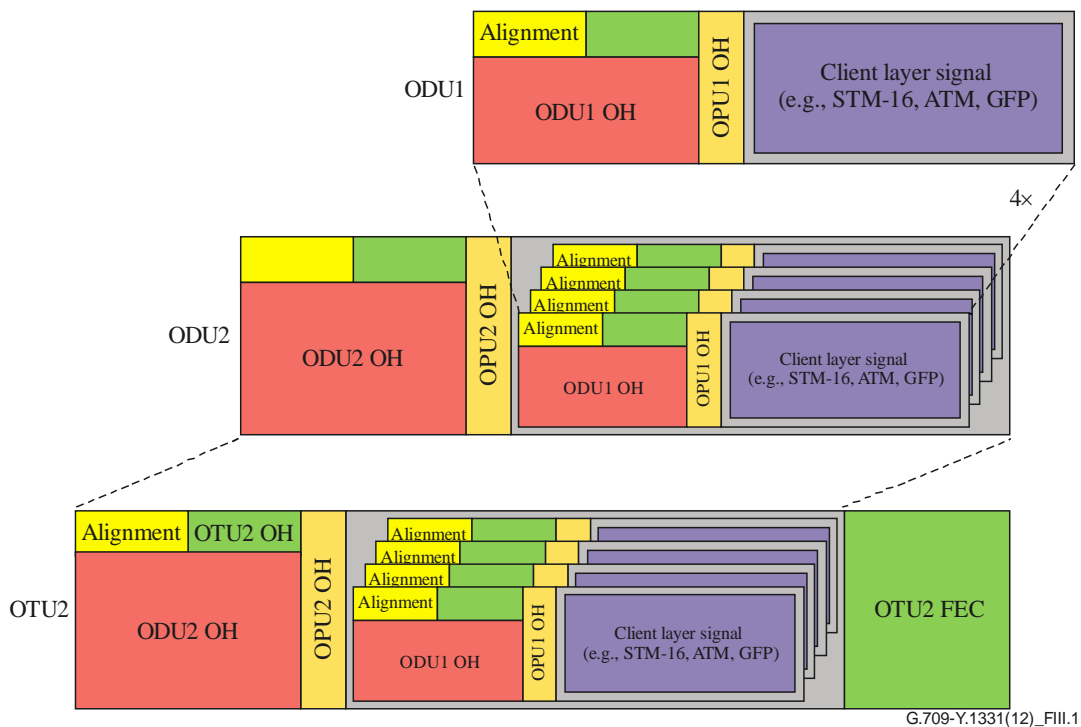
## Appendix III

### Example of ODUk multiplexing

(This appendix does not form an integral part of this Recommendation.)

Figure III.1 illustrates the multiplexing of four ODU1 signals into an ODU2. The ODU1 signals including the frame alignment overhead and an all-0s pattern in the OTUk overhead locations are adapted to the ODU2 clock via justification (asynchronous mapping). These adapted ODU1 signals are byte interleaved into the OPU2 payload area, and their justification control and opportunity signals (JC, NJO) are frame interleaved into the OPU2 overhead area.

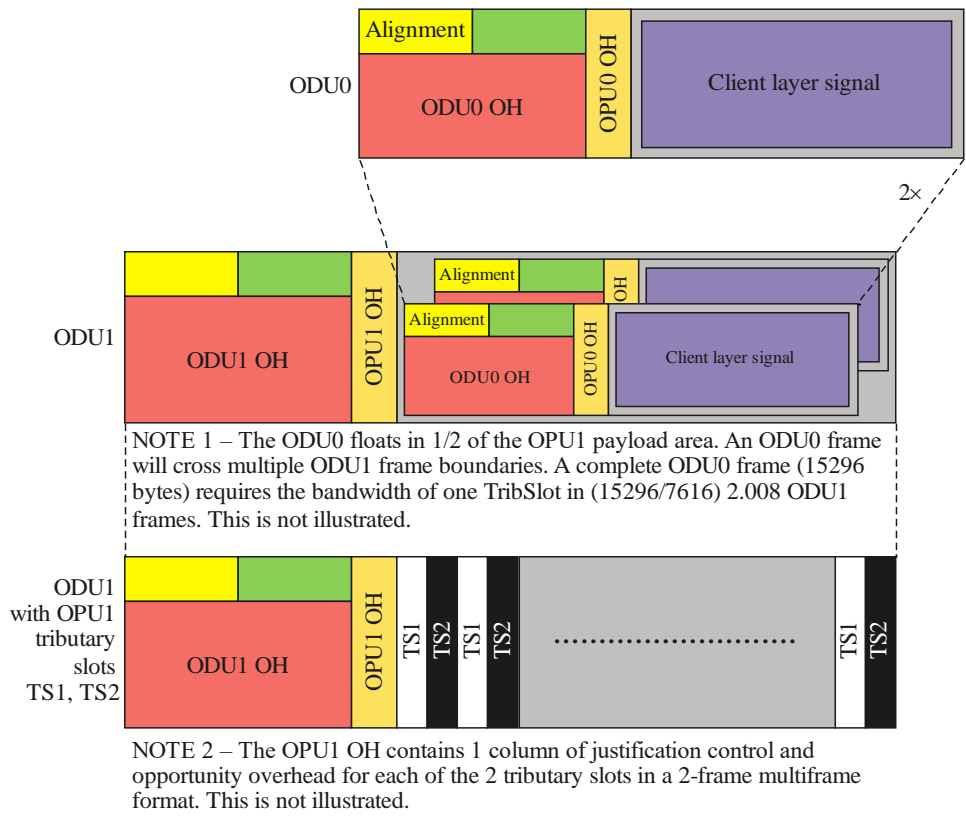
ODU2 overhead is added after which the ODU2 is mapped into the OTU2 [or OTU2V]. OTU2 [or OTU2V] overhead and frame alignment overhead are added to complete the signal for transport via an OTM signal.



NOTE – The ODU1 floats in a quarter of the OPU2 payload area. An ODU1 frame will cross multiple ODU2 frame boundaries. A complete ODU1 frame (15296 bytes) requires the bandwidth of (15296/3808) 4.017 ODU2 frames. This is not illustrated.

**Figure III.1 – Example of multiplexing 4 ODU1 signals into an ODU2**

Figure III.2 illustrates the multiplexing of two ODU0 signals into an ODU1. The ODU0 signals including the frame alignment overhead and an all-0s pattern in the OTUk overhead locations are adapted to the ODU1 clock via justification (asynchronous mapping). These adapted ODU0 signals are byte interleaved into the OPU1 payload area, and their justification control and opportunity signals (JC, NJO) are frame interleaved into the OPU1 overhead area and ODU1 overhead is added.



G.709-Y.1331(12)\_Fill.2

**Figure III.2 – Example of multiplexing 2 ODU0 signals into an ODU1**

## **Appendix IV**

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## Appendix V

### ODUk multiplex structure identifier (MSI) examples

(This appendix does not form an integral part of this Recommendation.)

The following figures present four examples of ODU1 and ODU2 carriage within an OPU3 and the associated MSI encoding.

	1	2	3	4	5	6	7	8	
<i>PSI[2]</i>	00					000000			<i>TS1</i>
<i>PSI[3]</i>	00					000001			<i>TS2</i>
<i>PSI[4]</i>	00					000010			<i>TS3</i>
<i>PSI[5]</i>	00					000011			<i>TS4</i>
<i>PSI[6]</i>	00					000100			<i>TS5</i>
<i>PSI[7]</i>	00					000101			<i>TS6</i>
<i>PSI[8]</i>	00					000110			<i>TS7</i>
<i>PSI[9]</i>	00					000111			<i>TS8</i>
<i>PSI[10]</i>	00					001000			<i>TS9</i>
<i>PSI[11]</i>	00					001001			<i>TS10</i>
<i>PSI[12]</i>	00					001010			<i>TS11</i>
<i>PSI[13]</i>	00					001011			<i>TS12</i>
<i>PSI[14]</i>	00					001100			<i>TS13</i>
<i>PSI[15]</i>	00					001101			<i>TS14</i>
<i>PSI[16]</i>	00					001110			<i>TS15</i>
<i>PSI[17]</i>	00					001111			<i>TS16</i>

**Figure V.1 – OPU3-MSI coding for the case of 16 ODU1s into OPU3**

	1	2	3	4	5	6	7	8		
PSI[2]	01		000000							TS1
PSI[3]	01		000001							TS2
PSI[4]	01		000010							TS3
PSI[5]	01		000011							TS4
PSI[6]	01		000000							TS5
PSI[7]	01		000001							TS6
PSI[8]	01		000010							TS7
PSI[9]	01		000011							TS8
PSI[10]	01		000000							TS9
PSI[11]	01		000001							TS10
PSI[12]	01		000010							TS11
PSI[13]	01		000011							TS12
PSI[14]	01		000000							TS13
PSI[15]	01		000001							TS14
PSI[16]	01		000010							TS15
PSI[17]	01		000011							TS16

**Figure V.2 – OPU3-MSI coding for the case of 4 ODU2s into OPU3 TS# (1, 5, 9, 13), (2, 6, 10, 14), (3, 7, 11, 15) and (4, 8, 12, 16)**

	1	2	3	4	5	6	7	8		
<i>PSI[2]</i>	01		000000							<i>TS1</i>
<i>PSI[3]</i>	01		000001							<i>TS2</i>
<i>PSI[4]</i>	01		000001							<i>TS3</i>
<i>PSI[5]</i>	01		000010							<i>TS4</i>
<i>PSI[6]</i>	01		000000							<i>TS5</i>
<i>PSI[7]</i>	01		000011							<i>TS6</i>
<i>PSI[8]</i>	01		000011							<i>TS7</i>
<i>PSI[9]</i>	01		000011							<i>TS8</i>
<i>PSI[10]</i>	01		000000							<i>TS9</i>
<i>PSI[11]</i>	01		000000							<i>TS10</i>
<i>PSI[12]</i>	01		000001							<i>TS11</i>
<i>PSI[13]</i>	01		000001							<i>TS12</i>
<i>PSI[14]</i>	01		000011							<i>TS13</i>
<i>PSI[15]</i>	01		000010							<i>TS14</i>
<i>PSI[16]</i>	01		000010							<i>TS15</i>
<i>PSI[17]</i>	01		000010							<i>TS16</i>

**Figure V.3 – OPU3-MSI coding for the case of 4 ODU2s into OPU3 TS# (1, 5, 9, 10), (2, 3, 11, 12), (4, 14, 15, 16) and (6, 7, 8, 13)**



	1	2	3	4	5	6	7	8	
<i>PSI[2]</i>	01					000000			<i>TS1</i>
<i>PSI[3]</i>	00					000001			<i>TS2</i>
<i>PSI[4]</i>	00					000010			<i>TS3</i>
<i>PSI[5]</i>	01					000001			<i>TS4</i>
<i>PSI[6]</i>	01					000000			<i>TS5</i>
<i>PSI[7]</i>	00					000101			<i>TS6</i>
<i>PSI[8]</i>	00					000110			<i>TS7</i>
<i>PSI[9]</i>	01					000001			<i>TS8</i>
<i>PSI[10]</i>	01					000000			<i>TS9</i>
<i>PSI[11]</i>	01					000001			<i>TS10</i>
<i>PSI[12]</i>	00					001010			<i>TS11</i>
<i>PSI[13]</i>	00					001011			<i>TS12</i>
<i>PSI[14]</i>	01					000000			<i>TS13</i>
<i>PSI[15]</i>	00					001101			<i>TS14</i>
<i>PSI[16]</i>	00					001110			<i>TS15</i>
<i>PSI[17]</i>	01					000001			<i>TS16</i>

**Figure V.4 – OPU3-MSI coding for the case of 5 ODU1s and 2 ODU2s into OPU3 TS# (2), (6), (11), (12), (14), (1, 5, 9, 13) and (4, 8, 10, 16) and OPU3 TS# 3, 7, 15 unallocated (default to ODU1)**

## Appendix VI

### Parallel logic implementation of the CRC-9, CRC-8, CRC-5 and CRC-6

(This appendix does not form an integral part of this Recommendation.)

#### CRC-9

Table VI.1 illustrates example logic equations for a parallel implementation of the CRC-9 using the  $g(x) = x^9 + x^3 + x^2 + 1$  polynomial over the  $\Sigma_{CND}$  fields of JC1, JC2, JC4 and JC5. An "X" in a column of the table indicates that the message bit of that row is an input to the Exclusive-OR equation for calculating the CRC bit of that row. JC4.D1 corresponds to bit 2 of the JC4 mapping overhead octet, JC4.D2 corresponds to bit 3 of the JC4 octet, etc. (See Figure 20-7.) After computation, CRC bits crc1 to crc9 are inserted into the JC6 and JC3 octets with crc1 occupying bit 2 of the JC6 octet and crc9 occupying bit 2 of the JC3 octet.

**Table VI.1 – Parallel logic equations for the CRC-9 implementation**

Mapping overhead bits	CRC checksum bits								
	crc1	crc2	crc3	crc4	crc5	crc6	crc7	crc8	crc9
JC4.D1		X	X			X			
JC4.D2			X	X			X		
JC4.D3				X	X			X	
JC4.D4					X	X			X
JC4.D5	X					X		X	
JC4.D6		X					X		X
JC4.D7	X		X				X		
JC1.D8		X		X				X	
JC1.D9			X		X				X
JC5.D10	X			X		X	X	X	
JC5.D11		X			X		X	X	X
JC5.D12	X		X			X	X		X
JC5.D13	X	X		X					
JC5.D14		X	X		X				
JC5.D15			X	X		X			
JC5.D16				X	X		X		
JC2.D17					X	X		X	
JC2.D18						X	X		X

#### CRC-8

Table VI.2 illustrates example logic equations for a parallel implementation of the CRC-8 using the  $g(x) = x^8 + x^3 + x^2 + 1$  polynomial over the JC1-JC2. An "X" in a column of the table indicates that the message bit of that row is an input to the Exclusive-OR equation for calculating the CRC bit of that row. JC1.C1 corresponds to the first bit (MSB) of the first mapping overhead octet (JC1), JC1.C2 corresponds to bit 2 of the first mapping overhead octet, etc. After computation, CRC bits crc1 to crc8 are inserted into the JC3 octet with crc1 occupying MSB and crc8 the LSB of the octet.

**Table VI.2 – Parallel logic equations for the CRC-8 implementation**

Mapping overhead bits	CRC checksum bits							
	crc1	crc2	crc3	crc4	crc5	crc6	crc7	crc8
JC1.C1		X				X		X
JC1.C2	X		X			X		
JC1.C3		X		X			X	
JC1.C4			X		X			X
JC1.C5	X			X			X	
JC1.C6		X			X			X
JC1.C7	X		X				X	
JC1.C8		X		X				X
JC2.C9	X		X		X	X	X	
JC2.C10		X		X		X	X	X
JC2.C11	X		X		X	X		X
JC2.C12	X	X		X				
JC2.C13		X	X		X			
JC2.C14			X	X		X		
JC2.II				X	X		X	
JC2.DI					X	X		X

**CRC-5**

Table VI.3 illustrates example logic equations for a parallel implementation of the CRC-5 using the  $g(x) = x^5 + x + 1$  polynomial over the JC4-JC5  $C_nD$  fields. An "X" in a column of the table indicates that the message bit of that row is an input to the Exclusive-OR equation for calculating the CRC bit of that row. JC4.D1 corresponds to the first bit (MSB) of the first mapping overhead octet (JC1), JC4.D2 corresponds to bit 2 of the first mapping overhead octet, etc. After computation, CRC bits crc1 to crc5 are inserted into the JC6 octet with crc1 occupying JC6 bit 4 and crc5 the JC6 bit 8.

**Table VI.3 – Parallel logic equations for the CRC-5 implementation**

Mapping overhead bits	CRC checksum bits				
	crc1	crc2	crc3	crc4	crc5
JC4.D1	X		X	X	
JC4.D2		X		X	X
JC4.D3	X		X		
JC4.D4		X		X	
JC4.D5			X		X
JC5.D6	X			X	X
JC5.D7	X	X			
JC5.D8		X	X		
JC5.D9			X	X	
JC5.D10				X	X

## CRC-6

Table VI.4 illustrates example logic equations for a parallel implementation of the CRC-6 using the  $g(x) = x^6 + x^3 + x^2 + 1$  polynomial over the JC1-JC2. An "X" in a column of the table indicates that the message bit of that row is an input to the Exclusive-OR equation for calculating the CRC bit of that row. JC1.C1 corresponds to bit 3 of the first mapping overhead octet (JC1), JC1.C2 corresponds to bit 4 of the first mapping overhead octet, etc. After computation, CRC bits crc1 to crc6 are inserted into the JC3 octet with crc1 occupying bit 3 and crc6 the LSB of the octet. (See Figure 20-7)

**Table VI.4 – Parallel logic equations for the CRC-6 implementation**

Mapping overhead bits	CRC checksum bits					
	crc1	crc2	crc3	crc4	crc5	crc6
JC1.C1			X		X	X
JC1.C2	X				X	X
JC1.C3	X	X		X	X	X
JC1.C4	X	X	X	X		X
JC1.C5	X	X	X			
JC1.C6		X	X	X		
JC2.C7			X	X	X	
JC2.C8				X	X	X
JC2.C9	X			X		X
JC2.C10	X	X		X		
JC2.II		X	X		X	
JC2.DI			X	X		X

## **Appendix VII**

### **OTL4.10 structure**

(This appendix does not form an integral part of this Recommendation.)

The information of this appendix is included in [b-ITU-T G-Sup.58].

## **Appendix VIII**

### **CPRI into ODU mapping**

(This appendix does not form an integral part of this Recommendation.)

The information of this appendix is included in [b-ITU-T G-Sup.56].

## Appendix IX

### Overview of CBR clients into OPU mapping types

(This appendix does not form an integral part of this Recommendation.)

As there are many different constant bit rate client signals and multiple mapping procedures, Table IX.1 provides an overview of the mapping procedure that is specified for each client.

**Table IX.1 – Overview of CBR client into OPUk mapping types**

	OPU0	OPU1	OPU2	OPU2e	OPU3	OPU4	OPUflex
STM-1	GMP with $C_{1D}$	–	–	–	–	–	–
STM-4	GMP with $C_{1D}$	–	–	–	–	–	–
STM-16	–	AMP, BMP	–	–	–	–	–
STM-64	–	–	AMP, BMP	–	–	–	–
STM-256	–	–	–	–	AMP, BMP	–	–
1000BASE-X	TTT+GM P no $C_{nD}$	–	–	–	–	–	–
10GBASE-R	–	–	–	16FS+BMP	–	–	–
25GBASE-R	–	–	–	–	–	–	BMP
40GBASE-R	–	–	–	–	TTT+GMP with $C_{8D}$	–	–
50GBASE-R	–	–	–	–	–	–	BMP
100GBASE-R	–	–	–	–	–	GMP with $C_{8D}$	–
200GBASE-R	–	–	–	–	–	–	BMP
400GBASE-R	–	–	–	–	–	–	BMP
FC-100	GMP no $C_{nD}$	–	–	–	–	–	–
FC-200	–	GMP with $C_{8D}$	–	–	–	–	–
FC-400	–	–	–	–	–	–	BMP
FC-800	–	–	–	–	–	–	BMP
FC-1200	–	–	–	TTT+16FS+ BMP (Note)	–	–	–
FC-1600	–	–	–	–	–	–	BMP
FC-3200	–	–	–	–	–	–	BMP
CM_GPON	–	AMP	–	–	–	–	–
CM_XGPON	–	–	AMP	–	–	–	–
IB SDR	–	–	–	–	–	–	BMP
IB DDR	–	–	–	–	–	–	BMP

**Table IX.1 – Overview of CBR client into OPUk mapping types**

	<b>OPU0</b>	<b>OPU1</b>	<b>OPU2</b>	<b>OPU2e</b>	<b>OPU3</b>	<b>OPU4</b>	<b>OPUflex</b>
IB QDR	–	–	–	–	–	–	BMP
SBCON/ESCON	GMP no C <sub>nD</sub>	–	–	–	–	–	–
DVB_ASI	GMP no C <sub>nD</sub>	–	–	–	–	–	–
SDI	GMP TBD C <sub>nD</sub>	–	–	–	–	–	–
1.5G SDI	–	GMP TBD C <sub>nD</sub>	–	–	–	–	–
3G SDI	–	–	–	–	–	–	BMP
FlexE Client	–	–	–	–	–	–	IMP
FlexE-aware	–	–	–	–	–	–	BGMP
NOTE – For this specific case the mapping used is byte synchronous.							



## Appendix X

### Overview of ODUj into OPuK mapping types

(This appendix does not form an integral part of this Recommendation.)

As there are many different ODUj bit rate signals and multiple mapping procedures, Table X.1 provides an overview of the mapping procedure that is specified for each ODUj.

**Table X.1 – Overview of ODUj client into OPuK mapping types**

	2.5G tributary slots		1.25G tributary slots					
	OPU2	OPU3	OPU1	OPU2	OPU3	OPU4	OPU25	OPU50
ODU0	–	–	ODTU01 AMP (PT=20)	ODTU2.1 GMP (PT=21)	ODTU3.1 GMP (PT=21)	ODTU4.1 GMP (PT=21)	ODTU25.1 GMP (PT=21)	ODTU50.1 GMP (PT=21)
ODU1	ODTU12 AMP (PT=20)	ODTU13 AMP (PT=20)	–	ODTU12 AMP (PT=21)	ODTU13 AMP (PT=21)	ODTU4.2 GMP (PT=21)	ODTU25.2 GMP (PT=21)	ODTU50.2 GMP (PT=21)
ODU2	–	ODTU23 AMP (PT=20)	–	–	ODTU23 AMP (PT=21)	ODTU4.8 GMP (PT=21)	ODTU25.8 GMP (PT=21)	ODTU50.8 GMP (PT=21)
ODU2e	–	–	–	–	ODTU3.9 GMP (PT=21)	ODTU4.8 GMP (PT=21)	ODTU25.8 GMP (PT=21)	ODTU50.8 GMP (PT=21)
ODU3	–	–	–	–	–	ODTU4.31 GMP (PT=21)	–	ODTU50.31 GMP (PT=21)
ODUflex	–	–	–	ODTU2.ts GMP (PT=21)	ODTU3.ts GMP (PT=21)	ODTU4.ts GMP (PT=21)	ODTU25.ts GMP (PT=21)	ODTU50.ts GMP (PT=21)
ODUflex(IB SDR)	–	–	–	ODTU2.3 GMP (PT=21)	ODTU3.3 GMP (PT=21)	ODTU4.2 GMP (PT=21)	ODTU25.2 GMP (PT=21)	ODTU50.2 GMP (PT=21)
ODUflex(IB DDR)	–	–	–	ODTU2.5 GMP (PT=21)	ODTU3.5 GMP (PT=21)	ODTU4.4 GMP (PT=21)	ODTU25.4 GMP (PT=21)	ODTU50.4 GMP (PT=21)
ODUflex(IB QDR)	–	–	–	–	ODTU3.9 GMP (PT=21)	ODTU4.8 GMP (PT=21)	ODTU25.8 GMP (PT=21)	ODTU50.8 GMP (PT=21)
ODUflex(FC- 400)	–	–	–	ODTU2.4 GMP (PT=21)	ODTU3.4 GMP (PT=21)	ODTU4.4 GMP (PT=21)	ODTU25.4 GMP (PT=21)	ODTU50.4 GMP (PT=21)
ODUflex(FC- 800)	–	–	–	ODTU2.7 GMP (PT=21)	ODTU3.7 GMP (PT=21)	ODTU4.7 GMP (PT=21)	ODTU25.7 GMP (PT=21)	ODTU50.7 GMP (PT=21)
ODUflex(FC- 1600)	–	–	–	–	ODTU3.12 GMP (PT=21)	ODTU4.11 GMP (PT=21)	ODTU25.11 GMP (PT=21)	ODTU50.11 GMP (PT=21)
ODUflex(FC- 3200)	–	–	–	–	ODTU3.23 GMP (PT=21)	ODTU4.22 GMP (PT=21)	–	ODTU50.22 GMP (PT=21)

**Table X.1 – Overview of ODU<sub>j</sub> client into OPU<sub>k</sub> mapping types**

	2.5G tributary slots		1.25G tributary slots					
	OPU2	OPU3	OPU1	OPU2	OPU3	OPU4	OPU25	OPU50
ODUflex(25G BASE-R)	–	–	–	–	ODTU3.21 GMP (PT=21)	ODTU4.20 GMP (PT=21)	ODTU25.20 GMP (PT=21)	ODTU50.20 GMP (PT=21)
ODUflex(50G BASE-R)	–	–	–	–	–	ODTU4.40 GMP (PT=21)	–	ODTU50.40 GMP (PT=21)
ODUflex(GFP)	–	–	–	ODTU2.ts (GMP) (PT=21)	ODTU3.ts (GMP) (PT=21)	ODTU4.ts (GMP) (PT=21)	ODTU25.ts (GMP) (PT=21)	ODTU50.ts (GMP) (PT=21)
ODUflex(GFP ,n,2), n=1, ... ,8 (ts=n)	–	–	–	ODTU2.ts (GMP) (PT=21)	ODTU3.ts (GMP) (PT=21)	ODTU4.ts (GMP) (PT=21)	ODTU25.ts (GMP) (PT=21)	ODTU50.ts (GMP) (PT=21)
ODUflex(GFP ,n,3), n=9, ... ,20 (ts=n)	–	–	–	–	ODTU3.ts (GMP) (PT=21)	ODTU4.ts (GMP) (PT=21)	ODTU25.ts (GMP) (PT=21)	ODTU50.ts (GMP) (PT=21)
ODUflex(GFP ,n,3), n=21, ... ,32 (ts=n)	–	–	–	–	ODTU3.ts (GMP) (PT=21)	ODTU4.ts (GMP) (PT=21)	–	ODTU50.ts (GMP) (PT=21)
ODUflex(GFP ), n=33, ... ,40 (ts=n)	–	–	–	–	–	ODTU4.ts (GMP) (PT=21)	–	ODTU50.ts (GMP) (PT=21)
ODUflex(GFP ,n,4), n=41, ... ,80 (ts=n)	–	–	–	–	–	ODTU4.ts (GMP) (PT=21)	–	–
ODUflex(IMP)	–	–	–	ODTU2.ts (GMP) (PT=21)	ODTU3.ts (GMP) (PT=21)	ODTU4.ts (GMP) (PT=21)	ODTU25.ts (GMP) (PT=21)	ODTU50.ts (GMP) (PT=21)
ODUflex (IMP,s), s=2	–	–	–	–	ODTU3.9 (GMP) (PT=21)	ODTU4.8 (GMP) (PT=21)	ODTU25.8 (GMP) (PT=21)	ODTU50.8 (GMP) (PT=21)
ODUflex(IMP, s), s=5	–	–	–	–	ODTU3.21 (GMP) (PT=21)	ODTU4.20 (GMP) (PT=21)	ODTU25.20 (GMP) (PT=21)	ODTU50.20 (GMP) (PT=21)
ODUflex(IMP, s), s=8	–	–	–	–	–	ODTU4.32 (GMP) (PT=21)	–	ODTU50.32 (GMP) (PT=21)
ODUflex(IMP, s), s=10	–	–	–	–	–	ODTU4.40 (GMP) (PT=21)	–	ODTU50.40 (GMP) (PT=21)
ODUflex(IMP, s), s=15,20 (ts=4xs)	–	–	–	–	–	ODTU4.ts (GMP) (PT=21)	–	–

## Appendix XI

### Derivation of recommended ODUflex(GFP) bit-rates based on $n \times$ ODUk.ts clock and examples of ODUflex(GFP,n,k) clock generation

(This appendix does not form an integral part of this Recommendation.)

#### XI.1 Introduction

The recommended bit-rates for ODUflex(GFP,n,k) are provided in Table 7-8. While in principle an ODUflex(GFP) may be of any bit-rate, there were at the time of the introduction of the ODUflex a variety of reasons for recommending particular rates for the ODUflex(GFP,n,k):

- To encourage a common set of bit-rates which can be expected to be supported by multiple manufacturers.
- To provide the largest amount of bandwidth possible within a given amount of resource (number of tributary slots) independent of the ODUk over which the ODUflex(GFP,n,k) may be routed.
- To maintain the number of tributary slots required if the ODUflex(GFP,n,k) must be rerouted, e.g., during a restoration.
- To satisfy a protocol requirement for ODUflex hitless resizing that a resizable ODUflex(GFP,n,k) must occupy the same number of tributary slots on every ODUk path over which it is carried, and that a resize operation must always add or remove at least one tributary slot.

#### XI.2 Tributary slot sizes

ODUflex(GFP,n,k) is mapped via GMP into a certain number of 1.25G tributary slots of a HO OPU2, OPU3, or OPU4. Each of these have different tributary slot sizes:

$$OPU2\_TS = \frac{238}{237} \times 4 \times STM16 \times \frac{476 \text{ columns}}{3808 \text{ columns}} = 1249409.620 \text{ kbit/s} \pm 20\text{ppm}$$

$$OPU3\_TS = \frac{238}{236} \times 16 \times STM16 \times \frac{119 \text{ columns}}{3808 \text{ columns}} = 1254703.729 \text{ kbit/s} \pm 20\text{ppm}$$

$$OPU4\_TS = \frac{238}{227} \times 40 \times STM16 \times \frac{47.5 \text{ columns}}{3808 \text{ columns}} = 1301709.251 \text{ kbit/s} \pm 20\text{ppm}$$

An ODUflex(GFP,n,2) that occupies 8 or fewer tributary slots may be routed over OPU2, OPU3, or OPU4. The smallest tributary slot that may be encountered along the route of the ODUflex(GFP,n,2) is that of OPU2. Even if the initially selected route does not chose a link of OPU2, the ODUflex(GFP,n,2) should be sized to a multiple of the OPU2 tributary slot size to preserve the possibility to restore the ODUflex(GFP,n,2) over a route that includes OPU2 without changing the size of the ODUflex or the number of tributary slots it occupies.

An ODUflex(GFP,n,3) that occupies at least 9, but no more than 32 tributary slots may be routed over OPU3 or OPU4. It does not fit over OPU2. Therefore such an ODUflex(GFP,n,3) may be sized to a multiple of the OPU3 tributary slot size. Even if the initially selected route does not chose a link of OPU3, the ODUflex(GFP,n,3) should be sized to a multiple of the OPU3 tributary slot size to preserve the possibility to restore the ODUflex(GFP,n,3) over a route that includes OPU3 without changing the size of the ODUflex or the number of tributary slots it occupies.

An ODUflex(GFP,n,4) that occupies at least 33, but no more than 80 tributary slots may only be carried via OPU4, and may therefore take advantage of the full size of the OPU4 tributary slot size.

A small margin must be left between the ODUflex(GFP,n,k) size and the integral multiple of the tributary slot size to accommodate possible clock variation along a sequence of OPUk links without overflowing the range of  $C_m$  in the GMP mapper.

Physical layers for data interfaces such as Ethernet and Fibre Channel have historically used a clock tolerance of  $\pm 100$  ppm. This range is sufficiently wide that specifying this as the clock tolerance for ODUflex(GFP,n,k) can accommodate a variety of mechanisms for generating an ODUflex(GFP,n,k) clock and remain within the clock tolerance range.

ODUk.ts as shown in Table 7-8 is an increment of bandwidth, which, when multiplied by a number of 1.25G tributary slots, gives the recommended size of an ODUflex(GFP,n,k) optimized to occupy a given number of tributary slots of a server OPUk. These values are chosen to allow sufficient margin that allows the OPUk and the ODUflex(GFP,n,k) to independently vary over their full clock tolerance range without exceeding the capacity of the allocated tributary slots.

The nominal values for ODUk.ts are chosen to be 186 ppm below the bandwidth of a single 1.25G tributary slot of a server OPUk. This allows the ODUflex(GFP,n,k) clock to be as much as 100 ppm above its nominal rate and the server OPUk to be as much as 20 ppm below its nominal clock rate, allowing approximately 66 ppm of margin to accommodate jitter and to ensure that the largest average  $C_m$  value even in the worst-case situation of the OPUk at -20 ppm from its nominal value and the ODUflex(GFP,n,k) at +100 ppm from its nominal value will be one less than the maximum value (i.e., the maximum average  $C_m$  is no more than 15231 out of 15232 for ODUflex(GFP,n,k) carried over OPU2 or OPU3, and no more than 15199 out of 15200 for ODUflex(GFP,n,k) carried over OPU4).

**Table XI.1 – Generation of ODUflex(GFP,n,k) clock from server OPUk clock using fixed C<sub>m</sub>**

OPUk	Nominal payload bit rate	Nominal 1.25G TS bit rate	ODU2.ts						
			C <sub>m</sub> out of	Bit-rate per TS					
OPU2	9'995'276.962	1'249'409.620	15230	1'249'245.570	ODU3.ts				
			15232						
			+20 ppm	1'249'270.555	C <sub>m</sub> out of	Bit-rate per TS			
			-20 ppm	1'249'220.585					
OPU3	40'150'519.322	1'254'703.729	15165	1'249'184.746	15230	1'254'538.983		ODU4.ts	
			15232		15232				
			+20 ppm	1'249'209.729		1'254'564.074	C <sub>m</sub> out of	Bit-rate per TS	
			-20 ppm	1'249'159.762		1'254'513.892			
OPU4	104'355'975.330	1'301'709.251	14587	1'249'212.687	14649	1'254'522.291	15198	1'301'537.974	
			15200		15200		15200		
			+20 ppm	1'249'237.671		1'254'547.381		1'301'564.004	
			-20 ppm	1'249'187.703		1'254'497.200		1'301'511.943	
			nominal	1'249'177.230		1'254'470.354		1'301'467.133	
			+100 ppm	1'249'302.148		1'254'595.801		1'301'597.280	
			-100 ppm	1'249'052.312		1'254'344.907		1'301'336.986	
			ODUk.ts						

### XI.3 Example methods for ODUflex(GFP,n,k) clock generation

#### XI.3.1 Generating ODUflex(GFP,n,k) clock from OPUk clock

The clock for an ODUflex(GFP,n,k) may be generated from the initial server OPUk over which the ODUflex(GFP,n,k) is carried by setting the value of  $C_m$  to a fixed value on the initial segment. Normal GMP processing on subsequent segments avoids the need to couple the server OPUk clocks along the path.

Table XI-1 illustrates how a clock for an ODUflex(GFP,n,k) occupying  $n \times$  ODUk.ts can be derived from the server OPUk clock using a fixed value of  $C_m$  in the initial segment of the path.

For example, for an ODUflex(GFP,n,k) occupying up to 8 tributary slots should be based on ODU2.ts, and therefore have a clock frequency of  $n \times 1'249'177.230$  kbit/s  $\pm 100$  ppm. This allows the ODUflex(GFP,n,k) to have a frequency of between  $n \times 1'249'052.312$  kbit/s and  $n \times 1'249'302.148$  kbit/s.

- If the initial segment over which the ODUflex(GFP,n,k) is carried is an OPU2, a clock in this range can be generated by fixing the value of  $C_m$  on the initial segment to 15230, which will result in the ODUflex having a clock of  $n \times 1'249'245.570$  kbit/s  $\pm 20$  ppm. While the center frequency of this range differs from the nominal value of ODU2.ts, the clock tolerance is narrower, being locked to the OPU2, so the possible clock range is fully within the  $\pm 100$  ppm range allowed.
- If the initial segment is an OPU3, the ODUflex(GFP,n,k) of a multiple of ODU2.ts can be generated using a fixed value of  $C_m=15165$  on the initial ODU3 segment, which will result in the ODUflex having a clock of  $n \times 1'249'184.746$  kbit/s  $\pm 20$  ppm,
- If the initial segment is an OPU4, the ODUflex(GFP,n,k) of a multiple of ODU2.ts can be generated using a fixed value of  $C_m=14587$  on the initial OPU4 segment, which will result in the ODUflex having a clock of  $n \times 1'249'212.687$  kbit/s  $\pm 20$  ppm.

The center frequencies of all of these ODUflex(GFP,n,k) are slightly different, but the resulting ranges for the clocks all fall within the  $\pm 100$  ppm window (see Figure XI.1). Fixed  $C_m$  for generating ODU3.ts and ODU4.ts from the initial OPUk can similarly be found from this table.

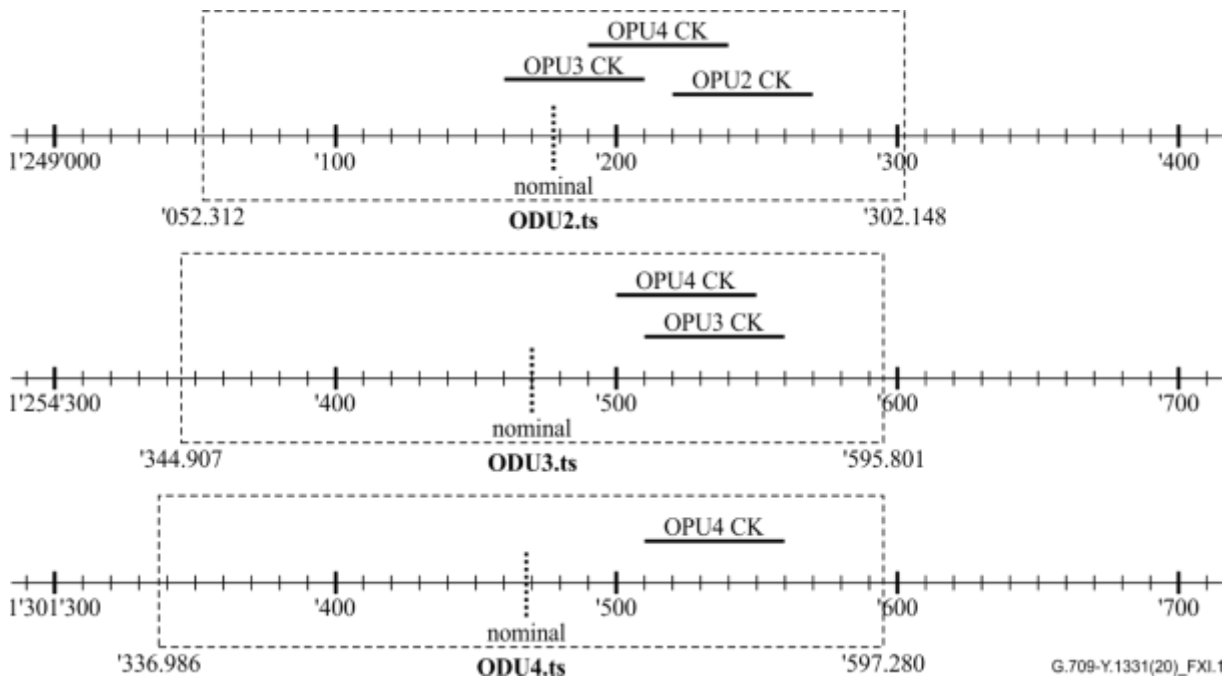


Figure XI.1 – Graphical representation of frequency ranges in Table XI.1

### **XI.3.2 Generating ODUflex(GFP,n,k) clock from system clock**

The clock for an ODUflex(GFP,n,k) may be generated using a multiplier from the internal system clock. Normally the internal system clock will have an accuracy of at least  $\pm 20$  ppm, perhaps even  $\pm 4.6$  ppm for a network element that supports both SDH and OTN interfaces. The exact multiplier to be used is implementation specific, and be chosen so that the range of the generated clock falls within the specified  $\pm 100$  ppm window around the nominal value of  $n \times \text{ODUk.ts}$ . Refer to Appendix XV for further information.

## Appendix XII

### Terminology changes between ITU-T G.709 Edition 4, Edition 5 and Edition 6

(This appendix does not form an integral part of this Recommendation.)

In Edition 5 of this Recommendation a number of terms used in Editions 1 to 4 have been modified. In Edition 6 of this Recommendation a number of terms used in Edition 5 have been modified. Table XII.1 provides the mapping between these terms in Editions 1 to 4, Edition 5, and Edition 6.

**Table XII.1 – Terminology mapping**

ITU-T G.709 Edition 1 to 4	ITU-T G.709 Edition 5	ITU-T G.709 Edition 6
OTM-0.m	SOTU	OTN point-to-point interface, type I
OTM-0.mvn	(multi-lane) SOTU	OTN point-to-point interface, type I
OTM-nr.m	MOTU	OTN point-to-point interface, type II
OTM-1.m	SOTUm	OTN optical networking interface, type II
OTM-n.m	MOTUm	OTN optical networking interface, type I
Optical Channel (OCh)	OCh	OCh
Optical Channel with reduced functionality (OChr)	OCh-P	OTSiG
Optical Channel Payload (OCh-P)	OCh-P	OTSiG
Optical Channel Overhead (OCh-OH)	OCh-O	OCh-O
Optical channel Transport Unit (OTU)	Optical Transport Unit (OTU)	Optical Transport Unit (OTU)
Optical channel Data Unit (ODU)	Optical Data Unit (ODU)	Optical Data Unit (ODU)
Optical channel Payload Unit (OPU)	Optical Payload Unit (OPU)	Optical Payload Unit (OPU)
Optical channel Data Tributary Unit (ODTU)	Optical Data Tributary Unit (ODTU)	Optical Data Tributary Unit (ODTU)
Optical channel Data Tributary Unit Group (ODTUG)	Optical Data Tributary Unit Group (ODTUG)	Optical Data Tributary Unit Group (ODTUG)
Optical Multiplex Unit (OMU)	–	–
Optical Channel Carrier (OCC)	–	–
Optical Channel Carrier – overhead (OCCo)	–	–
Optical Channel Carrier – payload (OCCp)	–	–
Optical Channel Carrier with reduced functionality (OCCr)	–	–
Optical Carrier Group (OCG)	–	–
Optical Carrier Group with reduced functionality (OCGr)	–	–
Optical Carrier Group of order n (OCG)	–	–
OTM Overhead Signal (OOS)	Optical Supervisory Channel (OSC)	Optical Supervisory Channel (OSC)



**Table XII.1 – Terminology mapping**

ITU-T G.709 Edition 1 to 4	ITU-T G.709 Edition 5	ITU-T G.709 Edition 6
Optical Transport Lane (OTLk.n)	OTLk.n lane	OTLk.n lane
Optical Transport Lane Carrier Group (OTLCG)	–	–
Optical Transport Lane Carrier (OTLC)	–	–
OPS0	OPS	–
OPSn	OPS	–
OPSMnk	OPS	–
OTS-OH	OTS-O	OTS-O
OMS-OH	OMS-O	OMS-O
ODUflex(GFP)	ODUflex(GFP)	ODUflex(GFP,n,k)
–	ODUflex(IMP)	ODUflex(IMP,s)

In Edition 5.0 of this Recommendation the following new terms are introduced:

**Table XII.2 – New terms in Edition 5**

Optical Tributary Signal (OTSi)  
 Optical Tributary Signal Group (OTSiG)  
 Optical Tributary Signal Group – Overhead (OTSiG-O)  
 Optical Tributary Signal Assembly (OTSiA)

The relationship between these new terms in and the OCh, OChr, OPS0, OPSn and OPSM terms is as follows:

**Table XII.3 – Relationship between OCh, OChr, OPS0, OPSn, OPSM and OTSi terminology**

OCh-P	OTSiG with one or more OTSi
OCh-O	Reduced version of OTSiG-O: – FDI-P, FDI-O and OCI: supported – TTI, BDI-P, BDI-O, TSI: not supported
OCh	Reduced version of OTSiA: – OTSiG with one or more OTSi – FDI-P, FDI-O and OCI: supported – TTI, BDI-P, BDI-O, TSI: not supported
OChr	OTSiG with one OTSi; no OTSiG-O
OPS0	OTSiG with one OTSi; no OTSiG-O
OPSMnk	OTSiG with m OTSi; no OTSiG-O
OPSn	n OTSiG and no OTSiG-O; each OTSiG with one OTSi

## Appendix XIII

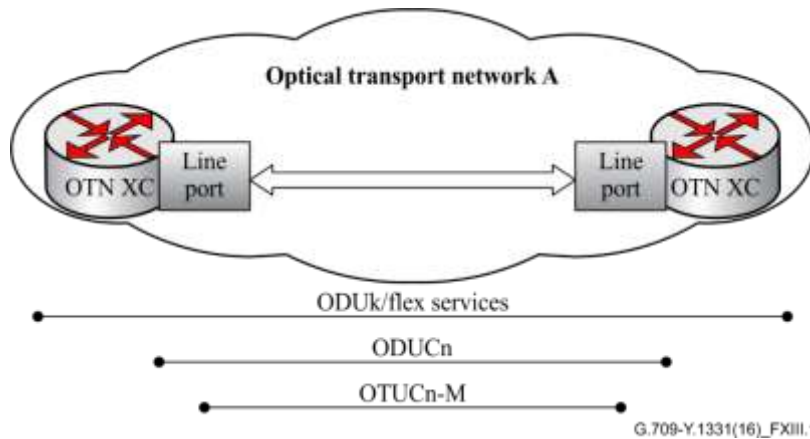
### OTUCn sub rates (OTUCn-M) Applications

(This appendix does not form an integral part of this Recommendation.)

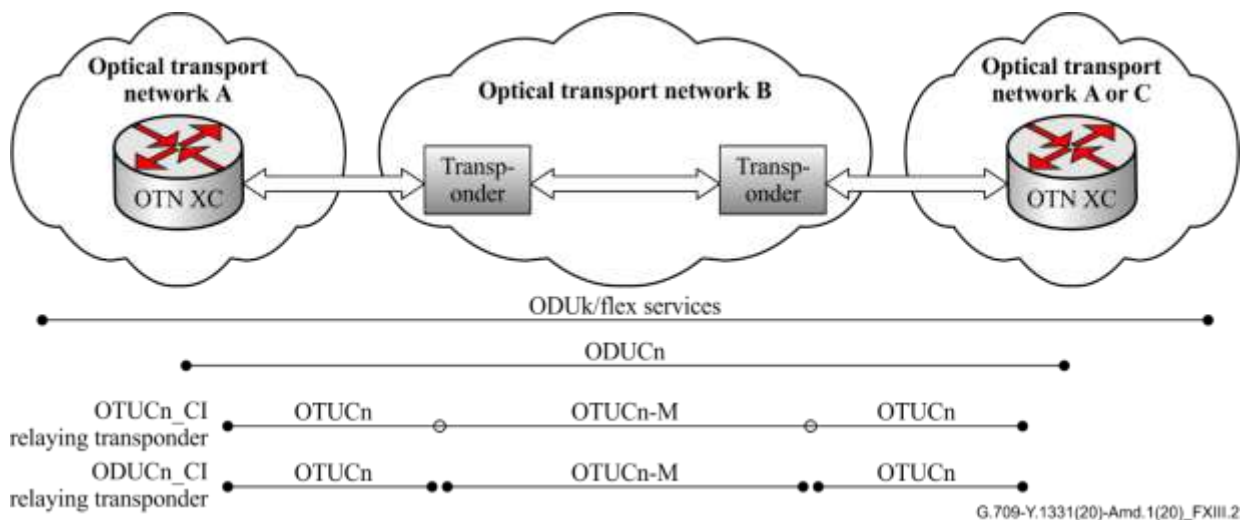
#### XIII.1 Introduction

This appendix describes OTUCn-M application scenarios for the OTUCn-M signal defined in Annex H. It is assumed that the OTUCn-M processing is performed in the PHY module so that the interface between the module and framer (MFI) is not changed.

Figures XIII.1 and XIII.2 illustrate two scenarios for subrating applications. The first scenario deploys subrating between two line ports connecting two ODU cross connects (XC). The second scenario deploys subrating between transponders which are in a different domain B, which are separated from the ODU XCs in domain A and/or C. The transponders could either relay the OTUCn\_CI or the ODUc\_n\_CI. In the former case, the OTUCn between domain B and domain A or C continue in domain B as OTUCn-M. In the latter case, the OTUCn and OTUCn-M are terminated in the two transponders and the ODUc\_n is forwarded.



**Figure XIII.1 – OTUCn sub rate application scenario A**



**Figure XIII.2 – OTUCn sub rate application scenario B**

### XIII.2 OTUCn-M frame format and rates

As defined in Annex H, the OTUCn-M frame is a type of OTUCn frame which contains n instances of OTUC, ODUc and OPUC overhead and M 5 Gbit/s OPUCn tributary slots. If a particular value of M is not indicated, the frame contains 20×n tributary slots.

The use of this notation is illustrated below:

- OTUC2-25: a 125 Gbit/s OTU signal with 25 (5 Gbit/s) tributary slots and 2 instances of OxUC overhead
- OTUC2-30: a 150 Gbit/s OTU signal with 30 (5 Gbit/s) tributary slots and 2 instances of OxUC overhead
- OTUC2: a 200 Gbit/s OTU signal with 40 (5 Gbit/s) tributary slots and 2 instances of OxUC overhead
- OTUC3-50: a 250 Gbit/s OTU signal with 50 (5 Gbit/s) tributary slots and 3 instances of OxUC overhead

The bit rate of an OTUCn-M signal is  $(10n + 119 \times M) / (10n + 119 \times 20 \times n) \times \text{OTUCn bit rate}$ . The choice of which TS are assigned to each of the OTUC instances, and hence the signal rate of that OTUC instance, is vendor or application specific.

### XIII.3 OTUCn-M fault condition

For the case where subrating is used between transponders the following checks should be made.

In the transmit (source) direction, transponder X should verify that the OPU tributary slots with the Availability bit of their OPUCn MSI overhead set to "available" are carried transparently by the OTUCn-M. For the case where one or more availability bits for the tributary slots that are not carried transparently are set to "available", an OTUCn-AIS or ODUc-AIS should be output by transponder Y. The behaviour between the two transponders is vendor specific and outside the scope of this Recommendation.

In the receive (sink) direction, transponder Y should check for a mismatch between received and expected OTUCn-M. If such a mismatch is detected an OTUCn-AIS or ODUc-AIS should be output by Transponder Y.

In the transmit (source) direction, transponder X should verify if the OTUCn signal contains OTUCn-AIS or ODUc-AIS. For such case, the OPUCn contains an all-1's pattern and OPU tributary slots can no longer be identified. OTUCn-AIS or ODUc-AIS should be output by transponder Y. The behaviour between the two transponders is vendor specific and outside the scope of this Recommendation.

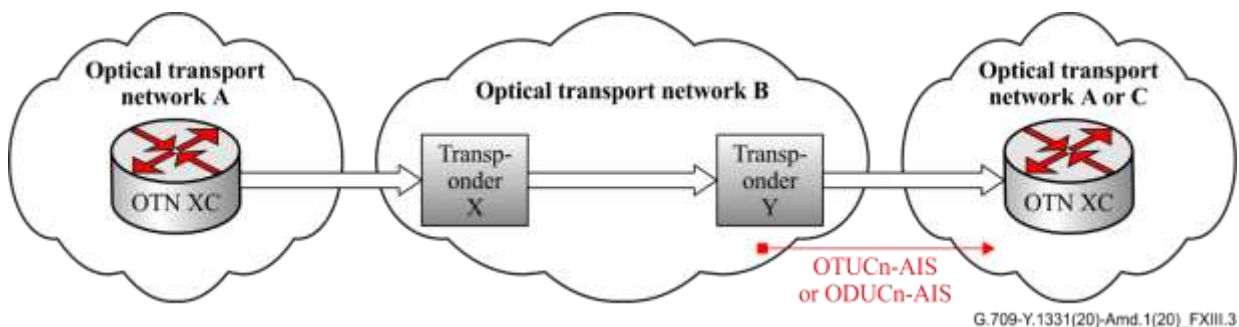


Figure XIII.3 – OTUCn sub rate mismatch fault condition

## Appendix XIV

### **Examples of interconnection of Ethernet UNI and FlexE Group UNI in two administrative domains in the OTN for the case that these UNIs deploy different mapping methods**

(This appendix does not form an integral part of this Recommendation.)

This appendix describes two cases to support the interconnection of an Ethernet UNI and a FlexE Group UNI in two administrative domains in the OTN, in which interconnection requires that the mapping method in one administrative domain is converted into the mapping method used in the other administrative domain.

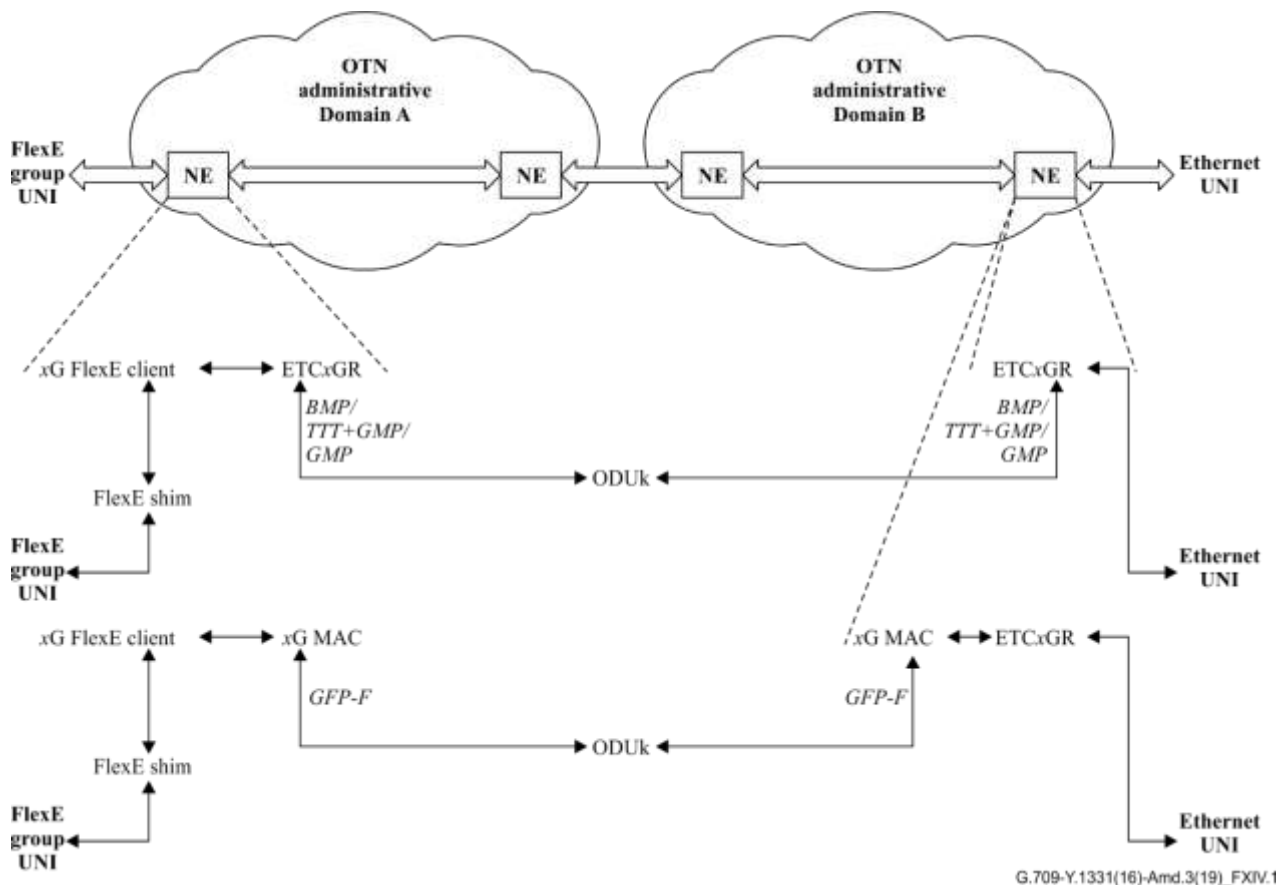
Case I is to perform the mapping method conversion at the FlexE group UNI-N port as shown in Figure XIV.1.

Case II is to perform the mapping method conversion at an intermediate node along the connection as shown in Figure XIV.2.

These conversion approaches provide for backward compatibility with Ethernet UNI-N ports designed prior to the definition of FlexE.

Figure XIV.1 illustrates an implementation of case I. For the case of an Ethernet PCS encoded client service, the FlexE Group UNI-N port converts the FlexE Client signal into the corresponding Ethernet PCS encoded signal and maps it into an ODUk using BMP, TTT+GMP or GMP as specified in clause 17. The ODUk is transported through the OTN and is terminated in the Ethernet UNI-N port.

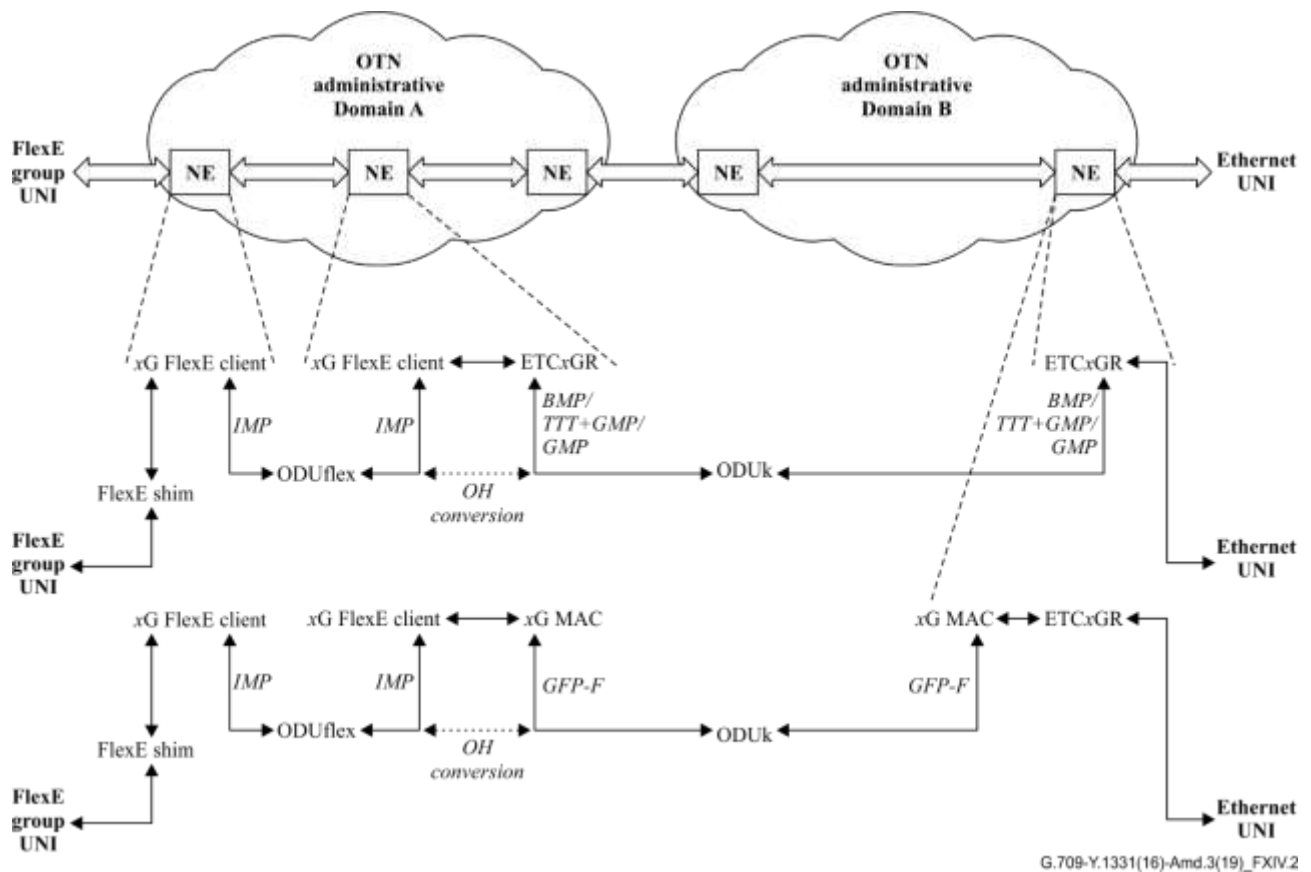
For the case of an Ethernet MAC client service with a bit rate up to and including 100 Gbit/s, the FlexE Group UNI-N port terminates the FlexE Client signal, extracts the Ethernet MAC frames stream and maps this MAC frames stream into an ODUk using GFP-F as specified in clause 17. The ODUk is transported through the OTN and is terminated in the Ethernet UNI-N port.



**Figure XIV.1 – Ethernet PCS encoded or MAC signal interconnection between an Ethernet UNI and a FlexE UNI in case I**

Figure XIV.2 illustrates an implementation of case II. For the case of an Ethernet PCS encoded client service, the mapping method conversion is performed at an intermediate node in the domain with the FlexE Group UNI. In this node, the FlexE Client signal is demapped from the ODUflex and then the FlexE Client signal is converted into the corresponding Ethernet PCS encoded signal and then mapped into an ODUk using BMP, TTT+GMP or GMP as specified in clause 17. At the same time, the overhead from ODUflex and OPUflex carrying the FlexE Client signal is converted into the overhead of ODUk and OPUk carrying the Ethernet PCS encoded signal. This conversion maintains the overhead information with the exception of the value of the Payload Type. The specific overhead conversion is vendor specific and outside the scope of this Recommendation.

For the case of an Ethernet MAC client service with a bit rate below and including 100 Gbit/s, the mapping method conversion is performed at an intermediate node in the domain with the FlexE Group UNI. In this node, the FlexE Client signal is demapped from the ODUflex and the Ethernet MAC frames stream is extracted. Then the Ethernet MAC frames stream is mapped into an ODUk using GFP-F as specified in clause 17. At the same time, the overhead from ODUflex and OPUflex carrying the FlexE Client signal is converted into the overhead of the ODUk and OPUk carrying the Ethernet MAC frames stream. This conversion maintains the overhead information with the exception of the value of the Payload Type. The specific overhead conversion is vendor specific and outside the scope of this Recommendation.



**Figure XIV.2 – Ethernet PCS encoded or Ethernet MAC client services interconnection between an Ethernet UNI and a FlexE UNI in case II**

## Appendix XV

### Examples of ODUflex(GFP) and ODUflex(IMP) clock generation methods

(This appendix does not form an integral part of this Recommendation.)

This appendix describes examples of clock generation methods that support ODUflex(GFP) and ODUflex(IMP) signals.

ODUflex(GFP) and ODUflex(IMP) signals are generated using a local clock or the timing of its client signal (if available). The local clock may be the local server ODU<sub>k</sub> (or OTU<sub>k</sub>) clock, the local ODU<sub>Cn</sub> (or OTU<sub>Cn</sub>) clock, or an equipment internal clock of the signal over which the ODUflex is carried through the equipment.

#### XV.1 Client timing based

In this method, the clock of the 64B/66B encoded packet client (e.g., FlexE Client) signal is used as reference clock for the generation of the ODUflex(IMP) signal and adjusted by means of a fixed X/Y value, with X = 239 and Y = 238. The ODUflex(IMP) bit rate is  $239/238 \times$  bit rate of 64B/66B encoded packet client.

#### XV.2 Local clock based

In this method, a local clock with a bit rate tolerance of  $\pm 20$  ppm is used as reference clock for the generation of the ODUflex(GFP) and ODUflex(IMP) signals. This local clock is the same clock that is used to generate a server ODU<sub>k</sub>/OTU<sub>k</sub> or ODU<sub>Cn</sub>/OTU<sub>Cn</sub> or equipment specific server signal over which the ODUflex is carried. The bit rates of the ODUflex(GFP) and ODUflex(IMP) signals generated at the A and Z ends of the trail will be  $X_A \pm 20$  ppm and  $X_Z \pm 20$  ppm. These two rates do not have to be identical. In the worst case, these two rates could be  $[2 \times (100 - 20)] = 160$  ppm apart from each other to comply with the ODUflex(GFP) and ODUflex(IMP) bit rate of X Gbit/s  $\pm 100$  ppm, in which X represents the nominal bidirectional bit rate as illustrated in Figure XV.1.

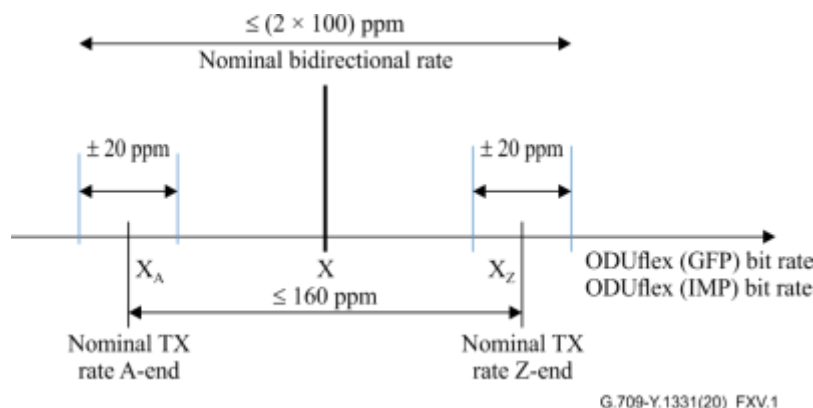


Figure XV.1 – General ODUflex(GFP) and ODUflex(IMP) bit rate and tolerance

In a first instance, the clock of the server ODU is used as reference clock to generate the ODUflex(GFP) and ODUflex(IMP) clock rate and adjusted by means of a fixed  $C_m$  value, similar to the case of ODUflex(GFP,n,k), or of two alternating  $C_m$  values  $X/X+1$  (similar to the case of ODUflex(FlexE Aware)).

NOTE 1 – The main difference between the ODUflex(GFP) and ODUflex(IMP) clock rate and the ODUflex(GFP,n,k) clock rate is that this latter rate is the maximum rate that can be supported by M 1.25G OPU<sub>k</sub> tributary slots whereas the first clock rate is just the rate that is sufficient to carry the packet client signal in a GFP-F frame stream or in a 64B/66B encoded signal.

In a second instance, the bit rate of an ODUflex(GFP) and ODUflex(IMP) signal may be generated by means of a local clock circuit that multiplies a local free run clock rate with an Register1/Register2 multiplier of which the value of Register1 is configured via a first N-bit register and the value of Register2 is configured via a second N-bit register so that the ODUflex(GFP) and ODUflex(IMP) bit rate is equal to Register1/Register2  $\times$  Datapath\_Width  $\times$  System\_Clock rate, with  $N \geq 16$ . The Register1/Register2 value is related to the agreed bandwidth of the packet client signal (i.e.,  $238/239 \times$  Register1/Register2). For the case of ODUflex(IMP), this clock is also provided to the packet client as reference clock for the generation of the 64B/66B encoded signal to restrict the difference in bit rate of the 64B/66B encoded packet client and the bandwidth of the OPUflex(IMP)\_Payload to a value that is within the range that IMP can address.

NOTE 2 – ODUflex(GFP,n,k) signals can be supported by ODUflex(GFP) signals; for example for the case of a Datapath\_Width  $\times$  System\_Clock rate being equal to 99.5328 Gbit/s  $\pm$  20 ppm the ODUflex(GFP,n,k=2) is supported by e.g., ODUflex(GFP, REG1= $n \times 28$ , REG2=2231), the ODUflex(GFP,n,k=3) is supported by e.g., ODUflex(GFP, REG1= $n \times 35$ , REG2=2777), and the ODUflex(GFP,n,k=4) is supported by e.g., ODUflex(GFP, REG1= $n \times 44$ , REG2=3365).

NOTE 3 – ODUflex(IMP,s) signals can be supported by ODUflex(IMP) signals; for example, for the case of a Datapath\_Width  $\times$  System\_Clock rate being equal to 99.5328 Gbit/s  $\pm$  20 ppm the ODUflex(IMP,s) is supported by e.g., ODUflex(IMP, REG1= $s \times 9$ , REG2=173).



## Appendix XVI

### Implications of OTSiG (de)modulator processes and OCh|OTSiG overhead trail termination functions being located in adjacent network elements

(This appendix does not form an integral part of this Recommendation.)

This appendix describes the implications on fault management and its alarm suppression for the case that the OTSiG (de)modulator processes and OCh|OTSiG overhead trail termination functions are located in adjacent and thus different network elements.

#### XVI.1 Introduction

OTN equipment often consists of an electrical cross connect (EXC) subsystem and an optical cross connect or optical add/drop multiplexer (OXC/OADM) subsystem. These subsystems have traditionally been interconnected via fibres that connect the OTUk/OTUCn line cards with the OTSi(G) add/drop cards. More recently, these subsystems can be interconnected via an optical backplane that replaces the fibres.

The OCh/OTSiG overhead is typically terminated in the OXC/OADM subsystem (e.g., on the OTSiG add/drop cards), while the OTSiG is typically terminated in the EXC subsystem (on the OTUk/OTUCn line cards).

When both subsystems are from the same system vendor, fault management of both subsystems can be interconnected to support alarm suppression as specified for OTN in [ITU-T G.798]. From the functional model perspective, both subsystems behave as a single undivided system in which it does not matter how the system vendor has distributed the processes over the cards. Refer to Figure XVI.1.

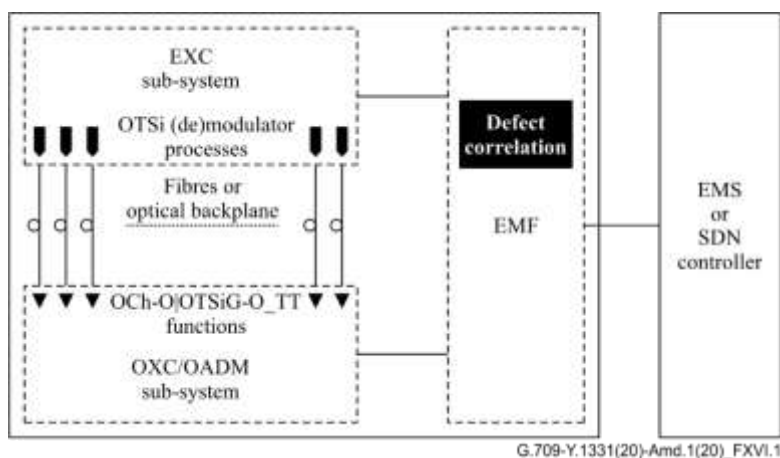
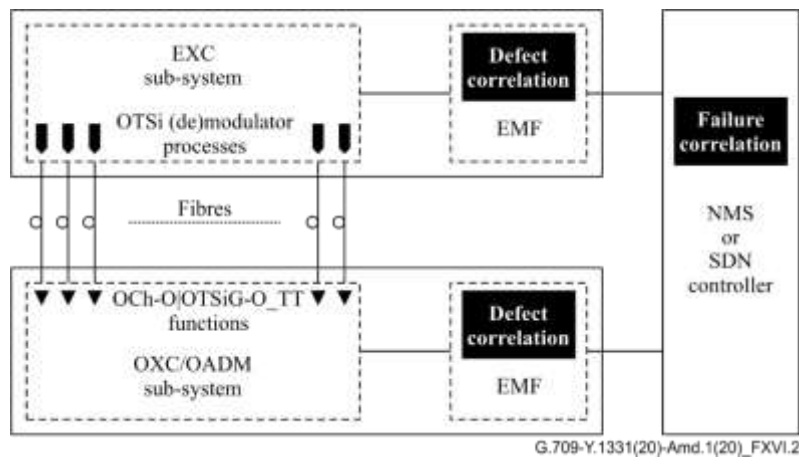


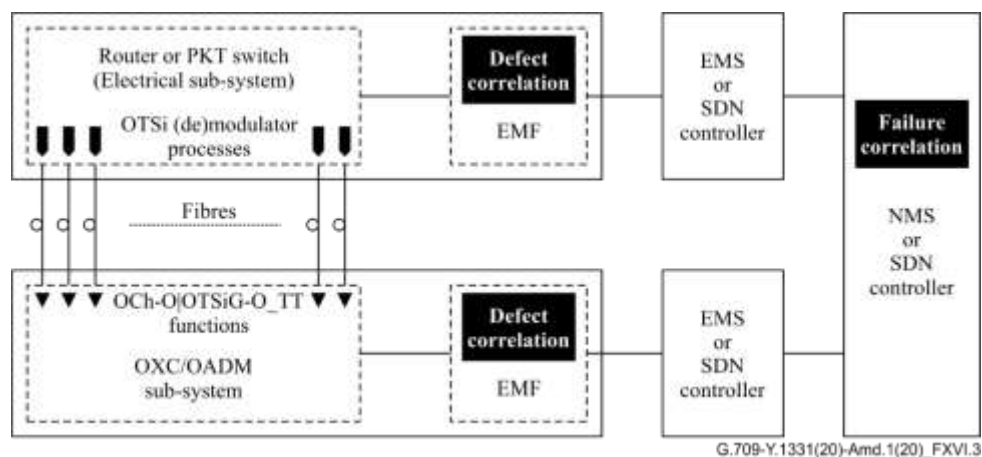
Figure XVI.1 – Single vendor OTN EXC and OXC/OADM scenario

When both subsystems are from different system vendors, fault management of both subsystems is typically not interconnected and alarm suppression as specified for OTN in G.798 is "broken". The OTN element management system or SDN controller that manages/controls both subsystems has to "glue together" the fault management and its alarm suppression. Refer to Figure XVI.2.



**Figure XVI.2 – Multi vendor OTN EXC and OXC/OADM scenario**

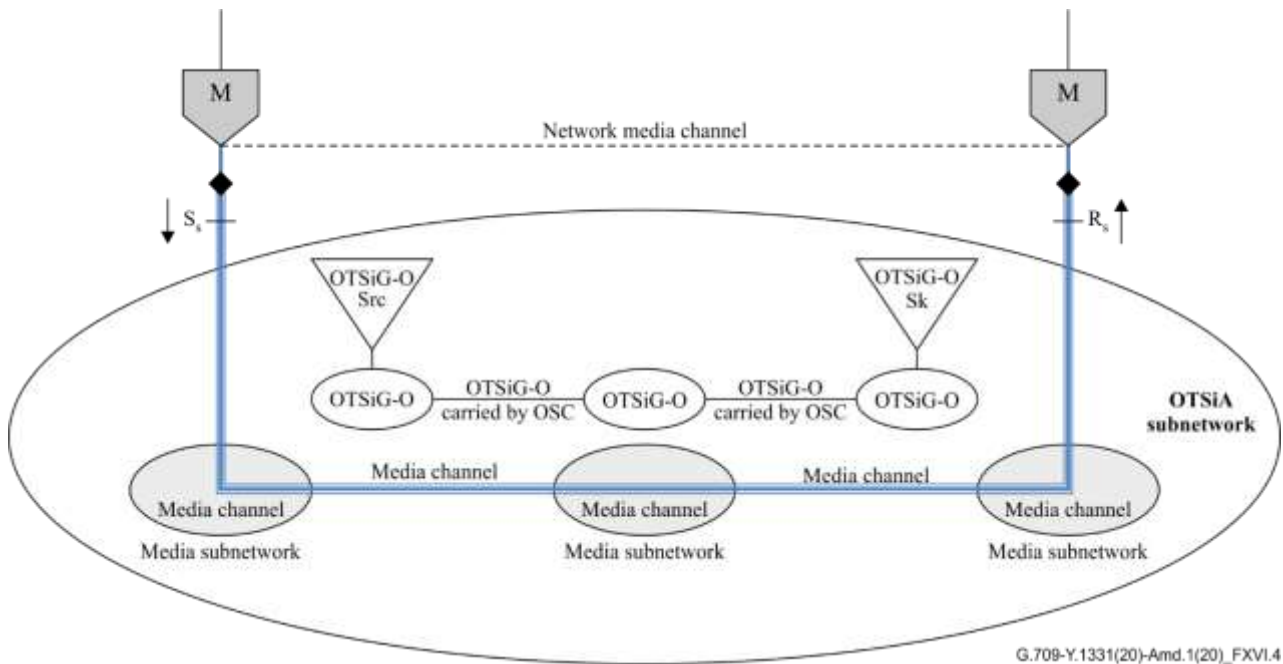
A similar situation is present when instead of an OTN EXC, a router or packet switch equipment's line cards (with OTSiG (de)modulator processes) are connected with the OTN OXC/OADM subsystem (with OCh|OTSiG overhead trail termination). For such case, different EMS or SDN controllers may be deployed, and therefore the network management system or SDN controller that manages/controls both circuit and packet layers has to "glue together" the fault management and alarm suppression. Refer to Figure XVI.3.



**Figure XVI.3 – Multi vendor router/PKT switch and OTN OXC/OADM scenario**

**XVI.2 Black link deployment without co-location of OTSiG (de)modulator and OTSiG-O\_TT/OCh-O\_TT function**

The two multi-vendor scenarios in Figures XVI.2 and XVI.3 are black link scenarios and ITU-T G.709 and [ITU-T G.7712] specify that the optical and electrical subsystems can be interconnected to transport the OCh|OTSiG overhead between the optical and electrical subsystems by means of an overhead communication channel (OCC) that is supported by the overhead communication network (OCN). The OCh-O\_TT or OTSiG-O\_TT functions and their OCh/OTSiG overhead processes would then be relocated to and supported in the electrical sub-system.



**Figure XVI.4 – Black link deployment without collocation of OTSiG (de)modulator and OTSiG-O\_TT/OCh-O\_TT function**

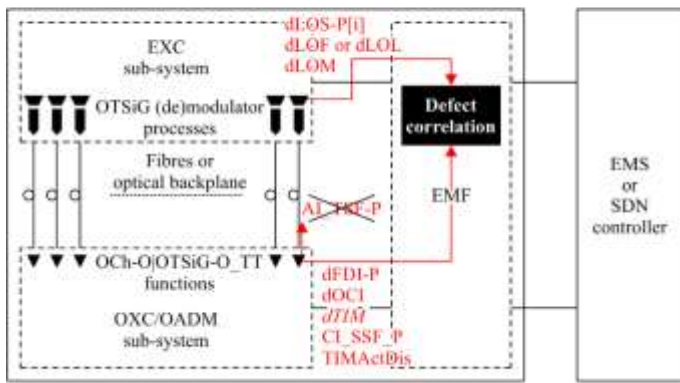
In black link scenarios without an OCC, as shown in Figure XVI.4, the OCh-O\_TT and OTSiG-O\_TT functions at the end of the black link are providing tandem connection monitoring for the OCh|OTSiA rather than path/network connection monitors.

Network connection monitoring for such case will rely on digital client (e.g., OTUk/OTUCn or ETH) related connection monitoring. Alarm suppression of OTSi loss of signal will have to be performed in the EMS, NMS or SDN controller by combining failure reports associated with the OCh-O\_TT\_Sk or OTSiG-O\_TT\_Sk functions at the edge of the OCh|OTSiA subnetwork with the loss-of-signal, -frame, -lock and -multi-frame failure reports associated with the OTSi(G)/<client>\_A function in the client equipment.

### **XVI.3 Failure correlation for black link deployment without collocation of OTSiG (de)modulator and OTSiG-O\_TT/OCh-O\_TT function**

Figure XVI.5 illustrates the defect correlation in the single vendor OTN EXC and OXC/OADM scenario, in which the defect correlation of the OTSi(G)/<client>\_A\_Sk function located in the EXC sub-system is performed in the common EMF, which mitigates for the missing AI\_TSF-P signal. The AI\_TSF-P term in the fault causes  $cXXX \leftarrow dXXX$  and ..... and (not AI\_TSF-P) is replaced by its set of defect conditions detected in the OCh-O\_TT\_Sk or OTSiG-O\_TT\_Sk functions; i.e., by CI\_SSF\_P or dOCI or dFDI-P or (dTIM and (not TIMActDIS)).

$cLOS-P \leftarrow \sum dLOS-P[i]$  and (not (CI\_SSF-P or dOCI or dFDI or (dTIM and (not TIMActDis))))  
 $cLOF \leftarrow dLOF$  and (not  $\sum dLOS-P[i]$ ) and (not (CI\_SSF-P or dOCI or dFDI-P or (dTIM and (not TIMActDis))))  
 $cLOL \leftarrow dLOL$  and (not  $\sum dLOS-P[i]$ ) and (not (CI\_SSF-P or dOCI or dFDI-P or (dTIM and (not TIMActDis))))  
 $cLOM \leftarrow dLOM$  and (not  $\sum dLOS-P[i]$ ) and (not dLOF) and (not (CI\_SSF-P or dOCI or dFDI-P or (dTIM and (not TIMActDis))))  
 $cLOM \leftarrow dLOM$  and (not dLOL) and (not (CI\_SSF-P or dOCI or dFDI-P or (dTIM and (not TIMActDis))))



G.709-Y.1331(20)-Amd.1(20)\_FXV1.5

$AI\_TSF-P = aTSF-P \leftarrow CI\_SSF-P$  or dOCI or dFDI-P or (dTIM and (not TIMActDis))

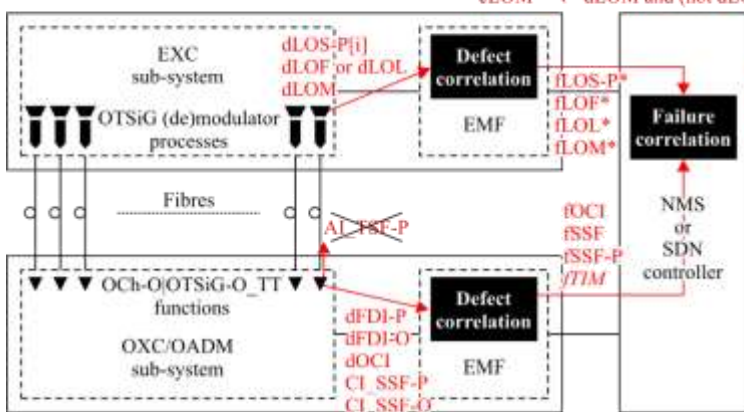
**Figure XVI.5 – Defect correlation in single vendor OTN EXC and OXC/OADM scenario**

Figure XVI.6 illustrates the failure correlation in the multi-vendor OTN EXC and OXC/OADM scenario, in which the defect correlation of the OTSi(G)/<client>\_A\_Sk function located in the EXC sub-system can only partly be performed in the EMF in absence of the AI\_TSF-P input signal. The fault causes are therefore marked with a "\*" (cXXX\*), as well as the failures (fXXX\*).

The correlation with the AI\_TSF-P term is to be performed in a Failure Correlation process in the EMS or SDN controller. Instead of defects, this correlation has to use the failures from the OCh-O\_TT\_Sk or OTSiG-O\_TT\_Sk function: fOCI, fSSF, fSSF-P and fTIM.

The AI\_TSF-P term in the failures  $fXXX \leftarrow fXXX^*$  and (not AI\_TSF-P) is replaced by its set of failures from the OCh-O\_TT\_Sk or OTSiG-O\_TT\_Sk functions; i.e., by fSSF or SSF-P or fOCI or fTIM.

$cLOS-P^* \leftarrow \sum dLOS-P[i]$   
 $cLOF^* \leftarrow dLOF$  and (not  $\sum dLOS-P[i]$ )  
 $cLOL^* \leftarrow dLOL$  and (not  $\sum dLOS-P[i]$ )  
 $cLOM^* \leftarrow dLOM$  and (not  $\sum dLOS-P[i]$ ) and (not dLOF)  
 $cLOM^* \leftarrow dLOM$  and (not dLOL)



G.709-Y.1331(20)-Amd.1(20)\_FXV1.6

$fLOS-P \leftarrow fLOS-P^*$  and (not (fSSF or fSSF-P or fOCI or fTIM))  
 $fLOF \leftarrow fLOF^*$  and (not (fSSF or fSSF-P or fOCI or fTIM))  
 $fLOL \leftarrow fLOL^*$  and (not (fSSF or fSSF-P or fOCI or fTIM))  
 $fLOM \leftarrow fLOM^*$  and (not (fSSF or fSSF-P or fOCI or fTIM))  
 $cOCI \leftarrow dOCI$  and (not CI\_SSF-P) and (not CI\_SSF-O) and (not FDI-O) and (not FDI-P)  
 $cSSF \leftarrow (CI\_SSF-P$  or dFDI-P) and (CI\_SSF-O or dFDI-O)  
 $cSSF-P \leftarrow (CI\_SSF-P$  or dFDI-P) and (not cSSF)  
 $cSSF-O \leftarrow (CI\_SSF-O$  or dFDI-O) and (not cSSF)

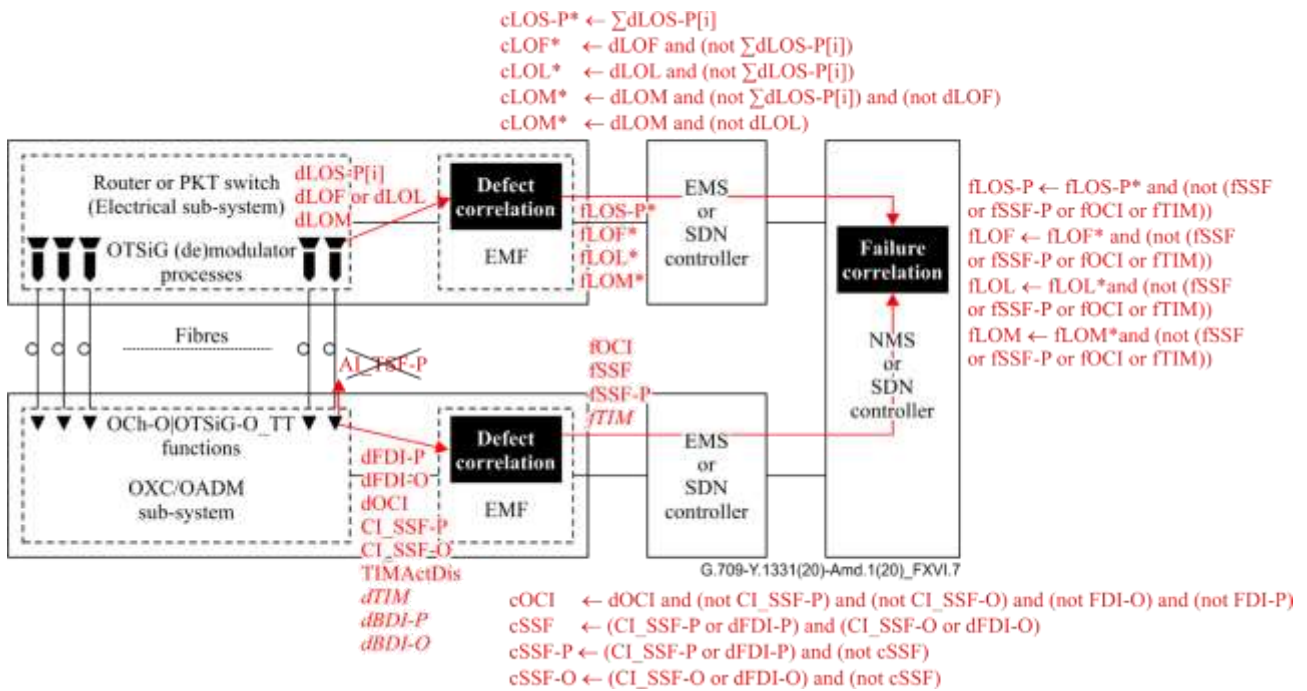
**Figure XVI.6 – Failure correlation in multi-vendor OTN EXC and OXC/OADM scenario**

Figure XVI.7 illustrates the failure correlation in the multi-vendor router/PKT switch and OXC/OADM scenario, in which the defect correlation of the OTSi(G)/<client>\_A\_Sk function

located in the router/PKT switch sub-system can only partly be performed in the EMF in absence of the AI\_TSF-P input signal. The fault causes are therefore marked with a "\*" (cXXX\*) as well as the failures (fXXX\*).

The correlation with the AI\_TSF-P term is to be performed in a Failure Correlation process in the EMS or SDN Controller. Instead of defects, this correlation has to use the failures from the OCh-O\_TT\_Sk or OTSiG-O\_TT\_Sk function: fOCI, fSSF, fSSF-P and fTIM.

The AI\_TSF-P term in the failures  $fXXX \leftarrow fXXX^*$  and (not AI\_TSF-P) is replaced by its set of failures from the OCh-O\_TT\_Sk or OTSiG-O\_TT\_Sk functions; i.e. by fSSF or SSF-P or fOCI or fTIM.



**Figure XVI.7 – Failure correlation in multi-vendor router/PKT switch and OTN OXC/OADM scenario**

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