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**OTU4 long-reach interface**

Recommendation ITU-T G.709.2/Y.1331.2

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# Recommendation ITU-T G.709.2/Y.1331.2

## OTU4 long-reach interface

### Summary

Recommendation ITU-T G.709.2/Y.1331.2 specifies an interface for an OTU4 long-reach interconnect application. The text of this recommendation is intentionally kept separate from the main ITU-T G.709 text and from other adjoints like the ITU-T G.709.1 and ITU-T G.709.3 texts.

### History

Edition	Recommendation	Approval	Study Group	Unique ID*
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### Keywords

FEC, OTN, OTU4, long reach, staircase FEC.

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# Recommendation ITU-T G.709.2/Y.1331.2

## OTU4 long-reach interface

### 1 Scope

This Recommendation specifies requirements for the optical transport network (OTN) long-reach interface OTU4-SC (completely standardized 100G optical transport unit order 4 for long-reach applications with staircase forward error correction (FEC)), which is intended for those OTU4-type applications that require a higher FEC coding gain than available from the ITU-T G.709 FEC.

The OTU4-SC interface complements the existing functions specified in [ITU-T G.709], such as OTUk frame, ODUk/flex (where ODU is optical data unit), with a new hard-decision FEC codec, which uses the same overhead (OH) rate (~6.7%) as the OTU4 FEC codec.

This Recommendation makes use of existing [ITU-T G.709], [ITU-T G.798] and [b-ITU-T G-Sup. 58] functions by reference and it provides specifications for new functions that are specific to this new interface type. In addition, some introduction material for intended applications is included.

### 2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

- [ITU-T G.709] Recommendation ITU-T G.709/Y.1331 (2016), *Interfaces for the optical transport network*.
- [ITU-T G.798] Recommendation ITU-T G.798 (2017), *Characteristics of optical transport network hierarchy equipment functional blocks*.
- [ITU-T G.870] Recommendation ITU-T G.870/Y.1352 (2016), *Terms and definitions for optical transport networks (OTN)*.
- [ITU-T G.872] Recommendation ITU-T G.872 (2017), *Architecture of optical transport networks*.
- [ITU-T G.959.1] Recommendation ITU-T G.959.1 (2018), *Optical transport network physical layer interfaces*.
- [ITU-T G.975.1] Recommendation ITU-T G.975.1 (2004), *Forward error correction for high bit-rate DWDM submarine systems*.

### 3 Definitions

#### 3.1 Terms defined elsewhere

This Recommendation uses the following terms defined elsewhere:

##### 3.1.1 Terms defined in [ITU-T G.709]:

- completely standardized OTUk (OTUk)
- functionally standardized OTUk (OTUkV)

- optical data unit k (ODUk)
- optical payload unit k (OPUk)
- optical transport network (OTN)

### 3.1.2 Terms defined in [ITU-T G.959.1]:

- optical tributary signal (OTSi)

### 3.1.3 Terms defined in [ITU-T G.975.1]:

- coding gain
- net coding gain (NCG)

## 3.2 Terms defined in this Recommendation

This Recommendation defines the following terms:

**3.2.1 Base Block:** A Base Block is the  $8 \times 32640$  bit block as illustrated in Figure A.4 (left), consisting of an  $8 \times 30592$  bit "base information block" and an  $8 \times 2048$  bit "base parity block".

**3.2.2 OTU4-SC:** A completely standardized 100G optical transport unit order 4 for long-reach applications with staircase forward error correction (OTU4-SC) is an information structure consisting of an OTU4-v that uses staircase forward error correction (FEC) parity and overhead.

**3.2.3 OTL4.4-SC:** A group of four optical transport lanes that carry one completely standardized 100G optical transport unit order 4 for long-reach applications with staircase forward error correction (OTL4.4-SC) is an OTU4-SC interface using four parallel OTL4.4-SC lanes.

NOTE – "OTL4.4-SC" is the OTU4-SC equivalent of "OTLk.m" for OTUk as defined in [ITU-T G.709].

**3.2.4 OTL4.4-SC lane:** A group of four optical transport lanes that carry one completely standardized 100G optical transport unit order 4 for long-reach applications with staircase forward error correction (OTL4.4-SC) lane is an electrical or optical lane of an OTL4.4-SC.

## 4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

AWGN	Additive White Gaussian Noise
BCH	Bose, Chaudhuri and Hocquenghem
BER	Bit Error Rate
DWDM	Dense Wavelength Division Multiplexing
EDD	Error Decorrelator De-interleaver
EDI	Error Decorrelator Interleaver
EXC	Electrical Cross-Connect
FEC	Forward Error Correction
FlexO	Flexible Optical transport network
GF	Galois Field
HD	Hard Decision
L	Level
LSB	Least Significant Bit
MBAS	Multi Block Alignment Signal



MFAS	Multi-Frame Alignment Signal
MSB	Most Significant Bit
NCG	Net Coding Gain
OCh	Optical Channel
ODU	Optical Data Unit
ODU4	Optical Data Unit order 4
OH	Overhead
OPU	Optical Payload Unit
OTL4.4-SC	group of four Optical Transport Lanes that carry one OTU4-SC
OTN	Optical Transport Network
OTSi	Optical Tributary Signal
OTSiA	Optical Tributary Signal Assembly
OTU	Optical Transport Unit
OTUk-v	Optical Transport Unit k with vendor specific OTU FEC
OTU4	completely standardized Optical Transport Unit order 4
OTU4-SC	completely standardized 100G Optical Transport Unit order 4 for long-reach applications with Staircase forward error correction
PMOH	Path Monitoring Overhead
RS	Reed-Solomon
SC FEC	Staircase Forward Error Correction
TCTandem Connection	
TCMOH	Tandem Connection Monitoring Overhead

## 5 Conventions

This Recommendation uses the following conventions specified in [ITU-T G.709]:

- k
- m
- n
- r

**Transmission order:** The order of transmission of information in all diagrams in this Recommendation is first from left to right and then from top to bottom. Within each byte, the most significant bit (MSB) is transmitted first. The MSB (bit 1) is illustrated at the left in all diagrams.

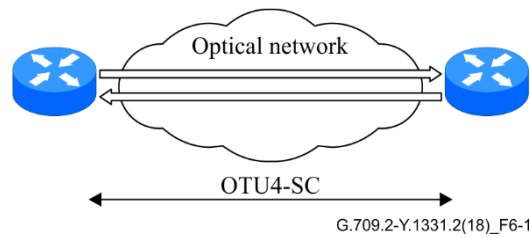
**Value of reserved bit(s):** The value of an OH bit, which is reserved or reserved for future international standardization, shall be set to "0".

**Value of non-sourced bit(s):** Unless stated otherwise, any non-sourced bits shall be set to "0".

## 6 Introduction and applications

OTU4-SC is an interoperable interface for metro or long-reach application. It provides connections over dense wavelength division multiplexing (DWDM) as depicted in Figure 6-1.

In order to mitigate the impairments of accumulated noise it uses a hard decision-forward error correction (HD-FEC) with ~6.7% redundancy that provides a net-coding gain of 8.35 dB (see also clause A.5.3) at an output bit error rate (BER) of  $10^{-12}$  on the additive white gaussian noise (AWGN) channel.



**Figure 6-1 – OTU4-SC deployment overview**

The OTU4-SC interface may be deployed in various scenarios, in particular for completely standardized optical transport unit order 4-type (OTU4-type) applications requiring a higher FEC coding gain than available from the ITU-T G.709 FEC.

Example applications are given in Appendix I.

## **7 Structure and processes**

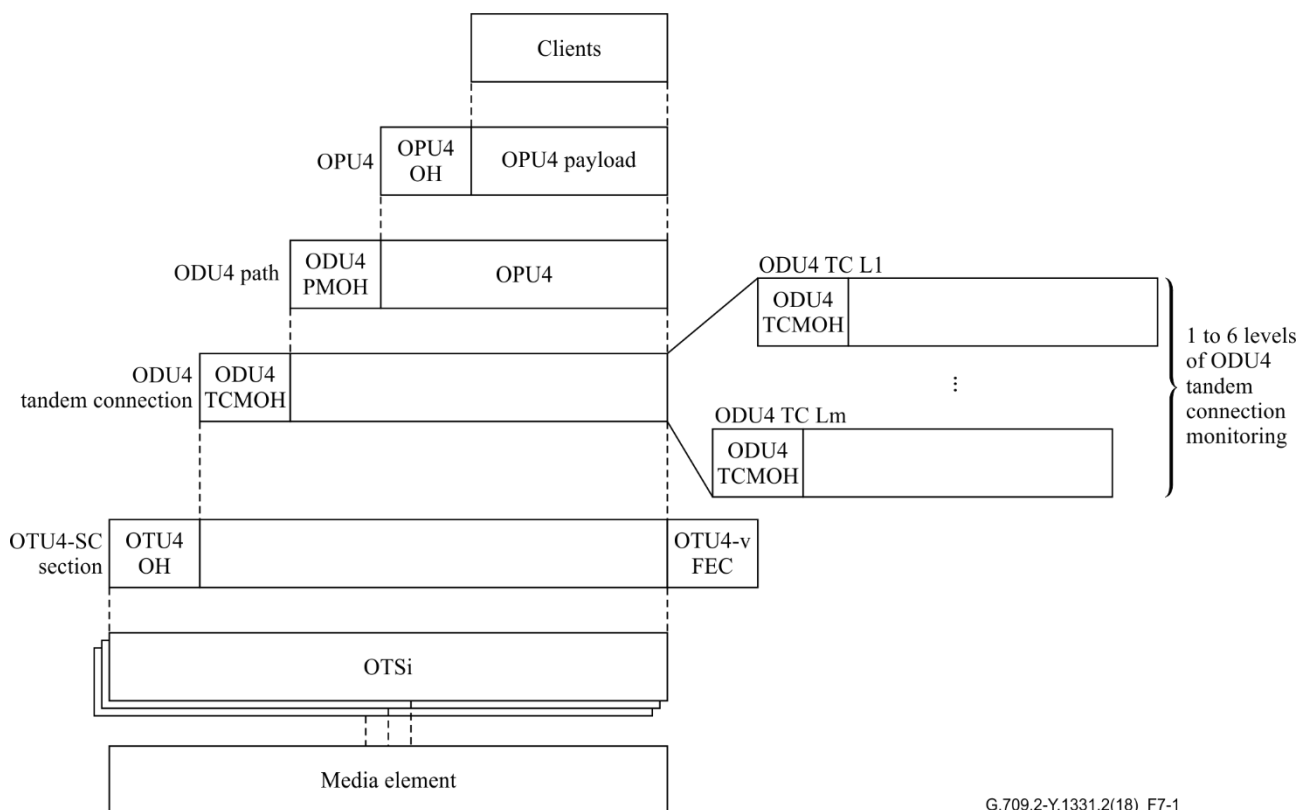
This clause specifies the basic signal structure, processes and atomic functions for the OTU4-SC interface.

### **7.1 Basic signal structure**

The OTU4-SC interface is specified for long-reach applications with the OTU4-SC functional model specified in [ITU-T G.872].

NOTE – The physical optical interface specifications lie outside the scope of this Recommendation.

The information structure for the OTU4-SC interface is represented by information containment relationships and information flows. The principal information containment relationship is shown in Figure 7-1.



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**Figure 7-1 – OTU4-SC principal information containment relationship**

## 7.2 Processing and information flow

Functions and information flows are specified in [ITU G.798].

## 8 OTU4-SC frame

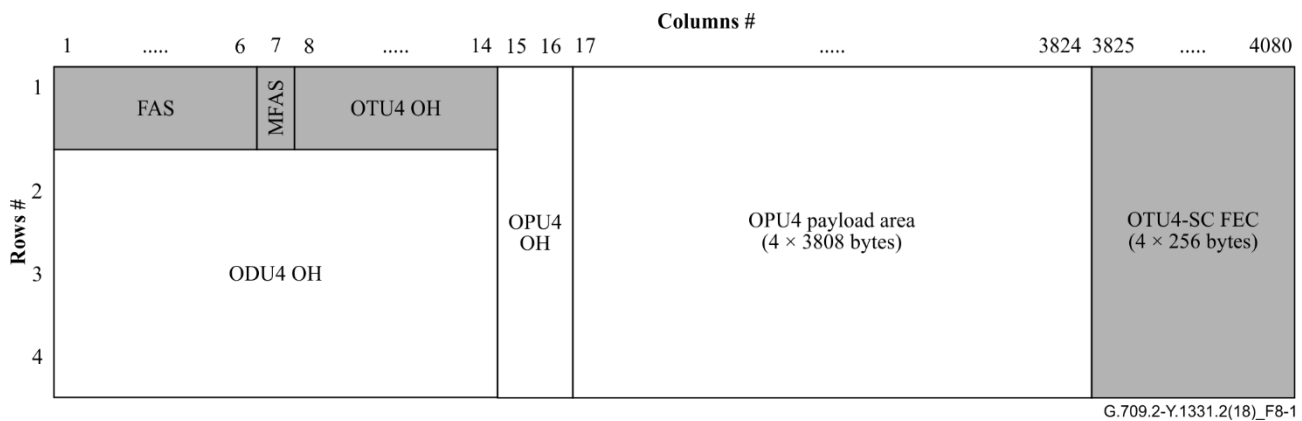
An OTU4-SC frame is based on an optical transport unit  $k$  with vendor specific OTU FEC (OTU $k$ -v ( $k = 4$ )) frame and transport unit as specified in [ITU-T G.709] and uses an alternative FEC that consumes the same OH byte allocation as the RS(255,239) code (where RS is Reed-Solomon) specified in [ITU-T G.709] for OTU4.

For the OTU4-SC FEC specification, see clause 8.3.

### 8.1 Frame structure

The OTU4-SC frame structure follows the specification given in clause 11.1 of [ITU-T G.709], i.e., it is based on the optical data unit order 4 (ODU4) frame structure, but extends it with an FEC as shown in Figure 8-1. Added to the ODU4 frame are 256 columns for the FEC. The reserved OH bytes in row 1, columns 8 to 14 of the ODU4 OH are used for an OTU4 specific OH, resulting in an octet-based block frame structure with four rows and 4080 columns. The MSB in each octet is bit 1, the least significant bit (LSB) is bit 8

NOTE – The OTU4-SC frame structure is similar to Figure II.2 of [ITU-T G.709].



**Figure 8-1 – OTU4-SC frame structure**

## 8.2 Bit rate

The OTU4-SC bit rate is  $255/227 \times 99\,532\,800$  kbit/s  $\pm 20$  ppm. It is the same bit rate as specified in [ITU-T G.709] for OTU4.

NOTE – The nominal OTU4-SC bit rate is approximately 111 809 973.568 kbit/s.

## 8.3 Forward error correction

The OTU4-SC FEC code is a generalized staircase code based on 512-bit  $\times$  510-bit blocks that works in conjunction with an error decorrelator function. The error decorrelator function is used to randomize the positions of the bit errors as seen by the decoder in order to reduce the impact of correlated errors on FEC performance. The staircase FEC code is a systematic code and the codec uses the same 6.7% FEC OH area as the ITU-T G.709 FEC.

The generic operation of a staircase FEC codec (including error decorrelator) is specified in Annex A. The OTU4-SC specific aspects of the staircase FEC operation are specified in Annex B.

## 9 Overhead

The OTU4-SC frame supports OTU4 OH as specified in clauses 15.6 and 15.7 of [ITU-T G.709].

## 10 Scrambling

Scrambling of the OTU4-SC signal is performed after FEC computation and insertion into the OTU4-SC signal as specified in clause 11.2 of [ITU-T G.709].

## 11 Adaptation of OTU4-SC to a 4-lane interface

The adaptation of the OTU4-SC data signal to four lanes follows the OTL4.4 format specified in Annex C of [ITU-T G.709]. This includes lane reordering and de-skewing.

Each OTL4.4-SC physical lane carries five bit-multiplexed logical lanes of an OTU4-SC following the logical lane format specified in Annex C of [ITU-T G.709].

The OTL4.4-SC bit rate of a lane is  $255/227 \times 24\,883\,200$  kbit/s  $\pm 20$  ppm. It is the same bit rate as specified in [ITU-T G.709] for OTL4.4.

NOTE – The nominal OTL4.4-SC bit rate is approximately 27 952 493.392 kbit/s.

## Annex A

### Forward error correction using $512 \times 510$ staircase codes

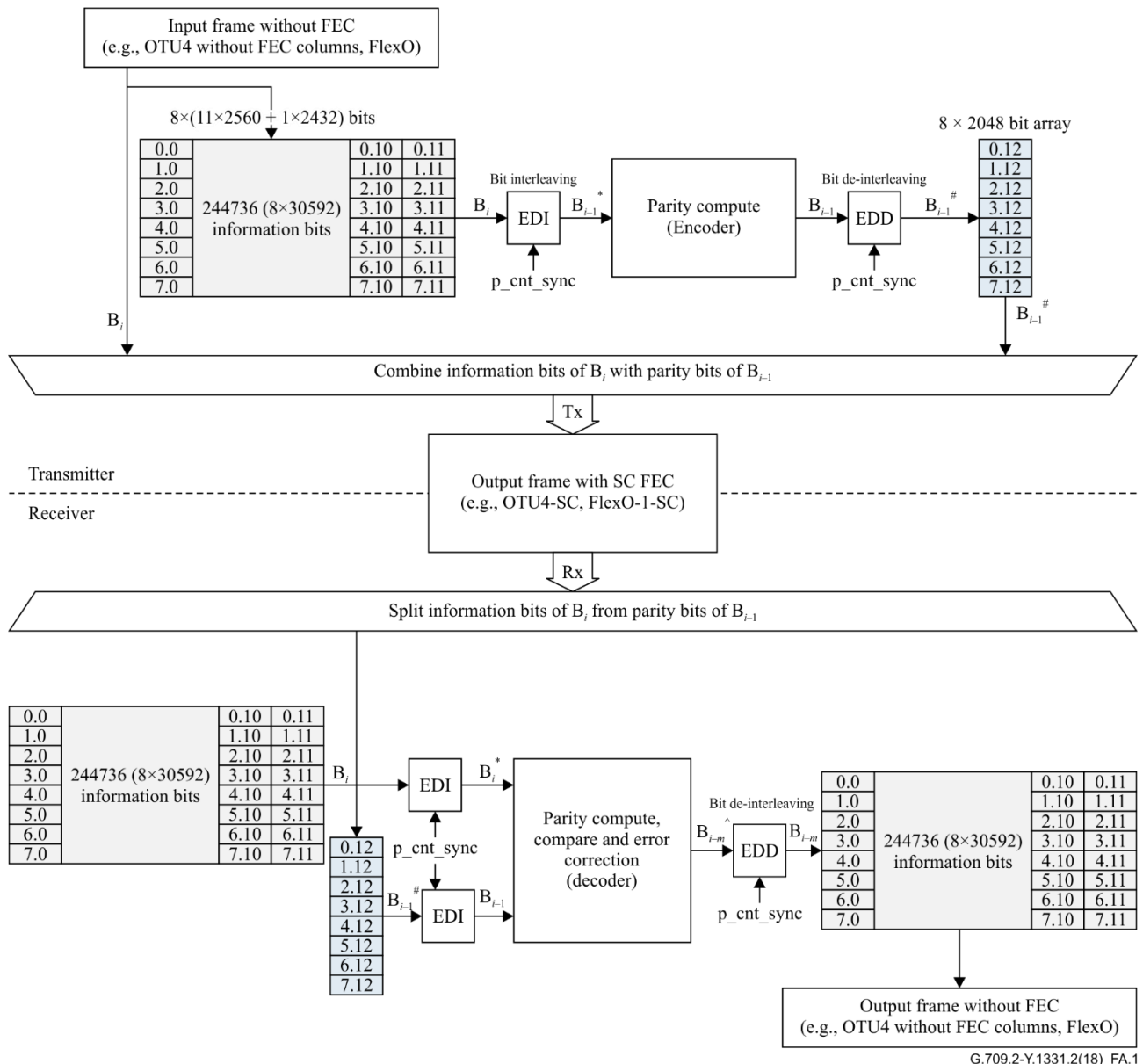
(This annex forms an integral part of this Recommendation.)

#### A.1 Introduction

Appendix II describes the general principles of FEC using blockwise recursively encoded staircase forward error correction (SC FEC) of  $m \times m$  staircase blocks. This annex specifies the operation of an FEC codec for a  $512 \times 510$  staircase code (SC FEC), which is sandwiched between a  $30592 + 2048$  bit wide optimized error decorrelator interleaver (EDI) and error decorrelator de-interleaver (EDD) as illustrated for the transmit side in Figure A.1.

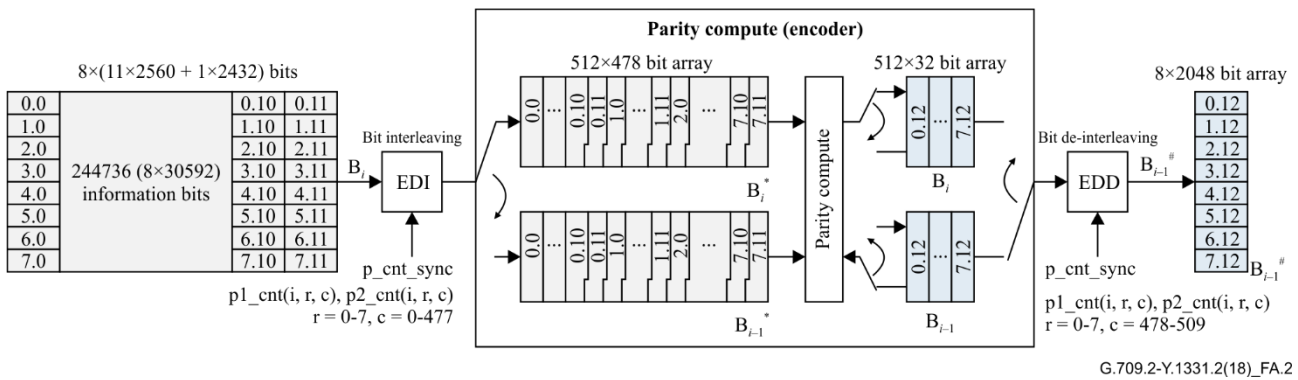
The SC FEC codec can be used for multiple types of signals, e.g., OTU4 and flexible optical transport network (FlexO) data streams. The information bits from an input signal frame are mapped into an SC FEC specific  $8 \times 30592$  bit "base information block" format (see clause A.2), after which SC FEC specific transmit side processing is performed and parity bits become available in an SC FEC specific  $8 \times 2048$  bit "base parity block" format (see clause A.2). As a last step, the information bits and the computed parity bits are mapped into the output frame. On the receive side, the information and parity bits in the input signal frame are mapped into SC FEC specific "base information and parity blocks" after which SC FEC specific receive side processing is performed and decoded information bits become available in the SC FEC specific "base information block" format. These decoded information bits are then output in the signal specific frame format.

For each type of signal, e.g., OTU4 and FlexO data streams, a specification will be provided (in an Annex B of the corresponding Recommendation) that describes the relationship between input and output frames at the FEC encoder and decoder.



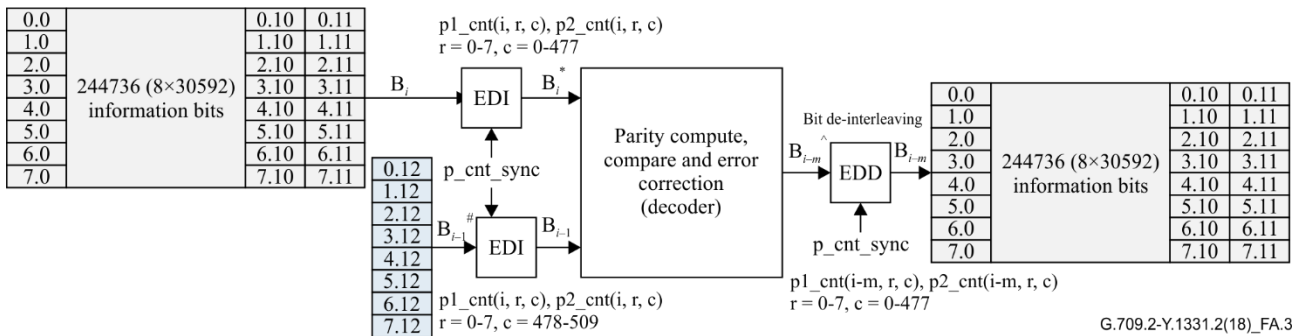
**Figure A.1 – Transmitter and receiver staircase forward error correction processing**

In the transmitter (Figure A.2), the information bits of an  $8 \times 30592$  bit "base information block"  $B_i$  (in a row-by-row, i.e., a left-to-right, top-to-bottom order) are passed through an EDI process (see clause A.3) after which the interleaved information bits in block  $B_i^*$  are written into a  $512 \times 478$  bit array (in a column-by-column, i.e., top-to-bottom, left-to-right order). In parallel, the parity bits in a  $512 \times 32$  bit array holding the parity computed over the previous  $8 \times 30592$  bit "base information block"  $B_{i-1}$  are passed through (in a column-by-column, i.e., top-to-bottom, left-to-right order) an EDD process (see A.3) after which the de-interleaved parity bits  $B_{i-1}^\#$  are written into a  $8 \times 2048$  bit array. SC FEC parity is computed over the information bits of the block ( $B_i^*$ ) within the  $512 \times 478$  bit array, the information bits of the previous block ( $B_{i-1}^*$ ) that are located in the other  $512 \times 478$  bit array and the parity bits in a  $512 \times 32$  bit array containing the parity bits of the previous computation ( $B_{i-1}$ ) as specified in A.5.1. The computed parity bits are written in a row-by-row basis in the other  $512 \times 32$  bit parity array ( $B_i$ ). The information bits of  $B_i$  and the computed parity bits of block  $i - 1$  ( $B_{i-1}^\#$ ) are combined and transmitted within the output frame format.



**Figure A.2 – Transmitter staircase forward error correction processing**

In the receiver (Figure A.3), the received information bits of  $B_i$  and parity bits of  $B_{i-1}$  are passed through an EDI process (see clause A.3), after which the interleaved information and parity bits are written into one of  $m$   $512 \times 478$  and  $512 \times 32$  bit arrays (in a column-by-column, i.e., top-to-bottom, left-to-right order); details for  $m$  are specified in clause A.5.2. In parallel, the corrected information bits in a  $512 \times 478$  bit array holding the interleaved bits of information of block  $i - m$  ( $B_{i-m}^\wedge$ ) are passed through (in a column-by-column, i.e., top-to-bottom, left-to-right order) an EDD process after which the de-interleaved information bits  $B_{i-m}$  are mapped in a  $8 \times 30592$  bit block structure (in a row-by-row, i.e., a left-to-right, top-to-bottom order). SC FEC codes are decoded by iteratively decoding the component codewords within a decoding window as specified in clause A.5.2. The decoded information bits in block  $B_{i-m}$  are written in a row-by-row basis into the  $8 \times 30592$  bit "base information block".



**Figure A.3 – Receiver staircase forward error correction processing**

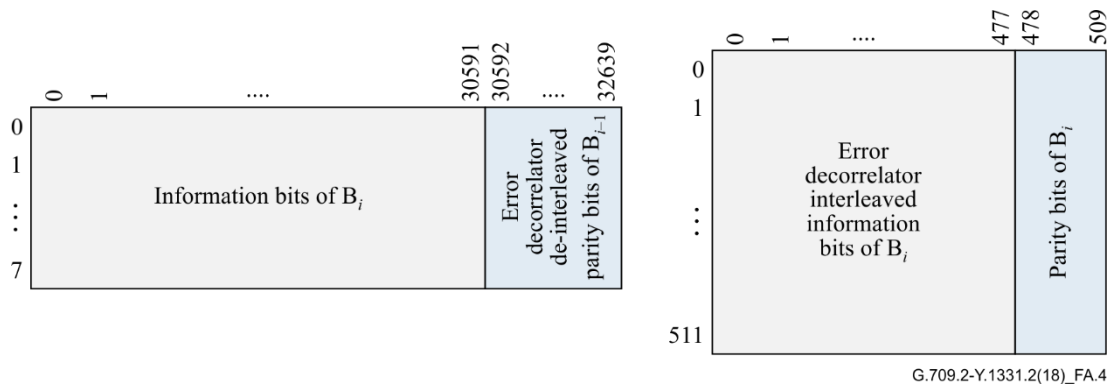
## A.2 $8 \times 32640$ bit base block (Base Block) and $512 \times 510$ bit staircase block

This clause specifies an  $8 \times 32640$  bit base block (Base Block), a  $512 \times 510$  bit staircase block (Figure A.4) and a mapping of bits between these two block formats (Figure A.5).

A Base Block ( $8 \times 32640$  bit) (Figure A.4, left) consists of 261120 bits, 244736 information bits and 16384 parity bits. The information bits are located in the first 30592 1-bit columns (0 to 30591) and the parity bits are located in the last 2048 1-bit columns (30592 to 32639). The first 30592 columns contain the information bits of  $B_i$ , while the last 2048 columns contain the error decorrelator de-interleaved parity bits of  $B_{i-1}$ . As shown in Figure A.4, the Base Block carries the information bits of the current  $512 \times 510$  bit staircase block  $B_i$  and the parity bits of the previous  $512 \times 510$  bit staircase block  $B_{i-1}$ .

A  $512 \times 510$  bit staircase block (Figure A.4, right) consists of 261120 bits, 244736 information bits and 16384 parity bits. The information bits are located in the first 478 1-bit columns (0 to 477) and the parity bits are located in the last 32 1-bit columns (478 to 509). The first 478 columns contain the

error decorrelator interleaved information bits of  $B_i$ , while the last 32 columns contain the parity bits of  $B_i$ .



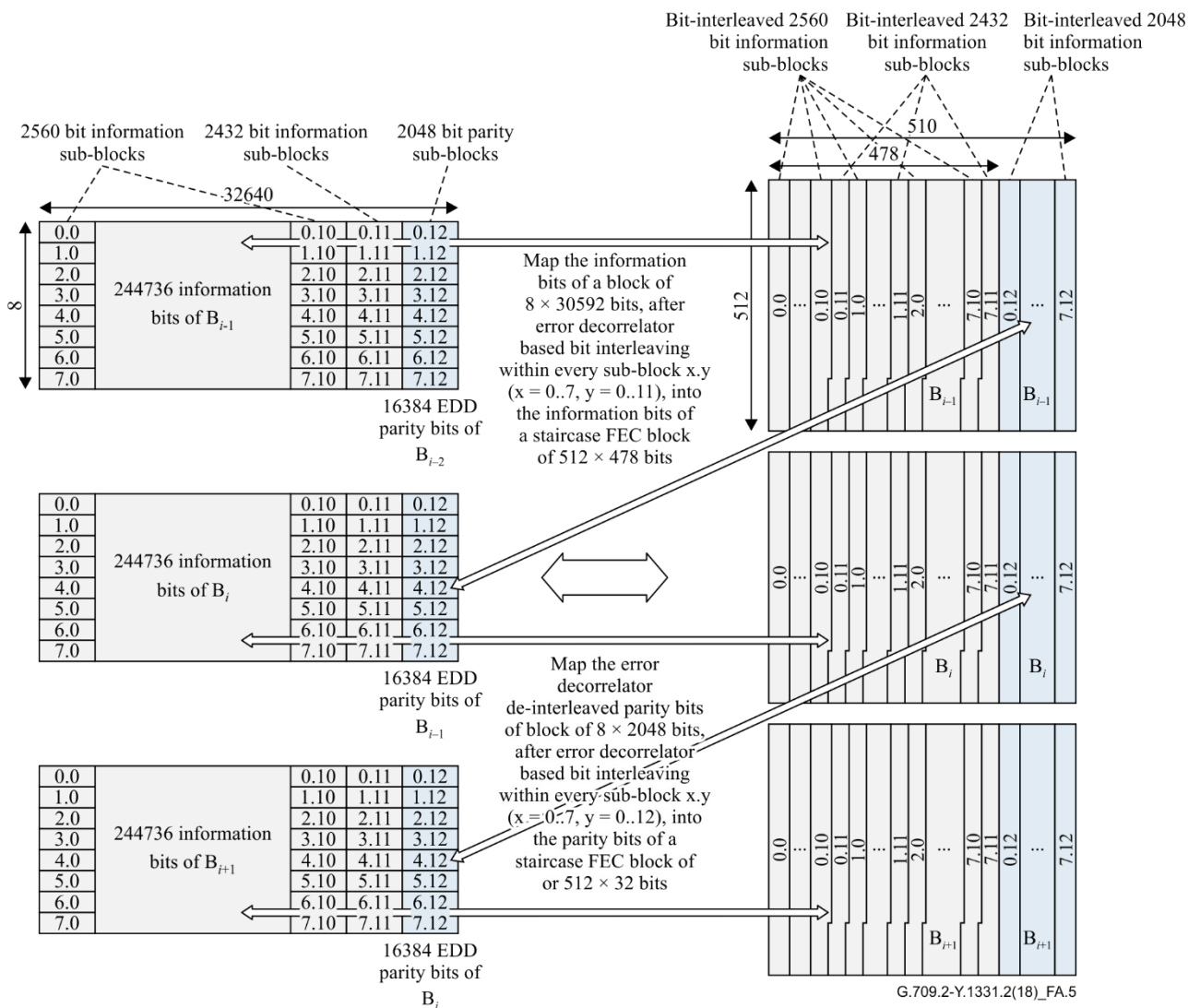
**Figure A.4 –  $8 \times 32640$  bit base block (Base Block, left) and  $512 \times 510$  bit staircase block formats (right)**

The relationship of the bits in these two block formats is illustrated in Figure A.5.

Each 32640 bit row in the Base Block is divided into 13 sub-blocks  $x.y$ , with  $x = 0..7$  and  $y = 0..12$ . Sub-blocks  $x.0$  to  $x.10$  contain  $40 \times 64 = 2560$  bits, sub-blocks  $x.11$  contain  $38 \times 64 = 2432$  bits and sub-blocks  $x.12$  contain  $32 \times 64 = 2048$  bits (specified in clause A.3 and illustrated in Appendix III).

- The  $512 \times 510$  bit staircase block contains error decorrelator interleaved versions of these  $x.y$  sub-blocks in the  $8 \times 32640$  bit input and output block as illustrated in Figure A.2. The 2560, 2432 and 2048 interleaved bits in a sub-block are mapped in a top-to-bottom, left-to-right order into the equivalent  $x.y$  sub-blocks in the  $512 \times 510$  bit staircase block. For example, the error decorrelator interleaved 2560 bits of sub-block 0.0 in the first row of the Base Block  $i$  are located in the first five columns of a  $512 \times 510$  bit staircase block  $B_i$ . The first bit of the interleaved 2560 bits of sub-block 0.0 is located in the bit in row #0, column #0 of the  $512 \times 510$  bit staircase block, the second bit of the interleaved 2560 bits of sub-block 0.0 is located in the bit in row #1, column #0 and the last bit of the interleaved 2560 bits of sub-block 0.0 is located in the bit in row #511, column #4.
- The error decorrelator interleaved 2048 bits of sub-block 7.12 in the last row of the Base Block  $i$  are located in the last four columns of a  $512 \times 510$  bit staircase block  $B_{i-1}$ . The first bit of the interleaved 2048 bits of sub-block 7.12 is located in the bit in row #0, column #506 of the  $512 \times 510$  bit staircase block, the second bit of the interleaved 2048 bits of sub-block 7.12 is located in the bit in row #1, column #506 and the last bit of the interleaved 2048 bits of sub-block 7.12 is located in the bit in row #511, column #509.





**Figure A.5 – Bit relationship between  $8 \times 32640$  bit and  $512 \times 510$  bit formats**

### A.3 $8 \times 32640$ bit base block (Base Block) error decorrelator interleaver and de-interleaver

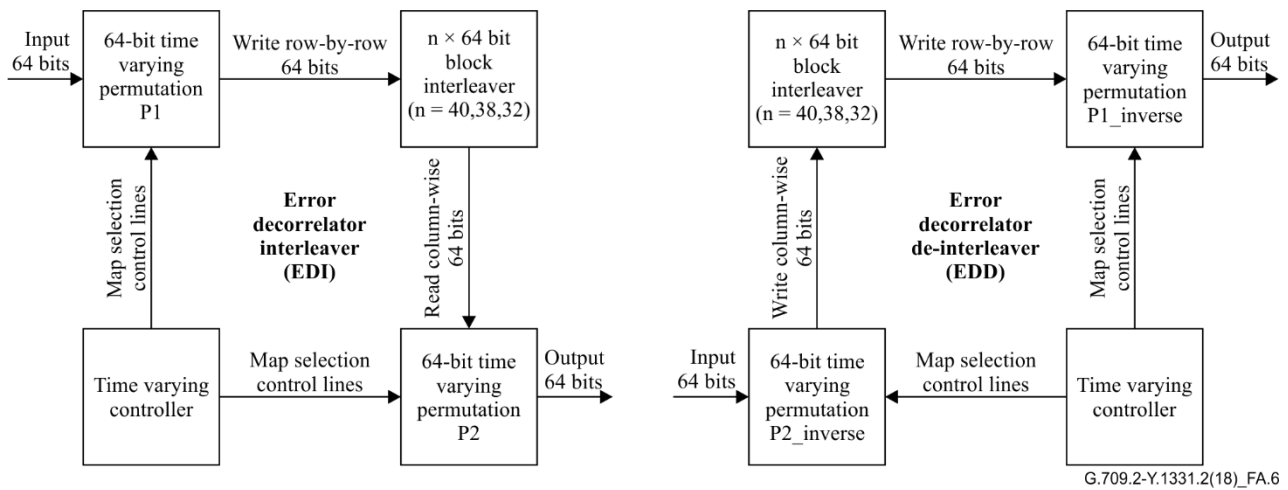
The error decorrelator function described in clause II.2 is designed for an  $m \times m$  bit SC FEC block. An adaptation for a  $512 \times 510$  SC FEC block is required. Figure A.6 illustrates this adaptation, which is located in the block interleaver process. Instead of a  $64 \times 64$  bit block interleaver, the  $512 \times 510$  staircase block interleaver process provides a  $40, 38$  or  $32 \times 64$  bit block interleaver process.

The left side of Figure A.6 shows a 2560, 2432 or 2048 bit interleaver, implemented by passing a  $40, 38$  or  $32 \times 64$ -bit data stream through a time-varying 64-bit block permutation P1, the output of which is written to a  $40/38/32 \times 64$  bit block interleaver array in row-by-row fashion. This block of data is then read columnwise (top-to-bottom, left-to-right) and every block of 64-bits is passed through a 64-bit time-varying 64-element block permutation P2.

The right side of Figure A.6 shows a 2560, 2432 or 2048 bit de-interleaver, implemented by passing a  $40, 38$  or  $32 \times 64$ -bit data stream through a time-varying 64-bit block permutation P2<sub>inverse</sub>, the output of which is written to a  $40/38/32 \times 64$  bit block interleaver array in column-wise fashion. This block of data is then read row-by-row and every 64-bit block is passed through a 64-bit time-varying 64-element block permutation P1<sub>inverse</sub>.

Refer to Appendix III for an illustration of the block interleaver and de-interleaver arrays.

With this set of fixed block interleavers, the data and parity are never mixed.



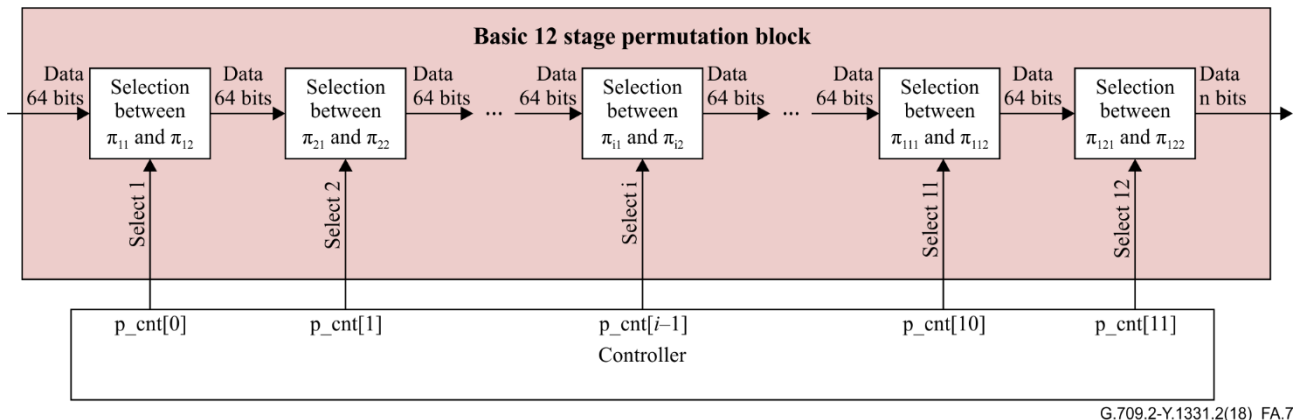
**Figure A.6 – Error decorrelator interleaver and de-interleaver (EDI, EDD)**

### Time-varying Permutations

P1 and P2 are implemented via a cascade of 12 "elementary" permutations stages; in each stage, one of two fixed permutations ( $\pi_{i1}$  when "Select  $i$ " is a "1",  $\pi_{i2}$  when "Select  $i$ " is a "0") is performed on the 64-bit input data, the choice of which is controlled by a pair of time-varying 12-bit control signals  $p\_cnt[11:0]$ , of which  $p\_cnt[11]$  is the MSB and  $p\_cnt[0]$  is the LSB. A block diagram of the implementation is provided in Figure A.7.

Select  $i$  is controlled by  $p\_cnt[i-1]$  as illustrated in Figure A.7.

The  $\pi_{i1}$  is set to the identity mapping. The  $\pi_{i2}$  is selected from one of the five options specified in clause A.8.

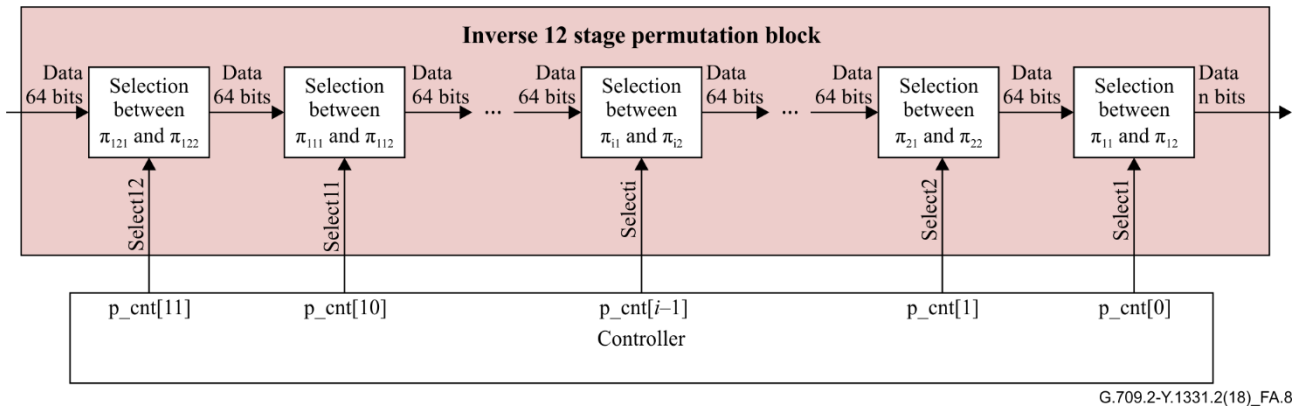


**Figure A.7 – The 12 stage permutation for P1 and P2**

P1\_inverse and P2\_inverse are implemented via a cascade of 12 "elementary" inverse permutations stages; in each stage, one of two fixed permutations ( $\pi_{i1}$  when "Select  $i$ " is a "1",  $\pi_{i2}$  when "Select  $i$ " is a "0") is performed on the 64-bit input data, the choice of which is controlled by a pair of time-varying 12-bit control signals  $p\_cnt[11:0]$ , of which  $p\_cnt[11]$  is the MSB and  $p\_cnt[0]$  is the LSB. A block diagram of the implementation is provided in Figure A.8.

Select  $i$  is controlled by  $p\_cnt[i-1]$  as illustrated in Figure A.8.

The  $\pi_{i1}$  is set to the identity mapping. The  $\pi_{i2}$  is selected from one of the five options specified in clause A.8.



**Figure A.8 – The 12 stage permutation for P1\_inverse and P2\_inverse**

NOTE – The connectivity of the 12-bit control signals p\_cnt[11:0] bits to the permutation stages is the reverse to that in Figure A.7.

#### A.4 Error decorrelator synchronization

The Base Blocks can be considered for the operation of the EDI to consist of a repeating multi-block structure of 128 blocks, numbered between 0 and 127 as illustrated in Figure A.9. Each Base Block ( $8 \times 32640$  bit) contains eight rows, numbered 0 to 7, and 510 64-bit columns, numbered 0 to 509.

To generate the control signals to the P1, P2, P1\_inverse and P2\_inverse stages, two binary counters p1\_cnt and p2\_cnt are used; p1\_cnt ranges from 0 to 4094 and p2\_cnt ranges from 0 to (4094-41). The maximum values of p1\_cnt and p2\_cnt differ by 41. Because the set of integers {41, 4053, 4094} are pairwise relatively prime, the pair (p1\_cnt, p2\_cnt) will go through a large number of combinations before wraparound. The updates happen every  $5 \times 64$ -bits.

The p1\_cnt and p2\_cnt values are a function of the block number  $i$  (values 0-127), the row number  $r$  (values 0-7) and the 64-bit column number  $c$  (values (0-509) as follows:

- $p1\_cnt = ((8 \times i + r) \times 102 + \lfloor c/5 \rfloor) \bmod 4095$
- $p2\_cnt = ((8 \times i + r) \times 102 + \lfloor c/5 \rfloor) \bmod (4095-41)$ .

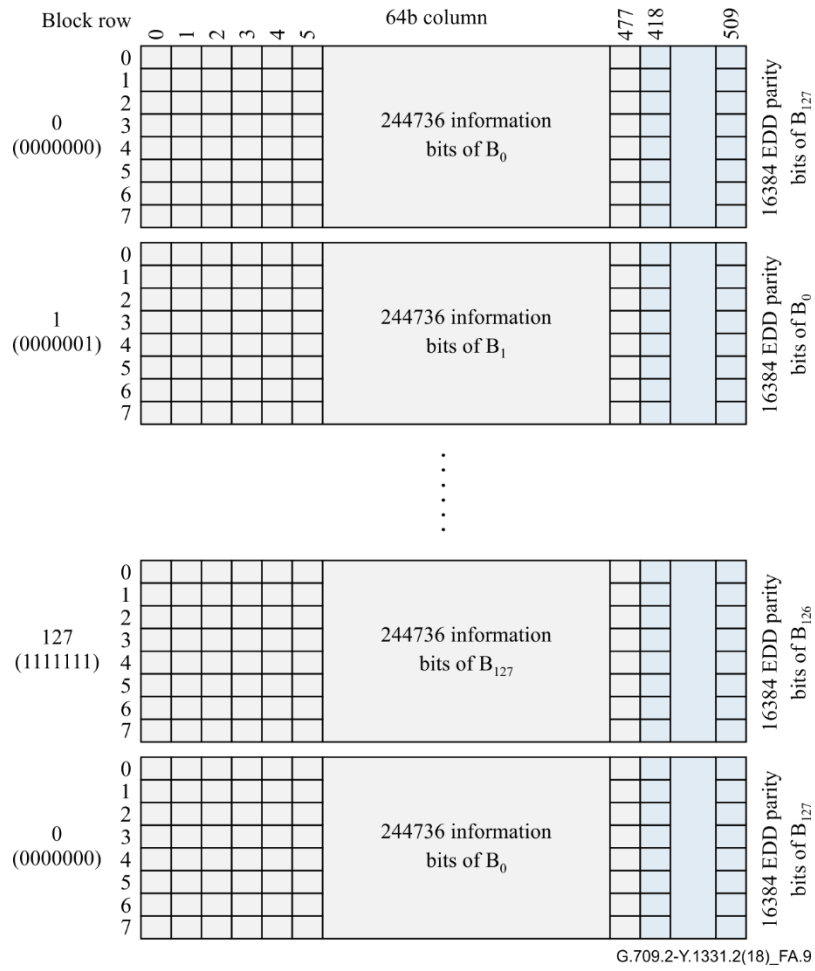
NOTE – " $\lfloor x \rfloor$ " represents the integer floor function.

Example: p1\_cnt for the bits in block #0, row #0 and 64b columns #0-4 is 0 (0x000), for the bits in block #0, row #0 and 64b columns 475-479 is 95 (0x05F), for the bits in block #1 row #0 and 64b columns 0-4 is 816 (0x32F) and for the bits in block #127, row #7, 64b columns 505-509 is 2072 (0x818).

The  $\pi_{i2}$  selection is a function of the 64-bit column number  $c$  (values (0-509) as follows:

- $\pi_{i2}[c] = \pi_{i2}[1 + c \bmod 5]$ .

Figures A.10 and A.11 illustrate the p1\_cnt, p2\_cnt and  $\pi_{i2}$  values within the multi-block structure.



**Figure A.9 – The 128 block repetition of Base Blocks**

block	row	P11	P12	P13	P14	P15	P11	P12	P13	P14	P15	P11	P12	P13	P14	P15	P11	P12	P13	P14	P15	
0	0	0																				
0	1	102		103																		
0	2	204		205																		
0	3	306		307																		
0	4	408		409																		
0	5	510		511																		
0	6	612		613																		
0	7	714		715																		
1	0	816		817																		
1	1	918		919																		
1	2	1020		1021																		
1	3	1122		1123																		
1	4	1224		1225																		
1	5	1326		1327																		
1	6	1428		1429																		
1	7	1530		1531																		
2	0	1632		1633																		
2	1	1734		1735																		
2	2	1836		1837																		
2	3	1938		1939																		
2	4	2040		2041																		
2	5	2142		2143																		
2	6	2244		2245																		
2	7	2346		2347																		
127	0	1257		1258																		
127	1	1359		1360																		
127	2	1461		1462																		
127	3	1563		1564																		
127	4	1665		1666																		
127	5	1767		1768																		
127	6	1869		1870																		
127	7	1971		1972																		

Figure A.10 – p1\_cnt and  $\pi_{i2}$

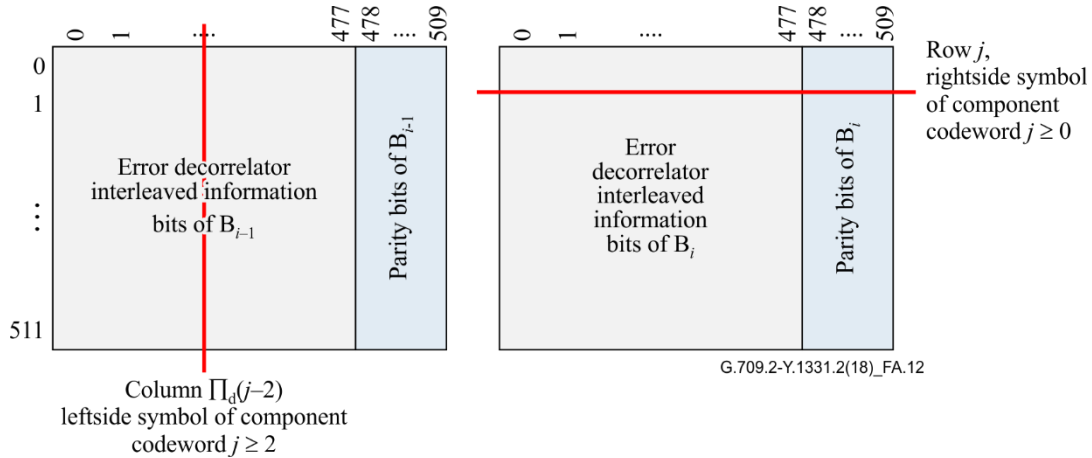
block	row	P21	P22	P23	P24	P25	P21	P22	P23	P24	P25	P21	P22	P23	P24	P25	P21	P22	P23	P24	P25	
0	0	0																				
0	1	102		103																		101
0	2	204		205																		203
0	3	306		307																		305
0	4	408		409																		407
0	5	510		511																		509
0	6	612		613																		611
0	7	714		715																		713
1	0	816		817																		815
1	1	918		919																		917
1	2	1020		1021																		1019
1	3	1122		1123																		1121
1	4	1224		1225																		1223
1	5	1326		1327																		1325
1	6	1428		1429																		1427
1	7	1530		1531																		1529
2	0	1632		1633																		1631
2	1	1734		1735																		1733
2	2	1836		1837																		1835
2	3	1938		1939																		1937
2	4	2040		2041																		2039
2	5	2142		2143																		2141
2	6	2244		2245																		2243
2	7	2346		2347																		2345
127	0	2282		2283																		2447
127	1	2384		2385																		2447
127	2	2486		2487																		2447
127	3	2588		2589																		2447
127	4	2690		2691																		2447
127	5	2792		2793																		2447
127	6	2894		2895																		2447
127	7	2996		2997																		2447

Figure A.11 – p2\_cnt and  $\pi_i$

## A.5 The 512 × 510 staircase forward error correction code

### A.5.1 Encoding a 512 × 510 staircase forward error correction block

Encoding of a 512-bit × 510-bit SC FEC block is accomplished by considering two-dimensional blocks  $B_i$  of binary data, each with 512 rows and 510 columns as illustrated in Figure A.12.

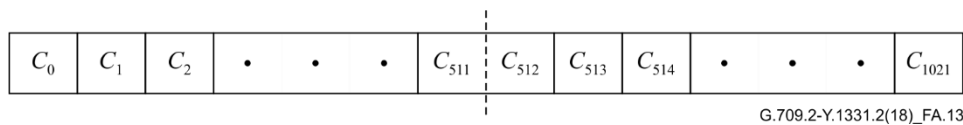


**Figure A.12 – Encoding of a 512-bit × 510-bit staircase forward error correction block**

Due to the staircase construction, it is convenient to classify the symbols – in the context of this Recommendation, symbols are equivalent to bits – of each component BCH(1022,990) codeword (where BCH stands for Bose, Chaudhuri, and Hocquenghem) as occupying the "leftside" or "rightside". The component codewords in the 512 × 510 SC FEC code consist of 512 leftmost bits (which are contributed from the previous SC FEC block) and 510 rightmost bits. As illustrated in Figure A.13, the bits  $(C_0, C_1, \dots, C_{511})$  constitute the leftside, and  $(C_{512}, C_{513}, \dots, C_{1021})$  the rightside of the component BCH(1022,990) codeword. The first two rows of  $B_i$  correspond to shortened codewords, which can be exploited in the decoder.

NOTE 1 – In the description of the calculation of the parity bits, the first two rows are treated as a special case, in that no bits from the previous staircase block are used in computing the parity bits on the first two rows (i.e., these are shortened codewords).

NOTE 2 – The introduction of the shortened codewords (and the related deviation of the staircase blocks from the perfect  $m \times m$  squares in Appendix II to a 512 × 510 rectangle with 261 120 bits) is necessitated by the first OTN implementation and the resulting desire to map the staircase block to two OTN OTUk frames consisting of  $2 \times 4 \times 32640 = 261120$  bits.



**Figure A.13 – Component codeword**

The binary value stored in position (row,column) =  $(j,k)$  of  $B_i$  is denoted  $d_i \{j,k\}$ . In each block, information bits are stored as  $d_i \{j,k\}$ ,  $0 \leq j \leq 511$ ,  $0 \leq k \leq 477$ , and parity bits are stored as  $d_i \{j,k\}$ ,  $0 \leq j \leq 511$ ,  $478 \leq k \leq 509$ .

The parity bits are computed as follows:

- 1) For row  $j$ ,  $0 \leq j \leq 1$ , calculate  $[d_i\{j, 478\}, d_i\{j, 479\}, \dots, d_i\{j, 509\}]$  as
 
$$[d_i\{j, 478\}, d_i\{j, 479\}, \dots, d_i\{j, 509\}] = [0, 0, \dots, 0, d_i\{j, 0\}, d_i\{j, 1\}, \dots, d_i\{j, 477\}]P$$

where  $P$  is a  $990 \times 32$  parity-generation matrix, specified in clause A.7.3.

- 2) For row  $j, 2 \leq j \leq 511$ , calculate  $[d_i\{j, 478\}, d_i\{j, 479\}, \dots, d_i\{j, 509\}]$  as
- $$[d_i\{j, 478\}, d_i\{j, 479\}, \dots, d_i\{j, 509\}] = [d_{i-1}\{0, l\}, d_{i-1}\{1, l\}, \dots, d_{i-1}\{511, l\}, d_i\{j, 0\}, d_i\{j, 1\}, \dots, d_i\{j, 477\}]P$$

where  $l = \Pi_d(j - 2)$ , and  $\Pi_d$  is a permutation function specified in clause A.7.1.

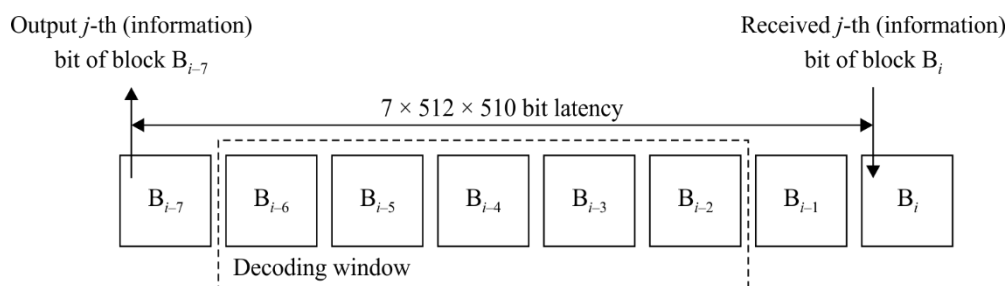
NOTE 3 – As illustrated in Figure A.10, the permutation function specifies the column  $l = \Pi_d(j - 2)$  of block  $B_{i-1}$  that provides the bits for the leftside of the component codeword corresponding to row  $j$  of block  $B_i$ . The permutation function is designed to admit a simple mapping of error locations (i.e., roots of an error locator polynomial) in the *decoder* to positions in a component BCH(1022,990) codeword. Explicitly, if  $512 \times 510$  SC FEC blocks are stored in permuted column order (and the corresponding rightmost 510 columns of the parity check matrix  $H$  are similarly permuted), the binary representation of an error locator in the Galois field,  $GF(2^{10})$ , maps *linearly* to the (permuted) codeword position. Finally, with SC FEC blocks re-arranged in the permuted column order, the bits of column  $j - 2$  in block  $B_{i-1}$  correspond to the leftside of the component codeword with ‘rightside’ bits in row  $j$  of block  $B_i$ .

### A.5.2 Decoding a $512 \times 510$ staircase forward error correction code

SC FEC codes are decoded by iteratively decoding the BCH component codewords within a decoding window; a decoding window consists of an implementation-specific number of consecutive staircase blocks.

The  $512 \times 510$  SC FEC decoder deploys as a minimum a 5-block decoding window (illustrated in Figure A.14) to perform iterative decoding of its BCH(1022,990) component codewords.

The total latency in this minimum configuration is 7 SC FEC blocks. The decoding window moves forward in time (i.e., to the right) once the parity bits corresponding to block  $B_{i-1}$  are received. At every shift in the decoding window, iterative decoding is performed over the component codewords within the decoding window.



NOTE – Parity bits of block  $B_{i-1}$  are received concurrently with information bits of  $B_i$

G.709.2-Y.1331.2(18)\_FA.14

**Figure A.14 – The 5-block staircase forward error correction decoding window**

### A.5.3 Error correction capability

Based on the terms and definitions given in clause 7 of [ITU-T G.975.1], Table A.1 shows the results for the  $512 \times 510$  SC FEC code. Data are measured, not extrapolated from simulations. The stream is decoded iteratively as specified in clause A.5.2.

**Table A.1 – Error correcting capability of the  $512 \times 510$  staircase code**

Input bit error rate	Output bit error rate	Net coding gain (dB)	Coding gain (dB)	Q-limit (dB)
$4.75 \times 10^{-3}$	$10^{-9}$	7.0	7.28	8.28
$4.71 \times 10^{-3}$	$10^{-10}$	7.5	7.78	8.29



**Table A.1 – Error correcting capability of the 512 × 510 staircase code**

Input bit error rate	Output bit error rate	Net coding gain (dB)	Coding gain (dB)	Q-limit (dB)
$4.67 \times 10^{-3}$	$10^{-11}$	7.95	8.23	8.30
$4.62 \times 10^{-3}$	$10^{-12}$	8.35	8.63	8.31
$4.58 \times 10^{-3}$	$10^{-13}$	8.72	9.00	8.32
$4.54 \times 10^{-3}$	$10^{-14}$	9.06	9.34	8.33
$4.50 \times 10^{-3}$	$10^{-15}$	9.38	9.64	8.34

The Flaring threshold is  $<1 \times 10^{-22}$ .

The latency of the minimum 512 × 510 Staircase decoder is  $7 \times 512 \times 510 = 1,827,840$  bits.

### A.6 Representation of elements in $GF(2^{10})$

For a root  $\alpha$  of the primitive polynomial  $p(x) = 1 + x^3 + x^{10}$ , the non-zero field elements of  $GF(2^{10})$  can be represented as

$$\alpha^i, \quad 0 \leq i \leq 1022,$$

which we refer to as the "power" representation, where  $\alpha^{1023} = \alpha^0 = 1$ . Equivalently, we can write

$$\alpha^i = b_9\alpha^9 + b_8\alpha^8 + \dots + b_0, \quad 0 \leq i \leq 1022;$$

we refer to the integer  $l = b_92^9 + b_82^8 + \dots + b_0$  as the "binary" representation of the field element. We further define the function  $\log$  and its inverse  $\exp$  such that for  $l$ , the binary representation of  $\alpha^l$ , we have

$$\log(l) = i$$

and

$$\exp(i) = l.$$

### A.7 Staircase forward error correction component code mapping

#### A.7.1 Specification of $\Pi_d$

$\Pi_d$  is a permutation function on the integers  $i, 0 \leq i \leq 509$ . In the following,  $\Pi_d(M: M + N) = K: K + N$  is shorthand for  $\Pi_d(M) = K, \Pi_d(M + 1) = K + 1, \dots, \Pi_d(M + N) = K + N$ . Values of  $\Pi_d$  are listed in Table A.2.

**Table A.2 – Values of  $\Pi_d$**

$\Pi_d(0:7) = 478:485$	$\Pi_d(8) = 0$	$\Pi_d(9:11) = 486:488$	$\Pi_d(12) = 1$
$\Pi_d(13) = 489$	$\Pi_d(14:16) = 2:4$	$\Pi_d(17:19) = 490:492$	$\Pi_d(20) = 5$
$\Pi_d(21) = 493$	$\Pi_d(22:24) = 6:8$	$\Pi_d(25) = 494$	$\Pi_d(26:32) = 9:15$
$\Pi_d(33:35) = 495:497$	$\Pi_d(36) = 16$	$\Pi_d(37) = 498$	$\Pi_d(38:40) = 17:19$
$\Pi_d(41) = 499$	$\Pi_d(42:48) = 20:26$	$\Pi_d(49) = 500$	$\Pi_d(50:64) = 27:41$
$\Pi_d(65:67) = 501:503$	$\Pi_d(68) = 42$	$\Pi_d(69) = 504$	$\Pi_d(70:72) = 43:45$
$\Pi_d(73) = 505$	$\Pi_d(74:80) = 46:52$	$\Pi_d(81) = 506$	$\Pi_d(82:128) = 53:99$
$\Pi_d(129) = 507$	$\Pi_d(130) = 100$	$\Pi_d(131) = 508$	$\Pi_d(132:256) = 101:225$
$\Pi_d(257) = 509$	$\Pi_d(258:509) = 226:477$		

## A.7.2 Parity check Matrix

Consider the function  $f$  which maps an integer  $i$ ,  $1 \leq i \leq 1023$ , to the column vector

$$f(i) = \begin{bmatrix} \beta_i \\ \beta_i^3 \\ \beta_i^5 \\ F(\beta_i) \\ \overline{F(\beta_i)} \end{bmatrix},$$

where:

$$\beta_i = \alpha^{\log(i)},$$

and:

$$F(\beta_i) = b_2^l \overline{b_1^l} \overline{b_0^l} \vee \overline{b_2^l} b_1^l \vee \overline{b_2^l} \overline{b_1^l} b_0^l,$$

for  $l$  the binary representation of  $\beta_i$ , and  $\bar{x}$  is the complement of  $x$ . Then,

$$H = [f(1021) \ f(1022) \ f(1) \ \cdots \ f(510) \ f(511 + \Pi^{-1}(0)) \ \cdots \ f(511 + \Pi^{-1}(509))]$$

(Note that the field primitive  $\alpha$  is specified in clause A.6.)

## A.7.3 Generator matrix

To obtain the generator matrix, we first replace each element in the first three rows of  $H$  by its corresponding 10-bit binary representation, and perform elementary row operations (over  $GF(2)$ ) on  $H$  to obtain its row-reduced echelon form (with the identity matrix on the right)  $H_{ENC}$ . Since

$$H_{ENC} = [P^T; I],$$

we have

$$G = [I; P],$$

where the resulting  $990 \times 32$  matrix  $P$  provides the encoder's parity-generating masks.

## A.8 Error decorrelator permutation maps

### A.8.1 Generic permutation maps

Mapping for P1, Option 1 for the 12 stages are shown in the  $64 \times 12$  matrix P1<sub>1</sub>

Mapping for P1, Option 2 for the 12 stages are shown in the  $64 \times 12$  matrix P1<sub>2</sub>

Mapping for P1, Option 3 for the 12 stages are shown in the  $64 \times 12$  matrix P1<sub>3</sub>

Mapping for P1, Option 4 for the 12 stages are shown in the  $64 \times 12$  matrix P1<sub>4</sub>

Mapping for P1, Option 5 for the 12 stages are shown in the  $64 \times 12$  matrix P1<sub>5</sub>

Mapping for P2, Option 1 for the 12 stages are shown in the  $64 \times 12$  matrix P2<sub>1</sub>

Mapping for P2, Option 2 for the 12 stages are shown in the  $64 \times 12$  matrix P2<sub>2</sub>

Mapping for P2, Option 3 for the 12 stages are shown in the  $64 \times 12$  matrix P2<sub>3</sub>

Mapping for P2, Option 4 for the 12 stages are shown in the  $64 \times 12$  matrix P2<sub>4</sub>

Mapping for P2, Option 5 for the 12 stages are shown in the  $64 \times 12$  matrix P2<sub>5</sub>

The de-interleaver is the inverse of the interleaver. We only specify the interleaver map here.

For the sake of illustration, consider the permutation maps  $\pi_{i2}$  specified in the matrix  $P1_1$ . Note that each column (there are 12 columns, in one-to-one correspondence with the 12 stages illustrated in Figure A.7) is a 64-element permutation on the values 1 to 64.

By convention, the elements of the permutation table are represented such that 1 corresponds to the first position in transmission order (of the input/output), 2 to the second position in transmission order, 3 to the third position, and so on.

For example, if we consider the first column  $\pi_{12}$  of  $P1_1$ , the permutation specifies that the bit in position 38 of the input to the corresponding permutation stage appears in the output of the permutation stage at position 1, the bit in position 55 of the input appears in the output at position 2, the bit in position 37 of the input appears in the output at position 3, and so on.

P1 <sub>1</sub>	Permutation stage $\pi_{i2}$											Output	
	$\pi_{12}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$		$\pi_{122}$
Permutation element	38	48	19	58	58	21	29	34	26	32	50	60	1
	55	61	33	15	55	55	5	56	42	51	34	53	2
	37	4	22	63	52	25	7	36	49	12	48	29	3
	15	1	12	2	49	42	37	15	1	55	9	46	4
	48	33	59	48	1	54	35	1	2	22	30	21	5
	50	41	61	28	34	29	34	12	6	63	32	22	6
	54	18	38	12	35	22	61	51	60	61	49	1	7
	8	32	60	3	13	63	2	50	34	9	3	5	8
	19	36	64	62	41	52	28	8	59	1	42	11	9
	13	2	52	34	19	43	46	39	43	52	55	25	10
	53	22	47	33	18	8	8	5	16	5	20	13	11
	9	57	5	32	56	11	23	17	46	24	25	27	12
	24	23	37	44	14	7	51	6	12	38	28	7	13
	18	55	54	36	27	19	22	31	27	34	40	62	14
	2	54	62	17	62	28	19	28	44	47	14	17	15
	29	51	55	56	42	32	48	47	64	7	59	49	16
	57	31	20	10	32	16	62	44	5	45	6	64	17
	63	5	13	9	51	14	53	53	3	15	1	28	18
	43	40	34	18	23	26	11	48	36	39	60	32	19
	14	62	56	31	17	10	17	16	37	11	54	59	20
	52	63	10	35	54	1	47	23	48	54	41	61	21
	22	29	42	21	61	37	15	13	45	58	15	50	22
	1	46	46	57	28	38	4	2	52	2	18	4	23
	39	43	26	14	60	5	57	4	62	37	17	55	24
	16	15	31	25	47	34	14	26	15	14	22	51	25
	21	42	41	49	10	53	20	63	33	36	35	26	26
	64	50	15	4	36	18	64	45	23	62	56	34	27
	59	49	63	54	11	33	38	35	32	56	12	39	28
	17	37	23	42	15	27	43	55	50	19	53	20	29
	60	59	32	5	3	51	36	7	28	31	26	36	30
	6	60	44	46	26	36	42	18	38	4	38	3	31
	58	39	11	27	25	9	27	24	13	8	62	6	32
	35	26	1	13	59	15	31	58	19	23	57	44	33
	51	47	43	40	20	23	49	33	10	64	33	19	34
	4	35	16	37	8	56	10	30	63	6	47	8	35
	3	52	58	30	39	30	40	42	11	35	29	58	36
	26	58	14	26	12	24	63	9	20	18	45	10	37
	33	21	28	11	5	13	58	52	35	33	61	45	38
	56	25	6	38	57	61	9	29	31	48	27	18	39
	41	7	25	55	37	47	30	57	8	28	11	31	40
	7	6	30	50	29	60	1	25	54	41	24	2	41
	31	38	51	60	63	35	6	14	57	49	63	12	42
	42	45	29	20	44	6	25	10	56	53	46	33	43
	45	53	17	22	43	20	32	43	17	46	19	24	44
	23	13	3	39	50	62	33	49	21	27	51	48	45
	11	20	40	53	38	48	18	37	24	13	10	41	46
	30	56	9	16	4	46	21	60	41	25	5	14	47
	32	3	57	47	46	45	3	64	22	26	44	9	48
	49	10	21	6	16	4	41	32	58	3	58	30	49
	47	64	50	59	22	59	60	61	9	21	21	37	50
	62	17	48	1	2	58	52	59	18	16	23	54	51
	34	8	27	23	64	40	59	54	39	29	43	42	52
	36	44	8	29	6	3	13	3	7	40	37	35	53
	20	28	18	24	48	50	50	62	40	10	4	40	54
	40	30	4	19	30	17	16	38	4	44	2	23	55
	27	24	49	8	53	41	55	19	55	60	39	15	56
	10	16	2	51	24	12	45	21	30	42	64	63	57
	25	14	24	52	45	31	39	41	53	59	52	56	58
	12	9	35	7	40	57	12	27	25	20	16	38	59
	46	34	36	61	33	44	26	11	29	57	7	43	60
	61	27	45	45	21	2	44	22	51	43	36	57	61
	5	19	39	64	31	39	54	46	61	30	8	16	62
	28	11	53	43	9	49	56	20	47	17	13	47	63
	44	12	7	41	7	64	24	40	14	50	31	52	64

<b>P1<sub>2</sub></b>	<b>Permutation stage <math>\pi_{i,2}</math></b>											<b>Output</b>	
	$\pi_{1,2}$	$\pi_{2,2}$	$\pi_{3,2}$	$\pi_{4,2}$	$\pi_{5,2}$	$\pi_{6,2}$	$\pi_{7,2}$	$\pi_{8,2}$	$\pi_{9,2}$	$\pi_{10,2}$	$\pi_{11,2}$		$\pi_{12,2}$
	27	56	39	24	30	14	33	11	60	46	30	9	<b>1</b>
	19	31	61	33	35	52	40	22	41	39	56	33	<b>2</b>
	20	12	18	10	1	7	9	3	12	52	44	14	<b>3</b>
	44	59	12	59	56	19	48	21	45	31	8	38	<b>4</b>
	41	50	40	42	28	60	24	57	5	49	57	24	<b>5</b>
	22	23	33	25	29	38	15	53	37	58	24	47	<b>6</b>
	12	14	19	8	48	17	10	18	29	29	10	48	<b>7</b>
	11	38	3	20	42	20	46	9	8	3	13	22	<b>8</b>
	45	44	62	55	53	33	52	7	20	42	49	1	<b>9</b>
	25	24	20	48	58	15	3	44	36	21	20	19	<b>10</b>
	28	32	16	39	39	50	35	32	46	64	26	13	<b>11</b>
	23	34	46	36	45	5	14	24	56	23	42	61	<b>12</b>
	16	61	45	46	26	57	27	27	61	45	33	32	<b>13</b>
	33	2	34	18	3	2	5	2	25	48	52	3	<b>14</b>
	21	28	38	19	6	28	1	13	33	50	36	60	<b>15</b>
	39	43	44	15	47	11	45	4	58	24	28	52	<b>16</b>
	34	17	60	9	8	54	41	64	54	27	25	11	<b>17</b>
	60	42	15	6	36	26	25	54	49	25	18	37	<b>18</b>
	5	54	55	32	7	41	18	56	18	32	58	53	<b>19</b>
	64	25	41	43	10	29	37	35	13	26	19	2	<b>20</b>
	43	36	7	34	2	46	31	23	24	38	1	63	<b>21</b>
	49	55	56	28	40	39	53	47	44	22	47	51	<b>22</b>
	36	58	63	29	5	4	28	49	64	51	9	7	<b>23</b>
	48	18	26	44	9	30	23	55	62	37	60	40	<b>24</b>
	37	22	6	60	20	24	6	37	1	35	14	56	<b>25</b>
	3	8	64	58	63	27	7	1	63	16	61	10	<b>26</b>
	1	9	9	56	50	25	60	42	40	4	11	27	<b>27</b>
	6	27	36	41	55	35	61	50	39	33	16	29	<b>28</b>
	47	37	43	26	19	56	55	48	42	13	38	21	<b>29</b>
	38	11	47	16	37	49	44	19	34	54	62	57	<b>30</b>
	4	52	29	12	44	23	8	12	57	11	35	50	<b>31</b>
	61	60	22	27	18	53	58	46	19	47	2	31	<b>32</b>
	57	1	25	11	17	16	56	5	15	44	6	55	<b>33</b>
	51	10	42	7	43	9	17	34	2	59	17	6	<b>34</b>
	52	48	21	21	62	42	26	17	32	9	59	62	<b>35</b>
	18	4	59	61	11	21	47	29	43	6	4	49	<b>36</b>
	7	35	5	62	13	55	11	20	59	10	48	8	<b>37</b>
	55	47	54	31	41	44	62	52	52	57	22	34	<b>38</b>
	40	64	27	22	12	47	49	28	28	15	41	16	<b>39</b>
	62	19	31	45	52	36	59	31	7	28	51	30	<b>40</b>
	50	16	28	35	21	1	39	25	3	5	55	5	<b>41</b>
	9	6	52	57	25	58	20	36	27	2	40	45	<b>42</b>
	42	26	32	40	46	48	38	15	9	41	15	58	<b>43</b>
	54	45	24	23	4	18	43	63	48	18	3	20	<b>44</b>
	26	15	50	5	60	31	54	14	55	30	46	15	<b>45</b>
	24	20	1	13	61	62	2	59	47	63	53	26	<b>46</b>
	10	3	51	1	32	40	21	39	11	8	64	42	<b>47</b>
	56	49	11	50	24	37	19	60	53	61	37	39	<b>48</b>
	14	39	8	4	16	6	51	16	23	53	31	28	<b>49</b>
	31	51	48	14	15	51	63	30	21	62	54	25	<b>50</b>
	29	40	37	53	57	32	13	51	17	34	27	18	<b>51</b>
	35	7	10	49	31	12	30	38	31	7	50	43	<b>52</b>
	59	57	49	38	34	63	16	26	22	56	32	54	<b>53</b>
	8	5	17	54	22	59	34	40	16	12	29	17	<b>54</b>
	30	29	14	2	51	3	42	43	26	55	12	12	<b>55</b>
	58	63	53	64	23	34	32	45	10	40	7	4	<b>56</b>
	32	41	13	37	64	45	29	61	4	60	43	23	<b>57</b>
	53	53	4	47	27	43	12	58	38	17	23	44	<b>58</b>
	17	13	58	30	14	64	57	10	30	19	5	35	<b>59</b>
	2	33	23	17	54	8	22	8	14	36	39	59	<b>60</b>
	46	30	2	51	33	61	64	33	50	1	45	36	<b>61</b>
	13	46	35	63	49	22	50	62	6	43	34	46	<b>62</b>
	63	21	30	3	38	10	4	41	51	14	21	64	<b>63</b>
	15	62	57	52	59	13	36	6	35	20	63	41	<b>64</b>

P1 <sub>3</sub>	Permutation stage $\pi_{i2}$											Output	
	$\pi_{12}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$		$\pi_{122}$
	18	63	36	6	9	26	57	55	31	62	30	22	1
	43	23	18	40	4	6	51	56	4	29	22	3	2
	27	44	45	11	31	10	47	36	20	3	26	64	3
	58	43	48	59	25	45	46	63	9	55	10	45	4
	23	2	10	1	53	44	24	15	43	12	33	19	5
	12	8	5	55	11	53	16	33	64	21	8	27	6
	54	49	30	17	28	57	39	52	40	51	32	34	7
	55	36	63	46	22	59	40	50	18	47	13	25	8
	32	53	28	47	36	7	4	61	27	54	56	8	9
	6	7	51	45	1	11	62	19	13	37	18	58	10
	36	33	8	2	37	5	59	28	29	18	48	15	11
	57	28	32	9	18	43	56	48	42	39	39	48	12
	40	16	52	32	51	56	23	43	52	32	63	49	13
	42	1	16	19	64	9	21	16	23	50	52	18	14
	30	54	54	62	17	2	64	32	36	7	38	20	15
	31	12	6	7	57	52	11	31	53	15	41	37	16
	10	58	25	37	38	23	34	1	6	63	11	43	17
	33	60	43	35	19	42	28	49	34	10	60	24	18
	4	45	11	25	55	8	35	12	22	48	6	40	19
	17	40	42	16	13	27	58	5	37	20	34	46	20
	61	17	34	10	23	24	8	29	1	40	16	16	21
	26	22	56	30	33	35	25	30	33	34	23	39	22
	52	9	22	31	15	15	44	7	17	4	51	41	23
	45	4	59	58	41	37	49	51	38	26	29	33	24
	16	30	17	60	47	1	10	59	7	33	21	10	25
	59	29	27	4	52	54	13	45	14	41	19	2	26
	39	50	24	3	62	60	6	27	3	5	44	47	27
	7	51	20	52	54	38	48	22	57	27	53	26	28
	29	31	1	49	42	4	14	9	32	56	59	38	29
	25	38	2	54	29	20	42	38	54	13	47	55	30
	41	32	14	56	8	30	9	8	45	14	58	54	31
	20	39	3	36	12	63	41	41	62	16	61	52	32
	28	24	61	51	44	39	26	46	60	60	27	23	33
	8	61	35	24	63	55	30	23	39	24	35	14	34
	47	14	29	50	16	13	45	37	21	44	37	17	35
	21	19	62	28	48	51	5	20	24	52	45	6	36
	53	13	55	33	43	12	60	4	25	42	24	36	37
	37	34	60	39	34	29	52	58	2	61	50	35	38
	48	64	50	57	21	25	54	34	61	22	42	31	39
	34	56	53	29	14	22	37	54	50	6	20	53	40
	5	55	13	20	7	3	19	40	5	38	3	5	41
	46	18	31	5	32	61	31	64	41	9	46	28	42
	51	20	41	14	27	32	2	21	47	8	43	30	43
	60	37	12	18	59	28	18	35	58	2	36	1	44
	35	25	64	63	5	21	15	26	48	30	57	32	45
	11	6	26	15	6	62	50	25	63	11	2	63	46
	63	59	57	64	24	46	55	17	55	1	49	44	47
	14	52	38	44	3	14	53	2	10	23	12	29	48
	13	42	19	21	61	19	1	62	49	46	5	11	49
	44	3	40	13	2	64	3	10	30	31	14	12	50
	2	26	37	34	45	34	20	18	56	58	31	57	51
	1	47	15	22	35	47	27	3	8	17	28	21	52
	9	21	46	61	20	31	61	44	19	53	55	62	53
	62	48	4	12	60	17	33	57	51	35	7	56	54
	19	35	39	42	40	58	7	24	11	36	1	51	55
	56	5	21	8	49	36	22	39	16	57	54	4	56
	22	10	9	26	50	33	17	11	28	19	4	59	57
	15	11	44	48	46	41	32	42	15	25	15	9	58
	38	27	47	53	10	18	36	6	44	28	25	60	59
	3	41	23	43	30	40	43	14	12	59	40	42	60
	49	15	33	27	56	49	63	53	46	49	17	7	61
	64	57	58	38	58	48	12	60	59	45	64	50	62
	24	62	7	41	26	16	38	47	26	43	62	61	63
	50	46	49	23	39	50	29	13	35	64	9	13	64

P14	Permutation stage $\pi_{i2}$											Output	
	$\pi_{12}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$		$\pi_{122}$
Permutation element	17	54	46	15	42	61	19	25	16	8	57	39	1
	34	35	21	50	21	48	7	57	7	2	52	62	2
	61	32	6	63	29	63	57	10	53	59	62	12	3
	4	29	56	25	2	18	56	64	48	7	49	22	4
	46	37	60	59	28	9	24	40	50	4	55	9	5
	14	25	20	16	3	51	32	45	14	61	45	25	6
	2	16	9	48	31	14	44	62	31	19	42	13	7
	19	8	16	26	15	38	5	43	26	15	17	7	8
	10	48	49	54	26	49	63	20	15	57	46	29	9
	64	14	3	18	52	4	23	18	43	1	41	2	10
	38	3	40	19	45	52	6	7	11	54	25	37	11
	26	60	29	64	44	10	40	63	5	33	23	16	12
	32	9	7	38	19	43	61	55	8	20	19	51	13
	1	45	50	8	23	23	47	36	44	35	60	10	14
	24	1	55	61	12	29	18	33	59	53	54	56	15
	62	51	57	22	41	35	21	12	6	34	30	48	16
	11	33	26	52	1	24	14	39	64	14	35	27	17
	29	39	39	33	5	8	52	22	38	42	48	40	18
	13	34	24	14	63	39	20	11	23	64	10	35	19
	53	62	44	47	27	64	53	30	42	13	7	44	20
	20	11	38	37	54	62	43	41	27	48	31	47	21
	8	61	22	35	56	6	11	49	45	40	8	49	22
	39	56	52	27	25	57	34	14	28	43	24	31	23
	50	23	54	2	55	36	15	24	19	49	53	60	24
	5	64	2	49	22	44	50	56	1	24	18	34	25
	33	42	4	24	4	20	59	46	9	23	61	58	26
	51	43	27	4	39	28	22	59	33	11	39	23	27
	9	10	36	31	59	17	51	17	54	16	51	21	28
	40	2	61	11	32	3	13	42	47	51	26	3	29
	25	6	5	36	16	50	30	16	12	39	29	53	30
	18	40	62	29	37	5	4	3	21	18	16	11	31
	31	44	37	56	9	27	58	4	4	46	4	52	32
	16	31	47	43	10	12	62	38	55	25	6	30	33
	59	50	28	7	35	32	55	34	20	28	5	8	34
	54	55	41	45	49	47	54	31	32	45	58	45	35
	43	38	14	12	40	37	3	26	13	30	34	18	36
	55	19	45	40	33	60	25	28	2	47	9	61	37
	3	63	23	60	48	25	60	51	49	37	27	55	38
	21	59	42	20	20	58	36	54	30	17	1	41	39
	37	46	63	53	47	7	38	23	36	50	22	20	40
	42	53	31	46	36	46	33	48	17	5	56	42	41
	41	57	58	9	30	42	17	60	57	62	47	33	42
	56	47	48	42	18	41	39	29	46	36	3	4	43
	30	58	32	28	13	34	31	6	25	6	20	26	44
	6	7	17	21	53	19	27	15	37	10	64	32	45
	15	20	11	44	51	33	10	27	60	26	14	46	46
	22	24	10	51	58	13	64	5	62	22	15	50	47
	63	52	59	62	24	11	35	50	39	55	13	54	48
	45	22	30	6	46	55	49	53	41	31	50	1	49
	48	18	18	57	34	40	42	13	18	60	11	24	50
	7	12	12	13	43	21	26	61	35	9	38	6	51
	35	30	34	39	60	54	9	21	22	32	43	36	52
	57	4	43	1	11	30	41	58	52	41	2	17	53
	28	13	51	23	6	1	45	1	51	12	33	43	54
	52	5	64	30	14	15	1	8	10	3	32	5	55
	58	17	53	41	64	22	29	35	3	56	12	19	56
	23	21	19	55	61	56	12	44	40	58	37	38	57
	47	41	8	34	62	2	48	47	61	27	44	28	58
	49	36	25	3	17	16	28	52	24	63	59	64	59
	60	27	15	17	57	59	2	9	63	29	36	14	60
	44	26	35	58	7	45	8	32	34	21	40	63	61
	12	49	1	5	38	31	16	37	56	52	63	59	62
	36	28	33	10	50	53	37	2	29	38	28	15	63
	27	15	13	32	8	26	46	19	58	44	21	57	64

P15	Permutation stage $\pi_{i2}$											Output	
	$\pi_{12}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$		$\pi_{122}$
Permutation element	44	15	62	64	32	19	50	36	6	19	43	51	1
	1	25	4	48	62	56	4	2	21	7	45	39	2
	27	24	40	25	49	42	45	27	12	20	4	25	3
	60	53	18	34	14	60	58	9	14	24	62	47	4
	32	64	29	30	33	52	64	37	28	22	38	44	5
	21	58	14	22	44	41	21	40	37	4	32	50	6
	13	60	12	14	52	47	5	13	49	2	20	45	7
	48	23	51	32	21	32	8	3	52	26	40	2	8
	46	57	24	60	48	2	54	62	16	35	64	7	9
	14	21	30	45	9	63	37	47	39	17	15	1	10
	59	39	44	40	39	39	25	45	45	44	10	6	11
	62	28	49	39	40	33	24	5	36	14	46	3	12
	10	55	37	59	28	24	33	57	40	54	60	41	13
	45	12	50	15	4	14	59	10	46	32	19	49	14
	38	32	58	61	47	58	32	21	25	61	3	12	15
	6	29	42	51	54	6	15	48	31	6	59	8	16
	20	3	34	31	34	22	26	8	8	52	48	24	17
	17	49	17	5	29	43	13	64	64	64	50	18	18
	16	62	60	24	57	55	38	25	59	58	42	63	19
	40	61	53	2	27	50	47	26	56	21	24	22	20
	63	59	46	18	43	26	6	34	20	13	33	14	21
	18	22	45	1	26	3	36	44	26	49	37	37	22
	19	10	48	56	20	12	9	51	17	33	23	55	23
	2	43	19	6	17	11	11	28	2	51	16	53	24
	3	40	28	46	42	4	28	49	32	28	31	33	25
	58	34	27	47	5	27	35	60	62	5	41	62	26
	5	2	8	11	11	23	31	33	24	27	13	21	27
	50	20	64	27	25	59	62	63	7	18	1	15	28
	61	35	52	29	10	20	60	50	42	30	63	26	29
	56	18	43	57	7	48	56	17	10	40	12	40	30
	49	48	54	44	55	29	7	56	5	41	57	13	31
	43	6	25	20	6	54	41	52	30	8	51	60	32
	30	4	1	62	61	30	23	4	55	36	49	27	33
	4	16	9	58	12	8	30	35	51	10	30	48	34
	57	26	13	4	56	46	19	1	33	3	55	46	35
	12	27	55	8	53	53	3	12	53	23	56	54	36
	31	47	38	55	22	57	40	7	19	39	11	36	37
	54	14	26	28	35	28	43	39	50	55	21	56	38
	36	30	7	41	41	7	49	43	57	45	61	16	39
	51	54	22	38	2	38	16	22	35	1	58	28	40
	55	38	16	49	19	44	12	29	60	43	39	52	41
	53	13	57	53	3	13	48	53	38	37	34	34	42
	28	42	15	3	13	1	53	32	43	62	54	43	43
	34	63	35	26	64	17	63	38	18	53	44	29	44
	42	36	5	42	23	40	46	24	9	59	29	59	45
	47	8	56	35	18	62	14	41	29	60	6	10	46
	41	46	59	21	15	45	1	15	27	46	7	64	47
	35	7	6	23	45	34	61	58	11	11	26	4	48
	26	11	32	9	63	16	55	54	61	31	53	31	49
	52	31	39	52	8	36	22	42	63	16	47	20	50
	9	44	11	16	16	31	17	55	58	12	25	19	51
	8	5	3	19	24	64	29	31	47	9	22	9	52
	11	1	2	13	60	37	51	59	3	38	9	38	53
	23	51	61	63	30	51	18	61	41	15	36	32	54
	25	9	20	50	46	21	39	18	15	34	5	35	55
	37	41	36	17	59	15	2	23	23	56	8	57	56
	39	50	63	12	38	10	42	6	44	47	17	23	57
	15	19	10	33	51	18	27	46	1	29	35	61	58
	29	45	33	36	1	5	57	19	54	48	18	5	59
	22	17	21	10	37	49	20	14	4	57	2	58	60
	7	33	41	37	36	61	10	30	13	25	52	17	61
	33	52	31	43	31	25	52	11	34	42	27	30	62
	24	37	47	54	50	35	44	16	22	63	14	42	63
	64	56	23	7	58	9	34	20	48	50	28	11	64



P2 <sub>i</sub>	Permutation stage $\pi_{i2}$											Output	
	$\pi_{12}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$		$\pi_{122}$
	3	42	27	13	63	9	52	17	31	7	10	25	1
	14	29	55	29	10	36	56	59	40	12	57	3	2
	30	47	43	61	59	42	22	64	33	58	39	54	3
	38	30	63	64	46	13	14	4	49	49	59	15	4
	61	17	37	3	40	14	13	53	5	23	1	12	5
	36	27	33	57	19	50	50	41	41	64	8	34	6
	39	34	6	49	7	25	36	19	19	17	54	18	7
	48	10	29	48	52	60	2	11	52	21	46	35	8
	29	36	41	26	12	28	49	8	4	56	2	53	9
	62	26	30	28	56	54	41	12	29	62	60	48	10
	17	9	21	24	43	19	1	24	42	27	62	41	11
	5	28	35	52	49	56	62	63	11	11	19	64	12
	33	49	18	1	32	22	44	26	17	40	9	58	13
	40	4	9	14	25	17	4	1	57	51	13	42	14
	35	15	4	17	60	34	39	14	27	60	44	9	15
	50	1	58	9	54	2	42	2	58	46	45	44	16
	41	41	60	37	30	37	46	30	32	37	7	2	17
	34	39	15	35	58	26	9	23	18	41	21	33	18
	11	62	1	6	9	40	24	9	25	2	38	63	19
	51	6	31	32	44	30	5	54	60	53	61	61	20
	6	40	17	41	61	4	6	22	8	9	17	16	21
	64	23	56	34	55	21	47	61	37	36	28	11	22
	10	57	8	60	34	5	26	29	21	24	33	52	23
	58	43	5	42	28	7	18	49	48	44	35	26	24
	1	59	47	53	1	49	63	13	24	8	27	6	25
	56	50	32	22	6	61	59	32	26	33	50	36	26
	45	55	16	62	16	53	8	39	45	30	53	40	27
	12	13	48	63	33	11	15	45	61	32	36	56	28
	9	33	44	8	15	39	35	47	62	45	51	55	29
	49	32	13	27	11	6	33	10	13	48	49	31	30
	7	63	52	10	37	64	32	56	46	5	47	28	31
	37	24	36	19	13	20	34	50	35	29	24	30	32
	55	22	34	46	29	29	10	60	3	6	41	27	33
	57	11	51	33	62	59	60	40	23	25	18	14	34
	13	20	62	4	45	27	25	44	1	52	3	50	35
	24	25	40	16	5	51	64	3	30	16	22	59	36
	15	18	49	55	48	3	21	58	7	18	48	57	37
	59	61	24	54	47	24	16	55	12	57	40	24	38
	31	8	2	20	31	16	61	28	16	1	30	17	39
	16	3	61	5	24	23	11	38	34	14	14	1	40
	46	45	25	51	64	48	55	7	56	59	6	23	41
	23	58	54	2	51	45	37	18	53	38	20	4	42
	53	12	23	7	21	18	27	35	22	10	12	47	43
	20	7	42	23	23	43	23	25	9	3	5	29	44
	42	64	50	47	27	38	31	16	59	13	64	46	45
	21	60	10	58	38	63	48	21	14	63	58	10	46
	28	35	19	12	4	8	30	15	64	26	11	7	47
	22	37	57	50	36	1	53	42	55	28	37	8	48
	2	53	12	59	50	15	51	48	10	35	32	38	49
	27	31	39	38	42	46	28	34	51	43	15	20	50
	19	5	22	36	18	58	57	36	63	50	43	39	51
	25	21	7	45	2	57	19	31	38	31	4	60	52
	4	46	11	43	20	62	43	52	15	19	42	19	53
	43	52	3	21	14	44	17	33	54	55	55	5	54
	52	16	28	25	39	32	3	5	36	22	31	32	55
	44	56	20	30	26	12	20	20	43	15	56	22	56
	63	44	46	39	35	55	40	46	39	42	63	37	57
	60	38	64	56	57	31	58	57	50	20	34	13	58
	47	2	45	18	22	10	7	6	44	34	26	43	59
	18	51	26	31	3	47	54	51	6	39	29	49	60
	54	14	53	15	41	35	12	37	20	54	16	45	61
	8	19	14	44	17	52	38	43	2	61	25	21	62
	32	48	59	11	8	33	45	62	47	4	23	62	63
	26	54	38	40	53	41	29	27	28	47	52	51	64

P2 <sub>2</sub>	Permutation stage $\pi_{i2}$											Output	
	$\pi_{12}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$		$\pi_{122}$
Permutation element	60	44	53	17	7	62	53	55	51	39	41	33	1
	42	62	62	40	31	55	14	59	13	11	46	55	2
	29	14	32	57	3	51	64	15	14	43	51	45	3
	1	26	14	31	22	60	51	28	52	12	23	11	4
	30	35	42	51	54	2	63	58	60	31	21	9	5
	16	34	37	53	4	37	42	20	58	60	56	63	6
	36	10	60	48	27	59	22	10	35	37	61	31	7
	5	27	23	45	39	24	9	52	5	50	12	2	8
	62	32	61	5	60	49	16	30	27	9	58	62	9
	44	9	41	62	47	43	60	3	20	62	27	1	10
	41	20	17	25	8	17	19	54	32	25	10	7	11
	13	48	40	36	35	61	49	13	33	17	7	38	12
	33	42	35	55	16	25	23	5	55	22	16	46	13
	61	40	44	35	14	63	11	6	34	57	22	14	14
	28	25	10	20	26	34	45	25	31	61	42	15	15
	21	45	31	1	18	22	15	61	28	29	57	39	16
	4	52	22	27	61	21	8	56	64	3	45	53	17
	25	15	27	52	63	40	10	50	2	8	54	19	18
	32	8	3	19	45	26	35	47	42	27	39	20	19
	63	59	21	34	2	1	43	33	63	42	34	21	20
	9	3	25	24	6	9	39	37	10	47	35	29	21
	15	47	30	26	52	32	55	60	59	21	60	37	22
	14	16	64	56	37	46	37	21	26	20	3	64	23
	55	7	57	32	51	30	46	2	49	7	9	12	24
	50	38	43	13	19	39	24	63	30	58	31	36	25
	48	64	4	60	58	10	4	41	24	55	24	23	26
	58	54	55	29	28	14	12	22	29	4	8	44	27
	49	2	5	39	10	12	41	32	11	41	62	17	28
	54	12	1	54	11	18	28	7	9	14	29	50	29
	22	43	63	38	41	56	20	23	15	40	36	5	30
	59	30	11	44	24	35	27	8	8	46	25	22	31
	10	63	58	10	49	44	44	46	41	28	4	60	32
	24	37	47	37	21	8	18	29	1	56	37	26	33
	46	29	54	30	12	15	13	39	56	24	40	18	34
	19	4	13	43	33	33	3	38	4	54	52	42	35
	31	1	48	23	50	36	48	17	48	13	63	28	36
	2	51	24	50	48	20	57	49	45	19	30	34	37
	53	61	34	16	29	53	38	40	6	23	6	10	38
	56	13	50	12	59	57	59	4	62	6	38	24	39
	47	49	6	8	57	27	17	48	19	16	59	16	40
	52	46	8	11	43	13	1	45	17	34	2	43	41
	6	50	52	59	64	52	40	26	21	49	18	3	42
	45	55	19	7	36	11	7	42	37	18	48	58	43
	64	23	29	4	25	45	50	62	36	45	1	41	44
	8	5	18	2	44	54	36	11	18	63	49	61	45
	37	17	33	28	55	5	26	64	57	48	11	57	46
	17	11	56	63	53	38	47	24	3	15	26	8	47
	34	39	15	6	42	16	52	16	53	33	15	47	48
	7	57	7	15	15	19	58	44	22	26	5	56	49
	35	6	36	22	13	29	5	27	38	1	14	13	50
	39	33	59	21	32	7	30	1	23	53	47	40	51
	11	19	28	42	30	4	61	36	44	10	13	6	52
	18	24	38	47	62	41	56	51	50	35	55	27	53
	12	31	26	46	23	28	34	43	40	59	43	59	54
	43	28	49	18	46	64	25	31	46	32	53	48	55
	51	53	2	58	40	31	62	53	16	5	44	30	56
	57	60	39	14	1	42	2	57	25	51	32	52	57
	3	36	12	41	38	23	6	9	54	38	20	25	58
	27	58	51	61	56	47	29	34	61	44	33	51	59
	38	22	45	3	20	3	54	14	7	52	64	4	60
	20	56	16	64	17	50	33	12	12	2	28	32	61
	23	21	46	33	9	6	31	35	47	30	19	54	62
	40	41	9	49	34	48	21	19	43	36	17	35	63
	26	18	20	9	5	58	32	18	39	64	50	49	64

P2 <sub>3</sub>	Permutation stage $\pi_{i2}$											Output	
	$\pi_{12}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$		$\pi_{122}$
Permutation element	5	1	35	55	25	38	12	22	7	2	10	44	1
	2	51	37	20	39	13	42	64	33	17	16	20	2
	55	33	36	43	5	11	60	40	10	9	51	30	3
	35	32	24	50	54	54	61	48	5	32	25	63	4
	54	57	30	44	17	8	14	31	39	51	34	54	5
	33	36	20	35	15	1	41	1	64	58	59	50	6
	36	45	55	23	45	59	6	46	60	12	19	55	7
	29	22	9	21	49	2	48	63	44	53	28	23	8
	12	14	18	19	63	25	49	60	50	5	30	64	9
	24	37	41	40	13	5	52	47	18	30	6	34	10
	34	52	59	17	3	29	18	50	54	6	17	59	11
	7	29	2	36	36	56	64	23	30	49	61	28	12
	26	4	25	8	16	37	39	49	47	11	40	8	13
	10	41	19	13	26	58	8	30	4	59	33	21	14
	57	10	56	52	38	44	16	58	49	13	4	22	15
	1	62	40	61	24	51	59	27	20	43	64	37	16
	58	26	32	60	7	31	2	14	35	23	43	29	17
	44	6	27	28	57	6	38	42	62	35	29	46	18
	22	20	6	62	61	52	26	2	48	15	63	10	19
	9	8	33	42	43	64	47	32	51	55	49	60	20
	64	34	46	38	53	61	51	57	26	19	26	42	21
	20	58	11	25	23	30	55	17	57	48	42	40	22
	13	24	38	48	42	20	19	6	14	22	45	5	23
	16	60	53	64	48	42	9	56	29	26	46	33	24
	14	53	44	32	14	39	36	26	13	60	47	15	25
	42	3	13	53	55	28	13	29	17	27	14	26	26
	37	16	49	54	51	40	44	28	56	40	57	31	27
	48	28	10	24	4	21	21	62	23	42	22	32	28
	3	43	15	63	47	46	31	18	22	21	38	13	29
	8	5	62	59	2	62	50	45	3	63	18	51	30
	21	23	12	37	46	36	25	25	63	41	50	14	31
	41	42	28	12	44	41	1	59	41	50	23	47	32
	51	56	58	27	37	26	45	34	59	29	20	27	33
	61	30	42	58	10	3	63	9	37	20	32	12	34
	46	15	47	16	12	17	15	38	34	31	9	43	35
	59	35	63	2	30	50	29	55	43	14	1	61	36
	15	38	22	31	41	33	22	4	8	39	12	16	37
	31	18	45	46	29	14	33	36	61	8	58	19	38
	43	55	34	7	22	24	62	33	52	52	54	41	39
	62	50	14	11	1	34	24	7	21	24	8	53	40
	45	46	26	51	62	47	23	44	53	16	11	4	41
	28	59	39	1	34	55	43	20	2	56	21	52	42
	19	48	61	56	28	48	54	13	24	3	41	11	43
	25	17	60	39	64	16	46	61	45	28	24	25	44
	56	19	4	47	20	18	37	12	38	18	5	49	45
	32	21	57	33	59	63	28	10	1	46	56	9	46
	52	49	50	10	33	12	4	39	19	1	15	3	47
	53	11	54	30	32	43	10	24	16	38	44	57	48
	30	2	64	6	9	15	35	52	6	45	3	62	49
	11	25	31	29	40	27	57	41	28	33	55	45	50
	6	63	17	57	60	53	7	51	25	64	39	56	51
	38	40	51	22	35	9	30	16	46	25	27	39	52
	4	47	8	4	31	10	58	11	15	62	36	17	53
	49	27	43	5	18	60	20	8	40	10	60	58	54
	63	31	48	9	52	22	56	21	11	7	53	24	55
	40	64	5	3	58	49	53	54	31	34	13	48	56
	18	54	1	34	56	45	40	3	27	37	7	35	57
	60	12	52	14	11	32	17	43	55	47	52	1	58
	17	13	16	18	8	7	5	53	9	57	31	18	59
	39	61	3	15	50	57	34	37	36	54	62	6	60
	47	39	23	41	21	23	32	35	58	61	48	36	61
	50	44	29	49	19	4	27	15	42	4	2	38	62
	27	9	7	26	6	35	3	5	12	36	37	7	63
	23	7	21	45	27	19	11	19	32	44	35	2	64

P24	Permutation stage $\pi_{i2}$											Output	
	$\pi_{12}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$		$\pi_{122}$
Permutation element	55	58	6	39	62	11	20	20	23	13	4	19	1
	49	35	20	33	30	8	13	24	12	38	59	62	2
	52	11	25	55	40	16	46	21	14	27	31	40	3
	14	14	56	19	3	45	44	50	28	11	57	30	4
	46	51	52	10	34	40	38	19	25	41	16	42	5
	22	4	19	31	29	15	49	4	56	18	52	8	6
	7	33	34	24	15	48	50	6	11	6	47	16	7
	54	56	15	12	10	37	54	16	52	15	44	25	8
	35	48	45	35	46	41	33	9	22	4	20	63	9
	64	3	35	41	51	22	24	43	38	32	32	10	10
	4	28	2	29	23	39	1	55	49	17	23	38	11
	19	9	14	56	37	29	8	62	19	56	64	3	12
	26	44	10	22	55	21	10	27	50	36	34	57	13
	10	15	12	20	17	35	19	10	2	12	63	2	14
	39	22	24	28	9	64	32	42	18	47	26	33	15
	5	24	50	1	52	50	52	45	17	59	60	58	16
	33	47	32	46	61	23	56	60	60	3	50	7	17
	31	16	21	53	36	63	21	40	8	55	39	4	18
	8	46	29	64	59	1	12	26	55	26	14	15	19
	9	59	3	42	28	51	41	31	20	22	7	37	20
	6	31	37	8	14	43	57	13	39	48	54	49	21
	45	19	39	37	49	27	16	46	33	8	61	50	22
	20	13	30	5	54	60	42	11	1	14	3	26	23
	51	62	42	13	12	47	45	64	57	64	38	61	24
	23	1	41	63	20	34	48	56	48	31	5	32	25
	60	27	48	40	57	61	36	2	63	57	8	44	26
	41	63	4	57	64	26	17	38	16	40	43	34	27
	13	10	40	26	4	42	2	61	6	60	28	6	28
	30	38	43	52	18	13	64	29	9	35	11	41	29
	36	18	53	51	1	36	51	15	31	21	18	21	30
	59	40	36	23	43	57	29	12	10	29	9	64	31
	48	36	64	50	32	17	18	14	26	23	30	51	32
	53	64	55	60	7	58	9	8	62	61	56	20	33
	29	2	59	34	8	25	5	28	34	63	2	17	34
	44	17	38	54	50	56	6	48	46	20	40	24	35
	43	34	54	7	16	14	26	52	41	50	33	23	36
	32	20	31	58	33	62	14	3	59	30	51	18	37
	47	53	1	18	31	59	7	39	45	51	24	5	38
	62	5	28	32	6	54	61	33	51	39	53	48	39
	42	49	47	48	60	7	53	35	64	24	35	52	40
	16	25	51	14	22	12	22	47	13	46	27	46	41
	3	29	23	21	53	10	37	7	58	52	17	56	42
	58	55	33	17	45	19	23	1	3	45	29	28	43
	2	42	8	45	25	18	25	49	24	28	10	53	44
	25	60	11	15	47	53	55	17	37	9	49	13	45
	50	50	49	36	42	4	31	54	36	43	46	39	46
	21	54	46	4	39	28	63	18	47	49	13	55	47
	63	32	7	25	44	38	59	63	7	58	48	54	48
	40	41	18	11	13	9	60	44	35	42	25	45	49
	12	23	44	38	11	2	4	37	21	10	37	59	50
	24	37	26	27	19	30	43	32	40	16	21	1	51
	57	21	5	61	35	31	34	41	32	5	22	29	52
	56	39	17	43	2	32	30	22	27	53	42	14	53
	1	57	16	9	63	49	35	34	61	37	55	60	54
	28	26	27	59	41	3	40	25	30	54	45	11	55
	17	52	63	62	27	46	58	53	29	1	58	12	56
	61	12	13	3	26	6	27	58	5	44	12	43	57
	18	8	61	2	24	33	39	30	15	2	19	31	58
	37	61	62	30	48	44	11	59	43	33	15	9	59
	11	30	9	44	38	5	47	23	44	62	36	35	60
	34	45	58	16	58	20	15	51	4	34	1	36	61
	27	6	22	49	21	24	62	57	53	7	62	27	62
	38	43	57	6	56	55	28	5	42	19	41	22	63
	15	7	60	47	5	52	3	36	54	25	6	47	64

P2 <sub>5</sub>	Permutation stage $\pi_{i2}$											Output	
	$\pi_{12}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$		$\pi_{122}$
Permutation element	52	51	43	56	37	48	2	9	6	8	4	48	1
	23	44	46	41	12	7	24	26	5	2	49	63	2
	13	48	16	12	28	47	62	10	46	15	17	39	3
	15	13	35	8	3	14	1	42	47	25	3	55	4
	44	17	41	11	31	45	38	7	43	52	14	19	5
	33	61	34	2	36	27	40	51	27	57	6	23	6
	34	63	40	49	4	53	13	21	25	41	46	22	7
	54	35	7	32	41	64	42	12	11	9	48	62	8
	3	34	44	57	35	21	12	59	41	22	24	6	9
	5	38	54	61	20	15	53	30	38	60	44	21	10
	29	21	11	39	22	6	7	32	59	53	27	29	11
	45	27	3	6	16	32	18	4	62	31	41	49	12
	50	40	62	55	63	36	43	20	7	12	59	33	13
	28	14	30	15	60	25	16	61	2	47	38	51	14
	51	41	26	28	8	35	11	36	48	51	61	31	15
	7	19	29	62	23	39	30	38	24	7	32	58	16
	59	30	49	22	27	8	5	8	64	61	15	17	17
	36	64	2	33	33	43	57	39	61	48	19	12	18
	27	42	25	43	14	37	64	47	20	14	55	32	19
	30	29	5	7	24	33	27	15	54	20	28	36	20
	56	12	27	19	2	24	21	2	16	34	33	16	21
	63	57	21	26	54	49	51	56	42	30	26	14	22
	17	6	17	14	48	17	45	11	56	58	25	45	23
	21	36	38	54	32	38	20	1	51	54	54	11	24
	43	9	8	18	21	30	28	46	31	43	36	5	25
	38	5	45	38	30	28	56	53	63	24	18	34	26
	48	8	56	5	61	16	46	23	17	5	5	9	27
	46	2	60	24	45	20	47	37	53	26	13	7	28
	40	59	42	45	59	19	41	3	58	55	35	1	29
	4	15	18	17	49	26	34	45	28	56	7	53	30
	2	60	13	30	43	55	59	48	8	18	2	37	31
	20	56	23	16	57	61	22	50	19	35	50	10	32
	42	53	32	4	5	10	44	52	30	50	40	56	33
	25	33	12	10	64	46	37	14	45	49	12	41	34
	22	23	9	23	51	50	61	27	36	19	39	59	35
	64	26	63	44	7	18	6	35	40	13	60	30	36
	14	37	15	34	40	1	49	5	26	46	42	52	37
	41	24	4	53	17	60	31	31	18	39	43	27	38
	32	31	51	31	6	3	29	34	4	28	22	13	39
	1	47	58	37	62	11	17	55	9	45	58	44	40
	53	10	53	29	15	12	10	28	50	42	31	20	41
	35	4	10	50	53	52	60	41	3	37	11	3	42
	60	7	1	42	58	9	15	16	37	21	57	35	43
	37	62	59	47	26	59	48	64	57	16	51	26	44
	6	43	14	59	1	51	26	17	33	32	30	25	45
	58	32	39	52	38	34	32	43	35	33	64	40	46
	12	20	64	9	42	2	8	13	34	4	21	2	47
	11	39	6	1	56	4	52	54	12	36	34	24	48
	9	22	28	64	19	42	35	22	49	3	47	42	49
	31	45	22	3	44	41	14	6	52	17	53	61	50
	18	16	57	46	47	31	4	57	32	63	16	38	51
	57	11	33	60	34	22	39	29	39	38	62	28	52
	8	54	61	13	18	29	3	49	60	40	29	60	53
	47	55	48	25	9	44	58	24	14	64	9	18	54
	26	49	20	58	55	40	33	33	10	23	63	50	55
	62	52	47	63	52	57	23	40	15	6	37	15	56
	49	58	55	48	10	23	63	19	23	59	45	43	57
	16	46	19	40	46	5	36	44	13	11	52	8	58
	55	1	36	35	50	54	54	18	29	10	23	54	59
	19	28	37	20	39	13	9	63	44	27	8	64	60
	61	3	50	36	11	56	50	58	21	44	10	46	61
	10	18	52	21	25	62	19	25	55	62	56	57	62
	39	25	24	27	29	58	25	60	22	1	1	4	63
	24	50	31	51	13	63	55	62	1	29	20	47	64

## Annex B

### Adaptation of $512 \times 510$ staircase forward error correction codes for OTU4-SC FEC

(This annex forms an integral part of this Recommendation.)

Annex A.2 describes a generic Base Block that is used to create the  $512 \times 510$  bit SC FEC block.

For generating SC FEC codewords of an OTU4-SC signal, this generic Base Block ( $8 \times 30592$  bit +  $8 \times 2048$  bit) will be created by mapping the OTU4 information and FEC bits into it.

This annex details these mapping specific aspects.

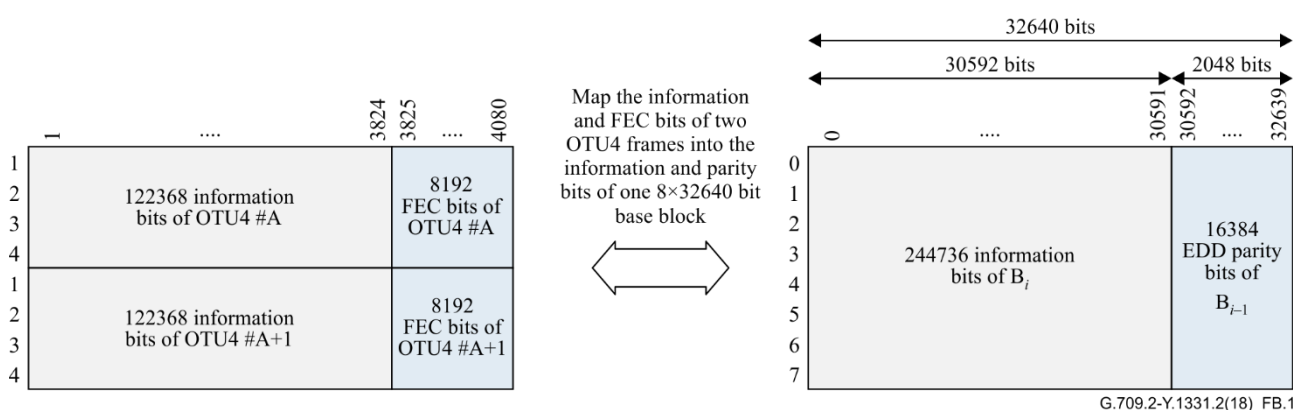
#### B.1 OTU4-SC bit and staircase forward error correction specific Base Block mapping relationship

The 122368 information bits in two consecutive OTU4-SC frames map into one  $8 \times 30592$  bit "information base block" and the associated 8192 FEC parity bits in the two consecutive OTU4-SC frames map into one  $8 \times 2048$  bit "parity base block" as illustrated in Figure B.1.

The mapping is one-to-one so that:

- bit 1 in column 1, row 1 of OTU4 #A maps into row 0, column 0 of the information base block  $B_i$ , bit 2 in column 1, row 1 of OTU4 #A maps into row 0, column 1 of the information base block  $B_i$ , bit 3 in column 1, row 1 of OTU4 #A maps into row 0, column 2 of the information base block  $B_i$ , etc. and bit 8 in column 3824 of OTU4 #A+1 maps into row 7, column 30591 of the information base block  $B_i$ .
- bit 1 column 3825, row 1 of OTU4 #A maps into row 0, column 30592 of the parity base block  $B_{i-1}$ , bit 2 in column 3825, row 1 of OTU4 #A maps into row 0, column 30593 of the parity base block  $B_{i-1}$ , bit 3 in column 3825, row 1 of OTU4 #A maps into row 0, column 30594 of the parity base block  $B_{i-1}$ , etc. and bit 8 in column 4080 of OTU4 #A+1 maps into row 7, column 32639 of the parity base block  $B_{i-1}$ .

Frame #A corresponds to the multi-frame alignment signal (MFAS) with bit 8 equal to 0 while frame #A+1 corresponds to the following frame with MFAS bit 8 equal to 1 (see also Figure B.2).



**Figure B.1 – OTU4-SC bit and staircase forward error correction specific Base Block ( $8 \times 30592$  bit +  $8 \times 2048$  bit "base information and parity blocks") mapping relationship**

#### B.2 Error decorrelator controller synchronization

To synchronize the state of the error decorrelator controllers between the receiver and the transmitter, the OTUk MFAS byte is used to identify the 128 blocks of the  $128 \times 8 \times 32640$  bit base multi-block

structure in clauses B.1 and A.4. The seven MSBs of the MFAS are locked to the multi block alignment signal (MBAS) sequence as illustrated in Figure B.2.

		7-bit multi-block alignment signal									
		1	2	3	4	5	6	7			
		8-bit MFAS OH									
		1	2	3	4	5	6	7	8		
		:									
0	0	0	0	0	0	0	0	0	0	0	OTU4 #A
0	0	0	0	0	0	0	0	0	0	1	OTU4 #A+1
1	0	0	0	0	0	0	0	0	1	0	OTU4 #A+2
1	0	0	0	0	0	0	0	0	1	1	OTU4 #A+3
2	0	0	0	0	0	0	1	0	0	0	OTU4 #A+4
2	0	0	0	0	0	0	1	0	1	0	OTU4 #A+5
3	0	0	0	0	0	0	1	1	0	0	OTU4 #A+6
3	0	0	0	0	0	0	1	1	1	1	OTU4 #A+7
		:									
		:									
126	1	1	1	1	1	1	1	0	1	0	OTU4 #A+253
127	1	1	1	1	1	1	1	1	1	0	OTU4 #A+254
127	1	1	1	1	1	1	1	1	1	1	OTU4 #A+255
0	0	0	0	0	0	0	0	0	0	0	OTU4 #A+256
0	0	0	0	0	0	0	0	0	0	1	OTU4 #A+257
1	0	0	0	0	0	0	0	1	0	0	OTU4 #A+258
		:									

G.709.2-Y.1331.2(18)\_FB.2

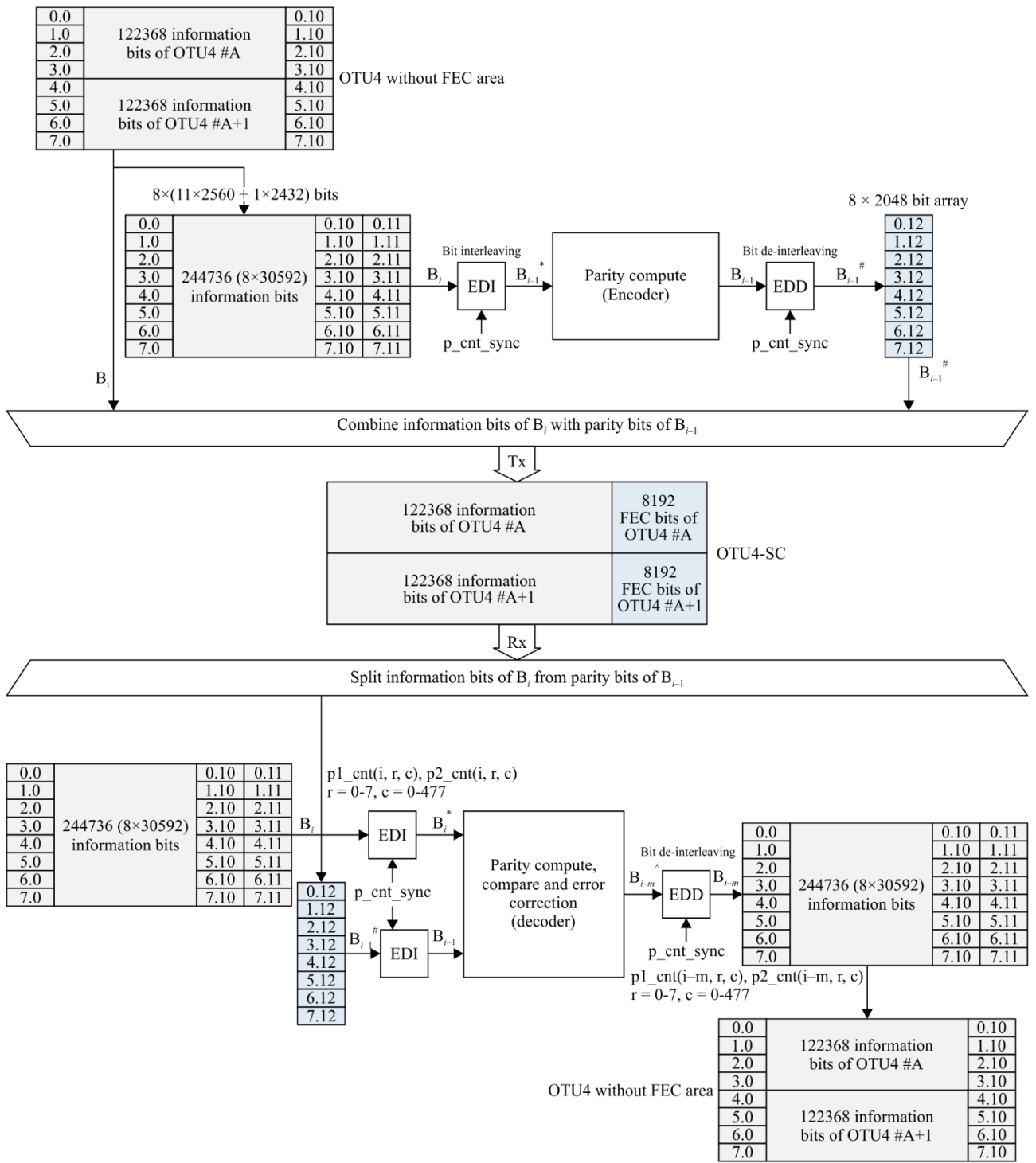
**Figure B.2 – Multi-block alignment signal**

### B.3 OTU4-SC transmitter and receiver staircase forward error correction processing

Figure B.3 presents an OTU4-SC specific version of Figure A.1. In Figure B.3, the "Input frame without FEC parity", "Output frame with SC FEC parity" and "Output frame without FEC parity" blocks are replaced by two OTU4 frames excluding FEC parity that contain 122368 information bits each, two OTU4-SC frames that contain 122368 information and 8192 parity bits each and two OTU4 without FEC frames that contain 122368 information bits each, respectively.

The information bits from two frames of an OTU4 signal are mapped into a staircase specific  $8 \times 30592$  bit base information block format (see clause B.1), after which the staircase specific transmit side processing is performed and parity bits become available in a staircase specific  $8 \times 2048$  bit base parity block format (see B.1). OTU4 information bits plus computed parity bits are then mapped into the OTU4-SC frame format.

On the receive side, the information and parity bits in the OTU4-SC signal are mapped into SC FEC specific information and parity blocks. Then SC FEC specific receive side processing is performed and decoded information bits are stored in the first 30592 columns of a Base Block. The information bits are then mapped to the OTU4 without FEC frame format.



G.709.2-Y.1331.2(18)\_FB.3

**Figure B.3 – OTU4-SC transmitter and receiver staircase forward error correction processing**



## Appendix I

### Example applications

(This appendix does not form an integral part of this Recommendation.)

OTU4-SC interfaces can be used in a variety of system interworking applications.

Example applications for using OTU4-SC interfaces are shown in Figure I.1 and Figure I.2. The first example is an OTN handoff between router (R) and transport (T) nodes within one administrative domain, while the second is a handoff between OTN equipment of different vendors within one administrative domain.

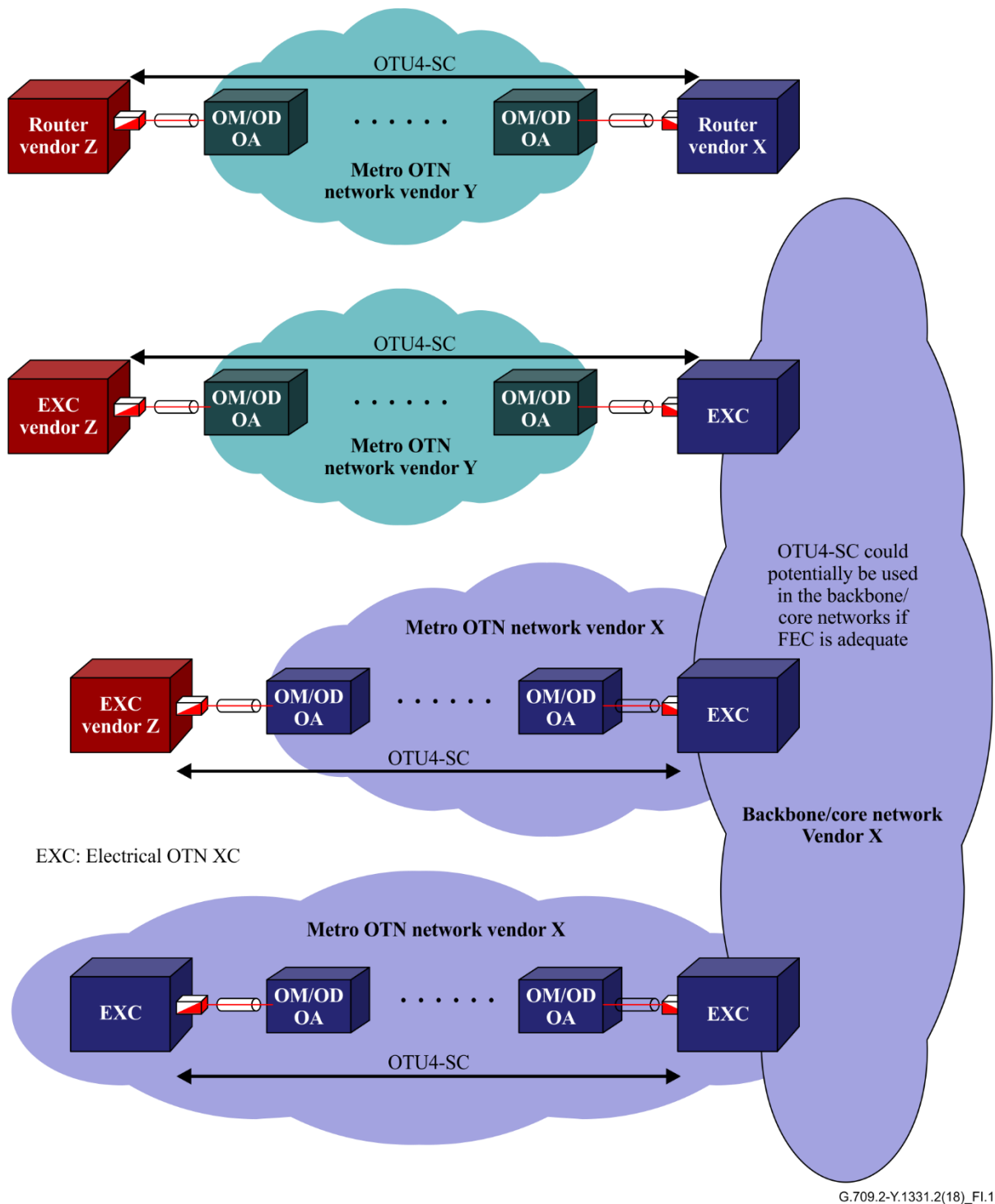
OTNs are typically subdivided into metro and core networks, where the core network interconnects metro networks. Transport services may stay in one metro network or they may extend over several. In the latter case, they may be passed through the core network.

Network elements in the metro network play different roles such as metro/core gateway, edge towards customer and transit nodes. The customer-facing functions lead to some diversity of client interfaces. Network elements from different vendors may be used to serve this broad scope of function. OTU4-SC interfaces could be used to interconnect network elements of different vendors or the same vendor enabling multi-vendor interworking.

Figure I.1 illustrates an OTN core network with associated metro networks, featuring:

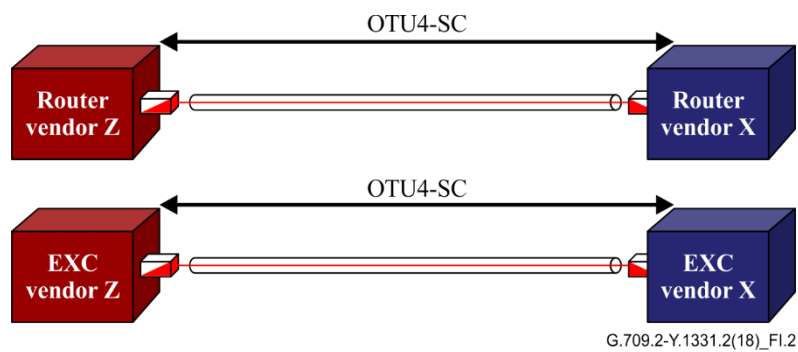
- OTN ODU cross-connect nodes with electrical switch fabric [labelled EXC (electrical cross-connect)] of vendor Z or X interconnected with EXC of vendor X using an OTU4-SC interface;
- packet switching nodes (labelled "Router") of vendor Z interconnected with the router of vendor X using an OTU4-SC interface;
- interconnection of the above EXC or router nodes through a metro OTN network;
- interconnection of the above EXC or router nodes, establishing a path over which the optical channel (OCh) or optical tributary signal assembly (OTSiA) OH can be exchanged as specified in [ITU-T G.872], [ITU-T G.709] and [b-ITU-T G.7712] enabling end-to-end optical path monitoring;
- interconnection in the backbone/core network is also possible if the OTU4-SC FEC is adequate.

Details of the optical path passed by the OTU4-SC signals are specified in [b-ITU-T G.698.2].



**Figure I.1 – Example OTU4-SC deployments in one administrative domain**

Figure I.2 illustrates interconnection of the EXC or router nodes through a point-to-point fibre, establishing an interdomain interface beyond the distances supported by the OTU4 specified in [ITU-T G.709] and [ITU-T G.959.1].



**Figure I.2 – Example OTU4-SC deployments establishing an interdomain interface beyond the distances supported by the OTU4**

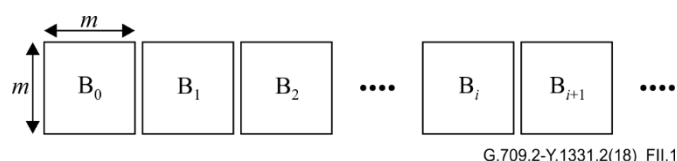
## Appendix II

### Generic principles of forward error correction using blockwise-recursively-encoded Staircase FEC

(This appendix does not form an integral part of this Recommendation.)

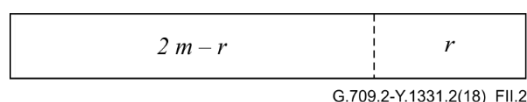
#### II.1 Staircase FEC codes: Specifications and basic properties

Staircase FEC (SC FEC) codes are a class of error-correcting codes that combine ideas from recursive convolutional coding and block coding, resulting in a "continuous" product-like code that is characterized by the relationship between successive matrices of symbols. Consider the (infinite) sequence  $B_0, B_1, B_2, \dots$  of  $m$  by  $m$  matrices  $B_i, i \in \mathbb{Z}^+$ , where the elements of  $B_i$  are binary (i.e., in  $GF(2)$ ), as illustrated in Figure I.1.



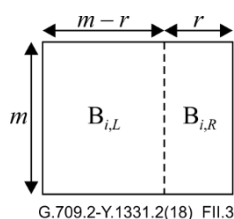
**Figure II.1 – A stream of  $m \times m$  arrays of symbols**

First, a conventional FEC block code (e.g., Hamming, BCH, RS) in systematic form is selected to serve as the component code; this code, which henceforth is referred to as  $C$ , is selected to have block length  $2m$  symbols,  $r$  of which are parity symbols. As illustrated in Figure II.2, the leftmost  $2m - r$  symbols constitute information positions of  $C$ , and the rightmost  $r$  symbols the parity positions of  $C$ .



**Figure II.2 – The subdivision of the length  $2m$  systematic component codeword into its leftmost  $2m - r$  information positions and its rightmost  $r$  parity positions**

In light of this choice, it is useful to further subdivide each block  $B_i$  into its  $m - r$  leftmost columns and its  $r$  rightmost columns, as illustrated in Figure II.3.



**Figure II.3 – The subdivision of block  $B_i$  into its  $m - r$  leftmost columns and its  $r$  rightmost columns**

Prior to encoding, block  $B_0$  is initialized to a reference state (e.g., block  $B_0$  could be initialized to the all-zeros state; note that the specific choice of initialization is unimportant, since the decoder is required to "bootstrap" itself from an unknown starting state, i.e., the decoder cannot exploit any knowledge of the reference state). Next,  $m(m - r)$  information bits are stored in  $B_{(1,L)}$ , then the values of  $B_{(1,R)}$  are calculated as follows:

- 1) Form the  $m \times (2m - r)$  matrix  $\Lambda = [B_0^T \ B_{(1,L)}]$ .

(NOTE –  $B_0^T$  is the transposed matrix of  $B_0$ .)

- 2) The elements of  $B_{(1,R)}$  are then computed such that each of the rows of the matrix  $[B_0^T \ B_{(1,L)} \ B_{(1,R)}]$  is a valid codeword of  $C$ . That is, the elements in the  $j$ th row of  $B_{(1,R)}$  are exactly the  $r$  parity symbols that result from encoding the  $2m - r$  "information" symbols in the  $j$ th row of  $\Lambda$ .

Generally, the relationship between successive blocks in a staircase code satisfies the following relation:

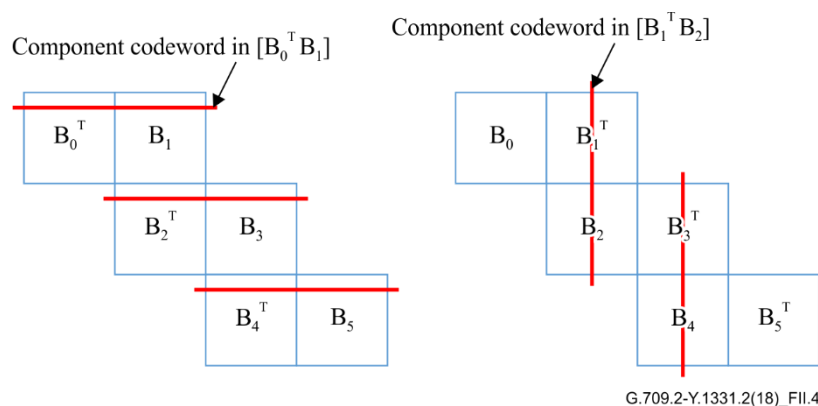
For any  $i \geq 1$ , each of the rows of the matrix

$$[B_{i-1}^T \ B_{(i)}]$$

is a valid codeword of the component code  $C$ .

NOTE –  $B_{i-1}^T$  is the transposed matrix of  $B_{i-1}$ .

An equivalent "visual" description, from which their name originates, is suggested by Figure II.4, in which every row and every column in the staircase array is a valid codeword of  $C$ .



**Figure II.4 – The 'staircase' visualization of the family of staircase forward error correction codes**

The rate of a SC FEC code is:

$$R = 1 - \frac{r}{m}$$

since encoding produces  $r$  parity symbols for every set of  $m - r$  "new" parity symbols. Note that the related product code has rate:

$$\left(\frac{2m-r}{2m}\right)^2 = 1 - \frac{r}{m} + \frac{r^2}{4m^2}$$

which is greater than the rate of the staircase code. However, for sufficiently high rates, their rate difference is small, and furthermore, the SC FEC code outperforms a product code of the same rate.

Similarly, while the block length of the related product code is  $m^2$ , the SC FEC codes are naturally unterminated (i.e., their block length is indeterminate), and thus admit a range of decoding strategies with varying latencies.

Finally, using arguments analogous to those used for product codes, a  $t$ -error-correcting component code  $C$  with minimum distance  $d$  results in a staircase code with minimum distance  $d^2$ .

## II.2 Error decorrelator function

Most FEC codes are designed to perform under AWGN, i.e., the decoder assumes that the noise samples are uncorrelated and gaussian distributed. The performance of these codes can substantially

decrease if the added noise is correlated. Error decorrelators can be added to the FEC encoder/decoder to reduce the correlation of noise samples, thus approaching the performance under AWGN.

In conjunction with the SC FEC encoder/decoder, the error decorrelator block can be used to randomize the position of the correlated error symbols to make sure the performance of the staircase code is not impacted by correlated errors.

### II.2.1 Error decorrelator datapath

The EDI and the corresponding EDD operate directly on framed data, in a complementary fashion at the input (and output) of the core encoder and decoder blocks, as illustrated in Figure II.5. The purpose of performing bit interleaving at the input (EDI) and output (EDD) of the SC FEC encoder is to preserve the "systematic" nature of the encoding function (i.e., the position of data bits in the data frame are unaffected). At the decoder, the EDI is applied to the input of the SC FEC decoder, which effectively randomizes the position of the channel errors. Finally, at the decoder output, the EDD is applied to restore the bits to their transmitted ordering.

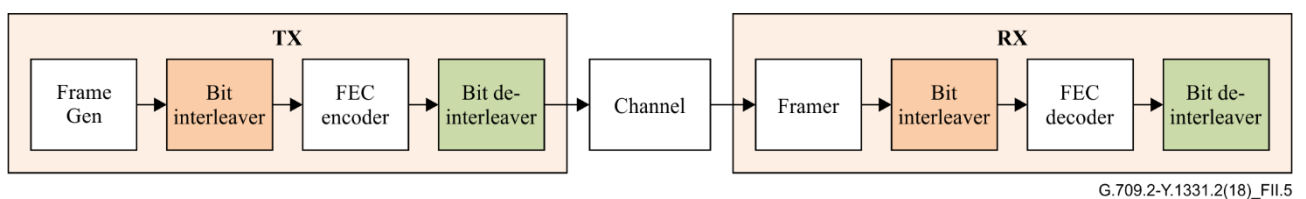


Figure II.5 – Error decorrelator

### II.2.2 Error decorrelator implementation

In order to efficiently implement a 2048-bit pseudorandom interleaver/de-interleaver, we restrict ourselves to a set of structured interleavers composed of simple building blocks. Figure II.6 shows an example of a 4096-element interleaver, implemented by passing a 64-bit data stream through a time-varying 64-element block permutation P1, the output of which is written to a 64 × 64 block interleaver in row-by-row fashion. This block of data is then read column-by-column and passed through a 64-bit time-varying 64-element block permutation P2.

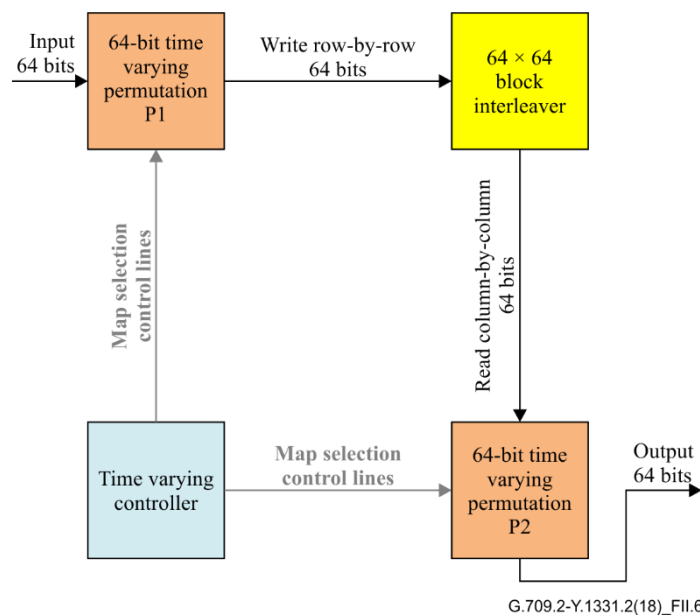
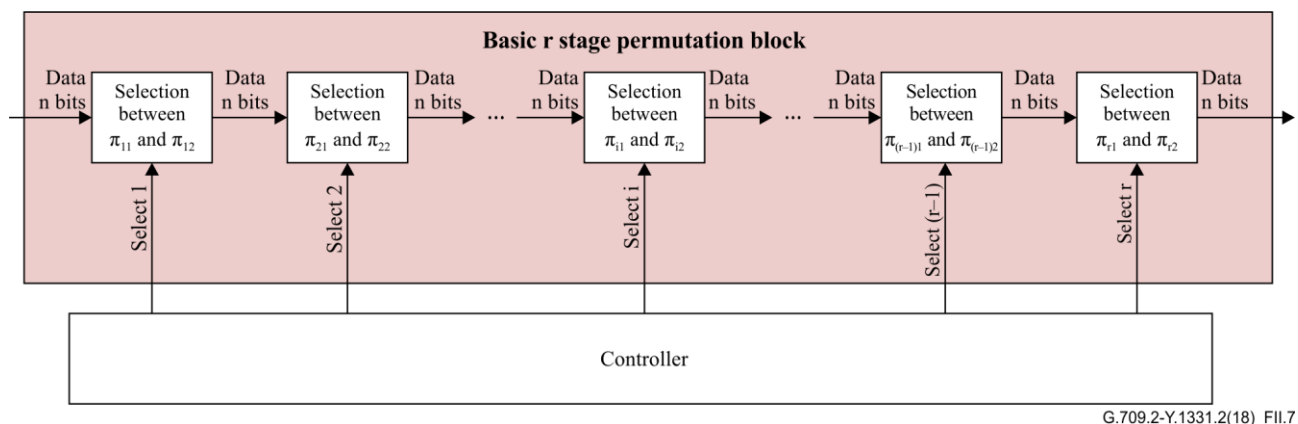


Figure II.6 – Illustrative example of error decorrelator architecture

In order to provide a simple mechanism to induce the pseudorandom nature of the overall interleaver, P1 and P2 are implemented via a cascade of  $r$  "elementary" permutation stages; in each stage, one of two fixed permutations ( $\pi_{i1}$  when "Select  $i$ " is a "0",  $\pi_{i2}$  when "Select  $i$ " is a "1") is performed on the 64-bit data, the choice of which is controlled by a pair of time-varying  $r$ -bit control signals. Figure II.7 is a block diagram of the implementation.



**Figure II.7 –  $r$  Stage permutation for P1 and P2**

The block interleaver does not vary with time, and is assumed to be "equivalent" to a matrix transpose operator (i.e., data are read-in row-by-row and read-out column-by-column).

### II.3 Decoding a $512 \times 510$ staircase forward error correction code

Syndrome-based iterative decoding can be used to decode the received signal. Generation of the syndromes is done in a similar fashion to the encoding. The resulting syndrome equation is solved using the standard FEC decoding scheme and error locations are determined. Error locations are then flipped and standard iterative decoding proceeds. The latency of the decoder is a function of number of blocks used in the decoding process. Generally increasing the number of blocks improves the coding gain.

The SC FEC code is an example of a highly iterative Code by which is meant that the decoder is designed in such a way that it may decode a single constituent code word many times. The SC FEC code is a continuously interleaved code which means that, on the receive side, the more blocks that are included in the decoding process, the better the coding gain. It turns out that, with a 6.7% HD-FEC, decoding over more than six blocks results in insignificant improvement in net-coding gain.

Instrumentation of this decoder has revealed that, operating in the presence of AWGN, on average, each codeword is decoded 3.2 times.

## Appendix III

### 40/38/32 × 64 bit block interleaver

(This appendix does not form an integral part of this Recommendation.)

This appendix provides an illustration of the  $n \times 64$  bit block interleavers ( $n = 40, 38, 32$ ) within an EDI or EDD process specified in clause A.3.

Figure III.1 illustrates the operation of the  $40 \times 64$  bit block interleaver in the EDI and EDD.

In the EDI, the 2560 (40 sets of 64) input bits (numbered 1 to 2560) that are output by the P1 permutation process are written into the  $40 \times 64$  bit array in a row-by-row fashion as shown in Figure III.1. Bit 1 is written into {row,column} bit position {0,0}, bit 2 in {0,1}, ..., bit 64 in {0,63}, bit 65 in {1,0}, ..., and bit 2560 in {39,63}. The 2560 bits are read out in a columnwise fashion and presented at the input of the P2 permutation process as 40 sets of 64 bits. The first 64 bits are bits 1, 64, 128, 192, ..., 2496, 1, 65, 129, ..., 1473, which are the yellow-marked bits in columns 0 and 1. The second 64 bits are bits 1537, 1601, 1665, ..., 467 which are the orange-marked bits in columns 1, 2 and 3. The third 64 bits are the yellow-marked bits in columns 3 and 4, etc. until the fortieth 64 bits in columns 62 and 63.

In the EDD, the 2560 bits that are output by the P2\_inverse permutation process are written into the  $40 \times 64$  bit array in a column-wise fashion, i.e., in the order {0,0}, {1,0}, {2,0}, ..., {39,0}, {0,1}, {1,1}, etc. until {39,63}. The 2560 bits are read out in a row-by-row fashion, first {0,0}, {0,1}, {0,2}, .., {0,63} secondly {1,0}, {1,1}, {1,2}, .., {1,63}, etc. and presented at the input of the P1\_inverse permutation process as 40 sets of 64 bits.

Figure III.2 illustrates the operation of the  $38 \times 64$  bit block interleaver in the EDI and EDD in a similar manner.

Figure III.3 illustrates the operation of the  $32 \times 64$  bit block interleaver in the EDI and EDD in a similar manner.

NOTE – The numbers in figures are readable with a zoom level of 250%.





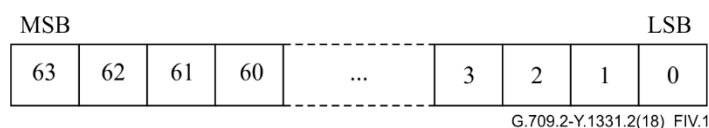


## Appendix IV

### Generic permutation maps in clause A.8.1 – Numbering according to bit weight

(This appendix does not form an integral part of this Recommendation.)

This appendix provides the generic permutation maps tables with bit numbering according to bit weight rather than transmission order as specified in clause A.8.1 and according to clause 5.



**Figure IV.1 – 64 bit numbering according to bit weight**

For the sake of illustration, consider the permutation maps  $\pi_{i2}$  specified in the matrix  $P1_1$ . Note that each column (there are 12 columns, in one-to-one correspondence with the 12 stages illustrated in Figure A.7) is a 64-element permutation on the values 0 to 63. Specifically, if we consider the first column  $\pi_{12}$  of  $P1_1$ , the permutation specifies that the bit in position 26 of the input to the corresponding permutation stage appears in the output of the permutation stage at position 63, the bit in position 9 of the input appears in the output at position 62, the bit in position 27 of the input appears in the output at position 61, and so on.

P1 <sub>1</sub>	Permutation stage $\pi_{i2}$												
	$\pi_{i2}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$	$\pi_{122}$	Output
Permutation element	26	16	45	6	6	43	35	30	38	32	14	4	63
	9	3	31	49	9	9	59	8	22	13	30	11	62
	27	60	42	1	12	39	57	28	15	52	16	35	61
	49	63	52	62	15	22	27	49	63	9	55	18	60
	16	31	5	16	63	10	29	63	62	42	34	43	59
	14	23	3	36	30	35	30	52	58	1	32	42	58
	10	46	26	52	29	42	3	13	4	3	15	63	57
	56	32	4	61	51	1	62	14	30	55	61	59	56
	45	28	0	2	23	12	36	56	5	63	22	53	55
	51	62	12	30	45	21	18	25	21	12	9	39	54
	11	42	17	31	46	56	56	59	48	59	44	51	53
	55	7	59	32	8	53	41	47	18	40	39	37	52
	40	41	27	20	50	57	13	58	52	26	36	57	51
	46	9	10	28	37	45	42	33	37	30	24	2	50
	62	10	2	47	2	36	45	36	20	17	50	47	49
	35	13	9	8	22	32	16	17	0	57	5	15	48
	7	33	44	54	32	48	2	20	59	19	58	0	47
	1	59	51	55	13	50	11	11	61	49	63	36	46
	21	24	30	46	41	38	53	16	28	25	4	32	45
	50	2	8	33	47	54	47	48	27	53	10	5	44
	12	1	54	29	10	63	17	41	16	10	23	3	43
	42	35	22	43	3	27	49	51	19	6	49	14	42
	63	18	18	7	36	26	60	62	12	62	46	60	41
	25	21	38	50	4	59	7	60	2	27	47	9	40
	48	49	33	39	17	30	50	38	49	50	42	13	39
	43	22	23	15	54	11	44	1	31	28	29	38	38
	0	14	49	60	28	46	0	19	41	2	8	30	37
	5	15	1	10	53	31	26	29	32	8	52	25	36
	47	27	41	22	49	37	21	9	14	45	11	44	35
	4	5	32	59	61	13	28	57	36	33	38	28	34
	58	4	20	18	38	28	22	46	26	60	26	61	33
	6	25	53	37	39	55	37	40	51	56	2	58	32
	29	38	63	51	5	49	33	6	45	41	7	20	31
	13	17	21	24	44	41	15	31	54	0	31	45	30
	60	29	48	27	56	8	54	34	1	58	17	56	29
	61	12	6	34	25	34	24	22	53	29	35	6	28
	38	6	50	38	52	40	1	55	44	46	19	54	27
	31	43	36	53	59	51	6	12	29	31	3	19	26
	8	39	58	26	7	3	55	35	33	16	37	46	25
	23	57	39	9	27	17	34	7	56	36	53	33	24
57	58	34	14	35	4	63	39	10	23	40	62	23	
33	26	13	4	1	29	58	50	7	15	1	52	22	
22	19	35	44	20	58	39	54	8	11	18	31	21	
19	11	47	42	21	44	32	21	47	18	45	40	20	
41	51	61	25	14	2	31	15	43	37	13	16	19	
53	44	24	11	26	16	46	27	40	51	54	23	18	
34	8	55	48	60	18	43	4	23	39	59	50	17	
32	61	7	17	18	19	61	0	42	38	20	55	16	
15	54	43	58	48	60	23	32	6	61	6	34	15	
17	0	14	5	42	5	4	3	55	43	43	27	14	
2	47	16	63	62	6	12	5	46	48	41	10	13	
30	56	37	41	0	24	5	10	25	35	21	22	12	
28	20	56	35	58	61	51	61	57	24	27	29	11	
44	36	46	40	16	14	14	2	24	54	60	24	10	
24	34	60	45	34	47	48	26	60	20	62	41	9	
37	40	15	56	11	23	9	45	9	4	25	49	8	
54	48	62	13	40	52	19	43	34	22	0	1	7	
39	50	40	12	19	33	25	23	11	5	12	8	6	
52	55	29	57	24	7	52	37	39	44	48	26	5	
18	30	28	3	31	20	38	53	35	7	57	21	4	
3	37	19	19	43	62	20	42	13	21	28	7	3	
59	45	25	0	33	25	10	18	3	34	56	48	2	
36	53	11	21	55	15	8	44	17	47	51	17	1	
20	52	57	23	57	0	40	24	50	14	33	12	0	

P1 <sub>2</sub>	Permutation stage $\pi_{12}$												Output
	$\pi_{12}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$	$\pi_{122}$	
Permutation element	37	8	25	40	34	50	31	53	4	18	34	55	63
	45	33	3	31	29	12	24	42	23	25	8	31	62
	44	52	46	54	63	57	55	61	52	12	20	50	61
	20	5	52	5	8	45	16	43	19	33	56	26	60
	23	14	24	22	36	4	40	7	59	15	7	40	59
	42	41	31	39	35	26	49	11	27	6	40	17	58
	52	50	45	56	16	47	54	46	35	35	54	16	57
	53	26	61	44	22	44	18	55	56	61	51	42	56
	19	20	2	9	11	31	12	57	44	22	15	63	55
	39	40	44	16	6	49	61	20	28	43	44	45	54
	36	32	48	25	25	14	29	32	18	0	38	51	53
	41	30	18	28	19	59	50	40	8	41	22	3	52
	48	3	19	18	38	7	37	37	3	19	31	32	51
	31	62	30	46	61	62	59	62	39	16	12	61	50
	43	36	26	45	58	36	63	51	31	14	28	4	49
	25	21	20	49	17	53	19	60	6	40	36	12	48
	30	47	4	55	56	10	23	0	10	37	39	53	47
	4	22	49	58	28	38	39	10	15	39	46	27	46
	59	10	9	32	57	23	46	8	46	32	6	11	45
	0	39	23	21	54	35	27	29	51	38	45	62	44
	21	28	57	30	62	18	33	41	40	26	63	1	43
	15	9	8	36	24	25	11	17	20	42	17	13	42
	28	6	1	35	59	60	36	15	0	13	55	57	41
	16	46	38	20	55	34	41	9	2	27	4	24	40
	27	42	58	4	44	40	58	27	63	29	50	8	39
	61	56	0	6	1	37	57	63	1	48	3	54	38
	63	55	55	8	14	39	4	22	24	60	53	37	37
	58	37	28	23	9	29	3	14	25	31	48	35	36
	17	27	21	38	45	8	9	16	22	51	26	43	35
	26	53	17	48	27	15	20	45	30	10	2	7	34
	60	12	35	52	20	41	56	52	7	53	29	14	33
	3	4	42	37	46	11	6	18	45	17	62	33	32
	7	63	39	53	47	48	8	59	49	20	58	9	31
	13	54	22	57	21	55	47	30	62	5	47	58	30
	12	16	43	43	2	22	38	47	32	55	5	2	29
	46	60	5	3	53	43	17	35	21	58	60	15	28
	57	29	59	2	51	9	53	44	5	54	16	56	27
	9	17	10	33	23	20	2	12	12	7	42	30	26
	24	0	37	42	52	17	15	36	36	49	23	48	25
	2	45	33	19	12	28	5	33	57	36	13	34	24
	14	48	36	29	43	63	25	39	61	59	9	59	23
	55	58	12	7	39	6	44	28	37	62	24	19	22
	22	38	32	24	18	16	26	49	55	23	49	6	21
	10	19	40	41	60	46	21	1	16	46	61	44	20
	38	49	14	59	4	33	10	50	9	34	18	49	19
	40	44	63	51	3	2	62	5	17	1	11	38	18
	54	61	13	63	32	24	43	25	53	56	0	22	17
	8	15	53	14	40	27	45	4	11	3	27	25	16
	50	25	56	60	48	58	13	48	41	11	33	36	15
33	13	16	50	49	13	1	34	43	2	10	39	14	
35	24	27	11	7	32	51	13	47	30	37	46	13	
29	57	54	15	33	52	34	26	33	57	14	21	12	
5	7	15	26	30	1	48	38	42	8	32	10	11	
56	59	47	10	42	5	30	24	48	52	35	47	10	
34	35	50	62	13	61	22	21	38	9	52	52	9	
6	1	11	0	41	30	32	19	54	24	57	60	8	
32	23	51	27	0	19	35	3	60	4	21	41	7	
11	11	60	17	37	21	52	6	26	47	41	20	6	
47	51	6	34	50	0	7	54	34	45	59	29	5	
62	31	41	47	10	56	42	56	50	28	25	5	4	
18	34	62	13	31	3	0	31	14	63	19	28	3	
51	18	29	1	15	42	14	2	58	21	30	18	2	
1	43	34	61	26	54	60	23	13	50	43	0	1	
49	2	7	12	5	51	28	58	29	44	1	23	0	

P1 <sub>3</sub>	Permutation stage $\pi_{i2}$												Output
	$\pi_{12}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$	$\pi_{122}$	
Permutation element	46	1	28	58	55	38	7	9	33	2	34	42	63
	21	41	46	24	60	58	13	8	60	35	42	61	62
	37	20	19	53	33	54	17	28	44	61	38	0	61
	6	21	16	5	39	19	18	1	55	9	54	19	60
	41	62	54	63	11	20	40	49	21	52	31	45	59
	52	56	59	9	53	11	48	31	0	43	56	37	58
	10	15	34	47	36	7	25	12	24	13	32	30	57
	9	28	1	18	42	5	24	14	46	17	51	39	56
	32	11	36	17	28	57	60	3	37	10	8	56	55
	58	57	13	19	63	53	2	45	51	27	46	6	54
	28	31	56	62	27	59	5	36	35	46	16	49	53
	7	36	32	55	46	21	8	16	22	25	25	16	52
	24	48	12	32	13	8	41	21	12	32	1	15	51
	22	63	48	45	0	55	43	48	41	14	12	46	50
	34	10	10	2	47	62	0	32	28	57	26	44	49
	33	52	58	57	7	12	53	33	11	49	23	27	48
	54	6	39	27	26	41	30	63	58	1	53	21	47
	31	4	21	29	45	22	36	15	30	54	4	40	46
	60	19	53	39	9	56	29	52	42	16	58	24	45
	47	24	22	48	51	37	6	59	27	44	30	18	44
	3	47	30	54	41	40	56	35	63	24	48	48	43
	38	42	8	34	31	29	39	34	31	30	41	25	42
	12	55	42	33	49	49	20	57	47	60	13	23	41
	19	60	5	6	23	27	15	13	26	38	35	31	40
	48	34	47	4	17	63	54	5	57	31	43	54	39
	5	35	37	60	12	10	51	19	50	23	45	62	38
	25	14	40	61	2	4	58	37	61	59	20	17	37
	57	13	44	12	10	26	16	42	7	37	11	38	36
	35	33	63	15	22	60	50	55	32	8	5	26	35
	39	26	62	10	35	44	22	26	10	51	17	9	34
	23	32	50	8	56	34	55	56	19	50	6	10	33
	44	25	61	28	52	1	23	23	2	48	3	12	32
	36	40	3	13	20	25	38	18	4	4	37	41	31
	56	3	29	40	1	9	34	41	25	40	29	50	30
	17	50	35	14	48	51	19	27	43	20	27	47	29
	43	45	2	36	16	13	59	44	40	12	19	58	28
	11	51	9	31	21	52	4	60	39	22	40	28	27
	27	30	4	25	30	35	12	6	62	3	14	29	26
	16	0	14	7	43	39	10	30	3	42	22	33	25
	30	8	11	35	50	42	27	10	14	58	44	11	24
	59	9	51	44	57	61	45	24	59	26	61	59	23
	18	46	33	59	32	3	33	0	23	55	18	36	22
13	44	23	50	37	32	62	43	17	56	21	34	21	
4	27	52	46	5	36	46	29	6	62	28	63	20	
29	39	0	1	59	43	49	38	16	34	7	32	19	
53	58	38	49	58	2	14	39	1	53	62	1	18	
1	5	7	0	40	18	9	47	9	63	15	20	17	
50	12	26	20	61	50	11	62	54	41	52	35	16	
51	22	45	43	3	45	63	2	15	18	59	53	15	
20	61	24	51	62	0	61	54	34	33	50	52	14	
62	38	27	30	19	30	44	46	8	6	33	7	13	
63	17	49	42	29	17	37	61	56	47	36	43	12	
55	43	18	3	44	33	3	20	45	11	9	2	11	
2	16	60	52	4	47	31	7	13	29	57	8	10	
45	29	25	22	24	6	57	40	53	28	63	13	9	
8	59	43	56	15	28	42	25	48	7	10	60	8	
42	54	55	38	14	31	47	53	36	45	60	5	7	
49	53	20	16	18	23	32	22	49	39	49	55	6	
26	37	17	11	54	46	28	58	20	36	39	4	5	
61	23	41	21	34	24	21	50	52	5	24	22	4	
15	49	31	37	8	15	1	11	18	15	47	57	3	
0	7	6	26	6	16	52	4	5	19	0	14	2	
40	2	57	23	38	48	26	17	38	21	2	3	1	
14	18	15	41	25	14	35	51	29	0	55	51	0	

P1 <sub>4</sub>	Permutation stage $\pi_{i2}$												Output
	$\pi_{12}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$	$\pi_{122}$	
Permutation element	47	10	18	49	22	3	45	39	48	56	7	25	63
	30	29	43	14	43	16	57	7	57	62	12	2	62
	3	32	58	1	35	1	7	54	11	5	2	52	61
	60	35	8	39	62	46	8	0	16	57	15	42	60
	18	27	4	5	36	55	40	24	14	60	9	55	59
	50	39	44	48	61	13	32	19	50	3	19	39	58
	62	48	55	16	33	50	20	2	33	45	22	51	57
	45	56	48	38	49	26	59	21	38	49	47	57	56
	54	16	15	10	38	15	1	44	49	7	18	35	55
	0	50	61	46	12	60	41	46	21	63	23	62	54
	26	61	24	45	19	12	58	57	53	10	39	27	53
	38	4	35	0	20	54	24	1	59	31	41	48	52
	32	55	57	26	45	21	3	9	56	44	45	13	51
	63	19	14	56	41	41	17	28	20	29	4	54	50
	40	63	9	3	52	35	46	31	5	11	10	8	49
	2	13	7	42	23	29	43	52	58	30	34	16	48
	53	31	38	12	63	40	50	25	0	50	29	37	47
	35	25	25	31	59	56	12	42	26	22	16	24	46
	51	30	40	50	1	25	44	53	41	0	54	29	45
	11	2	20	17	37	0	11	34	22	51	57	20	44
	44	53	26	27	10	2	21	23	37	16	33	17	43
	56	3	42	29	8	58	53	15	19	24	56	15	42
	25	8	12	37	39	7	30	50	36	21	40	33	41
	14	41	10	62	9	28	49	40	45	15	11	4	40
	59	0	62	15	42	20	14	8	63	40	46	30	39
	31	22	60	40	60	44	5	18	55	41	3	6	38
	13	21	37	60	25	36	42	5	31	53	25	41	37
	55	54	28	33	5	47	13	47	10	48	13	43	36
	24	62	3	53	32	61	51	22	17	13	38	61	35
	39	58	59	28	48	14	34	48	52	25	35	11	34
	46	24	2	35	27	59	60	61	43	46	48	53	33
	33	20	27	8	55	37	6	60	60	18	60	12	32
	48	33	17	21	54	52	2	26	9	39	58	34	31
	5	14	36	57	29	32	9	30	44	36	59	56	30
	10	9	23	19	15	17	10	33	32	19	6	19	29
	21	26	50	52	24	27	61	38	51	34	30	46	28
	9	45	19	24	31	4	39	36	62	17	55	3	27
	61	1	41	4	16	39	4	13	15	27	37	9	26
	43	5	22	44	44	6	28	10	34	47	63	23	25
	27	18	1	11	17	57	26	41	28	14	42	44	24
	22	11	33	18	28	18	31	16	47	59	8	22	23
	23	7	6	55	34	22	47	4	7	2	17	31	22
8	17	16	22	46	23	25	35	18	28	61	60	21	
34	6	32	36	51	30	33	58	39	58	44	38	20	
58	57	47	43	11	45	37	49	27	54	0	32	19	
49	44	53	20	13	31	54	37	4	38	50	18	18	
42	40	54	13	6	51	0	59	2	42	49	14	17	
1	12	5	2	40	53	29	14	25	9	51	10	16	
19	42	34	58	18	9	15	11	23	33	14	63	15	
16	46	46	7	30	24	22	51	46	4	53	40	14	
57	52	52	51	21	43	38	3	29	55	26	58	13	
29	34	30	25	4	10	55	43	42	32	21	28	12	
7	60	21	63	53	34	23	6	12	23	62	47	11	
36	51	13	41	58	63	19	63	13	52	31	21	10	
12	59	0	34	50	49	63	56	54	61	32	59	9	
6	47	11	23	0	42	35	29	61	8	52	45	8	
41	43	45	9	3	8	52	20	24	6	27	26	7	
17	23	56	30	2	62	16	17	3	37	20	36	6	
15	28	39	61	47	48	36	12	40	1	5	0	5	
4	37	49	47	7	5	62	55	1	35	28	50	4	
20	38	29	6	57	19	56	32	30	43	24	1	3	
52	15	63	59	26	33	48	27	8	12	1	5	2	
28	36	31	54	14	11	27	62	35	26	36	49	1	
37	49	51	32	56	38	18	45	6	20	43	7	0	

P1 <sub>5</sub>	Permutation stage $\pi_{i2}$												Output
	$\pi_{12}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$	$\pi_{122}$	
Permutation element	20	49	2	0	32	45	14	28	58	45	21	13	63
	63	39	60	16	2	8	60	62	43	57	19	25	62
	37	40	24	39	15	22	19	37	52	44	60	39	61
	4	11	46	30	50	4	6	55	50	40	2	17	60
	32	0	35	34	31	12	0	27	36	42	26	20	59
	43	6	50	42	20	23	43	24	27	60	32	14	58
	51	4	52	50	12	17	59	51	15	62	44	19	57
	16	41	13	32	43	32	56	61	12	38	24	62	56
	18	7	40	4	16	62	10	2	48	29	0	57	55
	50	43	34	19	55	1	27	17	25	47	49	63	54
	5	25	20	24	25	25	39	19	19	20	54	58	53
	2	36	15	25	24	31	40	59	28	50	18	61	52
	54	9	27	5	36	40	31	7	24	10	4	23	51
	19	52	14	49	60	50	5	54	18	32	45	15	50
	26	32	6	3	17	6	32	43	39	3	61	52	49
	58	35	22	13	10	58	49	16	33	58	5	56	48
	44	61	30	33	30	42	38	56	56	12	16	40	47
	47	15	47	59	35	21	51	0	0	0	14	46	46
	48	2	4	40	7	9	26	39	5	6	22	1	45
	24	3	11	62	37	14	17	38	8	43	40	42	44
	1	5	18	46	21	38	58	30	44	51	31	50	43
	46	42	19	63	38	61	28	20	38	15	27	27	42
	45	54	16	8	44	52	55	13	47	31	41	9	41
	62	21	45	58	47	53	53	36	62	13	48	11	40
	61	24	36	18	22	60	36	15	32	36	33	31	39
	6	30	37	17	59	37	29	4	2	59	23	2	38
	59	62	56	53	53	41	33	31	40	37	51	43	37
	14	44	0	37	39	5	2	1	57	46	63	49	36
	3	29	12	35	54	44	4	14	22	34	1	38	35
	8	46	21	7	57	16	8	47	54	24	52	24	34
	15	16	10	20	9	35	57	8	59	23	7	51	33
	21	58	39	44	58	10	23	12	34	56	13	4	32
	34	60	63	2	3	34	41	60	9	28	15	37	31
	60	48	55	6	52	56	34	29	13	54	34	16	30
	7	38	51	60	8	18	45	63	31	61	9	18	29
	52	37	9	56	11	11	61	52	11	41	8	10	28
	33	17	26	9	42	7	24	57	45	25	53	28	27
	10	50	38	36	29	36	21	25	14	9	43	8	26
	28	34	57	23	23	57	15	21	7	19	3	48	25
	13	10	42	26	62	26	48	42	29	63	6	36	24
9	26	48	15	45	20	52	35	4	21	25	12	23	
11	51	7	11	61	51	16	11	26	27	30	30	22	
36	22	49	61	51	63	11	32	21	2	10	21	21	
30	1	29	38	0	47	1	26	46	11	20	35	20	
22	28	59	22	41	24	18	40	55	5	35	5	19	
17	56	8	29	46	2	50	23	35	4	58	54	18	
23	18	5	43	49	19	63	49	37	18	57	0	17	
29	57	58	41	19	30	3	6	53	53	38	60	16	
38	53	32	55	1	48	9	10	3	33	11	33	15	
12	33	25	12	56	28	42	22	1	48	17	44	14	
55	20	53	48	48	33	47	9	6	52	39	45	13	
56	59	61	45	40	0	35	33	17	55	42	55	12	
53	63	62	51	4	27	13	5	61	26	55	26	11	
41	13	3	1	34	13	46	3	23	49	28	32	10	
39	55	44	14	18	43	25	46	49	30	59	29	9	
27	23	28	47	5	49	62	41	41	8	56	7	8	
25	14	1	52	26	54	22	58	20	17	47	41	7	
49	45	54	31	13	46	37	18	63	35	29	3	6	
35	19	31	28	63	59	7	45	10	16	46	59	5	
42	47	43	54	27	15	44	50	60	7	62	6	4	
57	31	23	27	28	3	54	34	51	39	12	47	3	
31	12	33	21	33	39	12	53	30	22	37	34	2	
40	27	17	10	14	29	20	48	42	1	50	22	1	
0	8	41	57	6	55	30	44	16	14	36	53	0	



P2 <sub>1</sub>	Permutation stage $\pi_{i2}$												Output
	$\pi_{12}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$	$\pi_{122}$	
Permutation element	61	22	37	51	1	55	12	47	33	57	54	39	63
	50	35	9	35	54	28	8	5	24	52	7	61	62
	34	17	21	3	5	22	42	0	31	6	25	10	61
	26	34	1	0	18	51	50	60	15	15	5	49	60
	3	47	27	61	24	50	51	11	59	41	63	52	59
	28	37	31	7	45	14	14	23	23	0	56	30	58
	25	30	58	15	57	39	28	45	45	47	10	46	57
	16	54	35	16	12	4	62	53	12	43	18	29	56
	35	28	23	38	52	36	15	56	60	8	62	11	55
	2	38	34	36	8	10	23	52	35	2	4	16	54
	47	55	43	40	21	45	63	40	22	37	2	23	53
	59	36	29	12	15	8	2	1	53	53	45	0	52
	31	15	46	63	32	42	20	38	47	24	55	6	51
	24	60	55	50	39	47	60	63	7	13	51	22	50
	29	49	60	47	4	30	25	50	37	4	20	55	49
	14	63	6	55	10	62	22	62	6	18	19	20	48
	23	23	4	27	34	27	18	34	32	27	57	62	47
	30	25	49	29	6	38	55	41	46	23	43	31	46
	53	2	63	58	55	24	40	55	39	62	26	1	45
	13	58	33	32	20	34	59	10	4	11	3	3	44
	58	24	47	23	3	60	58	42	56	55	47	48	43
	0	41	8	30	9	43	17	3	27	28	36	53	42
	54	7	56	4	30	59	38	35	43	40	31	12	41
	6	21	59	22	36	57	46	15	16	20	29	38	40
	63	5	17	11	63	15	1	51	40	56	37	58	39
	8	14	32	42	58	3	5	32	38	31	14	28	38
	19	9	48	2	48	11	56	25	19	34	11	24	37
	52	51	16	1	31	53	49	19	3	32	28	8	36
	55	31	20	56	49	25	29	17	2	19	13	9	35
	15	32	51	37	53	58	31	54	51	16	15	33	34
	57	1	12	54	27	0	32	8	18	59	17	36	33
	27	40	28	45	51	44	30	14	29	35	40	34	32
	9	42	30	18	35	35	54	4	61	58	23	37	31
	7	53	13	31	2	5	4	24	41	39	46	50	30
	51	44	2	60	19	37	39	20	63	12	61	14	29
	40	39	24	48	59	13	0	61	34	48	42	5	28
	49	46	15	9	16	61	43	6	57	46	16	7	27
	5	3	40	10	17	40	48	9	52	7	24	40	26
	33	56	62	44	33	48	3	36	48	63	34	47	25
	48	61	3	59	40	41	53	26	30	50	50	63	24
18	19	39	13	0	16	9	57	8	5	58	41	23	
41	6	10	62	13	19	27	46	11	26	44	60	22	
11	52	41	57	43	46	37	29	42	54	52	17	21	
44	57	22	41	41	21	41	39	55	61	59	35	20	
22	0	14	17	37	26	33	48	5	51	0	18	19	
43	4	54	6	26	1	16	43	50	1	6	54	18	
36	29	45	52	60	56	34	49	0	38	53	57	17	
42	27	7	14	28	63	11	22	9	36	27	56	16	
62	11	52	5	14	49	13	16	54	29	32	26	15	
37	33	25	26	22	18	36	30	13	21	49	44	14	
45	59	42	28	46	6	7	28	1	14	21	25	13	
39	43	57	19	62	7	45	33	26	33	60	4	12	
60	18	53	21	44	2	21	12	49	45	22	45	11	
21	12	61	43	50	20	47	31	10	9	9	59	10	
12	48	36	39	25	32	61	59	28	42	33	32	9	
20	8	44	34	38	52	44	44	21	49	8	42	8	
1	20	18	25	29	9	24	18	25	22	1	27	7	
4	26	0	8	7	33	6	7	14	44	30	51	6	
17	62	19	46	42	54	57	58	20	30	38	21	5	
46	13	38	33	61	17	10	13	58	25	35	15	4	
10	50	11	49	23	29	52	27	44	10	48	19	3	
56	45	50	20	47	12	26	21	62	3	39	43	2	
32	16	5	53	56	31	19	2	17	60	41	2	1	
38	10	26	24	11	23	35	37	36	17	12	13	0	

P2 <sub>2</sub>	Permutation stage $\pi_{i2}$												Output
	$\pi_{12}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$	$\pi_{122}$	
Permutation element	4	20	11	47	57	2	11	9	13	25	23	31	63
	22	2	2	24	33	9	50	5	51	53	18	9	62
	35	50	32	7	61	13	0	49	50	21	13	19	61
	63	38	50	33	42	4	13	36	12	52	41	53	60
	34	29	22	13	10	62	1	6	4	33	43	55	59
	48	30	27	11	60	27	22	44	6	4	8	1	58
	28	54	4	16	37	5	42	54	29	27	3	33	57
	59	37	41	19	25	40	55	12	59	14	52	62	56
	2	32	3	59	4	15	48	34	37	55	6	2	55
	20	55	23	2	17	21	4	61	44	2	37	63	54
	23	44	47	39	56	47	45	10	32	39	54	57	53
	51	16	24	28	29	3	15	51	31	47	57	26	52
	31	22	29	9	48	39	41	59	9	42	48	18	51
	3	24	20	29	50	1	53	58	30	7	42	50	50
	36	39	54	44	38	30	19	39	33	3	22	49	49
	43	19	33	63	46	42	49	3	36	35	7	25	48
	60	12	42	37	3	43	56	8	0	61	19	11	47
	39	49	37	12	1	24	54	14	62	56	10	45	46
	32	56	61	45	19	38	29	17	22	37	25	44	45
	1	5	43	30	62	63	21	31	1	22	30	43	44
	55	61	39	40	58	55	25	27	54	17	29	35	43
	49	17	34	38	12	32	9	4	5	43	4	27	42
	50	48	0	8	27	18	27	43	38	44	61	0	41
	9	57	7	32	13	34	18	62	15	57	55	52	40
	14	26	21	51	45	25	40	1	34	6	33	28	39
	16	0	60	4	6	54	60	23	40	9	40	41	38
	6	10	9	35	36	50	52	42	35	60	56	20	37
	15	62	59	25	54	52	23	32	53	23	2	47	36
	10	52	63	10	53	46	36	57	55	50	35	14	35
	42	21	1	26	23	8	44	41	49	24	28	59	34
	5	34	53	20	40	29	37	56	56	18	39	42	33
	54	1	6	54	15	20	20	18	23	36	60	4	32
	40	27	17	27	43	56	46	35	63	8	27	38	31
	18	35	10	34	52	49	51	25	8	40	24	46	30
	45	60	51	21	31	31	61	26	60	10	12	22	29
	33	63	16	41	14	28	16	47	16	51	1	36	28
	62	13	40	14	16	44	7	15	19	45	34	30	27
	11	3	30	48	35	11	26	24	58	41	58	54	26
	8	51	14	52	5	7	5	60	2	58	26	40	25
	17	15	58	56	7	37	47	16	45	48	5	48	24
	12	18	56	53	21	51	63	19	47	30	62	21	23
	58	14	12	5	0	12	24	38	43	15	46	61	22
19	9	45	57	28	53	57	22	27	46	16	6	21	
0	41	35	60	39	19	14	2	28	19	63	23	20	
56	59	46	62	20	10	28	53	46	1	15	3	19	
27	47	31	36	9	59	38	0	7	16	53	7	18	
47	53	8	1	11	26	17	40	61	49	38	56	17	
30	25	49	58	22	48	12	48	11	31	49	17	16	
57	7	57	49	49	45	6	20	42	38	59	8	15	
29	58	28	42	51	35	59	37	26	63	50	51	14	
25	31	5	43	32	57	34	63	41	11	17	24	13	
53	45	36	22	34	60	3	28	20	54	51	58	12	
46	40	26	17	2	23	8	13	14	29	9	37	11	
52	33	38	18	41	36	30	21	24	5	21	5	10	
21	36	15	46	18	0	39	33	18	32	11	16	9	
13	11	62	6	24	33	2	11	48	59	20	34	8	
7	4	25	50	63	22	62	7	39	13	32	12	7	
61	28	52	23	26	41	58	55	10	26	44	39	6	
37	6	13	3	8	17	35	30	3	20	31	13	5	
26	42	19	61	44	61	10	50	57	12	0	60	4	
44	8	48	0	47	14	31	52	52	62	36	32	3	
41	43	18	31	55	58	33	29	17	34	45	10	2	
24	23	55	15	30	16	43	45	21	28	47	29	1	
38	46	44	55	59	6	32	46	25	0	14	15	0	

P2 <sub>3</sub>	Permutation stage $\pi_{i2}$												Output
	$\pi_{i2}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$	$\pi_{122}$	
Permutation element	59	63	29	9	39	26	52	42	57	62	54	20	63
	62	13	27	44	25	51	22	0	31	47	48	44	62
	9	31	28	21	59	53	4	24	54	55	13	34	61
	29	32	40	14	10	10	3	16	59	32	39	1	60
	10	7	34	20	47	56	50	33	25	13	30	10	59
	31	28	44	29	49	63	23	63	0	6	5	14	58
	28	19	9	41	19	5	58	18	4	52	45	9	57
	35	42	55	43	15	62	16	1	20	11	36	41	56
	52	50	46	45	1	39	15	4	14	59	34	0	55
	40	27	23	24	51	59	12	17	46	34	58	30	54
	30	12	5	47	61	35	46	14	10	58	47	5	53
	57	35	62	28	28	8	0	41	34	15	3	36	52
	38	60	39	56	48	27	25	15	17	53	24	56	51
	54	23	45	51	38	6	56	34	60	5	31	43	50
	7	54	8	12	26	20	48	6	15	51	60	42	49
	63	2	24	3	40	13	5	37	44	21	0	27	48
	6	38	32	4	57	33	62	50	29	41	21	35	47
	20	58	37	36	7	58	26	22	2	29	35	18	46
	42	44	58	2	3	12	38	62	16	49	1	54	45
	55	56	31	22	21	0	17	32	13	9	15	4	44
	0	30	18	26	11	3	13	7	38	45	38	22	43
	44	6	53	39	41	34	9	47	7	16	22	24	42
	51	40	26	16	22	44	45	58	50	42	19	59	41
	48	4	11	0	16	22	55	8	35	38	18	31	40
	50	11	20	32	50	25	28	38	51	4	17	49	39
	22	61	51	11	9	36	51	35	47	37	50	38	38
	27	48	15	10	13	24	20	36	8	24	7	33	37
	16	36	54	40	60	43	43	2	41	22	42	32	36
	61	21	49	1	17	18	33	46	42	43	26	51	35
	56	59	2	5	62	2	14	19	61	1	46	13	34
	43	41	52	27	18	28	39	39	1	23	14	50	33
	23	22	36	52	20	23	63	5	23	14	41	17	32
	13	8	6	37	27	38	19	30	5	35	44	37	31
	3	34	22	6	54	61	1	55	27	44	32	52	30
	18	49	17	48	52	47	49	26	30	33	55	21	29
	5	29	1	62	34	14	35	9	21	50	63	3	28
	49	26	42	33	23	31	42	60	56	25	52	48	27
	33	46	19	18	35	50	31	28	3	56	6	45	26
	21	9	30	57	42	40	2	31	12	12	10	23	25
	2	14	50	53	63	30	40	57	43	40	56	11	24
	19	18	38	13	2	17	41	20	11	48	53	60	23
36	5	25	63	30	9	21	44	62	8	43	12	22	
45	16	3	8	36	16	10	51	40	61	23	53	21	
39	47	4	25	0	48	18	3	19	36	40	39	20	
8	45	60	17	44	46	27	52	26	46	59	15	19	
32	43	7	31	5	1	36	54	63	18	8	55	18	
12	15	14	54	31	52	60	25	45	63	49	61	17	
11	53	10	34	32	21	54	40	48	26	20	7	16	
34	62	0	58	55	49	29	12	58	19	61	2	15	
53	39	33	35	24	37	7	23	36	31	9	19	14	
58	1	47	7	4	11	57	13	39	0	25	8	13	
26	24	13	42	29	55	34	48	18	39	37	25	12	
60	17	56	60	33	54	6	53	49	2	28	47	11	
15	37	21	59	46	4	44	56	24	54	4	6	10	
1	33	16	55	12	42	8	43	53	57	11	40	9	
24	0	59	61	6	15	11	10	33	30	51	16	8	
46	10	63	30	8	19	24	61	37	27	57	29	7	
4	52	12	50	53	32	47	21	9	17	12	63	6	
47	51	48	46	56	57	59	11	55	7	33	46	5	
25	3	61	49	14	7	30	27	28	10	2	58	4	
17	25	41	23	43	41	32	29	6	3	16	28	3	
14	20	35	15	45	60	37	49	22	60	62	26	2	
37	55	57	38	58	29	61	59	52	28	27	57	1	
41	57	43	19	37	45	53	45	32	20	29	62	0	

P2 <sub>4</sub>	Permutation stage $\pi_{12}$												Output
	$\pi_{1/2}$	$\pi_{2/2}$	$\pi_{3/2}$	$\pi_{4/2}$	$\pi_{5/2}$	$\pi_{6/2}$	$\pi_{7/2}$	$\pi_{8/2}$	$\pi_{9/2}$	$\pi_{10/2}$	$\pi_{11/2}$	$\pi_{12/2}$	
Permutation element	9	6	58	25	2	53	44	44	41	51	60	45	63
	15	29	44	31	34	56	51	40	52	26	5	2	62
	12	53	39	9	24	48	18	43	50	37	33	24	61
	50	50	8	45	61	19	20	14	36	53	7	34	60
	18	13	12	54	30	24	26	45	39	23	48	22	59
	42	60	45	33	35	49	15	60	8	46	12	56	58
	57	31	30	40	49	16	14	58	53	58	17	48	57
	10	8	49	52	54	27	10	48	12	49	20	39	56
	29	16	19	29	18	23	31	55	42	60	44	1	55
	0	61	29	23	13	42	40	21	26	32	32	54	54
	60	36	62	35	41	25	63	9	15	47	41	26	53
	45	55	50	8	27	35	56	2	45	8	0	61	52
	38	20	54	42	9	43	54	37	14	28	30	7	51
	54	49	52	44	47	29	45	54	62	52	1	62	50
	25	42	40	36	55	0	32	22	46	17	38	31	49
	59	40	14	63	12	14	12	19	47	5	4	6	48
	31	17	32	18	3	41	8	4	4	61	14	57	47
	33	48	43	11	28	1	43	24	56	9	25	60	46
	56	18	35	0	5	63	52	38	9	38	50	49	45
	55	5	61	22	36	13	23	33	44	42	57	27	44
	58	33	27	56	50	21	7	51	25	16	10	15	43
	19	45	25	27	15	37	48	18	31	56	3	14	42
	44	51	34	59	10	4	22	53	63	50	61	38	41
	13	2	22	51	52	17	19	0	7	0	26	3	40
	41	63	23	1	44	30	16	8	16	33	59	32	39
	4	37	16	24	7	3	28	62	1	7	56	20	38
	23	1	60	7	0	38	47	26	48	24	21	30	37
	51	54	24	38	60	22	62	3	58	4	36	58	36
	34	26	21	12	46	51	0	35	55	29	53	23	35
	28	46	11	13	63	28	13	49	33	43	46	43	34
	5	24	28	41	21	7	35	52	54	35	55	0	33
	16	28	0	14	32	47	46	50	38	41	34	13	32
	11	0	9	4	57	6	55	56	2	3	8	44	31
	35	62	5	30	56	39	59	36	30	1	62	47	30
	20	47	26	10	14	8	58	16	18	44	24	40	29
	21	30	10	57	48	50	38	12	23	14	31	41	28
	32	44	33	6	31	2	50	61	5	34	13	46	27
	17	11	63	46	33	5	57	25	19	13	40	59	26
	2	59	36	32	58	10	3	31	13	25	11	16	25
	22	15	17	16	4	57	11	29	0	40	29	12	24
	48	39	13	50	42	52	42	17	51	18	37	18	23
	61	35	41	43	11	54	27	57	6	12	47	8	22
	6	9	31	47	19	45	41	63	61	19	35	36	21
	62	22	56	19	39	46	39	15	40	36	54	11	20
	39	4	53	49	17	11	9	47	27	55	15	51	19
	14	14	15	28	22	60	33	10	28	21	18	25	18
	43	10	18	60	25	36	1	46	17	15	51	9	17
	1	32	57	39	20	26	5	1	57	6	16	10	16
24	23	46	53	51	55	4	20	29	22	39	19	15	
52	41	20	26	53	62	60	27	43	54	27	5	14	
40	27	38	37	45	34	21	32	24	48	43	63	13	
7	43	59	3	29	33	30	23	32	59	42	35	12	
8	25	47	21	62	32	34	42	37	11	22	50	11	
63	7	48	55	1	15	29	30	3	27	9	4	10	
36	38	37	5	23	61	24	39	34	10	19	53	9	
47	12	1	2	37	18	6	11	35	63	6	52	8	
3	52	51	61	38	58	37	6	59	20	52	21	7	
46	56	3	62	40	31	25	34	49	62	45	33	6	
27	3	2	34	16	20	53	5	21	31	49	55	5	
53	34	55	20	26	59	17	41	20	2	28	29	4	
30	19	6	48	6	44	49	13	60	30	63	28	3	
37	58	42	15	43	40	2	7	11	57	2	37	2	
26	21	7	58	8	9	36	59	22	45	23	42	1	
49	57	4	17	59	12	61	28	10	39	58	17	0	

P2 <sub>5</sub>	Permutation stage $\pi_{i2}$												Output
	$\pi_{12}$	$\pi_{22}$	$\pi_{32}$	$\pi_{42}$	$\pi_{52}$	$\pi_{62}$	$\pi_{72}$	$\pi_{82}$	$\pi_{92}$	$\pi_{102}$	$\pi_{112}$	$\pi_{122}$	
Permutation element	12	13	21	8	27	16	62	55	58	56	60	16	63
	41	20	18	23	52	57	40	38	59	62	15	1	62
	51	16	48	52	36	17	2	54	18	49	47	25	61
	49	51	29	56	61	50	63	22	17	39	61	9	60
	20	47	23	53	33	19	26	57	21	12	50	45	59
	31	3	30	62	28	37	24	13	37	7	58	41	58
	30	1	24	15	60	11	51	43	39	23	18	42	57
	10	29	57	32	23	0	22	52	53	55	16	2	56
	61	30	20	7	29	43	52	5	23	42	40	58	55
	59	26	10	3	44	49	11	34	26	4	20	43	54
	35	43	53	25	42	58	57	32	5	11	37	35	53
	19	37	61	58	48	32	46	60	2	33	23	15	52
	14	24	2	9	1	28	21	44	57	52	5	31	51
	36	50	34	49	4	39	48	3	62	17	26	13	50
	13	23	38	36	56	29	53	28	16	13	3	33	49
	57	45	35	2	41	25	34	26	40	57	32	6	48
	5	34	15	42	37	56	59	56	0	3	49	47	47
	28	0	62	31	31	21	7	25	3	16	45	52	46
	37	22	39	21	50	27	0	17	44	50	9	32	45
	34	35	59	57	40	31	37	49	10	44	36	28	44
	8	52	37	45	62	40	43	62	48	30	31	48	43
	1	7	43	38	10	15	13	8	22	34	38	50	42
	47	58	47	50	16	47	19	53	8	6	39	19	41
	43	28	26	10	32	26	44	63	13	10	10	53	40
	21	55	56	46	43	34	36	18	33	21	28	59	39
	26	59	19	26	34	36	8	11	1	40	46	30	38
	16	56	8	59	3	48	18	41	47	59	59	55	37
	18	62	4	40	19	44	17	27	11	38	51	57	36
	24	5	22	19	5	45	23	61	6	9	29	63	35
	60	49	46	47	15	38	30	19	36	8	57	11	34
	62	4	51	34	21	9	5	16	56	46	62	27	33
	44	8	41	48	7	3	42	14	45	29	14	54	32
	22	11	32	60	59	54	20	12	34	14	24	8	31
	39	31	52	54	0	18	27	50	19	15	52	23	30
	42	41	55	41	13	14	3	37	28	45	25	5	29
	0	38	1	20	57	46	58	29	24	51	4	34	28
	50	27	49	30	24	63	15	59	38	18	22	12	27
	23	40	60	11	47	4	33	33	46	25	21	37	26
	32	33	13	33	58	61	35	30	60	36	42	51	25
	63	17	6	27	2	53	47	9	55	19	6	20	24
	11	54	11	35	49	52	54	36	14	22	33	44	23
	29	60	54	14	11	12	4	23	61	27	53	61	22
	4	57	63	22	6	55	49	48	27	43	7	29	21
	27	2	5	17	38	5	16	0	7	48	13	38	20
	58	21	50	5	63	13	38	47	31	32	34	39	19
	6	32	25	12	26	30	32	21	29	31	0	24	18
	52	44	0	55	22	62	56	51	30	60	43	62	17
	53	25	58	63	8	60	12	10	52	28	30	40	16
	55	42	36	0	45	22	29	42	15	61	17	22	15
	33	19	42	61	20	23	50	58	12	47	11	3	14
	46	48	7	18	17	33	60	7	32	1	48	26	13
	7	53	31	4	30	42	25	35	25	26	2	36	12
	56	10	3	51	46	35	61	15	4	24	35	4	11
	17	9	16	39	55	20	6	40	50	0	55	46	10
	38	15	44	6	9	24	31	31	54	41	1	14	9
	2	12	17	1	12	7	41	24	49	58	27	49	8
	15	6	9	16	54	41	1	45	41	5	19	21	7
	48	18	45	24	18	59	28	20	51	53	12	56	6
	9	63	28	29	14	10	10	46	35	54	41	10	5
	45	36	27	44	25	51	55	1	20	37	56	0	4
	3	61	14	28	53	8	14	6	43	20	54	18	3
	54	46	12	43	39	2	45	39	9	2	8	7	2
	25	39	40	37	35	6	39	4	42	63	63	60	1
40	14	33	13	51	1	9	2	63	35	44	17	0	

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