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International Telecommunication Union
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Recommendation

ITU-T G.709.5 (03/2024)

SERIES G: Transmission systems and media, digital systems and networks

Digital terminal equipments – General

Flexible OTN short-reach interfaces

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Recommendation ITU-T G.709.5

Flexible OTN short-reach interfaces

Summary

Recommendation ITU-T G.709.5 specifies 100G, 200G, 400G and 800G flexible optical transport network (FlexO) short-reach interfaces. This Recommendation specifies the structure using forward error correction (FEC) code with a coding gain suitable for short-reach applications, and references common elements from Recommendation ITU-T G.709.1.

History *

Edition	Recommendation	Approval	Study Group	Unique ID
1.0	ITU-T G.709.5	2024-03-08	15	11.1002/1000/15794

Keywords

Digital client signal, FlexO, FlexO-x-RS, RS, short-reach.

* To access the Recommendation, type the URL https://handle.itu.int/ in the address field of your web browser, followed by the Recommendation's unique ID.

FOREWORD

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Recommendation ITU-T G.709.5

Flexible OTN short-reach interfaces

1 Scope

Recommendation ITU-T G.709.5 specifies a set of interoperable flexible optical transport network (FlexO) short-reach interfaces. The rates in scope for FlexO-x-<int> are 100G, 200G, 400G and 800G (x=1, 2, 4 and 8). This Recommendation specifies the structure using forward error correction (FEC) code with a coding gain suitable for short-reach applications, and references common elements from [ITU-T G.709.1].

The types of FlexO short-reach interfaces that can serve as FlexO-x-RS-m interface group members are covered by application codes which are at the time of publication: 4I1-9D1F, 4L1-9C1F, C4S1-9D1F, 4L1-9D1F, C4S1-4D1F, 8R1-4D1F, 4I1-4D1F and 8I1-4D1F. These application codes are presented in [ITU-T G.695] and [ITU-T G.959.1].

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T G.695] Recommendation ITU-T G.695 (2018), *Optical interfaces for coarse wavelength division multiplexing applications*.

[ITU-T G.709] Recommendation ITU-T G.709/Y.1331 (2020), *Interfaces for the optical transport network*.

[ITU-T G.709.1] Recommendation ITU-T G.709.1 (2024), *Flexible OTN common elements*.

[ITU-T G.798] Recommendation ITU-T G.798 (2023), *Characteristics of optical transport network hierarchy equipment functional blocks*.

[ITU-T G.959.1] Recommendation ITU-T G.959.1 (2024*), Optical transport network physical layer interfaces*.

[IEEE 802.3] IEEE Std. 802.3-2022, *IEEE Standard for Ethernet.*

[IEEE 802.3df] IEEE Std. 802.3df-2024, *IEEE Standard for Ethernet Amendment 9: Media Access Control Parameters for 800 Gb/s and Physical Layers and Management Parameters for 400 Gb/s and 800 Gb/s Operation*.

3 Definitions

3.1 Terms defined elsewhere

This Recommendation uses the following terms defined elsewhere:

3.1.1 Terms defined in [ITU-T G.709]

– completely standardized optical transport unit order Cn (OTUCn)

– optical transport network (OTN)

– optical tributary signal (OTSi)

– optical tributary signal assembly (OTSiA)

3.1.2 Terms defined in [ITU-T G.709.1]

– FlexO
– FlexO-n
– FlexO-x
– FlexO-x-<int>
– FlexO-x-<int> interface
– FlexO-x-<int>-m interface group
– FOICx.k-<int>

3.2 Terms defined in this Recommendation

This Recommendation defines the following terms:

None.

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

AMi	Alignment Marker of index i
AM	Alignment Mechanism
BOH	Basic Overhead Field
CAUI	(Chip to) 100 Gb/s Attachment Unit Interface
CM	Common Marker
EOH	Extended Overhead Field
FEC	Forward Error Correction
FlexO	Flexible Optical Transport Network
GID	Group Identification
LSB	Least Significant Bit
MSB	Most Significant Bit
OH	Overhead
OTL	Optical Transport Lane
OTN	Optical Transport Network
OTSi	Optical Tributary Signal
OTU	Optical Transport Unit
OTUCn	OTU order Cn
PCS	Physical Coding Sublayer
RS	Reed-Solomon
UM	Unique Marker
UP	Unique Pad

5 Conventions

This Recommendation uses the following conventions:

Names of information structures and interfaces:

The terms FlexO-n, FlexO-x, FlexO-x-<int>, FlexO-x-<int>-m, and FOICx.k-<int> are used to refer to FlexO information structures and interfaces that are optimized for the optical transport network (OTN) bit rates.

n: The index "n" is used to represent the number of FlexO instances that are in a FlexO group.

x: The index "x" is used to represent the bit rate of the FlexO interface, in 100G increments. For example, x=1 for 100G, x=2 for 200G, x=4 for 400G, etc.

m: The index "m" is used to represent the number of interfaces in a FlexO group. m is also used to represent the number of bits in a block of data / stuff in client mappings.

k: The index "k" is used to represent the number of lanes on an FOICx.k-<int> interface.

<int>: The <int> placeholder is used by this Recommendation as RS to name the short-reach interface which includes Reed-Solomon (RS) FEC.

The term "logical lanes" is equivalent to the term physical coding sublayer "PCS lanes" for Ethernet BASE-R interfaces. It is used to identify the internal lanes over which a FlexO-x-RS signal is distributed. One or more "logical lanes" can be multiplexed and carried on a physical lane at an OTSi interface.

Transmission order: The order of transmission of information in all the diagrams in this Recommendation is first from left to right and then from top to bottom. Within each byte the most significant bit (MSB) is transmitted first. The most significant bit (bit 1) is illustrated on the left side of all diagrams.

Value of reserved bit(s): The value of an overhead (OH) bit, which is reserved for future international standardization, shall be set to "0".

Value of non-sourced bit(s): Unless stated otherwise, any non-sourced bits shall be set to "0".

6 Introduction and applications

The FlexO short-reach interface groups specified in this Recommendation provide an interoperable interface reusing Ethernet client modules. The FlexO interfaces only support OTUCn clients.

Refer to clause 6.1 of [ITU-T G.709.1] and Appendix I of [ITU-T G.709.1] for short-reach applications.

7 Structure and processes

This clause introduces the FlexO-x-RS-m interface group's basic signal structure, processes and information flow.

7.1 Basic signal structure

The information structure for FlexO-x-RS groups is represented by information containment relationships and flows. The principal information containment relationship is described in Figure 7-1. The higher layers of the containment relationship are shown in Figure 7-1 of [ITU-T G.709.1].

The n FlexO instances from the FlexO-n signal are mapped into one FlexO-x-RS-m signal, consisting of $m = \lceil n/x \rceil$ FlexO-x-RS interfaces. Each FlexO-x-RS interface contains one padded and scrambled FlexO-x signal consisting of "x" interleaved FlexO signals, plus RS FEC parity.

Each FlexO-x-RS information structure is split into k FOICx.k-RS lanes. Depending on the pluggable optical module, each electrical lane signal may be modulated onto one OTSi and the set of k OTSi is transported as an OTSiG via one media element as illustrated in Figure 7-1 below.

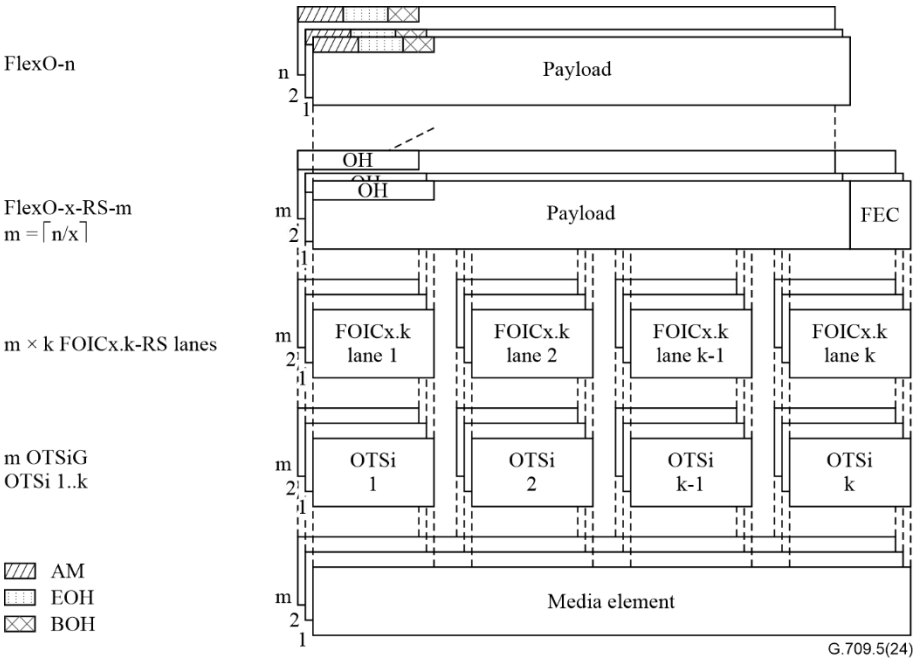

Figure 7-1 – FlexO-x-RS-m interface group principal information containment relationship

7.2 Processing and information flow

Functions, processes, and information flows are more formally specified in [ITU-T G.798].

8 FlexO frame

Refer to clause 8 of [ITU-T G.709.1].

The short-reach interfaces in this Recommendation use z=10 interleaving granularity.

9 Overhead

Refer to clause 9.1 of [ITU-T G.709.1] for a general description of the alignment mechanism (AM) overhead and to the clauses below for descriptions of the FlexO-x-RS alignment markers.

Refer to clauses 9.2 and 9.3 of [ITU-T G.709.1] for the basic overhead field (BOH) and extended overhead field (EOH) definitions.

9.1 Alignment markers

Lane alignment markers in the AM field are used for lane delineation, lane deskewing and lane ordering.

Four 120-bit lane alignment markers fit in the AM field of a FlexO frame.

A lane alignment marker, as shown in Figure 9-1, consists of a common portion across all lanes, a unique portion per lane and some pad bits.

– CMx = 8-bit common marker field (common across lanes) – used for aligning lanes;

– UMx = 8-bit unique marker field – used for identifying lanes;

– UPx = 8-bit unique pad field – used for providing a DC balance when multiplexing lanes.

NOTE – Alignment marker area length specified by clause 91 of [IEEE 802.3] for 100 Gbit/s Ethernet interfaces, is 1 285-bit per alignment marker FEC frame period (every 4 096 FEC codewords). It consists of 20 alignment marker blocks of 64-bit, plus 5-bit extra padding required for 257b block alignment.

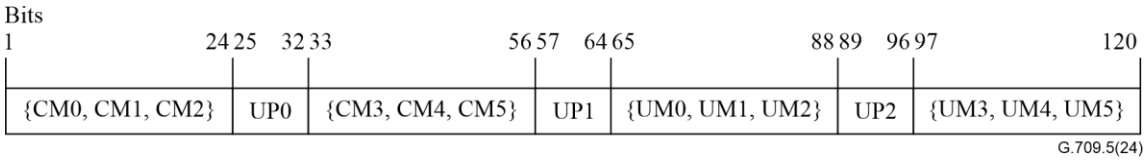

Figure 9-1 – FlexO-x-RS lane alignment marker format

9.2 FlexO-1-RS alignment markers

The FlexO-1-RS signal supports the distribution into four logical lanes, numbered 0, 1, 2 and 3. Each lane carries a 120-bit lane alignment marker (am_i, i = 0, 1, 2, 3) as specified in Table 9-1. Rows of Table 9-1 give the values of the alignment marker of index i (am_i) transmitted over logical lane i.

Table 9-1 – FlexO-1-RS alignment marker encodings

Logical lane	Encoding														
	CM_0	CM_1	CM_2	UP_0	CM_3	CM_4	CM_5	UP_1	UM_0	UM_1	UM_2	UP_2	UM_3	UM_4	UM_5
0	59	52	64	6D	A6	AD	9B	9B	80	8E	CF	64	7F	71	30
1				20				E6	5A	7B	7E	19	A5	84	81
2				62				7F	7C	CF	6A	80	83	30	95
3				5A				21	61	01	0B	DE	9E	FE	F4
NOTE – The value in each byte of this table is in MSB-first transmission order. Note that this per-byte bit ordering is the reverse of the alignment marker values found in [IEEE 802.3], which uses a least significant bit (LSB)-first bit transmission format.															

The 480-bit FlexO-1 AM field contains 10-bit interleaved parts of am_0, am_1, am_2 and am_3 in repeating order, as illustrated in Figure 9-2.

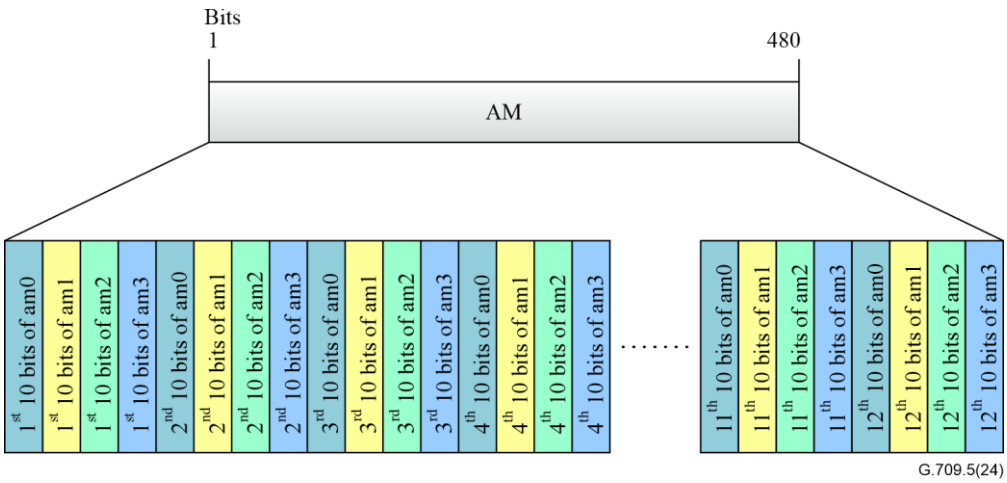

Figure 9-2 – FlexO-1-RS AM field with four interleaved lane alignment markers

9.3 FlexO-2-RS alignment markers

The FlexO-2-RS signal supports the distribution into eight logical lanes, numbered 0, 1, 2 to 7. Each lane carries a 120-bit lane alignment marker (am_i, i = 0, 1, 2 to 7) as specified in Table 9-2. Rows of Table 9-2 give the values of am_i transmitted over logical lane i.

Table 9-2 – FlexO-2-RS alignment marker encodings

Logical lane	Encoding														
	CM0	**CM1**	**CM2**	**UP0**	**CM3**	**CM4**	**CM5**	**UP1**	**UM0**	**UM1**	**UM2**	**UP2**	**UM3**	**UM4**	**UM5**
0	59	52	64	A0	A6	AD	9B	6B	CD	03	31	94	32	FC	CE
1				20				E6	5A	7B	7E	19	A5	84	81
2				62				7F	7C	CF	6A	80	83	30	95
3				5A				21	61	01	0B	DE	9E	FE	F4
4				87				98	54	8A	4F	67	AB	75	B0
5				4F				72	48	F2	8B	8D	B7	0D	74
6				BC				77	42	39	85	88	BD	C6	7A
7				44				4C	6B	6E	DA	B3	94	91	25
NOTE – The value in each byte of this table is in MSB-first transmission order. Note that this per-byte bit ordering is the reverse of the alignment marker values found in [IEEE 802.3], which uses an LSB-first bit transmission format.															

The 960-bit FlexO-2 AM field contains 10-bit interleaved parts of am_0, am_1, am_2, am_3, am_4, am_5, am_6 and am_7 as illustrated in Figure 9-3. Note that for even numbered interleaved sequences (i.e., the 2nd 10 bits sequence, the 4th … the 12th 10 bits sequence) the interleaving of lane alignment markers is odd/even (i.e., am_1, am_0, am_3, am_2, am_5, am_4, am_7, am_6).

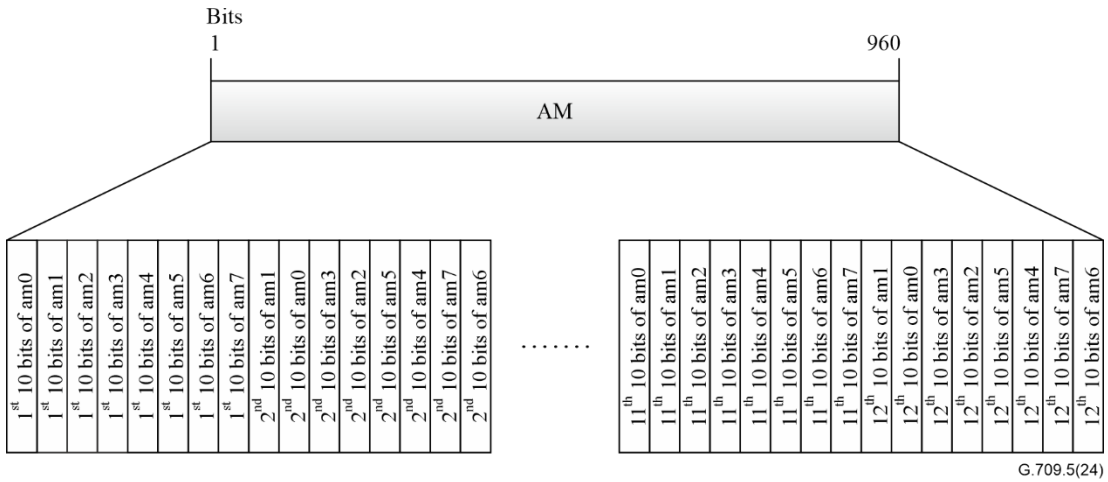

Figure 9-3 – FlexO-2-RS AM field with eight interleaved lane alignment markers

9.4 FlexO-4-RS alignment markers

The FlexO-4-RS signal supports the distribution into sixteen logical lanes, numbered 0, 1, 2 to 15. Each lane carries a 120-bit lane alignment marker (am_i, i = 0, 1, 2 to 15) as specified in Table 9-3. Rows of Table 9-3 give the values of am_i transmitted over logical lane i.

Table 9-3 – FlexO-4-RS alignment marker encodings

Logical lane	Encoding														
	CM0	CM1	CM2	UP0	CM3	CM4	CM5	UP1	UM0	UM1	UM2	UP2	UM3	UM4	UM5
0	59	52	64	6D	A6	AD	9B	9B	80	8E	CF	64	7F	71	30
1				20				E6	5A	7B	7E	19	A5	84	81
2				62				7F	7C	CF	6A	80	83	30	95
3				5A				21	61	01	0B	DE	9E	FE	F4
4				87				98	54	8A	4F	67	AB	75	B0
5				4F				72	48	F2	8B	8D	B7	0D	74
6				BC				77	42	39	85	88	BD	C6	7A
7				44				4C	6B	6E	DA	B3	94	91	25
8				06				F9	87	CE	AE	06	78	31	51
9				D6				45	8E	23	3C	BA	71	DC	C3
10				5F				20	A9	D7	1B	DF	56	28	E4
11				36				8E	44	66	1C	71	BB	99	E3
12				18				DA	45	6F	A9	25	BA	90	56
13				28				33	8C	E9	C3	CC	73	16	3C
14				0B				8D	53	DF	65	72	AC	20	9A
15				2D				6A	65	5D	9E	95	9A	A2	61

NOTE – The value in each byte of this table is in MSB-first transmission order. Note that this per-byte bit ordering is the reverse of the alignment marker values found in [IEEE 802.3], which uses an LSB-first bit transmission format.

The 1 920-bit FlexO-4 AM field contains 10-bit interleaved parts of am_0, am_1, am_2, am_3, am_4, am_5, am_6, am_7, am_8, am_9, am_{10}, am_{11}, am_{12}, am_{13}, am_{14} and am_{15} as illustrated in Figure 9-4. Note that for even numbered interleaved sequences (i.e., the 2nd 10 bits sequence, the 4th … the 12th 10 bits sequence) the interleaving of lane alignment markers is odd/even (i.e., am_1, am_0, am_3, am_2, am_5, am_4, am_7, am_6, am_9, am_8, am_{11}, am_{10}, am_{13}, am_{12}, am_{15}, am_{14}).

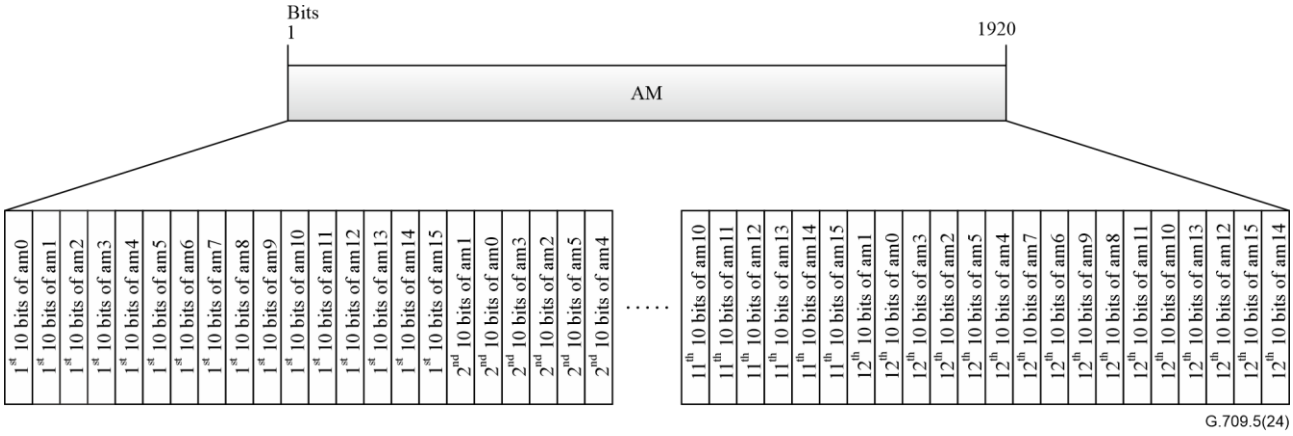

Figure 9-4 – FlexO-4-RS AM field with sixteen interleaved lane alignment markers

9.5 FlexO-8-RS alignment markers

The FlexO-8-RS signal supports distribution into thirty-two logical lanes. Each lane carries a 120-bit lane alignment marker (am_i, i = 0 to 32) as specified in Table 9-4. Rows of Table 9-4 give the values of am_i transmitted over logical lane i.

Table 9-4 – FlexO-8-RS alignment marker encodings

Logical lane	Encoding														
	CM_0	CM_1	CM_2	UP_0	CM_3	CM_4	CM_5	UP_1	UM_0	UM_1	UM_2	UP_2	UM_3	UM_4	UM_5
0	59	52	64	6D	A6	AD	9B	9B	7F	8E	CF	64	80	71	30
1				20				E6	A5	7B	7E	19	5A	84	81
2				62				7F	83	CF	6A	80	7C	30	95
3				5A				21	9E	01	0B	DE	61	FE	F4
4				87				98	AB	8A	4F	67	54	75	B0
5				4F				72	B7	F2	8B	8D	48	0D	74
6				BC				77	BD	39	85	88	42	C6	7A
7				44				4C	94	6E	DA	B3	6B	91	25
8				06				F9	78	CE	AE	06	87	31	51
9				D6				45	71	23	3C	BA	8E	DC	C3
10				5F				20	56	D7	1B	DF	A9	28	E4
11				36				8E	BB	66	1C	71	44	99	E3
12				18				DA	BA	6F	A9	25	45	90	56
13				28				33	73	E9	C3	CC	8C	16	3C
14				0B				8D	AC	DF	65	72	53	20	9A
15				2D				6A	9A	5D	9E	95	65	A2	61
16				6D				9B	80	71	30	64	7F	8E	CF
17				20				E6	5A	84	81	19	A5	7B	7E
18				62				7F	7C	30	95	80	83	CF	6A
19				5A				21	61	FE	F4	DE	9E	01	0B
20				87				98	54	75	B0	67	AB	8A	4F
21				4F				72	48	0D	74	8D	B7	F2	8B
22				BC				77	42	C6	7A	88	BD	39	85
23				44				4C	6B	91	25	B3	94	6E	DA
24				06				F9	87	31	51	06	78	CE	AE
25				D6				45	8E	DC	C3	BA	71	23	3C
26				5F				20	A9	28	E4	DF	56	D7	1B
27				36				8E	44	99	E3	71	BB	66	1C
28				18				DA	45	90	56	25	BA	6F	A9
29				28				33	8C	16	3C	CC	73	E9	C3
30				0B				8D	53	20	9A	72	AC	DF	65
31				2D				6A	65	A2	61	95	9A	5D	9E

NOTE – The value in each byte of this table is in MSB-first transmission order. Note that this per-byte bit ordering is the reverse of the alignment marker values found in [IEEE 802.3df], which uses an LSB-first bit transmission format.

The 3 840-bit FlexO-8 AM field is carried in two separate 1 920-bit AM fields, one in 400G flow #0 and one in 400G flow #1 (see Figure 14-4). The 400G flow #0 AM field contains 10-bit interleaved parts of am_0 through am_{15} and the 400G flow #1 AM field contains 10-bit interleaved parts of am_{16} through am_{31} as illustrated in Figure 9-5. Note that for even numbered interleaved sequences (e.g., the 2nd 10 bits sequence, the 4th … the 12th 10 bits sequence) the interleaving of lane alignment markers is odd/even (e.g., am_1, am_0, am_3, am_2, am_5, am_4, … am_{27}, am_{26}, am_{29}, am_{28}, am_{31}, am_{30}).

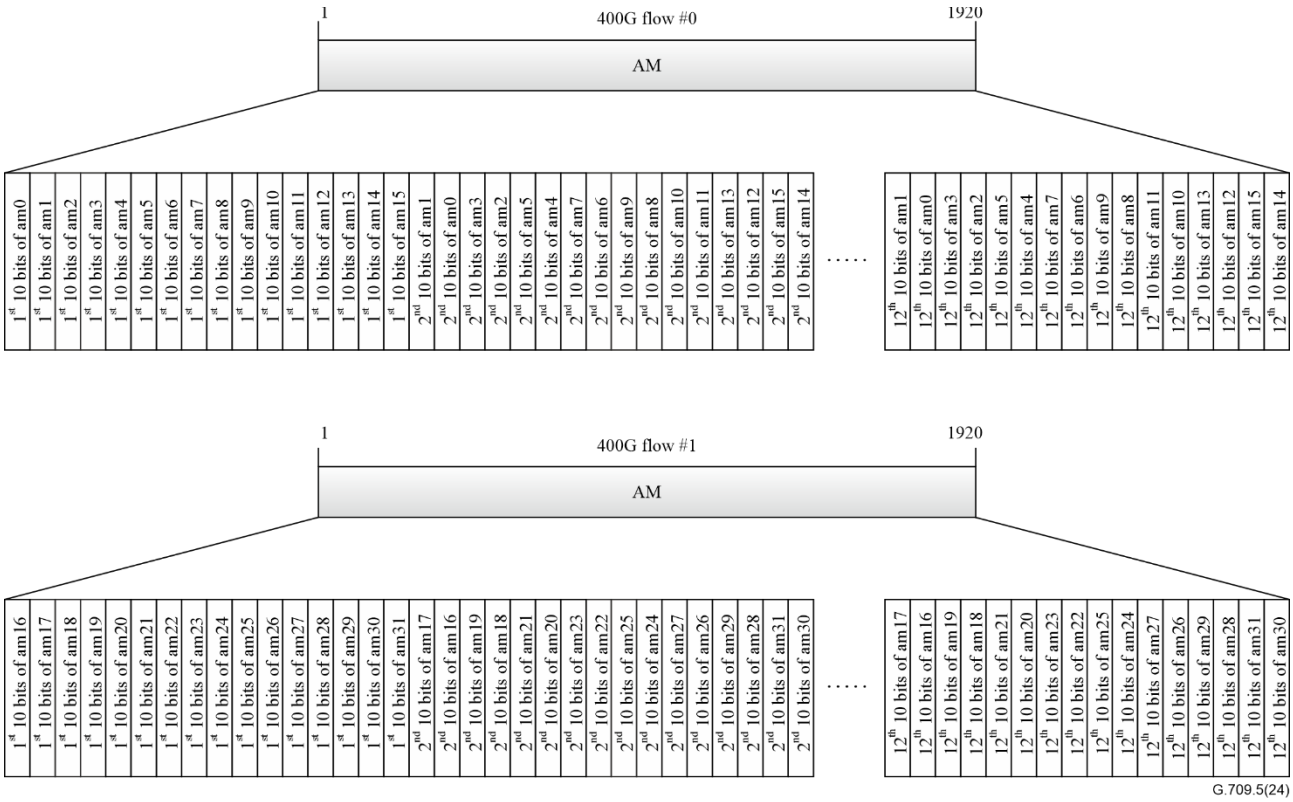

Figure 9-5 – FlexO-8-RS AM field with thirty-two interleaved lane alignment markers

10 FlexO mapping procedures

Refer to clause 10 of [ITU-T G.709.1].

Deskewing in the sink process is performed between OTUC instances within the OTUCn as specified in [ITU-T G.709.1] clause 10.4.

The skew requirements are intended to account for variations due to the digital mapping, and cable lengths related to the delay differences for relevant applications as defined by [ITU-T G.695] and [ITU-T G.959.1]. The skew tolerance requirement over short-reach FlexO interface groups is 300 ns.

11 100G FlexO-1-RS interface

11.1 Frame structure

The 100G FlexO-1-RS frame structure is shown in Figure 11-1 and consists of 128 rows by 5 440 1-bit columns. It contains a FlexO frame structure in columns 1 to 5 140 and a forward error correction (FEC) parity area in columns 5 141 to 5 440 in every row. FlexO-1-RS interfaces use alignment markers as described in clause 9.

Each row constitutes a 5 440-bit FEC codeword, with the last 300 bits used for the FEC parity bits. This results in a bit-oriented structure. The MSB in each FEC codeword is column 1, the LSB is column 5 440.

NOTE – The 100G FlexO-1-RS frame structure is derived from 100 Gbit/s Ethernet clause 91 [IEEE 802.3] FEC alignment and lane architecture, without any 66b alignment or 256b/257b transcoding functions.

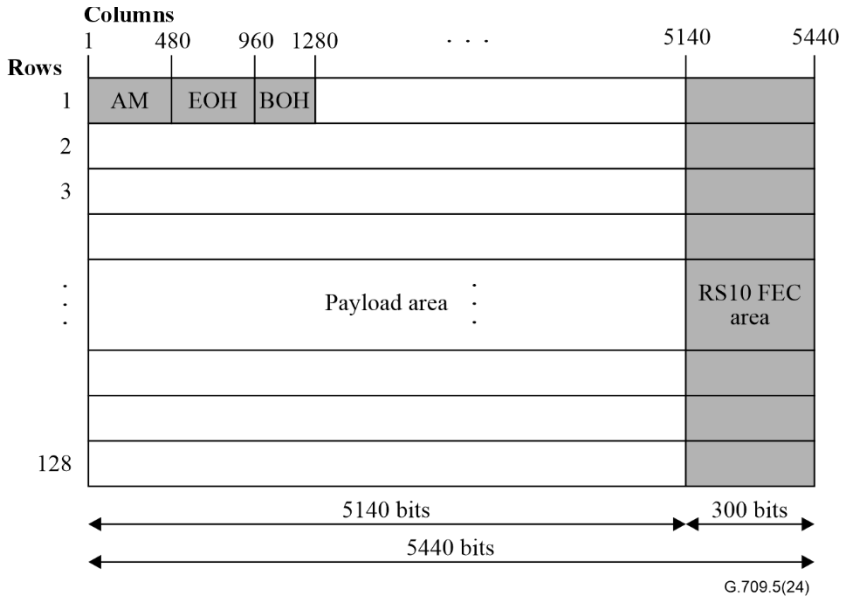

Figure 11-1 – 100G FlexO-1-RS frame structure

11.2 Bit rate and frame periods

The bit rate and tolerance of the 100G FlexO-1-RS signal are defined in Table 11-1.

The bit rate ratio between FlexO-x-RS and FlexO-x signals is shown in Figure 11-2. The number of columns 5 140 is not altered by the scrambling and AM insertion processes. The FEC encoder adds 300 columns resulting in 5 440. The lane distribution process does not alter the overall bit rate.

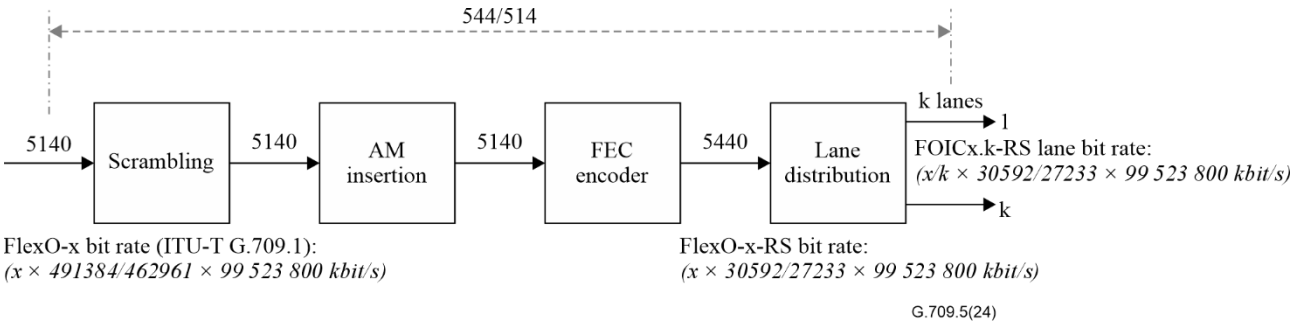

Figure 11-2 – FlexO-x-RS/FlexO-x bit rate ratio

Table 11-1 – 100G FlexO-1-RS bit rate

100G FlexO-1-RS nominal bit rate	Bit-rate tolerance
30592/27233 × 99 532 800 kbit/s	±20 ppm
NOTE 1 – The nominal 100G FlexO-1-RS bit rate is approximately: 111 809 474.446 kbit/s. NOTE 2 – The 100G FlexO-1-RS bit rate can be based on the OTUC bit rate as follows: 256/241 × OTUC bit rate = 256/241 × 239/226 × 99 532 800 kbit/s. NOTE 3 – The resulting 100G FlexO-1-RS bit rate is within a −4.46 ppm offset of the OTU4 nominal bit rate.	

The frame and multi-frame periods of the 100G FlexO-1-RS signal are defined in Table 11-2.

Table 11-2 – 100G FlexO-1-RS frame and multi-frame periods

Frame period (Note)	Multi-frame period (Note)
~6.228 µs	49.822 µs
NOTE – The period is an approximated value, rounded to three decimal places.	

11.3 Scrambling

The 100G FlexO-1-RS frame payload, fixed stuffing, basic overhead and extended overhead must be scrambled prior to transmission in order to provide DC balance and proper running disparity on the interface. The lane alignment markers (am_i, i = 0, 1, 2, 3) in the AM field are not scrambled and the chosen values have properties of already being DC balanced. Figure 11-4 below shows the scrambled parts of the frame as yellow.

The operation of the scrambler shall be functionally equivalent to that of a frame-synchronous additive scrambler with sequence length 65 535 and the generating polynomial shall be $x^{16} + x^{12} + x^{30} + x + 1$. See Figure 11-3 of [ITU-T G.709] for an illustration of this scrambler.

The scrambler operates on the entire frame, including the AM field and the FEC area which contain undefined values when the frame is input to the scrambler. This is illustrated in Figure 11-3 where yellow indicates bits that are scrambled. The scrambler resets to 0xFFFF on the most significant (first transmitted) bit of the start of the FlexO-1-RS frame. The scrambler state advances during each bit of the frame. In the source function, the alignment markers are inserted into the AM field after scrambling and prior to the FEC encoding The FEC encoder overwrites the FEC area. As such, the sink receives the unscrambled AM and FEC fields, as illustrated in Figure 11-4.

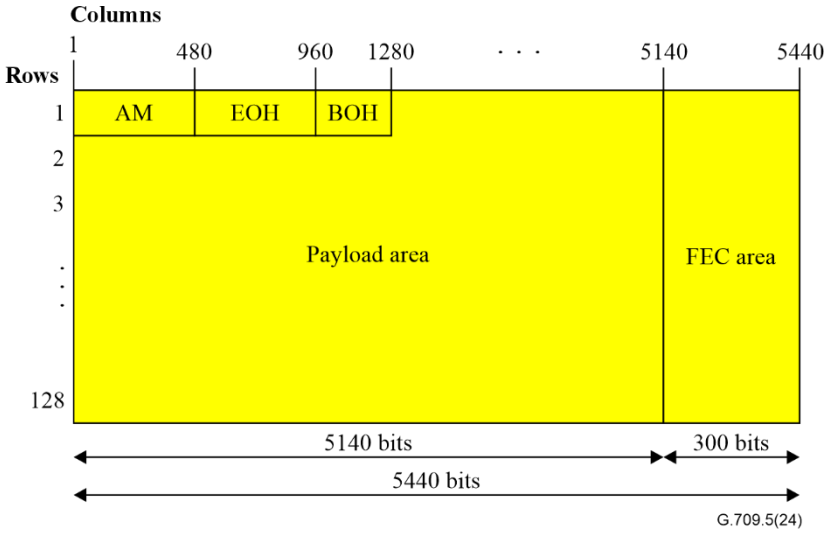

Figure 11-3 – 100G FlexO-1-RS frame after scrambling

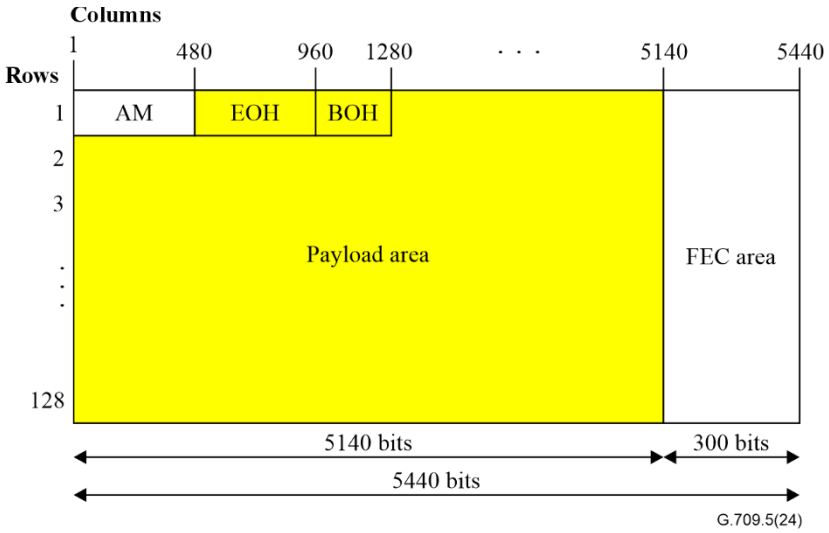

Figure 11-4 – 100G FlexO-1-RS frame after AM field and FEC insertion

11.4 Forward error correction (FEC)

The FlexO-1-RS FEC area contains the Reed-Solomon RS(544,514) FEC codes. The RS(544,514) FEC code shall be computed as specified in Annex A.

11.5 FOIC1.k-RS interface

11.5.1 FOIC1.4-RS interface

A FlexO-1-RS structure is adapted over multi-channel parallel interfaces, using four ~28 Gbit/s physical lanes. No lane bit-multiplexing is performed.

The alignment markers for the FlexO-1-RS are distributed on four FOIC1.4 lanes, resulting in 120 bits of data per lane. The alignment marker values are specified in clause 9. Each alignment marker has unique UMx and UPx values. The distribution of the four alignment markers to lanes 0, 1, 2 and 3, enables the unique values to be used for lane reordering in the sink function. The CMx values are replicated on all the four lanes to facilitate searching, alignment and the deskewing process.

After the FEC encoding, the FlexO-1-RS frame is distributed to four logical FOIC1.4 lanes, in groups of 10-bits, in a round-robin distribution scheme from the lowest to the highest numbered lanes. This distribution is the inverse of the 10-bit interleaving of the AM field, such that each FOIC1.4 lane ends up with the correct AM, as illustrated in Table 11-3 where the transmission order is from left to right.

NOTE 1 – The inverse multiplexing function is based on clause 91 [IEEE 802.3].

NOTE 2 – The mechanism is compatible and can reuse optical modules being developed for IEEE 100GBASE-LR4, -ER4 with OTU4 rate support.

NOTE 3 – The electrical specifications for an FOIC1.4-RS 25G lane is in [b-OIF CEI].

Table 11-3 – AM bit distribution over the four FOIC1.4-RS lanes

AM bits	Lane 0 10-bit symbol of AM0	Lane 1 10-bit symbol of AM1	Lane 2 10-bit symbol of AM2	Lane 3 10-bit symbol of AM3
1 – 40	0101100101	0101100101	0101100101	0101100101
41 – 80	0100100110	0100100110	0100100110	0100100110
81 – 120	0100011011	0100001000	0100011000	0100010110
121 – 160	0110100110	0010100110	1010100110	1010100110

Table 11-3 – AM bit distribution over the four FOIC1.4-RS lanes

AM bits	Lane 0 10-bit symbol of AM0	Lane 1 10-bit symbol of AM1	Lane 2 10-bit symbol of AM2	Lane 3 10-bit symbol of AM3
161 – 200	1010110110	1010110110	1010110110	1010110110
201 – 240	0110111001	0110111110	0110110111	0110110010
241 – 280	1011100000	0110010110	1111011111	0001011000
281 – 320	0010001110	1001111011	0011001111	0100000001
321 – 360	1100111101	0111111000	0110101010	0000101111
361 – 400	1001000111	0110011010	0000001000	0111101001
401 – 440	1111011100	0101100001	0011001100	1110111111
441 – 480	0100110000	0010000001	0010010101	1011110100
NOTE – Transmission order of each 10-bit word is left-to-right (MSB first). The transmission order within the FlexO frame is left-to-right across the row and down the table. The transmission order for each lane is per-word and down the table.				

An FOIC1.4-RS interface comprises four OTSi. Specifications of the OTSi carrying a FOIC1.4-RS lane are contained in [ITU-T G.695] and [ITU-T G.959.1].

A group of m FOIC1.4-RS optical interfaces may be used to carry a digital client signal (e.g., an OTUCn may be carried over m FOIC1.4-RS optical interfaces).

11.5.2 FOIC1.4-RS skew tolerance requirements

The lane skew tolerance requirement is 180 ns.

NOTE – These requirements are in line with (Chip to) 100 Gb/s attachment unit interface (CAUI4) [IEEE 802.3].

11.5.3 FOIC1.4-RS 28G lane bit rate

The FOIC1.4-RS lane is synchronous to the FlexO-1-RS frame. There are four lanes.

The bit rate and tolerance of the FOIC1.4-RS lane signal is defined in Table 11-4.

Table 11-4 – FOIC1.4-RS lane rate

FOIC1.4-RS nominal lane bit rate	Bit-rate tolerance
30592/27233 × 24 883 200 kbit/s	±20 ppm
NOTE 1 – The nominal lane rate is approximately: 27 952 368.611 kbit/s. NOTE 2 – FOIC1.4-RS_lane_rate = 100G_FlexO-1-RS_rate/4.	

NOTE – The 100G FlexO-1-RS rate is specified in clause 11.2.

This results in a FOIC1.4-RS lane bit rate with a −4.46 ppm offset from the optical transport lane OTL4.4 nominal bit rate.

11.5.4 FOIC1.1-RS interface

A FlexO-1-RS is adapted over a single ~112 Gbit/s physical lane by first creating an FOIC1.4-RS as described in clause 11.5.1 and then bit multiplexing the four logical lanes into a FOIC1.1-RS.

NOTE – The mechanism is compatible and can reuse optical modules with 100G per lane being developed for IEEE 100GBASE-FR1, -LR1, with 100G OTN rate support.

11.5.5 FOIC1.1-RS skew tolerance requirements

The lane skew tolerance requirement is 180 ns.

NOTE – These requirements are in line with 100GAUI-1 [IEEE 802.3].

11.5.6 FOIC1.1-RS 112G lane bit rate

The single FOIC1.1-RS lane is synchronous to the FlexO-1-RS frame.

The bit rate and tolerance of the FOIC1.1-RS lane signal is defined in Table 11-5.

Table 11-5 – FOIC1.1-RS lane rate

FOIC1.1-RS nominal lane bit rate	Bit-rate tolerance
30592/27233 × 99 532 800 kbit/s	±20 ppm
NOTE 1 – The nominal lane rate is approximately: 111 809 474.444 kbit/s. NOTE 2 – FOIC1.1-RS_lane_rate = 100G_FlexO-1-RS_rate.	

NOTE – The 100G FlexO-1-RS rate is specified in clause 11.2.

12 200G FlexO-2-RS interface

12.1 Frame structure

The 200G FlexO-2-RS frame structure is shown in Figure 12-2 and consists of two 10-bit interleaved 100G FlexO frame structures in columns 1 to 10 280 and an FEC area in columns 10 281 to 10 880 in every row as illustrated in Figure 12-2. FlexO-2-RS interfaces use alignment markers as described in clause 9.

NOTE – The 200G FlexO-2-RS frame structure is derived from 200 Gbit/s Ethernet clause 119 [IEEE 802.3] FEC alignment and lane architecture, without any 66b alignment or 256b/257b transcoding functions.

For the case that a FlexO-2-RS-m group carries a FlexO-n with n < 2m, the last FlexO-2-RS signal will contain only one equipped FlexO instance (see Figure 12-1). When a FlexO-2-RS contains fewer than 2 equipped instances, the equipped instance is the first 100G FlexO frame within this 200G FlexO-2-RS #m frame. The second 100G FlexO frame has its group identification (GID) field set to all-0s to indicate that it is unequipped.

The following rules govern unequipped instances:

– Unequipped instances must always be the highest numbered FlexO instance(s) in a FlexO-2-RS frame.

– There must always be at least one equipped instance in every FlexO-2-RS frame.

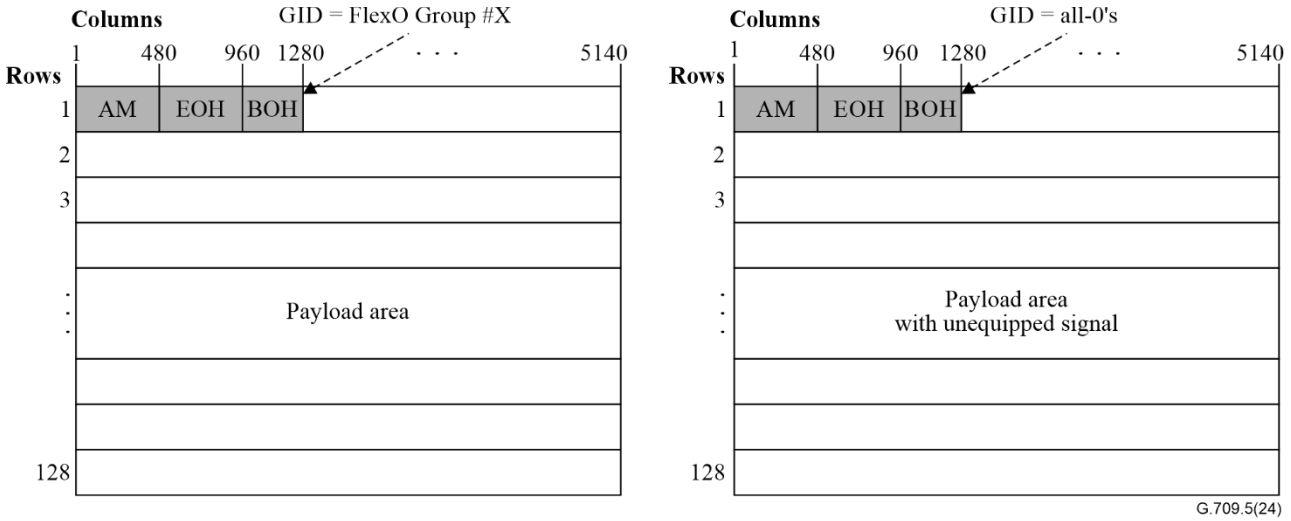

Figure 12-1 – 100G FlexO frames within 200G FlexO-2-RS #m signal for case of partial fill

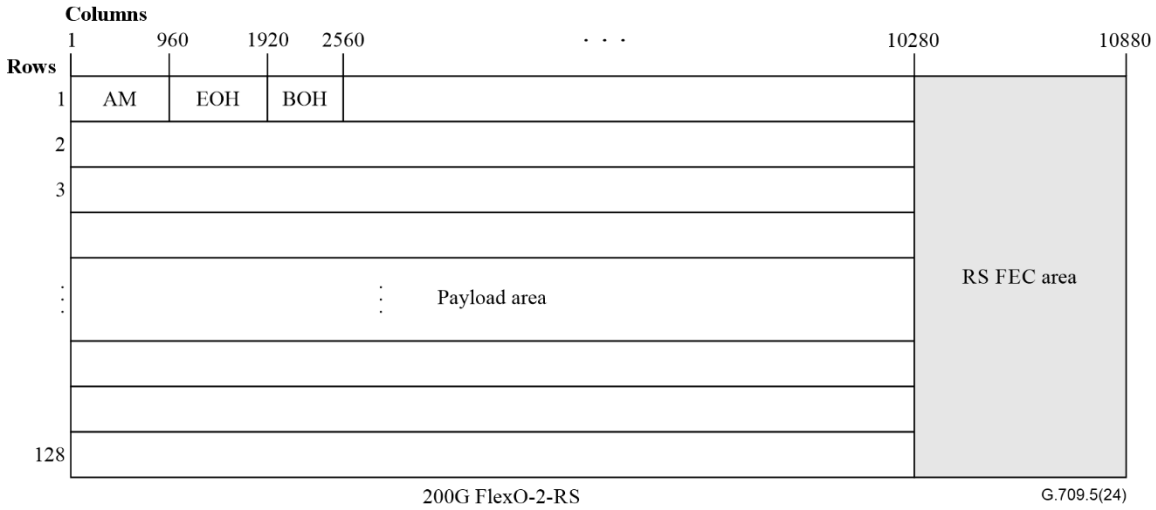

Figure 12-2 – 200G Flex-2-RS frame structure

12.2 Bit rate and frame periods

The bit rate and tolerance of the 200G FlexO-2-RS signal is defined in Table 12-1.

Table 12-1 – 200G FlexO-2-RS bit rate

200G FlexO-2-RS nominal bit rate	Bit-rate tolerance
2 × 30592/27233 × 99 532 800 kbit/s	±20 ppm
NOTE 1 – The nominal 200G FlexO-2-RS bit rate is approximately: 223 618 948.893 kbit/s. NOTE 2 – The 200G FlexO-2-RS bit rate can be based on the OTUC bit rate as follows: 2 × 256/241 × OTUC bit rate = 2 × 256/241 × 239/226 × 99 532 800 kbit/s.	

The frame and multi-frame periods of the 200G FlexO-2-RS signal are defined in Table 12-2.

Table 12-2 – 200G FlexO-2-RS frame and multi-frame periods

Frame period (Note)	Multi-frame period (Note)
~6.228 µs	49.822 µs
NOTE – The period is an approximated value, rounded to three decimal places.	

12.3 Scrambling

The operation of the 200G FlexO-2-RS scrambler is based on the interleaved 200G FlexO-2-RS frame structure shown in Figure 12-2 which is generated by the 10-bit interleaving of the two instances of 128 rows by 5 440 1-bit columns of the 200G FlexO-2-RS frame structure.

The interleaved 200G FlexO-2-RS frame payload, fixed stuffing, basic overhead and extended overhead must be scrambled prior to transmission in order to provide DC balance and proper running disparity on the interface. The lane alignment markers (am_i, i = 0, 1, 2, ...7) in the AM field are not scrambled and the chosen values have properties of already being DC balanced. Figure 12-3 below shows the scrambled parts of the frame as yellow.

The operation of the scrambler shall be functionally equivalent to that of a frame-synchronous additive scrambler of sequence length 65 535 and the generating polynomial shall be $x^{16} + x^{12} + x^3 + x + 1$. See Figure 11-3 of [ITU-T G.709] for an illustration of this scrambler.

The scrambler operates on the entire frame, including the AM field and FEC area which contain undefined values when the frame is input to the scrambler. This is illustrated in Figure 12-3 where yellow indicates bits that are scrambled. The scrambler resets to 0xFFFF on the most significant (first transmitted) bit of the start of the FlexO-2-RS frame. The scrambler state advances during each bit of the frame. In the source function, the alignment markers are inserted into the AM field after scrambling and prior to FEC encoding. The FEC encoder overwrites the FEC area. As such, the sink receives unscrambled AM and FEC fields, as illustrated in Figure 12-4.

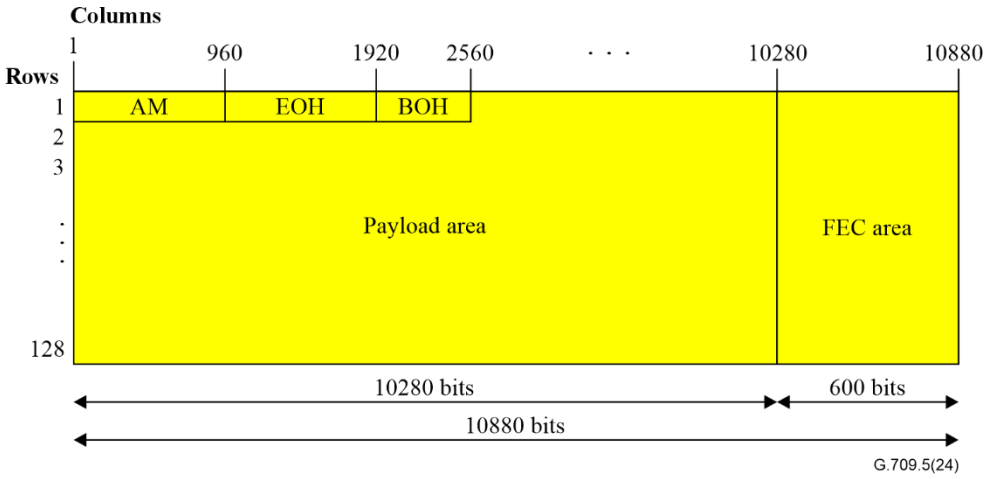

Figure 12-3 – 200G FlexO-2-RS frame after scrambling

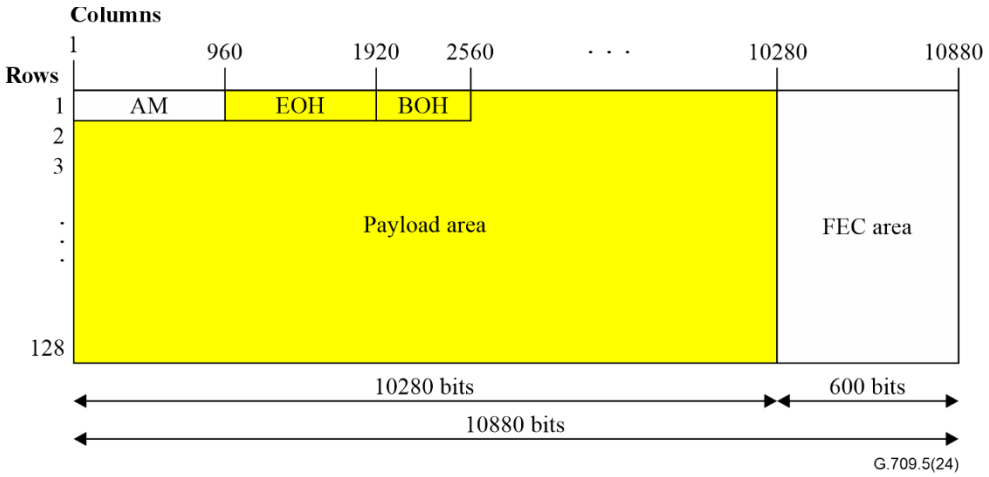

Figure 12-4 – 200G FlexO-2-RS frame after AM field and FEC insertion

12.4 Forward error correction (FEC)

The FlexO-2-RS FEC area contains the Reed-Solomon RS(544,514) FEC codes. The RS(544,514) FEC code shall be computed as specified in Annex A.

12.5 FOIC2.k-RS interface

12.5.1 FOIC2.4-RS interface

The FlexO-2-RS structure is adapted over multi-channel parallel interfaces, using four ~56 Gbit/s physical lanes.

The alignment markers for the FlexO-2-RS are distributed on eight logical FOIC2.4 lanes, resulting in 120 bits of data per logical lane. The alignment marker values are specified in clause 9. Each alignment marker has unique UMx and UPx values. The distribution of the eight alignment markers to lanes 0, 1, 2 to 7, enables the unique values to be used for lane reordering in the sink function. The CMx values are replicated on all eight lanes to facilitate the searching, alignment and deskewing process.

After the FEC encoding the FlexO-2-RS frame (see Annex A), each set of two sub-rows (i.e., two FEC codewords) are interleaved on a 10-bit basis and then distributed to eight logical lanes in a round-robin distribution scheme from the lowest to the highest numbered lanes. The specific scheme of interleaving and distribution is specified in clause 119.2.4.7 of [IEEE 802.3] for 200GBASE-R interface and is designed to ensure that the correct alignment marker appears in each of the eight lanes. The resulting per-lane transmitted values of the alignment markers are illustrated in Table 12-3 where the transmission order is from left to right.

The four physical lanes of a FOIC2.4-RS interface are generated by bit multiplexing pairs of logical lanes, e.g., bit multiplexing of lane 0 and lane 1, lane 2 and lane 3, lane 4 and lane 5, lane 6 and lane 7.

NOTE – The mechanism is compatible and can reuse optical modules being developed for IEEE 200GBASE-FR4, -LR4, -ER4 with 200G OTN rate support.

Table 12-3 – AM bit distribution over the eight logical lanes

AM bits	Lane 0 10-bit symbol of AM0	Lane 1 10-bit symbol of AM1	Lane 2 10-bit symbol of AM2	Lane 3 10-bit symbol of AM3	Lane 4 10-bit symbol of AM4	Lane 5 10-bit symbol of AM5	Lane 6 10-bit symbol of AM6	Lane 7 10-bit symbol of AM7
1 - 80	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101
81 - 160	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110
161 - 240	0100101000	0100001000	0100011000	0100010110	0100100001	0100010011	0100101111	0100010001
241 - 320	0010100110	0010100110	1010100110	1010100110	1110100110	1110100110	0010100110	0010100110
321 - 400	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110
401 - 480	0110110110	0110111110	0110110111	0110110010	0110111001	0110110111	0110110111	0110110100
481 - 560	1011110011	0110010110	1111011111	0001011000	1000010101	0010010010	0111010000	1100011010
561 - 640	0100000011	1001111011	0011001111	0100000001	0010001010	0011110010	1000111001	1101101110
641 - 720	0011000110	0111111000	0110101010	0000101111	0100111101	1000101110	1000010110	1101101010
721 - 800	0101000011	0110011010	0000001000	0111101001	1001111010	0011011011	0010001011	1100111001
801 - 880	0010111111	0101100001	0011001100	1110111111	1011011101	0111000011	1101110001	0100100100
881 - 960	0011001110	0010000001	0010010101	1011110100	0110110000	0101110100	1001111010	0100100101

NOTE – Transmission order of each 10-bit word is left-to-right (MSB first). The transmission order within the FlexO frame is left-to-right across the row and down the table. The transmission order for each lane is per-word and down the table.

An FOIC2.4-RS interface comprises four OTSi. Specifications of the OTSi carrying a FOIC2.4-RS lane are contained in [ITU-T G.695] and [ITU-T G.959.1].

A group of m FOIC2.4-RS optical interfaces may be used to carry a digital client signal (e.g., an OTUCn may be carried over m FOIC2.4-RS optical interfaces).

12.5.2 FOIC2.4-RS skew tolerance requirements

The lane skew tolerance requirement is 180 ns.

NOTE – These requirements are in line with 200GAUI-4 [IEEE 802.3].

12.5.3 FOIC2.4-RS 56G lane bit rate

The FOIC2.4-RS lane is synchronous to the FlexO-2-RS frame. There are four lanes.

The bit rate and tolerance of the FOIC2.4-RS lane signal is defined in Table 12-4.

Table 12-4 – FOIC2.4-RS lane rate

FOIC2.4-RS nominal lane bit rate	Bit-rate tolerance
30592/27233 × 49 766 400 kbit/s	±20 ppm
NOTE 1 – The nominal FOIC2.4-RS lane rate is approximately: 55 904 737.223 kbit/s. NOTE 2 – FOIC2.4-RS_lane_rate = 200G_FlexO-2-RS_rate/4.	

NOTE – The 200G FlexO-2-RS bit rate is specified in clause 12.2.

12.5.4 FlexO-2-RS interface processes

Figure 12-5 shows the processes of a FlexO-2-RS interface. The dashed lines in the Figure divide into processes that are reused from FlexO-1, processes that are unique to FlexO-2-RS, and processes that are reused from 200GBASE-R. The FOIC2.4 completely reuses all the processes from the 200GBASE-R PCS below the alignment insertion/removal processes, as well as the PMA and the PMD.

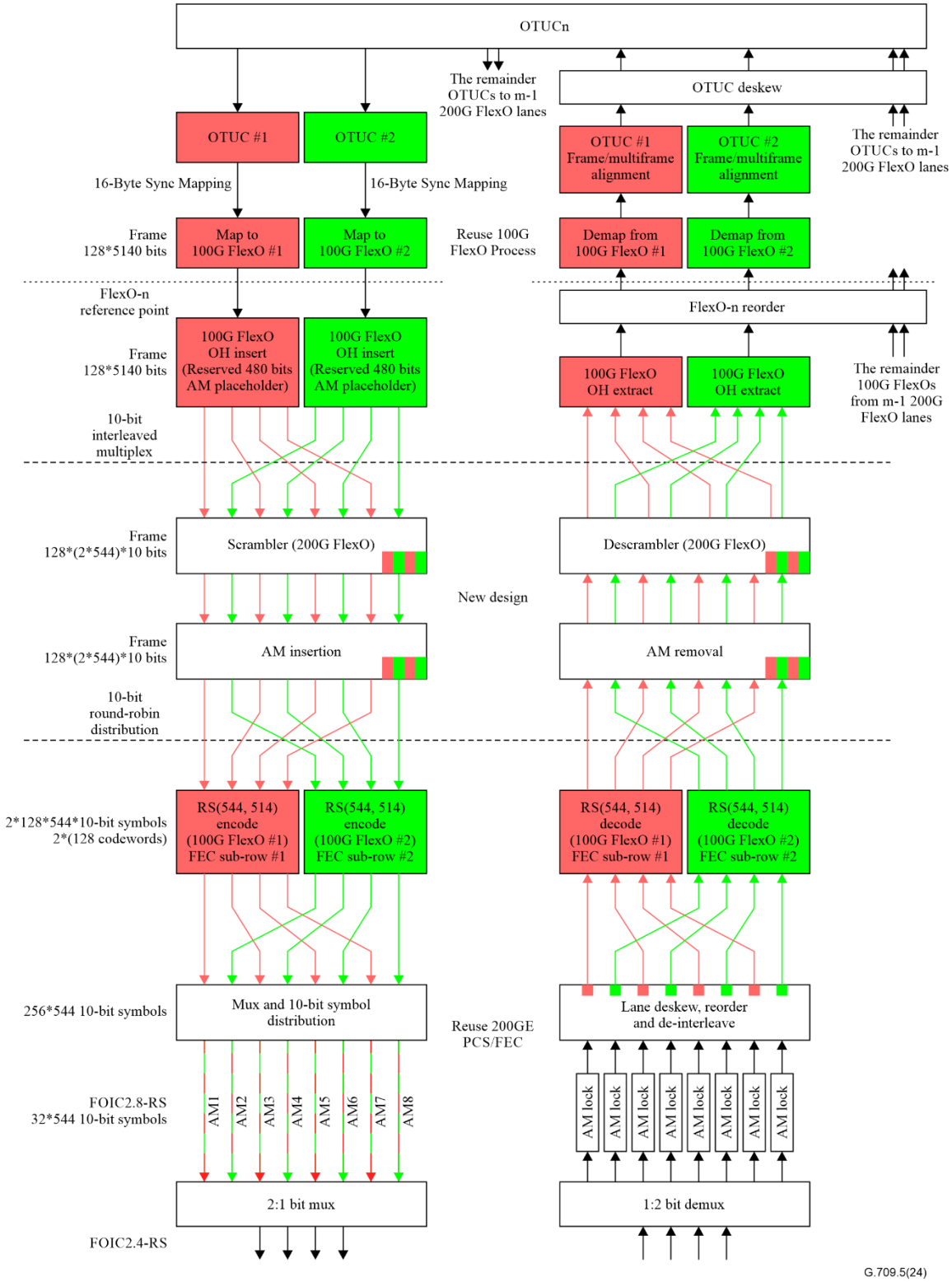

Figure 12-5 – 200G FlexO-2-RS interface processes

13 400G FlexO-4-RS interface

13.1 Frame structure

The 400G FlexO-4-RS frame structure is shown in Figure 13-2 and consists of four 10-bit interleaved FlexO frame structure instances in columns 1 to 10 280 and an FEC area in columns 10 281to 10 880 in every row as illustrated in Figure 13-2. FlexO-4-RS interfaces use alignment markers as described in clause 9.

NOTE – The 400G FlexO-4-RS frame structure is derived from 400 Gbit/s Ethernet clause 119 [IEEE 802.3] FEC alignment and lane architecture, without any 66b alignment or 256b/257b transcoding functions.

For the case that a FlexO-4-RS-m group carries a FlexO-n with n < 4m, the last FlexO-4-RS signal will contain one, two, or three equipped FlexO instances (see Figure 13-1). When a FlexO-4-RS frame contains fewer than four equipped instances, these three, two or one instance(s) is (are) located in the first one, two or three 100G FlexO frame(s) within this 400G FlexO-4-RS #m frame. The last one, two or three 100G FlexO frames have their GID field set to all-0s to indicate that the 100G FlexO frame is unequipped.

The same rules in clause 12.1 governing unequipped instances apply.

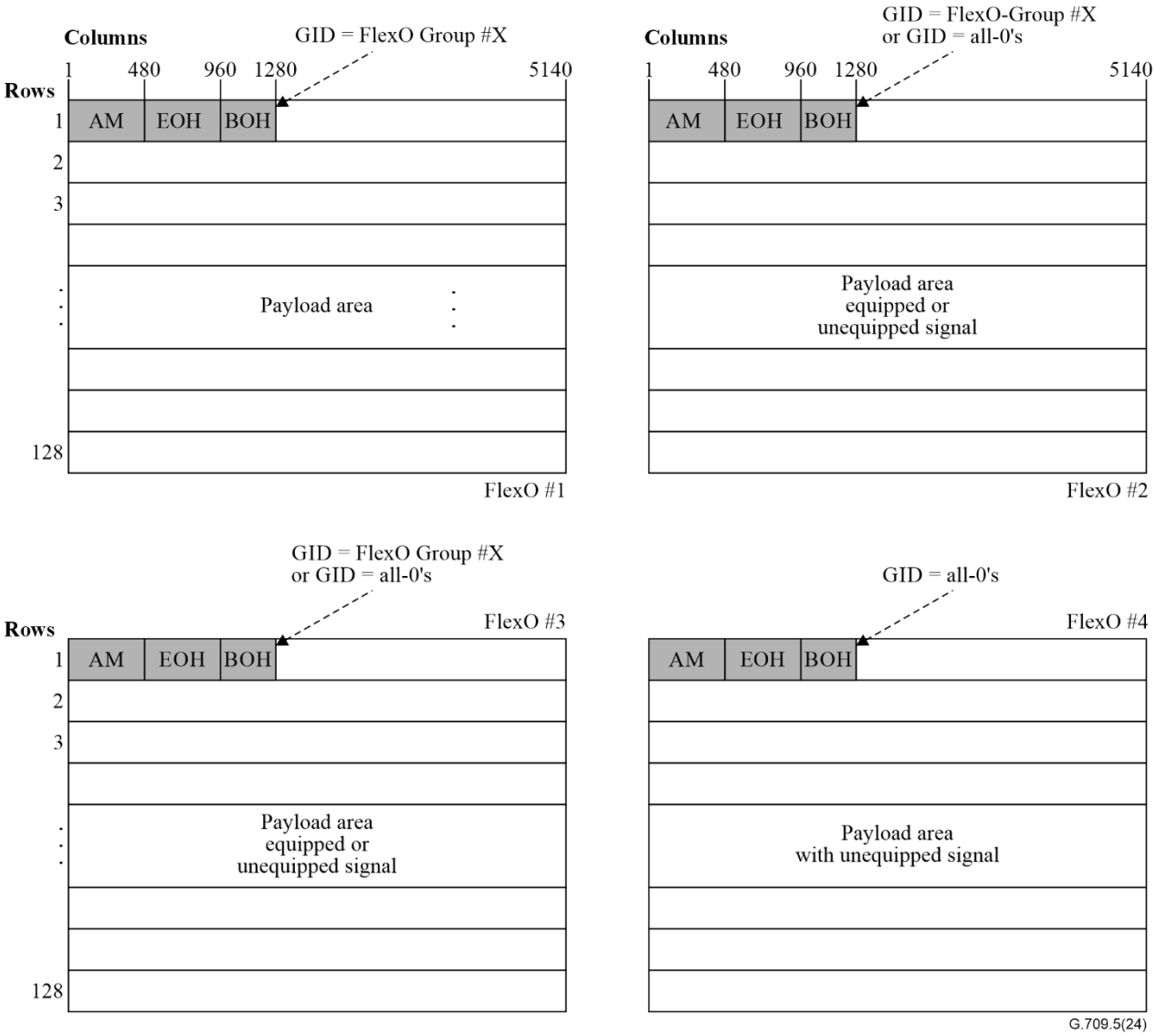

Figure 13-1 – 100G FlexO frames within 400G FlexO-4-RS #m signal for case of partial fill

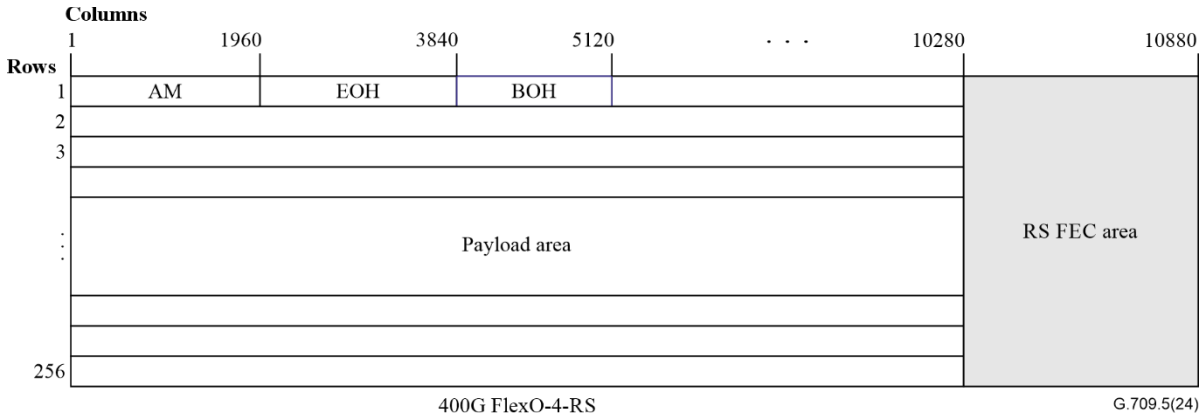

Figure 13-2 – 400G FlexO-4-RS frame structure

13.2 Bit rate and frame periods

The bit rate and tolerance of the 400G FlexO-4-RS signal is defined in Table 13-1.

Table 13-1 – 400G FlexO-4-RS bit rate

400G FlexO-4-RS nominal bit rate	Bit-rate tolerance
4 × 30592/27233 × 99 532 800 kbit/s	±20 ppm
NOTE 1 – The nominal 400G FlexO-4-RS bit rate is approximately: 447 237 897.786 kbit/s. NOTE 2 – The 400G FlexO-4-RS bit rate can be based on the OTUC bit rate as follows: 4 × 256/241 × OTUC bit rate = 4 × 256/241 × 239/226 × 99 532 800 kbit/s.	

The frame and multi-frame periods of the 400G FlexO-4-RS signal are defined in Table 13-2.

Table 13-2 – 400G FlexO-4-RS frame and multi-frame periods

Frame period (Note)	Multi-frame period (Note)
~6.228 µs	49.822 µs
NOTE – The period is an approximated value, rounded to three decimal places.	

13.3 Scrambling

The operation of the 400G FlexO-4-RS scrambler is based on the interleaved 400G FlexO-4-RS frame structure shown in Figure 13-2 which is generated by 10-bit multiplexing of the two instances of 256 rows by 5 440 1-bit columns of the 400G FlexO-4-RS frame structure.

The interleaved 400G FlexO-4-RS frame payload, fixed stuffing, basic overhead and extended overhead must be scrambled prior to transmission in order to provide DC balance and proper running disparity on the interface. The lane alignment markers (am_i, i = 0, 1, 2, ... 15) in the AM field are not scrambled and the chosen values have properties of already being DC balanced. Figure 13-4 below shows the scrambled parts of the frame as yellow.

The operation of the scrambler shall be functionally equivalent to that of a frame-synchronous scrambler of sequence 65 535 and the generating polynomial shall be $x^{16} + x^{12} + x^3 + x + 1$. See Figure 11-3 of [ITU-T G.709] for an illustration of this scrambler.

The scrambler operates on the entire frame, including the AM field and the FEC area which contain undefined values when the frame is input to the scrambler. This is illustrated in Figure 13-3 where yellow indicates bits that are scrambled. The scrambler resets to 0xFFFF on the most significant (first transmitted) bit of the start of the FlexO-4-RS frame. The scrambler state advances during each bit of

the frame. In the source function, the alignment markers are inserted into the AM field after scrambling and prior to FEC encoding. The FEC encoder overwrites the FEC area. As such, the sink receives unscrambled AM and FEC fields, as illustrated in Figure 13-4.

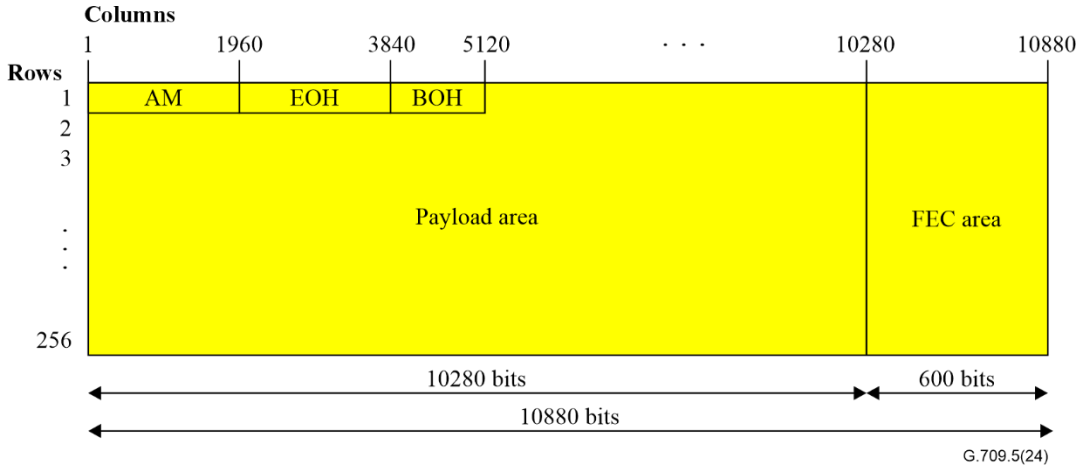

Figure 13-3 – 400G FlexO-4-RS frame after scrambling

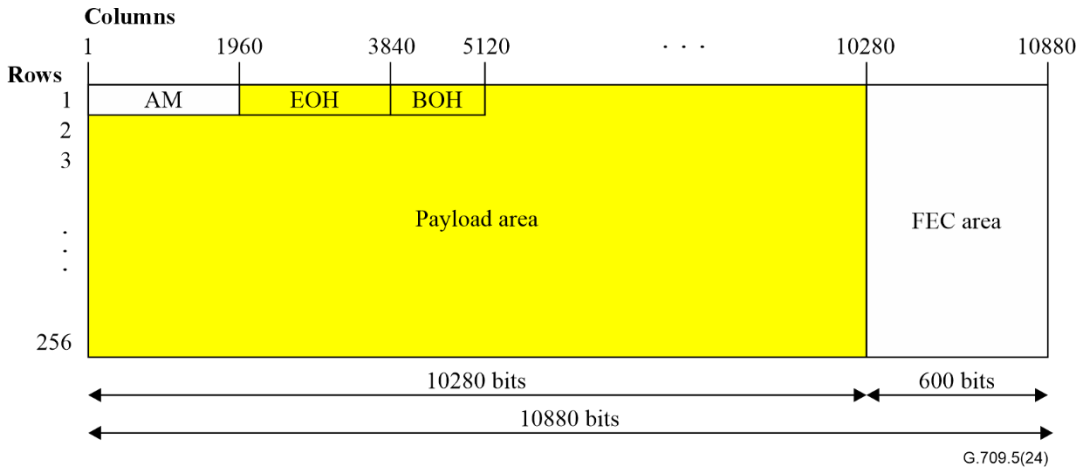

Figure 13-4 – 400G FlexO-4-RS frame after AM field and FEC insertion

13.4 Forward error correction (FEC)

The FlexO-4-RS FEC area contains the Reed-Solomon RS(544,514) FEC codes. The RS(544,514) FEC code shall be computed as specified in Annex A.

13.5 FOIC4.k-RS interface

13.5.1 FOIC4.8-RS interface

The FlexO-4-RS structure is adapted over multi-channel parallel interfaces, using eight ~56 Gbit/s physical lanes.

The alignment markers for the FlexO-4-RS are distributed on sixteen lanes, resulting in 120 bits of data per lane. The alignment marker values are specified in clause 9. Each alignment marker has unique UMx and UPx values. The distribution of the sixteen alignment markers to lanes 0, 1, 2 to 15, enables the unique values to be used for lane reordering in the sink function. The CMx values are replicated on all the sixteen lanes to facilitate the searching, alignment and deskewing process.

After the FEC encoding the FlexO-4-RS frame (see Annex A), each set of two sub-rows (i.e., two FEC codewords) are interleaved on a 10-bit basis and then distributed to eight logical lanes in a round-robin distribution scheme from the lowest to the highest numbered lanes.

The specific scheme of interleaving and distribution is specified in clause 119.2.4.7 of [IEEE 802.3] for 400GBASE-R interface and is designed to ensure that the correct alignment marker appears in each of the 16 lanes. The resulting per-lane transmitted values of the alignment markers are illustrated in Table 13-3 where the transmission order is from left to right.

The eight lanes of a FOIC4.8-RS interface are generated by bit multiplexing pairs of logical lanes, e.g., bit multiplexing of lane 0 and lane 1, lane 2 and lane 3, lane 4 and lane 5, lane 6 and lane 7, lane 8 and lane 9, lane 10 and lane 11, lane 12 and lane 13, lane 14 and lane 15.

NOTE – The mechanism is compatible and can reuse optical modules being developed for IEEE 400GBASE-FR8, -LR8, -ER8 with 400G OTN rate support.

Table 13-3 – AM bit distribution over the sixteen logical lanes

AM bits	**Lane 0 10-bit symbol of AM0**	**Lane 1 10-bit symbol of AM1**	**Lane 2 10-bit symbol of AM2**	**Lane 3 10-bit symbol of AM3**	**Lane 4 10-bit symbol of AM4**	**Lane 5 10-bit symbol of AM5**	**Lane 6 10-bit symbol of AM6**	**Lane 7 10-bit symbol of AM7**
1 - 80	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101
161 - 240	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110
321 - 400	0100011011	0100001000	0100011000	0100010110	0100100001	0100010011	0100101111	0100010001
481 - 560	0110100110	0010100110	1010100110	1010100110	1110100110	1110100110	0010100110	0010100110
641 - 720	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110
801 - 880	0110111001	0110111110	0110110111	0110110010	0110111001	0110110111	0110110111	0110110100
961 - 1040	1011100000	0110010110	1111011111	0001011000	1000010101	0010010010	0111010000	1100011010
1121 - 1200	0010001110	1001111011	0011001111	0100000001	0010001010	0011110010	1000111001	1101101110
1281 - 1360	1100111101	0111111000	0110101010	0000101111	0100111101	1000101110	1000010110	1101101010
1441 - 1520	1001000111	0110011010	0000001000	0111101001	1001111010	0011011011	0010001011	1100111001
1601 - 1680	1111011100	0101100001	0011001100	1110111111	1011011101	0111000011	1101110001	0100100100
1761 - 1840	0100110000	0010000001	0010010101	1011110100	0110110000	0101110100	1001111010	0100100101
AM bits	**Lane 8 10-bit symbol of AM8**	**Lane 9 10-bit symbol of AM9**	**Lane 10 10-bit symbol of AM10**	**Lane 11 10-bit symbol of AM11**	**Lane 12 10-bit symbol of AM12**	**Lane 13 10-bit symbol of AM13**	**Lane 14 10-bit symbol of AM14**	**Lane 15 10-bit symbol of AM15**
81 - 160	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101
241 - 320	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110
401 - 480	0100000001	0100110101	0100010111	0100001101	0100000110	0100001010	0100000010	0100001011
561 - 640	1010100110	1010100110	1110100110	1010100110	0010100110	0010100110	1110100110	0110100110
721 - 800	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110
881 - 960	0110111111	0110110100	0110110010	0110111000	0110111101	0110110011	0110111000	0110110110
1041 - 1120	1001100001	0101100011	0000101010	1110010001	1010010001	0011100011	1101010100	1010011001
1201 - 1280	1111001110	1000100011	0111010111	0001100110	0101101111	0011101001	1111011111	0101011101
1361 - 1440	1010111000	0011110010	0001101111	0001110001	1010100100	1100001111	0110010101	1001111010
1521 - 1600	0001100111	1110100111	0111110101	1100011011	1001011011	0011000111	1100101010	0101011001
1681 - 1760	1000001100	0001110111	0110001010	1011100110	1010100100	0011000101	1100001000	1010101000
1841 - 1920	0101010001	0011000011	0011100100	0111100011	0001010110	1000111100	0010011010	1001100001

NOTE – Transmission order of each 10-bit word is left-to-right (MSB first). The transmission order within the FlexO frame is left-to-right across the row and down the Table. The transmission order for each lane is per-word and down the Table.

An FOIC4.8-RS interface comprises eight OTSi. Specifications of the OTSi carrying a FOIC4.8-RS lane are contained in [ITU-T G.695] and [ITU-T G.959.1].

A group of m FOIC4.8-RS optical interfaces may be used to carry a digital client signal (e.g., an OTUCn may be carried over m FOIC4.8-RS optical interfaces).

13.5.2 FOIC4.8-RS skew tolerance requirements

The lane skew tolerance requirement is 180 ns.

NOTE – These requirements are in line with 400GAUI-4 [IEEE 802.3].

13.5.3 FOIC4.8-RS 56G lane bit rate

The FOIC4.8-RS lane is synchronous to the FlexO-4-RS frame. There are eight lanes.

The bit rate and tolerance of the FOIC4.8-RS lane signal is defined in Table 13-4.

Table 13-4 – FOIC4.8-RS lane rate

FOIC4.8-RS nominal lane bit rate	Bit-rate tolerance
30592/27233 × 49 766 400 kbit/s	±20 ppm
NOTE 1 – The nominal FOIC4.8-RS lane rate is approximately: 55 904 737.223 kbit/s. NOTE 2 – FOIC4.8-RS_lane_rate = 400G_FlexO-4-RS_rate/8.	

NOTE – The 400G FlexO-4-RS bit rate is specified in clause 13.2.

13.5.4 FlexO-4-RS interface processes

Figure 13-5 shows the processes of a FlexO-4-RS interface. The dashed lines in the figure divide into processes that are reused from FlexO-1, processes that are unique to FlexO-4-RS, and processes that are reused from 400GBASE-R. The FOIC4.8 completely reuses all the processes from the 400GBASE-R PCS below the alignment insertion/removal processes, as well as the PMA and the PMD.

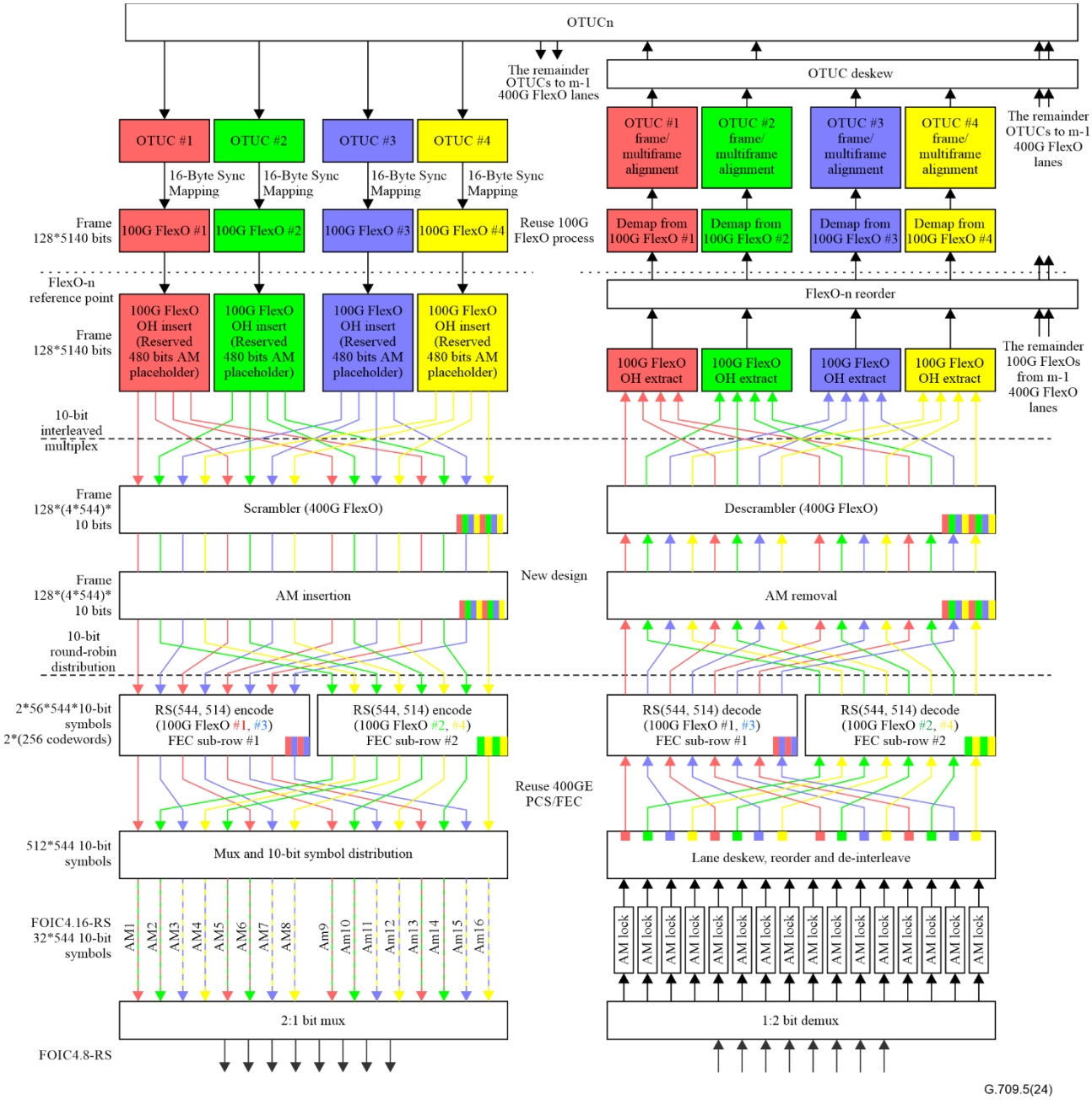

Figure 13-5 – 400G FlexO-4-RS interface processes

13.5.5 FOIC4.4-RS interface

The FlexO-4-RS structure is adapted over multi-channel parallel interfaces, using four ~112 Gbit/s physical lanes.

The four lanes of a FOIC4.4-RS interface are generated by bit multiplexing groups of four logical lanes, e.g., bit multiplexing of lane 0, lane 1, lane 2 and lane 3 (physical lane 0); and lane 4, lane 5, lane 6 and lane 7 (physical lane 1); and lane 8, lane 9, lane 10 and lane 11 (physical lane 2); and lane 12, lane 13, lane 14 and lane 15 (physical lane 3). The logical lanes and alignment marker values are identical to the sixteen logical lanes of FOIC4.8-RS as defined in clauses 13.5.1.

NOTE – The mechanism is compatible and can reuse optical modules with 100G per lane being developed for IEEE 400GBASE-FR4, -LR4-6 with 400G OTN rate support.

13.5.6 FOIC4.4-RS skew tolerance requirements

The lane skew tolerance requirement is 180 ns.

NOTE – These requirements are in line with 400GAUI-4 [IEEE 802.3].

13.5.7 FOIC4.4-RS 112G lane bit rate

The FOIC4.4-RS lane is synchronous to the FlexO-4-RS frame. There are four lanes.

The bit rate and tolerance of the FOIC4.4-RS lane signal is defined in Table 13-5.

Table 13-5 – FOIC4.4-RS lane rate

FOIC4.4-RS nominal lane bit rate	Bit-rate tolerance
30592/27233 × 99 532 800 kbit/s	±20 ppm
NOTE 1 – The nominal lane rate is approximately: 111 809 474.444 kbit/s. NOTE 2 – FOIC4.4-RS_lane_rate = 400G_FlexO-4-RS_rate/4.	

NOTE – The 400G FlexO-4-RS rate is specified in clause 13.2.

14 800G FlexO-8-RS interface

14.1 Frame structure

The 800G FlexO-8-RS frame structure is shown in Figure 14-2 and consists of eight 10-bit interleaved FlexO frame structure instances in columns 1 to 10 280 and an FEC area in columns 10 281 to 10 880 in every row. FlexO-8-RS interfaces use alignment markers as described in clause 9.

NOTE – The 800G FlexO-8-RS frame structure is derived from 800 Gbit/s Ethernet clause 172 [IEEE 802.3df] FEC alignment and lane architecture, without any 66b alignment or 256b/257b transcoding functions.

For the case that a FlexO-8-RS-m group carries a FlexO-n with n < 8m, the last FlexO-8-RS signal will contain from one to seven equipped FlexO instances (see Figure 14-1). When a FlexO-8-RS frame contains fewer than eight equipped instances, these instance(s) is (are) located in the first 1 to 7 100G FlexO frame(s) within this 800G FlexO 8-RS #m frame. The last 1 to 7 100G FlexO frames have their GID field set to all-0s to indicate that the 100G FlexO frame is unequipped.

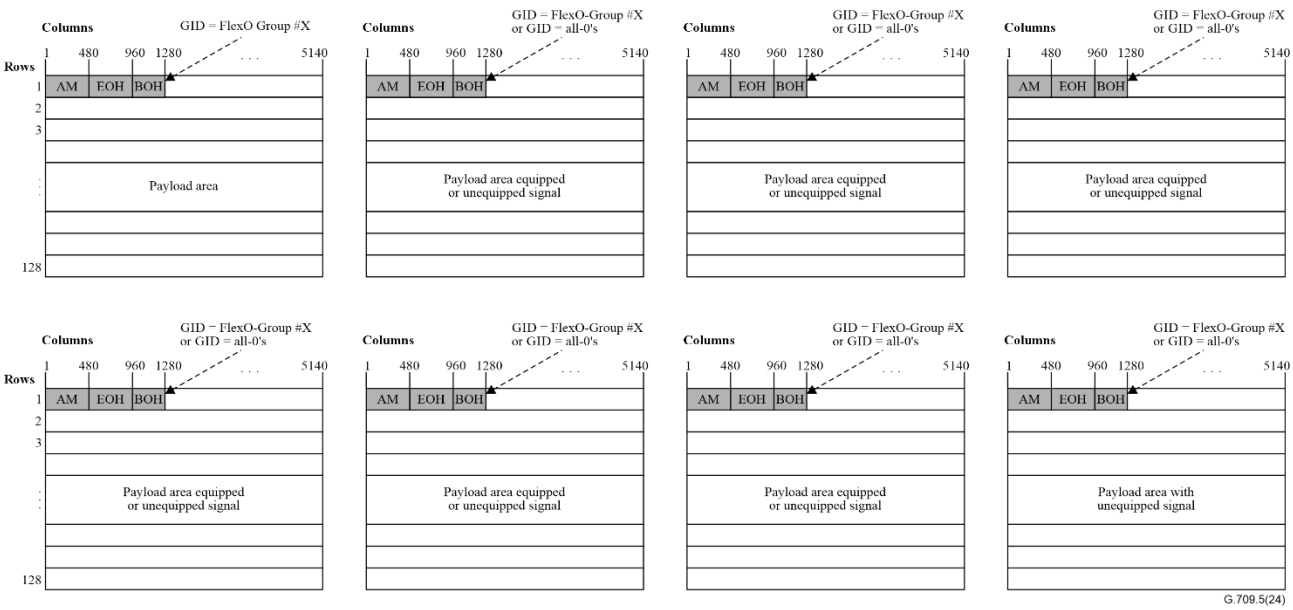

Figure 14-1 – 100G FlexO frames within 800G FlexO-8-RS #m signal for case of partial fill

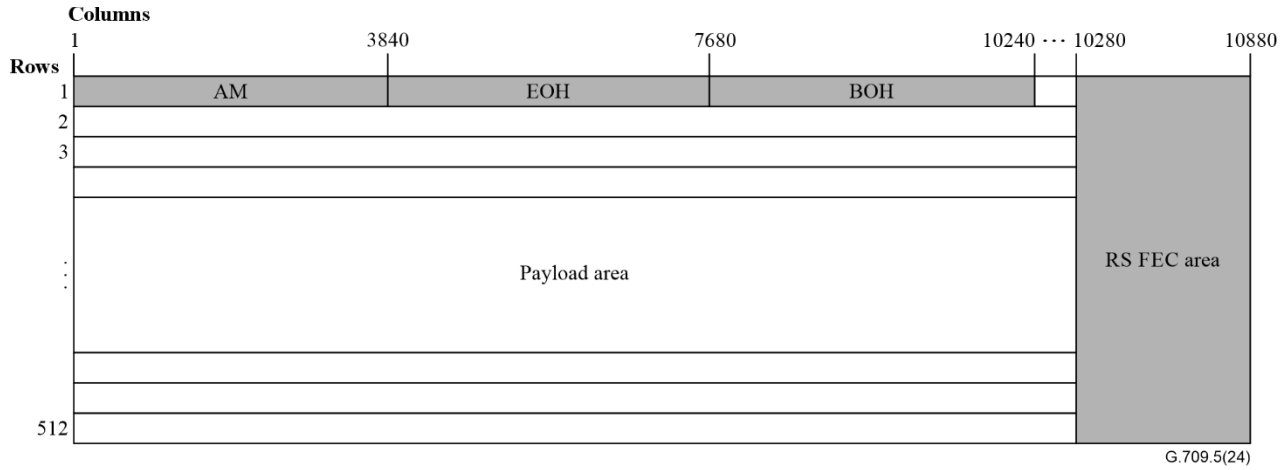

Figure 14-2 – 800G FlexO-8-RS frame structure

14.2 Bit rate and frame periods

The bit rate and tolerance of the 800G FlexO-8-RS signal is defined in Table 14-1.

Table 14-1 – 800G FlexO-8-RS bit rate

800G FlexO-8-RS nominal bit rate	Bit-rate tolerance
8 ×30592/27233 × 99 532 800 kbit/s	±20 ppm
NOTE 1 – The nominal 800G FlexO-8-RS bit rate is approximately: 894 475 795.571 kbit/s. NOTE 2 – The 800G FlexO-8-RS bit rate can be based on the OTUC bit rate as follows: 8 × 256/241 × OTUC bit rate = 8 × 256/241 × 239/226 × 99 532 800 kbit/s.	

The frame and multi-frame periods of the 800G FlexO-8-RS signal are defined in Table 14-2.

Table 14-2 – 800G FlexO-8-RS frame and multi-frame periods

Frame period (Note)	Multi-frame period (Note)
~6.228 µs	49.822 µs
NOTE – The period is an approximated value, rounded to three decimal places.	

14.3 Scrambling

The interleaved 800G FlexO-8-RS signal is carried in two 400G flows which are generated by 10-bit multiplexing of four 100G FlexO instances. Each 400G flow has a FlexO-4-RS frame structure as shown in Figure 13-2 and is individually scrambled as described in clause 13.3.

14.4 Forward error correction (FEC)

The FlexO-8-RS FEC area contains the Reed-Solomon RS(544,514) FEC codes. The RS(544,514) FEC code shall be computed as specified in Annex A.

14.5 FOIC8.k-RS interface

14.5.1 FOIC8.8-RS interface

The FlexO-8-RS structure is adapted over multi-channel parallel interfaces using eight ~112 Gbit/s physical lanes.

The alignment markers for the FlexO-8-RS are distributed in two 400G flows and on sixteen lanes for each flow, resulting in 120 bits of data per lane and thirty-two lanes in total. The alignment marker

values are specified in clause 9. Each alignment marker has unique UMx and UPx values. In flow #0, sixteen alignment markers are distributed to lanes 0, 1, 2 to 15. In flow #1, the other sixteen alignment markers are distributed to lanes 16, 17, 18 to 31. The unique values are used for lane reordering in the sink function. The CMx values are replicated on all thirty-two lanes to facilitate the searching, alignment and deskewing process.

In each flow, after FEC encoding the FlexO-4-RS frame (see Annex A), each set of two sub-rows (i.e., two FEC codewords) are interleaved (not round-robin) on a 10-bit basis and then distributed to the 16 logical lanes in a round-robin distribution scheme from the lowest to the highest numbered lanes.

The specific scheme of interleaving and distribution is specified in clause 172.2.4.7 of [IEEE 802.3df] for 800GBASE-R interface and is designed to ensure that the correct alignment marker appears in each of the thirty-two lanes. The resulting per lane transmitted values of the alignment markers are illustrated in Table 14-3 and Table 14-4 for both flows where the transmission order is from left to right.

The eight physical lanes of a FOIC8.8-RS interface are generated by bit-level multiplexing groups of four logical lanes with an additional constraint that each of the eight physical lanes contains two logical lanes from lane 0 to lane 15 followed by two logical lanes from lane 16 to lane 31.

This could be obtained for example (see Figure 14-3) by bit multiplexing the logical lanes as follows:

– lane 0, lane 1, lane 16 and lane 17 into physical lane 0;
– lane 2, lane 3, lane 18 and lane 19 into physical lane 1;
– lane 4, lane 5, lane 20 and lane 21 into physical lane 2;
– lane 6, lane 7, lane 22 and lane 23 into physical lane 3;
– lane 8, lane 9, lane 24 and lane 25 into physical lane 4;
– lane 10, lane 11, lane 26 and lane 27 into physical lane 5;
– lane 12, lane 13, lane 28 and lane 29 into physical lane 6;
– lane 14, lane 15, lane 30 and lane 31 into physical lane 7.

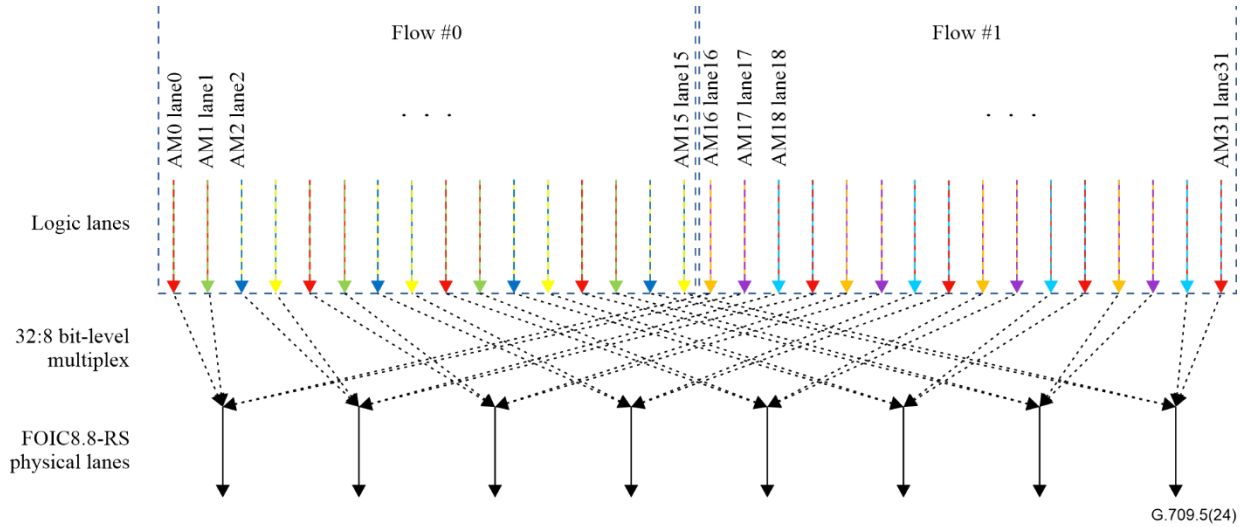

Figure 14-3 – Example of 32:8 bit level multiplexing

NOTE – The mechanism is compatible and can reuse the optical modules being developed for IEEE 800GBASE-FR4(IM-DD) and 800GBASE-LR1/ER1(coherent), with 800G OTN rate support.

Table 14-3 – AM bit distribution over the sixteen logical lanes of flow #0

AM bits	Lane 0 10-bit symbol of AM0	Lane 1 10-bit symbol of AM1	Lane 2 10-bit symbol of AM2	Lane 3 10-bit symbol of AM3	Lane 4 10-bit symbol of AM4	Lane 5 10-bit symbol of AM5	Lane 6 10-bit symbol of AM6	Lane 7 10-bit symbol of AM7
1 - 80	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101
161 - 240	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110
321 - 400	0100011011	0100001000	0100011000	0100010110	0100100001	0100010011	0100101111	0100010001
481-560	0110100110	0010100110	1010100110	1010100110	1110100110	1110100110	0010100110	0010100110
641 - 720	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110
801 - 880	0110111001	0110111110	0110110111	0110110010	0110111001	0110110111	0110110111	0110110100
961 - 1040	1011011111	0110101001	1111100000	0001100111	1000101010	0010101101	0111101111	1100100101
1121 - 1200	1110001110	0101111011	1111001111	1000000001	1110001010	1111110010	0100111001	0001101110
1281 - 1360	1100111101	0111111000	0110101010	0000101111	0100111101	1000101110	1000010110	1101101010
1441 - 1520	1001001000	0110010101	0000000111	0111100110	1001110101	0011010100	0010000100	1100110110
1601 - 1680	0000011100	1010100001	1100001100	0001111111	0100011101	1000000011	0010110001	1011100100
1761 - 1840	0100110000	0010000001	0010010101	1011110100	0110110000	0101110100	1001111010	0100100101
AM bits	**Lane 8 10-bit symbol of AM8**	**Lane 9 10-bit symbol of AM9**	**Lane 10 10-bit symbol of AM10**	**Lane 11 10-bit symbol of AM11**	**Lane 12 10-bit symbol of AM12**	**Lane 13 10-bit symbol of AM13**	**Lane 14 10-bit symbol of AM14**	**Lane 15 10-bit symbol of AM15**
81 - 160	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101
241 - 320	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110
401 - 480	0100000001	0100110101	0100010111	0100001101	0100000110	0100001010	0100000010	0100001011
561 - 640	1010100110	1010100110	1110100110	1010100110	0010100110	0010100110	1110100110	0110100110
721 - 800	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110
881 - 960	0110111111	0110110100	0110110010	0110111000	0110111101	0110110011	0110111000	0110110110
1041 - 1120	1001011110	0101011100	0000010101	1110101110	1010101110	0011011100	1101101011	1010100110
1201 - 1280	0011001110	0100100011	1011010111	1101100110	1001101111	1111101001	0011011111	1001011101
1361 - 1440	1010111000	0011110010	0001101111	0001110001	1010100100	1100001111	0110010101	1001111010
1521 - 1600	0001101000	1110101000	0111111010	1100010100	1001010100	0011001000	1100100101	0101010110
1681 - 1760	0111001100	1110110111	1001001010	0100100110	0101100100	1100000101	0011001000	0101101000
1841 - 1920	0101010001	0011000011	0011100100	0111100011	0001010110	1000111100	0010011010	1001100001

Table 14-4 – AM bit distribution over the sixteen logical lanes of flow #1

AM bits	Lane 16 10-bit symbol of AM16	Lane 17 10-bit symbol of AM17	Lane 18 10-bit symbol of AM18	Lane 19 10-bit symbol of AM19	Lane 20 10-bit symbol of AM20	Lane 21 10-bit symbol of AM21	Lane 22 10-bit symbol of AM22	Lane 23 10-bit symbol of AM23
1 - 80	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101
161 - 240	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110
321 - 400	0100011011	0100001000	0100011000	0100010110	0100100001	0100010011	0100101111	0100010001
481 - 560	0110100110	0010100110	1010100110	1010100110	1110100110	1110100110	0010100110	0010100110
641 - 720	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110
801 - 880	0110111001	0110111110	0110110111	0110110010	0110111001	0110110111	0110110111	0110110100
961 - 1040	1011100000	0110010110	1111011111	0001011000	1000010101	0010010010	0111010000	1100011010
1121 - 1200	0001110001	1010000100	0000110000	0111111110	0001110101	0000001101	1011000110	1110010001
1281 - 1360	0011000001	1000000100	1001010110	1111010011	1011000001	0111010010	0111101010	0010010110
1441 - 1520	1001000111	0110011010	0000001000	0111101001	1001111010	0011011011	0010001011	1100111001
1601 - 1680	1111100011	0101011110	0011110011	1110000000	1011100010	0111111100	1101001110	0100011011
1761 - 1840	1011001111	1101111110	1101101010	0100001011	1001001111	1010001011	0110000101	1011011010
AM bits	**Lane 24 10-bit symbol of AM24**	**Lane 25 10-bit symbol of AM25**	**Lane 26 10-bit symbol of AM26**	**Lane 27 10-bit symbol of AM27**	**Lane 28 10-bit symbol of AM28**	**Lane 29 10-bit symbol of AM29**	**Lane 30 10-bit symbol of AM30**	**Lane 31 10-bit symbol of AM31**
81 - 160	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101	0101100101
241 - 320	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110	0100100110
401 - 480	0100000001	0100110101	0100010111	0100001101	0100000110	0100001010	0100000010	0100001011
561 - 640	1010100110	1010100110	1110100110	1010100110	0010100110	0010100110	1110100110	0110100110
721 - 800	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110	1010110110
881 - 960	0110111111	0110110100	0110110010	0110111000	0110111101	0110110011	0110111000	0110110110
1041 - 1120	1001100001	0101100011	0000101010	1110010001	1010010001	0011100011	1101010100	1010011001
1201 - 1280	1100110001	1011011100	0100101000	0010011001	0110010000	0000010110	1100100000	0110100010
1361 - 1440	0101000100	1100001110	1110010011	1110001101	0101011000	0011110011	1001101001	0110000110
1521 - 1600	0001100111	1110100111	0111110101	1100011011	1001011011	0011000111	1100101010	0101011001
1681 - 1760	1000110011	0001001000	0110110101	1011011001	1010011011	0011111010	1100110111	1010010111
1841 - 1920	1010101110	1100111100	1100011011	1000011100	1110101001	0111000011	1101100101	0110011110

An FOIC8.8-RS interface comprises eight OTSi. Specifications of the OTSi carrying a FOIC8.8-RS lane are contained in [ITU-T G.695] and [ITU-T G.959.1].

A group of m FOIC8.8-RS optical interfaces may be used to carry a digital client signal (e.g., an OTUCn may be carried over m FOIC8.8-RS optical interfaces).

14.5.2 FOIC8.8-RS skew tolerance requirements

The lane skew tolerance requirement is 180 ns.

NOTE – These requirements are in line with 800GAUI-8 [IEEE 802.3df].

14.5.3 FOIC8.8-RS 112G lane bit rate

The FOIC8.8-RS lane is synchronous to the FlexO-8-RS frame. There are eight lanes.

The bit rate and tolerance of the FOIC8.8-RS lane signal is defined in Table 14-5.

Table 14-5 – FOIC8.8-RS lane rate

FOIC8.8-RS nominal lane bit rate	Bit-rate tolerance
30592/27233 × 99 532 800 kbit/s	±20 ppm
NOTE 1 – The nominal lane rate is approximately: 111 809 474.444 kbit/s. NOTE 2 – FOIC8.8-RS_lane_rate = 800G_FlexO-8-RS_rate/8.	

NOTE – The 800G FlexO-8-RS rate is specified in clause 14.2.

14.5.4 FlexO-8-RS interface processes

Figure 14-4 and Figure 14-5 show the processes of an 800G FlexO-8-RS interface. It can be seen that it is divided into three parts (the part reusing 100G FlexO, the part with two flows based on 400G FlexO-4-RS and the part reusing [IEEE 802.3df] 800GE PCS/FEC).

The processes of the scrambler/descrambler and AM insertion/removal are based on 400G FlexO-4-RS in each flow with the same scrambler and different AMs. Before the scrambler in the source and after the descrambler in the sink, the formation of the two 400G flows is a new design (i.e., FlexO instances #1, #2, #3, #4 are 10-bit interleaved into 400G Flow #0 and FlexO instances #5, #6, #7, #8 are 10-bit interleaved into 400G Flow #1) and the rest are completely the same processes as 100G FlexO.

In the part reusing [IEEE 802.3df] 800GE PCS lower-part and FEC, it completely reuses all those processes. 800G FlexO uses 2 × 200G KP4-FEC in each 400G flow.

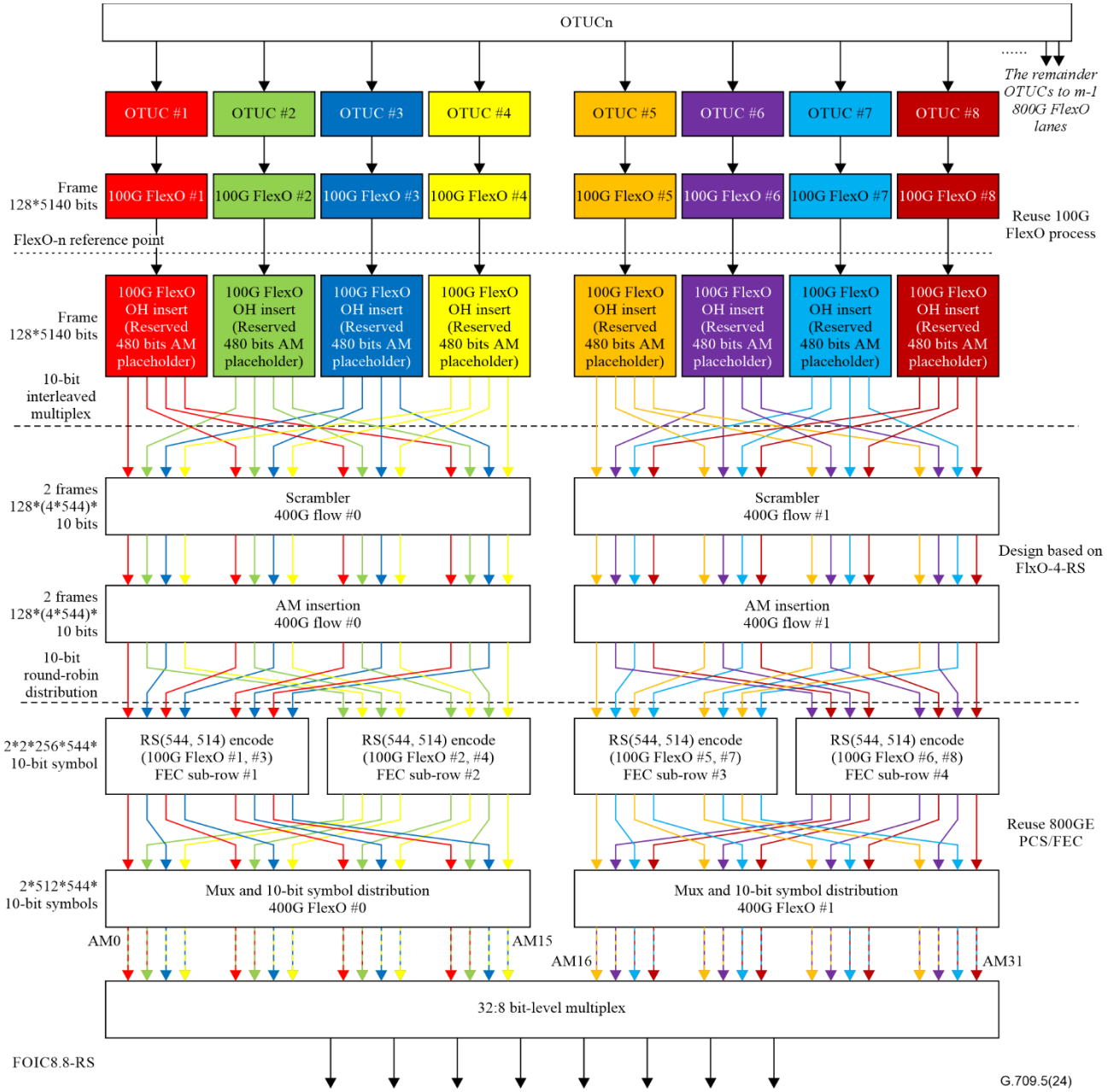

Figure 14-4 – 800G FlexO-8-RS interface transmit processes

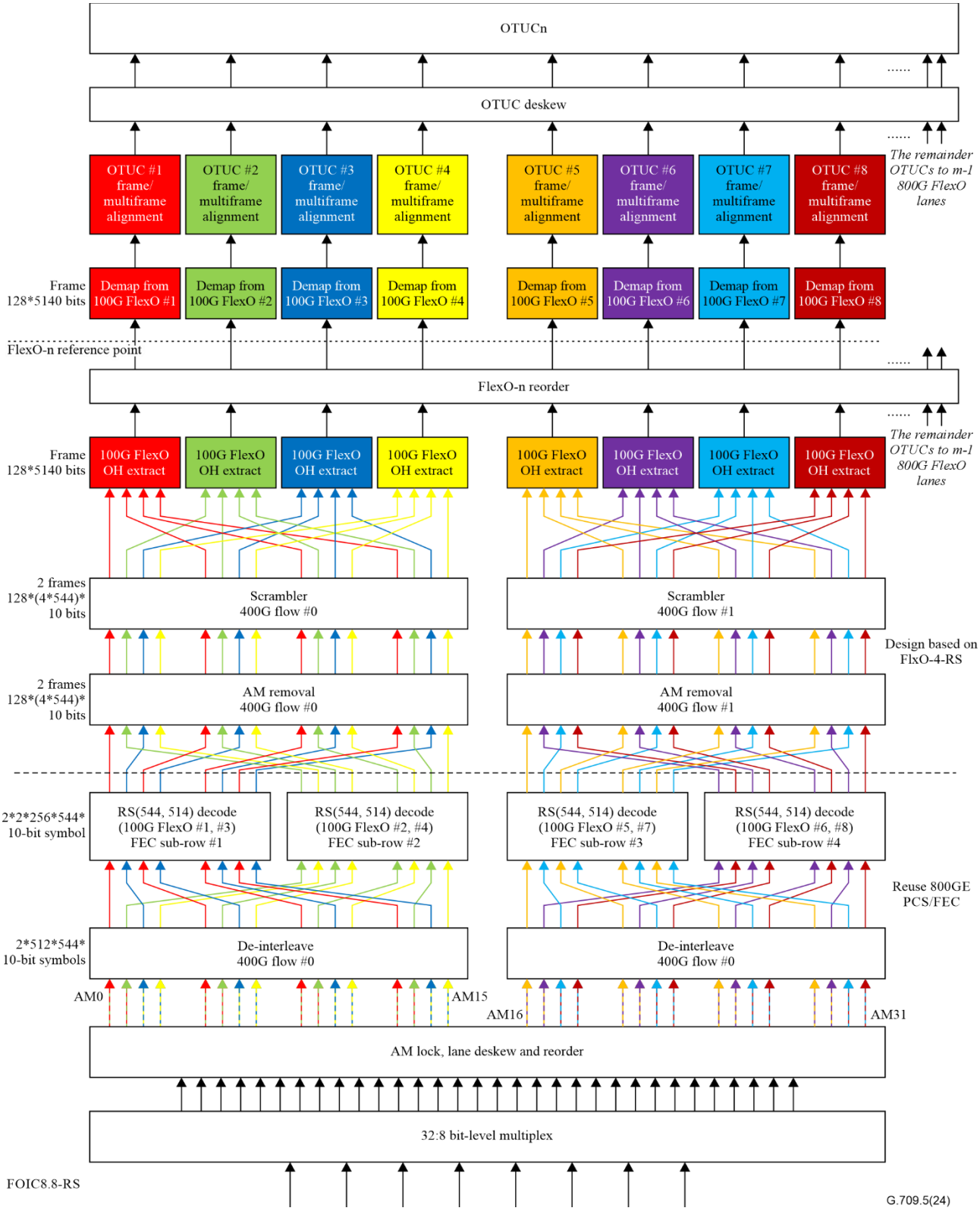

Figure 14-5 – 800G FlexO-8-RS interface receives processes

Annex A

Forward error correction for FlexO-x-RS using 10-bit RS(544,514) codecs

(This annex forms an integral part of this Recommendation.)

A.1 Generic processing and common code structure

The FlexO-x-RS FEC scheme is the RS(544,514) from [IEEE 802.3] for 100GBASE-R, 200GBASE-R, 400GBASE-R and 800GBASE-R interfaces from [IEEE 802.3df].

The FEC scheme employs a Reed-Solomon code operating over the Galois field GF(2^{10}), where the symbol size is 10 bits.

A Reed-Solomon code is denoted as RS(n,k) where k represents the number of message symbols to generate 2t parity symbols, which are appended to the message of total length n. The corresponding formula is n=k+2t, specifically:

n = 544

k = 514

t = 15

The FEC encoder processes 20 × 257-bit data blocks, resulting in the 5 140 data bits in the FEC codeword (row) and generates 20 × 15 = 300 bits of FEC parity.

The generator polynomial of the code is given by:

$$G(z) = \prod_{i=0}^{29}(z - \alpha^i)$$

where α is a root of the binary primitive polynomial $x^{10} + x^3 + 1$.

The FEC code word (see Figure A.1) consists of 10-bit information blocks and parity blocks (FEC redundancy) and is represented by the polynomial:

$$C(z) = I(z) + R(z)$$

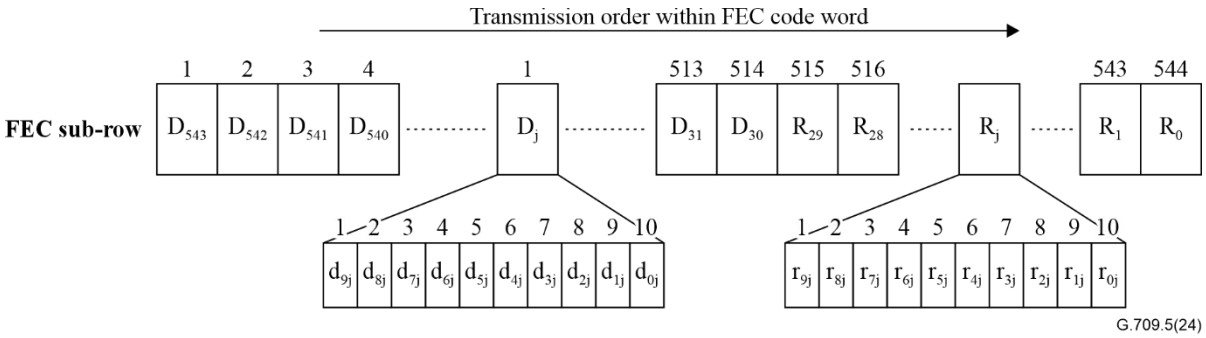

Figure A.1 – RS(544,514) FEC code word

10-bit information blocks are represented by:

$$I(z) = D_{543} \cdot z^{543} + D_{542} \cdot z^{542} + \cdots + D_{30} \cdot z^{30}$$

Where D_j (j = 30 to 1 087) is the 10-bit information block represented by an element out of GF(256) and:

$$D_j = d_{9j} \cdot \alpha^9 + d_{8j} \cdot \alpha^8 + \cdots + d_{1j} \cdot \alpha^1 + d_{0j}$$

Bit d_{9j} is the MSB and d_{0j} the LSB of the 10-bit information block.

D_{543} corresponds to 10-bit block 1 in the FEC sub-row and D_{30} to 10-bit block 514.

10-bit parity blocks are represented by:

$$R(z) = R_{29} \cdot z^{29} + R_{28} \cdot z^{28} + \cdots + R_1 \cdot z^1 + R_0$$

Where R_j (j = 0 to 29) is the 10-bit parity block represented by an element out of GF(2^{10}) and:

$$R_j = r_{9j} \cdot \alpha^9 + r_{8j} \cdot \alpha^8 + \cdots + r_{1j} \cdot \alpha^1 + r_{0j}$$

Bit r_{9j} is the MSB and r_{0j} the LSB of the 10-bit parity block.

R_{29} corresponds to the 10-bit block 515 in the FEC sub-row and R_0 to 10-bit block 544.

R(z) is calculated by:

$$R(z) = I(z) \bmod G(z)$$

where "mod" is the modulo calculation over the code generator polynomial *G(z)* with elements out of the GF(2^{10}). Each element in the GF(2^{10}) is defined by the binary primitive polynomial $x^{10} + x^3 + 1$.

The Hamming distance of the RS(544,514) code is $d_{min} = 31$. The code can correct up to 15 symbol errors in the FEC code word when it is used for error correction. The FEC can detect up to 30 symbol errors in the FEC code word when it is used for error detection capability only.

A.2 FlexO-1-RS FEC codeword adaptation

A 100G FlexO-1-RS FEC codeword occupies one row in the 100G FlexO-1-RS frame. The 100G FlexO-1-RS frame allocates 300 bits for FEC parity, per row, as shown in Figure 11-1.

NOTE – The 100G FlexO-1-RS FEC is based on RS(544,514), as specified in clause 91 of [IEEE 802.3] for 100GBASE-KP4 interfaces.

A.3 FlexO-2-RS and FlexO-4-RS FEC codeword adaptation

NOTE 1 – The FlexO-x-RS FEC (x = 2,4) is based on RS(544,514), as specified in clause 119 of [IEEE 802.3] for 200GBASE-R and 400GBASE-R interfaces.

The forward error correction for the FlexO-x-RS uses 10-bit interleaved codecs using a Reed-Solomon RS(544,514) code. The RS(544,514) code is a non-binary code (the FEC algorithm operates on 10-bit symbols) and belongs to the family of systematic linear cyclic block codes.

For FEC processing, a FlexO-x-RS row is separated into two sub-rows using 10-bit-interleaving as shown in Figure A.2. Each FEC encoder/decoder processes one of these sub-rows. The 10-bit FEC parity check blocks are calculated over the 10-bit information blocks 1 to 514 of each sub-row and transmitted in 10-bit blocks 515 to 544 of the same sub-row.

NOTE 2 – After the FEC encoding and before distribution to the logical lanes, the two sub-rows are 10-bit re-interleaved following the procedure described in clause 119.2.4.7 of [IEEE 802.3] that is not round-robin interleaving.

NOTE 3 – In [IEEE 802.3], sub-row #1 is referred to as A and sub-row #2 is referred to as B.

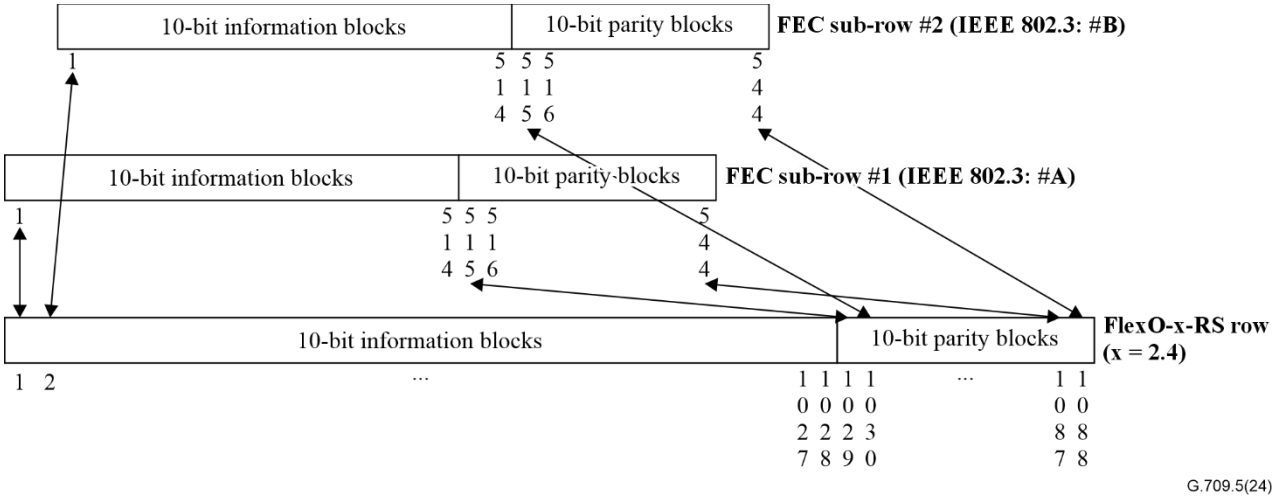

Figure A.2 – FEC sub-rows

The 10-bit blocks in a FlexO-x-RS row belonging to FEC sub-row X (X = 1,2) are defined by: $X + 10 \times (i - 1)$ (for i = 1 ... 544).

A.4 FlexO-8-RS FEC codeword adaptation

NOTE – The FlexO-8-RS FEC is based on RS(544,514), as specified in clause 172 of [IEEE 802.3df] for 800GBASE-R interfaces.

The FlexO-8-RS FEC encoder and decoder processes are illustrated in Figures 14-4 and 14-5, respectively. The encoder (decoder) process is composed of a pair of 400G RS encoders (decoders) operating on 400G flow #0 and 400G flow #1. The 400G RS encoder (decoder) is described in clause A.3.

Bibliography

[b-OIF CEI] Optical Internetworking Forum Implementation Agreement OIF-CEI-05.1 (2022), *Common Electrical I/O (CEI) – Electrical and Jitter Interoperability agreements for 6G+ bps, 11G+ bps, 25G+ bps, 56G+ bps and 112G+ bps I/O*.
<https://www.oiforum.com/wp-content/uploads/OIF-CEI-5.0.pdf>

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Published in Switzerland
Geneva, 2024