INTERNATIONAL TELECOMMUNICATION UNION

# ITU-T

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

# G.798

**Amendment 1**
(06/2002)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital terminal equipments – Other terminal equipment

# Characteristics of optical transport network hierarchy equipment functional blocks

## Amendment 1

ITU-T Recommendation G.798 (2002) – Amendment 1

ITU-T G-SERIES RECOMMENDATIONS

**TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS**

| | |
|---|---|
| INTERNATIONAL TELEPHONE CONNECTIONS AND CIRCUITS | G.100–G.199 |
| GENERAL CHARACTERISTICS COMMON TO ALL ANALOGUE CARRIER-TRANSMISSION SYSTEMS | G.200–G.299 |
| INDIVIDUAL CHARACTERISTICS OF INTERNATIONAL CARRIER TELEPHONE SYSTEMS ON METALLIC LINES | G.300–G.399 |
| GENERAL CHARACTERISTICS OF INTERNATIONAL CARRIER TELEPHONE SYSTEMS ON RADIO-RELAY OR SATELLITE LINKS AND INTERCONNECTION WITH METALLIC LINES | G.400–G.449 |
| COORDINATION OF RADIOTELEPHONY AND LINE TELEPHONY | G.450–G.499 |
| TESTING EQUIPMENTS | G.500–G.599 |
| TRANSMISSION MEDIA CHARACTERISTICS | G.600–G.699 |
| DIGITAL TERMINAL EQUIPMENTS | G.700–G.799 |
| General | G.700–G.709 |
| Coding of analogue signals by pulse code modulation | G.710–G.719 |
| Coding of analogue signals by methods other than PCM | G.720–G.729 |
| Principal characteristics of primary multiplex equipment | G.730–G.739 |
| Principal characteristics of second order multiplex equipment | G.740–G.749 |
| Principal characteristics of higher order multiplex equipment | G.750–G.759 |
| Principal characteristics of transcoder and digital multiplication equipment | G.760–G.769 |
| Operations, administration and maintenance features of transmission equipment | G.770–G.779 |
| Principal characteristics of multiplexing equipment for the synchronous digital hierarchy | G.780–G.789 |
| **Other terminal equipment** | **G.790–G.799** |
| DIGITAL NETWORKS | G.800–G.899 |
| DIGITAL SECTIONS AND DIGITAL LINE SYSTEM | G.900–G.999 |
| QUALITY OF SERVICE AND PERFORMANCE | G.1000–G.1999 |
| TRANSMISSION MEDIA CHARACTERISTICS | G.6000–G.6999 |
| DIGITAL TERMINAL EQUIPMENTS | G.7000–G.7999 |
| DIGITAL NETWORKS | G.8000–G.8999 |

*For further details, please refer to the list of ITU-T Recommendations.*

# ITU-T Recommendation G.798

## Characteristics of optical transport network hierarchy equipment functional blocks

## Amendment 1

**Summary**

This amendment contains extensions to the first version (2002) of ITU-T Rec. G.798, related to the addition of: Time division multiplexing of ODUj[/i] into ODUk.

**Source**

Amendment 1 to ITU-T Recommendation G.798 (2002) was prepared by ITU-T Study Group 15 (2001-2004) and approved under the WTSA Resolution 1 procedure on 13 June 2002.

## FOREWORD

The International Telecommunication Union (ITU) is the United Nations specialized agency in the field of telecommunications. The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of ITU. ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSA Resolution 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

## NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

## INTELLECTUAL PROPERTY RIGHTS

ITU draws attention to the possibility that the practice or implementation of this Recommendation may involve the use of a claimed Intellectual Property Right. ITU takes no position concerning the evidence, validity or applicability of claimed Intellectual Property Rights, whether asserted by ITU members or others outside of the Recommendation development process.

As of the date of approval of this Recommendation, ITU had not received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementors are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database.

## CONTENTS

# ITU-T Recommendation G.798

## Characteristics of optical transport network hierarchy equipment functional blocks

## Amendment 1

### 1 Introduction

This amendment contains extensions to the first version (2002) of ITU-T Rec. G.798, related to the addition of:

– Time division multiplexing of ODUj[/i] into ODUk.

### 2 Additions

#### 2.1 Clause 1

*Replace Figure 1-2 with the following figure which includes the ODUkP/ODU[i]j adaptation functions:*

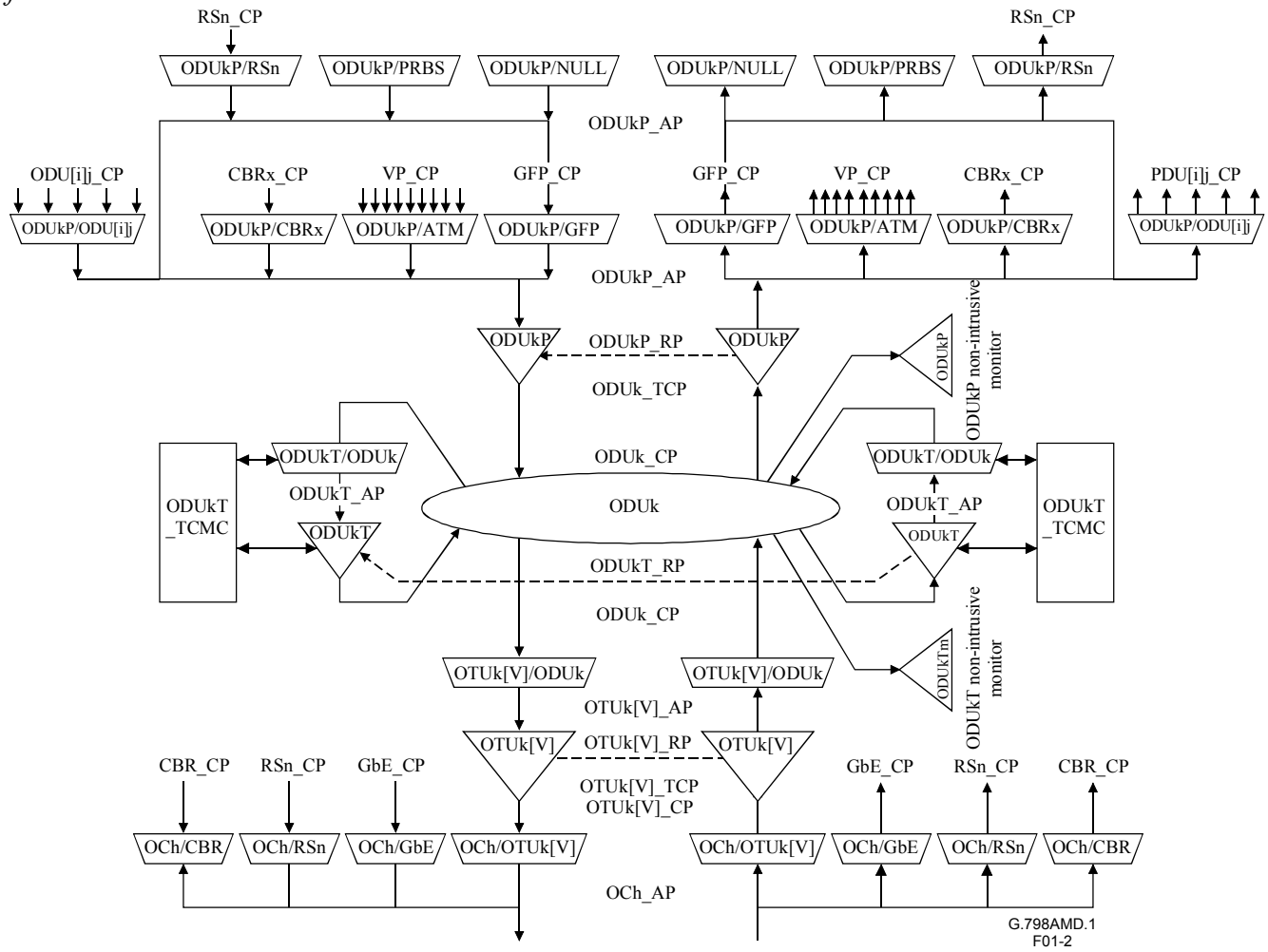


**Figure 1-2/G.798 – OTN common atomic functions**

## 2.2 Clause 4

*Add the following abbreviations alphabetically:*

| | |
|---|---|
| AcMSI | Accepted MSI |
| ExMSI | Expected MSI |
| LOFLOM | Loss of frame and multiframe |
| MSI | Multiplex Structutre Identifier |
| MSIM | Multiplex Structutre Identifier Mismatch |
| ODUi | Optical Data Unit of level i |
| ODU[i]j | Optical Data Unit of level j and i (i is optional; i<j) |
| ODUj | Optical Data Unit of level j |
| ODUj[/i] | Optical Data Unit of level j or i (i is optional; i<j) |
| TxMSI | Transmitted MSI |

## 2.3 Clause 6.2.5.3

*Add the following new clause for the ODUj[/i]loss of frame and multiframe defect detection:*

### 6.2.5.3 ODUj[/i] Loss of Frame and Multiframe defect (dLOFLOM)

ODUj[/i]dLOFLOM is generated based on the state of the frame alignment process defined in 8.2.3.

If the frame alignment process is in the out-of-frame (OOF) state for 3 ms, dLOFLOM shall be declared. To provide for the case of intermittent OOFs, the integrating timer shall not be reset to zero until an in-frame (IF) condition persists continuously for 3 ms. dLOFLOM shall be cleared when the IF state persists continuously for 3 ms.

## 2.4 Clause 6.2.9

*Add the following new clause for the multiplex structure identifier mismatch supervision:*

### 6.2.9 Multiplex Structure Identifier Mismatch supervision (dMSIM)

#### 6.2.9.1 dMSIM at the ODUkP layer

If automatic configuration of the multiplex structure is supported and activated (AutoMS = true), dMSIM shall be declared if the accepted multiplex structure identifier (AcMSI) has a invalid value that is not supported by the specific adaptation function (e.g. wrong tributary port, wrong ODU type). dMSIM shall be cleared if the AcMSI has a valid value.

If automatic configuration of the multiplex structure is not supported or not activated (AutoMS = false), dMSIM shall be declared if the AcMSI is not equal to the expected multiplex structure identifier (ExMSI). dMSIM shall be cleared if the AcMSI is equal to the ExMSI. ExMSI is either a fixed value or configured via the management interface. For details see 14.3.7.2 (ODUkP/ODU[i]j_A_Sk function).

For the AcMSI acceptance process see 8.7.2.

## 2.5 Clause 8.2.3

*Add the following new clause for the ODUj[/i] frame and multiframe alignment process:*

### 8.2.3 ODUj[/i] frame and multiframe alignment

The ODUj[/i] frame and multiframe alignment shall be found by searching for the framing pattern (OA1, OA2 FAS bytes) and checking the multiframe sequence (MFAS byte) (see ITU-T Rec. G.709/Y.1331) contained in the ODUj[/i] frame.

In the out-of-frame state the framing pattern searched for shall be the full set of the OA1 and OA2 bytes. The in-frame (IF) shall be entered if this set is found and confirmed one frame period later and an error-free multiframe sequence is found in the MFAS bytes of the two frames.

In the in-frame state (IF) the frame alignment signal shall be continuously checked with the presumed frame start position and the expected multiframe sequence. The framing pattern checked for shall be the OA1OA2 pattern (bytes 3 and 4 of the first row of the ODUj[/i] frame). The out of frame state (OOF) shall be entered if this subset is not found at the correct position in 5 consecutive frames or the received MFAS does not match with the expected multiframe number in 5 consecutive frames.

The frame and multiframe start shall be maintained during the OOF state.

## 2.6 Clause 8.7.2

*Add the following new clause for the multiplex structure indication acceptance process:*

### 8.7.2 Multiplex Structure Identifier (MSI) acceptance process

A new multiplex structure identifier MSI (AcMSI) is accepted if a new consistent value is received in the MSI bytes of the PSI overhead (PSI[2..5] for ODU2, PSI[2..17] for ODU3) in X consecutive multiframes. X shall be 3.

## 2.7 Clause 14.3.7

*Add the following new clause for the ODUkP/ODU[I]j adaptation functions and renumber subsequent figures and tables, and references to figures and tables, accordingly:*

### 14.3.7 ODUkP to ODU[i]j adaptation function (ODUkP/ODU[i]j_A)

The ODUkP to ODU[i]j adaptation functions perform the adaptation between the ODUkP (k = 2, 3) layer adapted information and the characteristic information of ODUj (j = 1, 2; j < k) [and ODUi (i = 1; i<j)] signals.

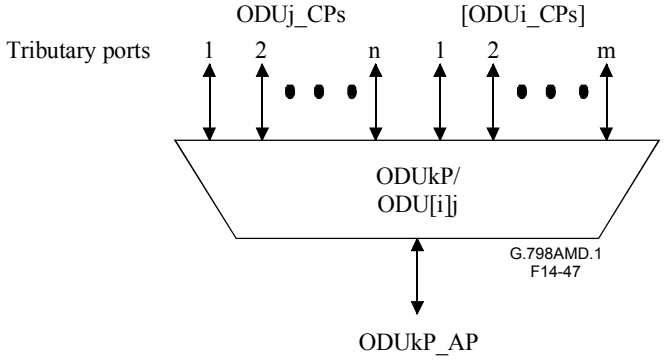


**Figure 14-47/G.798 – ODUkP/ODU[i]j_A function**

Four different types of functions are possible:

– the ODU2P/ODU1_A performs multiplexing/demultiplexing of 4 ODU1 into an ODU2;

– the ODU3P/ODU1_A performs multiplexing/demultiplexing of 16 ODU1 into an ODU3;

– the ODU3P/ODU2_A performs multiplexing/demultiplexing of 4 ODU2 into an ODU3;

– the ODU3P/ODU12_A performs multiplexing/demultiplexing of ODU1 and ODU2 into an ODU3.

The maximum number of tributary ports depends on the specific function type as listed in Table 14-18. Note that for the ODU3P/ODU12_A function, only a subset of the tributary signals can be active and transported via the ODU3 at a time. The number of active ODU1 ports, plus four times the number of active ODU2 ports, is limited to 16. The multiplex structure identifier (MSI) defines the configuration in this case.

Note that the ODU3P/ODU12_A function can interwork with the ODU2P/ODU1_A, ODU3P/ODU1_A and ODU3P/ODU2_A functions as it supports all related multiplex structures.

**Table 14-18/G.798 – ODUkP/ODU[i]j_A tributary ports**

| Function type | n ports | m ports |
|---|---|---|
| ODU2P/ODU1_A | 4 ODU1 | – |
| ODU3P/ODU1_A | 16 ODU1 | – |
| ODU3P/ODU2_A | 4 ODU2 | – |
| ODU3P/ODU12_A | 16 ODU1 | 4 ODU2 |

#### 14.3.7.1 ODUkP to ODU[i]j adaptation source function (ODUkP/ODU[i]j_A_So)

The ODUkP/ODU[i]j_A_So function creates the ODUk signal from a free running clock. It asynchronously maps the ODUj [and ODUi] client signal from the ODUj_[and ODUi] CPs into ODTUjk[/ik] including justification control (JC) information. The ODTUjk[/ik] are multiplexed into the payload area of the OPUk. It adds OPUk Overhead (RES, PT, MSI) and default ODUk Overhead.

The information flow and processing of the ODUkP/ODU[i]j_A_So function is defined with reference to Figures 14-48 and 14-49.

**Symbol**

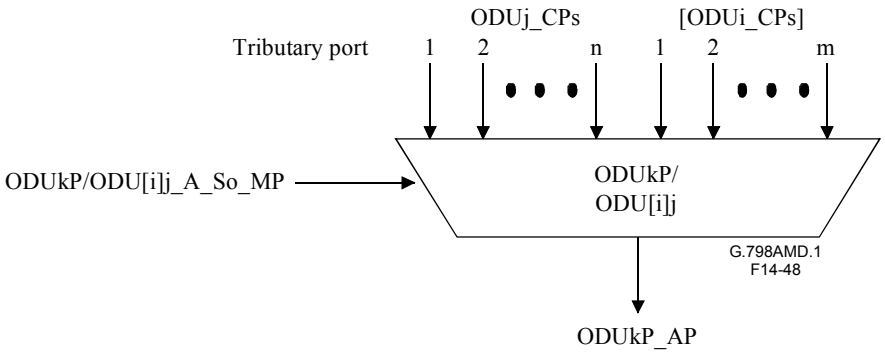


**Figure 14-48/G.798 – ODUkP/ODU[i]j_A_So function**

**Interfaces**

**Table 14-19/G.798 – ODUkP/ODU[i]j_A_So inputs and outputs**

| Input(s) | Output(s) |
|---|---|
| n x ODUj_CP:<br>ODUj_CI_CK<br>ODUj_CI_D<br>ODUj_CI_FS<br>ODUj_CI_MFS<br>m x ODUi_CP: (Note)<br>ODUi_CI_CK<br>ODUi_CI_D<br>ODUi_CI_FS<br>ODUi_CI_MFS<br>ODUkP/ODU[i]j_A_So_MP:<br>ODUkP/ODU[i]j_A_So_MI_Active<br>ODU3P/ODU12_A_So_MI_TxMSI (Note) | ODUkP_AP:<br>ODUkP_AI_CK<br>ODUkP_AI_D<br>ODUkP_AI_FS<br>ODUkP_AI_MFS |
| NOTE – for ODU3P/ODU12_A_So only | |

**Processes**

*Activation*

The ODUkP/ODU[i]j_A_So function shall access the access point when it is activated (MI_Active is true). Otherwise, it shall not access the access point.

The processes associated with the ODUkP/ODU[i]j_A_So function are specific processes for each ODUj[i/]_CP and common processes for the compound (multiplexed) signal as depicted in Figure 14-49.

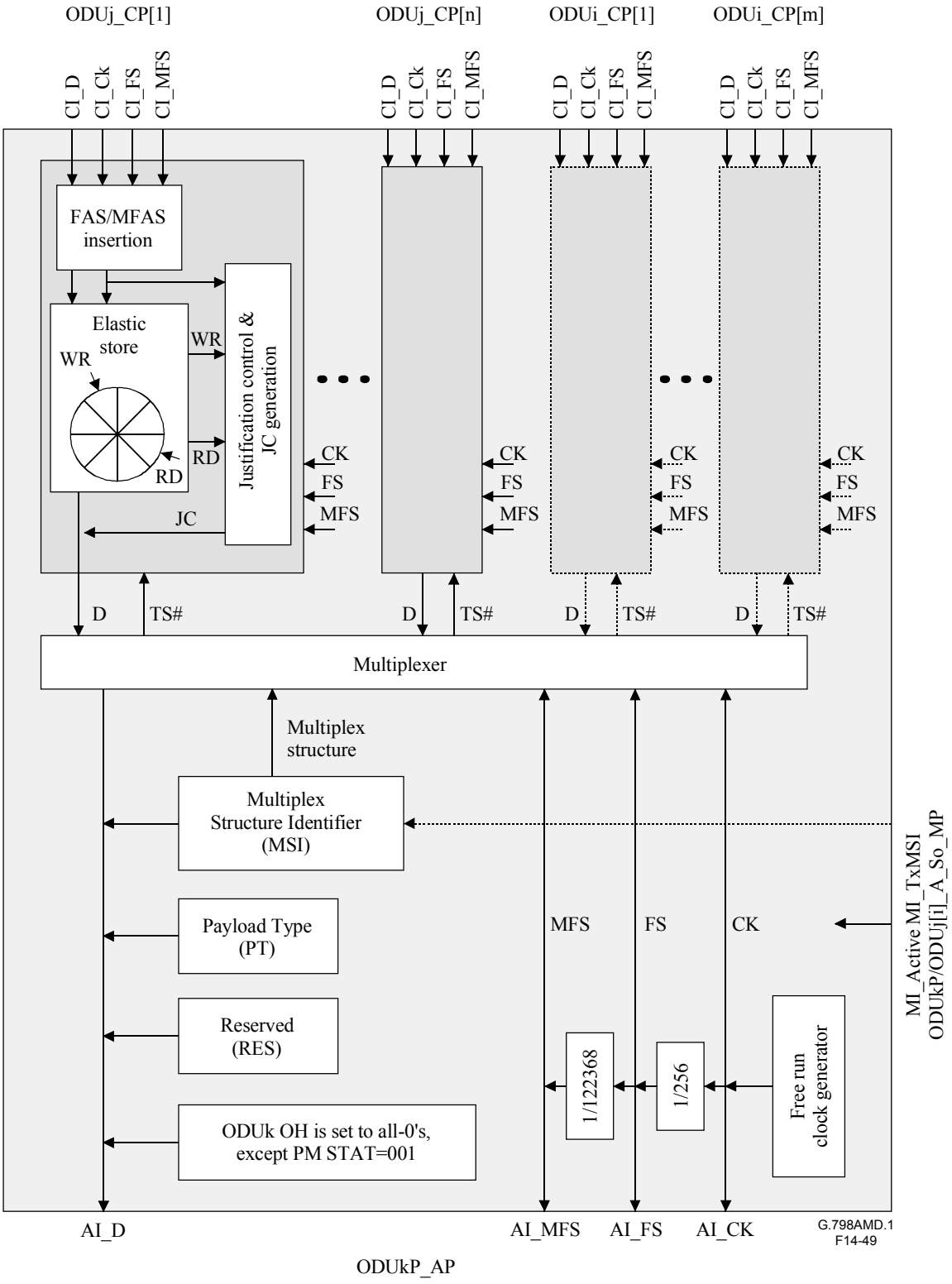


**Figure 14-49/G.798 – ODUkP/ODU[i]j_A_So processes**

## Specific processes

The specific processes are performed independently for each ODUj [and ODUi] client signal that is multiplexed into the ODUk. The specific processes perform the mapping of the ODUj[/i] into an ODTUjk[/ik].

**FAS/MFAS insertion**: The function shall extend the ODUj[/i] with the frame alignment overhead (FAS and MFAS) in row 1 bytes 1 to 7 as described in 15.6.2/G.709/Y.1331. Byte 8 to14 of row 1 are set to all-0's.

**Mapping, frequency justification and bit rate adaptation**: The function shall provide an elastic store (buffer) process for the ODUj[/i] client signal. The data signal ODUj[/i]_CI shall be written into the buffer under control of the associated input clock. The data shall be read out of the buffer and written onto the D, NJO, PJO1 and PJO2 bytes of the selected ODTUjk[/ik] frame under control of the ODUk clock and justification decisions as defined in 19.5/G.709/Y.1331.

A justification decision shall be performed every fourth frame for the ODTU12, every sixteenth frame for the ODTU13 and four times every sixteen frames for the ODTU23. Each justification decision results in a corresponding double positive, positive, negative or no justification action. Upon a double positive justification action, the reading of 2 data bytes out of the buffer shall be cancelled once. No ODUj[/i] data shall be written onto the PJO2, PJO1 and NJO byte. Upon a positive justification action, the reading of 1 data byte out of the buffer shall be cancelled once. No ODUj[/i] data shall be written onto the PJO1 and NJO byte and data shall be written onto the PJO2 byte. Upon a negative justification action, 1 extra data byte shall be read once out of the buffer. ODUj[/i] data shall be written onto the PJO2, PJO1 and NJO byte. If no justification action is to be performed, ODUj[/i] data shall be written onto the PJO2 and PJO1 byte and no ODUj[/i] data shall be written onto the NJO byte. The ODUk frame that contains the PJO2, PJO1 and NJO bytes depends on the time slot[s] of the ODTUjk[/ik].

The justification decisions determine the phase error introduced by the function.

**Buffer size**: In the presence of jitter as specified by ITU-T Rec. G.8251 and a frequency within the range $(239/(239–j[/i])) * 4^{(j[/i]–1)} * 2\,488\,320$ kHz ± 20 ppm, this mapping process shall not introduce any errors. The maximum buffer hysteresis, and therefore the maximum phase error introduced, shall be as listed in Table 14-20.

**Table 14-20/G.798 – Maximum buffer hysteresis**

| Mapping | Maximum buffer hysteresis |
|---|---|
| ODU1 → ODU2 or ODU3 | 2 bytes |
| ODU2 → ODU3 | 8 bytes |

**JC**: The function shall generate the justification control bits based on the justification decision (double positive, positive, negative, none) according the specification in 19.5/G.709/Y.1331. It shall insert the justification control bits in bit 7 and 8 of all three JC bytes of the frame in which the justification is performed. The remaining (RES) bits of the JC byte shall be set to all-0's. The ODUk frame that contains the JC bytes depends on the time slot[s] of the ODTUjk[/ik].

**Common processes**

**Clock and (Multi) Frame Start signal generation**: The function shall generate a local ODUk clock (ODUkP_AI_CK) of "$(239/(239–k)) * 4^{(k–1)} * 2\,488\,320$ kHz ± 20 ppm" from a free running oscillator. The clock parameters, including jitter and wander requirements, as defined in Annex A/G.8251 (ODCa clock) apply.

The function shall generate the (multi) frame start reference signals AI_FS and AI_MFS for the ODUk signal. The AI_FS signal shall be active once per 122 368 clock cycles. AI_MFS shall be active once every 256 frames.

**Multiplexing**: The function assigns the individual ODTUjk[/ik] to specific times slots of the OPUk payload area as defined by the multiplex structure (see 19.3 and 19.4.1/G.709/Y.1331.

**MSI**: The function shall insert the TxMSI into the MSI byte positions of the PSI overhead as defined in 19.4/G.709/Y.1331. The TxMSI value and as such the multiplex structure is either fixed or configurable via MI_TxMSI as shown in Table 14-21.

**PT**: The function shall insert code "0010 0000" (ODU multiplex structure) into the PT byte position of the PSI overhead as defined in 15.9.2.1/G.709/Y.1331.

**RES**: The function shall insert all-0's into the RES bytes.

All other bits of the ODUk overhead should be sourced as "0"s, except the ODUk-PM STAT field which should be set to the value "normal path signal" (001).

**Table 14-21/G.798 – Multiplex structure configuration and TxMSI values**

| Function | Multiplex structure | TxMSI value for fixed multiplex structure |
|---|---|---|
| ODU2P/ODU1_A | Fixed<br>4 ODU1 → ODU2 | 00 000000<br>00 000001<br>00 000010<br>00 000011 |
| ODU3P/ODU1_A | Fixed<br>16 ODU1 → ODU3 | 00 000000<br>00 000001<br>00 000010<br>00 000011<br>00 000100<br>00 000101<br>00 000110<br>00 000111<br>00 001000<br>00 001001<br>00 001010<br>00 001011<br>00 001100<br>00 001101<br>00 001110<br>00 001111 |
| ODU3P/ODU2_A | Fixed<br>4 ODU2 → ODU3 | 01 000000<br>01 000001<br>01 000010<br>01 000011<br>01 000000<br>01 000001<br>01 000010<br>01 000011<br>01 000000<br>01 000001<br>01 000010<br>01 000011<br>01 000000<br>01 000001<br>01 000010<br>01 000011 |
| ODU3P/ODU12_A | Configured via MI_TxMSI | – |

**Defects**: None.

**Consequent Actions**: None.

**Defect Correlations**: None.

**Performance Monitoring**: None.

#### 14.3.7.2 ODUkP to ODU[i]j adaptation sink function (ODUkP/ODU[i]j_A_Sk)

The ODUkP/ODU[i]j_A_Sk function extracts the OPUk Overhead (PT, MSI, and RES) and monitors the reception of the correct payload type. It demultiplexes the individual ODTUjk[/ik] from the payload area of the OPUk and recovers the ODUj[/i] signals using the justification control information (JC overhead). It determines the frame and multi-frame structure of the ODUj[/I].

The information flow and processing of the ODUkP/ODU[i]j_A_Sk function is defined with reference to Figures 14-50 and 14-51.

**Symbol**

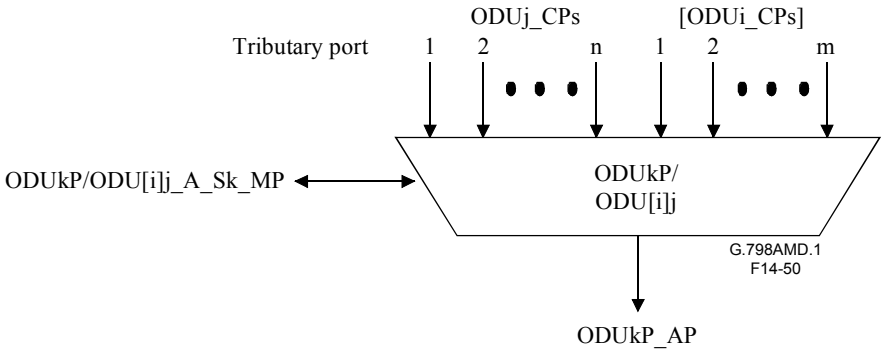


**Figure 14-50/G.798 – ODUkP/ODU[i]j_A_Sk function**

**Interfaces**

**Table 14-22/G.798 – ODUkP/ODU[i]j_A_Sk inputs and outputs**

| Input(s) | Output(s) |
|---|---|
| ODUkP_AP: | n x ODUj_CP: |
| ODUkP_AI_CK<br>ODUkP_AI_D<br>ODUkP_AI_FS<br>ODUkP_AI_MFS<br>ODUkP_AI_TSF | ODUj_CI_CK<br>ODUj_CI_D<br>ODUj_CI_FS<br>ODUj_CI_MFS<br>ODUj_CI_SSF |
| ODUkP/ODU[i]j_A_Sk_MP: | m x ODUi_CP: (Note) |
| ODUkP/ODU[i]j_A_Sk_MI_Active<br>ODU3P/ODU12_A_Sk_MI_AutoMS (Note)<br>ODU3P/ODU12_A_Sk_MI_ExMSI (Note) | ODUi_CI_CK<br>ODUi_CI_D<br>ODUi_CI_FS<br>ODUi_CI_MFS<br>ODUi_CI_SSF |
| | ODUkP/ODU[i]j_A_Sk_MP: |
| | ODUkP/ODU[i]j _A_Sk_MI_cPLM<br>ODUkP/ODU[i]j _A_Sk_MI_cMSIM<br>ODUkP/ODU[i]j _A_Sk_MI_AcPT<br>n x ODUkP/ODUj_A_Sk_MI_cLOFLOM<br>m x ODUkP/ODUi_A_Sk_MI_cLOFLOM (Note) |
| NOTE – for ODU3P/ODU12_A_Sk only | |

## Processes

*Activation*

The ODUkP/ODU[i]j_A_Sk function shall access the access point when it is activated (MI_Active is true). Otherwise, it shall not access the access point.

The processes associated with the ODUkP/ODU[i]j_A_Sk function are specific processes for each ODUj[i/]_CP and common processes for the compound (multiplexed) signal as depicted in Figure 14-51.

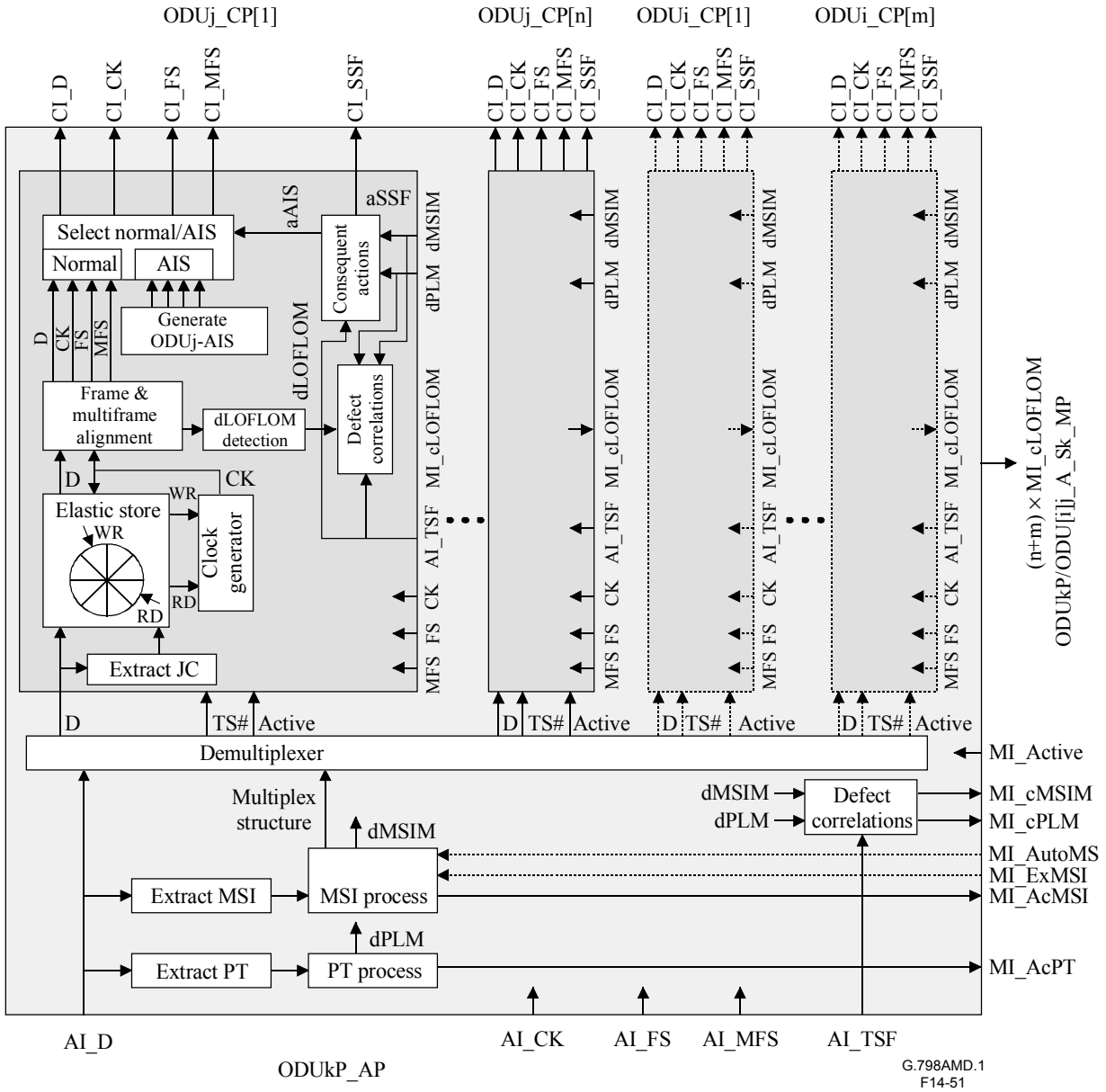


**Figure 14-51/G.798 – ODUkP/ODU[i]j_A_Sk processes**

## Common processes

**PT**: The function shall extract the PT byte from the PSI overhead as defined in 8.7.2. The accepted PT value is available at the MP (MI_AcPT) and is used for PLM defect detection.

**MSI**: The function shall extract the MSI from the PSI overhead as defined in 8.7.2. The accepted MSI (AcMSI) is available at the MP (MI_AcMSI). If MI_AutoMSI is supported and true the AcMSI defines the multiplex structure. Otherwise the multiplex structure is defined by ExMSI, which is either fixed or configurable via MI_ExMSI as shown in Table 14-23.

**RES**: The value in the RES bytes shall be ignored.

**Demultiplexing**: The function activates the ODTUjk[/ik] and assigns the times slots of the ODUk payload area to the individual ODTUjk[/ik] as defined by the multiplex structure (see 19.3 and 19.4.1/G.709/Y.1331).

**Table 14-23/G.798 – Multiplex structure configuration and ExMSI values**

| Function | Multiplex structure | ExMSI value for fixed multiplex structure |
|---|---|---|
| ODU2P/ODU1_A | Fixed<br>4 ODU1 → ODU2<br>AutoMS not supported | 00 000000<br>00 000001<br>00 000010<br>00 000011 |
| ODU3P/ODU1_A | Fixed<br>16 ODU1 → ODU3<br>AutoMS not supported | 00 000000<br>00 000001<br>00 000010<br>00 000011<br>00 000100<br>00 000101<br>00 000110<br>00 000111<br>00 001000<br>00 001001<br>00 001010<br>00 001011<br>00 001100<br>00 001101<br>00 001110<br>00 001111 |
| ODU3P/ODU2_A | Fixed<br>4 ODU2 → ODU3<br>AutoMS not supported | 01 000000<br>01 000001<br>01 000010<br>01 000011<br>01 000000<br>01 000001<br>01 000010<br>01 000011<br>01 000000<br>01 000001<br>01 000010<br>01 000011<br>01 000000<br>01 000001<br>01 000010<br>01 000011 |
| ODU3P/ODU12_A | Configured via MI_ExMSI or AcMSI if MI_AutoMS = true | – |

**Specific processes**

The specific processes are performed independently for each ODUj [and ODUi] client signal that is multiplexed into the ODUk. The specific processes recover the ODUj[/i] from the ODTUjk[/ik].

**JC**: The function shall interpret the justification control information in bit 7 and 8 of the JC bytes as defined in 19.5/G.709/Y.1331 in order to determine the justification action (double positive, positive, negative, none) for the current frame. A 2 out of 3 majority decision is used. RES bits in the JC bytes shall be ignored. The ODUk frame that contains the JC bytes depends on the time slot[s] of the ODTUjk[/ik].

**Demapping, CBR clock generation**: The function shall provide an elastic store (buffer) process. The ODUj[/i] data shall be written into the buffer from the D, NJO, PJO1 and PJO2 bytes in the ODTUjk[/ik] frame. The information extraction of the PJO2, PJO1 and NJO bytes shall be under control of the justification control information. The ODUj[/i] data (CI_D) shall be read out of the buffer under control of the ODUj[/i] clock (CI_CK).

Upon a double positive justification action, the writing of 2 data byte into the buffer shall be cancelled once. No ODUj[/i] data shall be read from the PJO2, PJO1 and NJO byte. Upon a positive justification action, the writing of 1 data byte into the buffer shall be cancelled once. No ODUj[/i] data shall be read from the PJO1 and NJO byte and data shall be read from the PJO2 byte. Upon a negative justification action, 1 extra data byte shall be written into the buffer once. ODUj[/i] data shall be read from the PJO2, PJO1 and NJO byte. If no justification action is to be performed, ODUj[/i] data shall be read from the PJO2 and PJO1 byte and no ODUj[/i] data shall be read from the NJO byte. The ODUk frame that contains the PJO2, PJO1 and NJO bytes depends on the time slot[s] of the ODTUjk[/ik].

**Smoothing & jitter limiting process**: The function shall provide for a clock smoothing and elastic store (buffer) process. The $(239/(239–j[/i])) * 4^{(j[/i]–1)} * 2\ 488\ 320$ kbit/s (k=1,2,3) data signal shall be written into the buffer under control of the associated (gapped) input clock (with a frequency accuracy within ± 20 ppm). The data signal shall be read out of the buffer under control of a smoothed (equally spaced) $(239/(239–j[/i])) * 4^{(j[/i]–1)} * 2\ 488\ 320$ kbit/s ± 20 ppm clock (the rate is determined by the ODUj[/i] signal at the input of the remote ODUkP/ODU[i]j_A_So).

The clock parameters, including jitter and wander requirements, as defined in Annex A/G.8251 (ODCp clock) apply.

**Buffer size**: In the presence of jitter as specified by ITU-T Rec. G.8251 and a frequency within the range $(239/(239–j[/i])) * 4^{(j[/i]–1)} * 2\ 488\ 320$ kbit/s ± 20 ppm, this justification process shall not introduce any errors.

Following a step in frequency of the $(239/(239–j[/i])) * 4^{(j[/i]–1)} * 2\ 488\ 320$ kbit/s signal transported (for example due to reception of ODUj[/i]_CI from a new ODUj[/i]_TT_So at the far end or removal of a ODU AIS signal with a frequency offset) there will be a maximum recovery time of X seconds after which this process shall not generate any bit errors. The value of X is for further study; a value of 1 second has been proposed.

**Frame & Multiframe alignment**: The function shall perform frame and multiframe alignment as described in 8.2.3.

**ODUj[/i]-AIS**: The function shall generate the ODUj[/i]–AIS signals as defined in ITU-T Rec. G.709/Y.1331. The clock, frame start and multiframes start shall be independent from the incoming clock. The clock has to be within $(239/(239–j[/i])) * 4^{(j[/i]–1)} * 2\ 488\ 320$ kHz ± 20 ppm. Jitter and wander requirements as defined in Annex A/G.8251 (ODCa clock) apply.

**Selector**: The normal signal may be replaced by the ODUj[/i]–AIS. ODUj[/i]–AIS is selected if aAIS is true.

**Defects**

The function shall detect for dPLM, dMSIM and dLOFLOM.

**dPLM**: see 6.2.4.1. The expected payload type is "0010 0000" (ODU multiplex structure) as defined in ITU-T Rec. G.709/Y.1331.

**dMSIM**: see 6.2.9.1

**dLOFLOM**: see 6.2.5.3. dLOFLOM is detected per active ODUj[/i].

**Consequent Actions**

for each ODUj[/i]:

aSSF ← AI_TSF or dPLM or dMSIM or dLOFLOM or (not Active)

for each ODUj[/i]:

aAIS ← AI_TSF or dPLM or dMSIM or dLOFLOM or (not Active)

On declaration of aAIS the function shall output an All-ONEs pattern/signal within 2 frames. On clearing of aAIS the All-ONEs pattern/signal shall be removed within 2 frames and normal data being output. The AIS clock, frame start and multiframe start shall be independent from the incoming clock, frame start and multiframe start. The AIS clock has to be within (239/(239–j[/i])) * $4^{(j[/i]-1)}$ * 2 488 320 kHz ± 20 ppm. Jitter and wander requirements as defined in Annex A/G.8251 (ODCa clock) apply.

**Defect Correlations**

cPLM ← dPLM and (not AI_TSF)

cMSIM ← dMSIM and (not dPLM) and (not AI_TSF)

for each ODUj[/i]:

cLOFLOM ← dLOFLOM and (not MSIM) and (not dPLM) and (not AI_TSF) and (Active)

**Performance monitoring**: None.

## SERIES OF ITU-T RECOMMENDATIONS

| | |
|---|---|
| Series A | Organization of the work of ITU-T |
| Series B | Means of expression: definitions, symbols, classification |
| Series C | General telecommunication statistics |
| Series D | General tariff principles |
| Series E | Overall network operation, telephone service, service operation and human factors |
| Series F | Non-telephone telecommunication services |
| **Series G** | **Transmission systems and media, digital systems and networks** |
| Series H | Audiovisual and multimedia systems |
| Series I | Integrated services digital network |
| Series J | Cable networks and transmission of television, sound programme and other multimedia signals |
| Series K | Protection against interference |
| Series L | Construction, installation and protection of cables and other elements of outside plant |
| Series M | TMN and network maintenance: international transmission systems, telephone circuits, telegraphy, facsimile and leased circuits |
| Series N | Maintenance: international sound programme and television transmission circuits |
| Series O | Specifications of measuring equipment |
| Series P | Telephone transmission quality, telephone installations, local line networks |
| Series Q | Switching and signalling |
| Series R | Telegraph transmission |
| Series S | Telegraph services terminal equipment |
| Series T | Terminals for telematic services |
| Series U | Telegraph switching |
| Series V | Data communication over the telephone network |
| Series X | Data networks and open system communications |
| Series Y | Global information infrastructure and Internet protocol aspects |
| Series Z | Languages and general software aspects for telecommunication systems |

Geneva, 2002