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SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital networks, digital sections and digital line systems – Design objectives for digital networks

## Considerations on timing and synchronization issues

Reedition of CCITT Recommendation G.810 published in the Blue Book, Fascicle III.5 (1989)

**NOTES**

1 CCITT Recommendation G.810 was published in Fascicle III.5 of the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression “Administration” is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

**Recommendation G.810**

# CONSIDERATIONS ON TIMING AND SYNCHRONIZATION ISSUES

*(Melbourne, 1988)*

## 1 General

This Recommendation provides information and guidance concerning the various timing and synchronization Recommendations as well as insight into the fundamental related issues.

## 2 Definitions

**primary reference clock**

A reference clock that provides a timing signal with long term frequency departure maintained at $1 \cdot 10^{-11}$ or better with verification to Universal Time Coordinated (UTC). Requirements for primary reference clocks are given in Recommendation G.811.

*Note 1* – The primary reference clock may generate a timing signal completely autonomous of other references or alternatively, the primary reference clock may not have a completely autonomous implementation, in which case it may employ direct control from standard UTC-derived frequency and time sources.

*Note 2* – This clock is sometimes referred to as a Stratum 1 clock (i.e. the highest quality clock in the network).

**synchronous network node**

A geographical location at which there are one or more interconnected synchronous digital equipments.

**transit node**

A synchronous network node which interfaces with other nodes and does not directly interface with customer equipment.

**local node**

A synchronous network node which interfaces directly with customer equipment.

**slave clock**

A clock whose timing output is phase-locked to the timing signal received from a higher quality clock. Requirements for slave clocks are given in Recommendation G.812.

*Note* – The highest quality slave clock is sometimes referrred to as a transit node clock, or a Stratum 2 clock. The second highest quality slave clock is sometimes referred to as a local node clock, or a Stratum 3 clock.

**jitter**

Short-term variations of the significant instants of a digital signal from their reference positions in time.

**timing jitter**

The short term variations of the significant instants of a digital signal from their ideal positions in time (where short term implies these variations are of frequency greater than or equal to 10 Hz).

**alignment jitter**

The short term variations between the optimum sampling instants of a digital signal and a sampling clock derived from it.

**wander**

The long term variations of the significant instances of a digital signal from their ideal positions in time (where long term implies that these variations are of frequency less than 10 Hz).

*Note* – For the purposes of this Recommendation and the following related Recommendations, this definition of wander does not include integrated frequency departure.

**frequency departure**

An underlying offset in the long term frequency of a timing signal from its ideal frequency.

**slip**

The repetition or deletion of a block of bits in a synchronous or plesiochronous bit stream due to a discrepancy in the read and write rates at a buffer.

## 3 Description of phase variation components

Phase variation is commonly separated into three components: jitter, wander and integrated frequency departure. In addition, phase discontinuities due to transient disturbances such as network re-routing, automatic protection switching, etc., may also be a source of phase variation.

## 4 Impairments caused by phase variation

### 4.1 *Types of impairments*

#### 4.1.1 *Errors*

Errors may occur at points of signal regeneration as a result of timing signals being displaced from their optimum positions in time.

#### 4.1.2 *Degradation of digitally encoded analogue information*

Degradation of digitally encoded analogue information may occur as a result of phase variation of the reconstructed samples in the digital to analogue conversion device at the end of the connection. This may have significant impact on digitally encoded video signals.

#### 4.1.3 *Slips*

Slips arise as a result of the inability of an equipment buffer store (and/or other mechanisms) to accommodate differences between the phases and/or frequencies of the incoming and outgoing signals in cases where the timing of the outgoing signal is not derived from that of the incoming signal. Slips may be controlled or uncontrolled depending on the slip control strategy.

### 4.2 *Control of impairments*

#### 4.2.1 *Errors*

The intent of both network and equipment jitter specifications is to ensure that jitter has no impact on the error performance of the network.

#### 4.2.2 *Degradation of digitally encoded analogue signals*

The intent of jitter specifications is to provide sufficient information to enable equipment designers to accommodate the expected levels of phase variation without incurring unacceptable degradations.

### 4.2.3 *Slips*

Slips may occur in asynchronous multiplexes and various synchronous equipments. Given the specified levels of phase variation, slip occurrences may be minimised in asynchronous muldexes by appropriate choice of justification and muldex buffer capacity within. For synchronous equipments, slip occurrences may be minimised by appropriate choice of buffer capacity as well as rigorous specification of clock performance.

It should be noted that it is impossible to eliminate slips when there is a frequency difference between the incoming and outgoing timing signals. Controlled slip performance objectives for an international connection are given in Recommendation G.822.

Various forms of aligning equipment may be used to minimise the impact of slips. The following two forms of aligning equipment are suitable for the termination of digital signals:

– frame aligner;

– time-slot aligner.

4.2.3.1 Where a frame aligner is used, a slip will consist of the insertion or removal of a consecutive set of digits amounting to a frame. In the case of frame structures defined in Recommendation G.704 the slip can consist of one complete frame. It is of importance that the maximum and mean delays introduced by the frame aligner should be as small as possible in order to minimize delay. It is also of importance that, after the frame aligner has produced a slip, it should be capable of absorbing substantial further changes in the arrival time of the frame alignment signals before a further slip is necessary.

4.2.3.2 Where a slot aligner is used, a slip will consist of the insertion or removal of eight consecutive digit positions of a channel time slot in one or more 64 kbit/s channels. Because slips may occur on different channels at different times, special control arrangements will be necessary in switches if octet sequence integrity of multiple time-slot services is to be maintained.

## 5 Purpose of phase variation specifications

### 5.1 *Jitter*

Jitter requirements given in Recommendations G.823 and G.824 fall into two basic categories:

– specification of the maximum permissible jitter at the output of hierarchical interfaces;

– sinusoidal jitter stress test specifications to ensure the input ports can accommodate expected levels of network jitter.

Additional jitter requirements for individual equipments may be found in the appropriate equipment Recommendations.

### 5.2 *Wander and long term frequency departure*

Relevant wander requirements fall into the following categories:

i) maximum permissible wander at the output of synchronous network nodes;

ii) stress tests to ensure that synchronous equipment input ports can accommodate expected levels of network wander;

iii) wander specifications for primary reference and slave clocks may include:

   a) intrinsic output wander under ideal conditions;

   b) intrinsic output wander under free-running conditions;

   c) output wander under stress test conditions;

   d) wander transfer characteristic.

The purpose of these Recommendations is not only to provide limits for the allowance wander accumulation along the transmission paths but also for the wander accumulation along the synchronization distribution paths arising from cascaded clocks.

## 6 Structure of synchronization networks

### 6.1 *Synchronization modes*

International networks usually work in the plesiochronous mode one with another.

The synchronization of national networks may be of the following types:

– fully synchronized, controlled by one or several primary reference clocks;

– fully plesiochronous;

– mixed, in which synchronized sub-networks are controlled by one or several primary reference clocks functioning plesiochronously one with another.

### 6.2 *Synchronization networks*

There are two fundamental methods of synchronizing nodal clocks:

– master-slave synchronization;

– mutual synchronization.

The master-slave synchronization system has a single primary reference clock to which all other clocks are phase-locked. Synchronization is achieved by conveying the timing signal from one clock to the next clock. Hierarchies of clocks can be established with some clocks being slaved from higher order clocks and in turn acting as master clocks for lower order clocks.

In a mutual synchronization system, all clocks are interconnected; there is no underlying hiearchical structure or unique primary reference clock.

Some practical synchronization strategies combine master-slave and mutual synchronization techniques.

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