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SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Design objectives for digital networks

Timing requirements at the outputs of primary reference clocks suitable for plesichronous operation of international digital links

Reedition of CCITT Recommendation G.811 published in the Blue Book, Fascicle III.5 (1989)

NOTES

1 CCITT Recommendation G.811 was published in Fascicle III.5 of the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Recommendation G.811

TIMING REQUIREMENTS AT THE OUTPUTS OF PRIMARY REFERENCE CLOCKS SUITABLE FOR PLESICHRONOUS OPERATION OF INTERNATIONAL DIGITAL LINKS

(Melbourne, 1988)

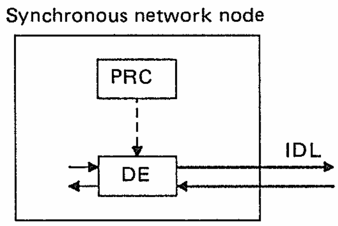
1 General

1.1 *International connections and network synchronization considerations*

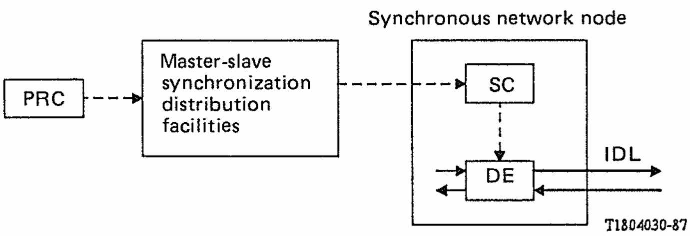
National digital networks, which may have a variety of internal synchronization arrangements, will usually be connected by international links which operate plesiochronously. International switching centres (ISCs) will be interconnected directly or indirectly via one or more intermediate ISCs, as indicated in the hypothetical reference connection (HRX) shown in Figure 1/G.801.

International connections terminate on synchronous network nodes that may or may not be co-located with a primary reference clock. Such network nodes may include slave clocks. Therefore, synchronous network node clock specifications are essential to ensure satisfactory operation of plesiochronous international digital links.

Figure 1/G.811 illustrates the two alternative international connections described above.



a) Case 1 – Synchronous network node including primary reference clock



b) Case 2 – Synchronous network node including slave clock

PRC Primary reference clock
SC Slave clock
DE Digital equipment such as digital exchange or digital muldex
IDL International digital link

Note – Other cases are for further study.

FIGURE 1/G.811

International connections terminating on synchronous network nodes

1.2 *Purpose of this Recommendation*

The purpose of this Recommendation is to specify requirements for primary reference clocks, promote understanding of associated timing requirements for plesiochronous operation of international digital links, and to clarify the relationship of the requirements for synchronous network nodes, constituent clocks and the use of satellite systems.

Administrations may apply this Recommendation, at their own discretion, to primary reference clocks other than those used in connection with international traffic.

1.3 *Interaction between plesiochronous and synchronous international operation*

It is important that the Recommendations for plesiochronous operation should not preclude the possibility of the later introduction of international synchronization.

When plesiochronous and synchronous operations coexist within the international network, the nodes will be required to provide for both types of operation. It is therefore important that the synchronization controls do not cause short-term frequency departures of the clocks which are unacceptable for plesiochronous operation. The magnitudes of the short-term frequency departures should satisfy the specifications in § 2.2.

1.4 *Maximum time interval error and relationship with frequency departure*

Maximum time interval error (MTIE) is the maximum peak-to-peak variation in the time delay of a given timing signal with respect to an ideal timing signal within a particular time period (Figure 2/G.811), i.e. MTIE(S) = max $x(t)$-min $x(t)$ for all t within S.

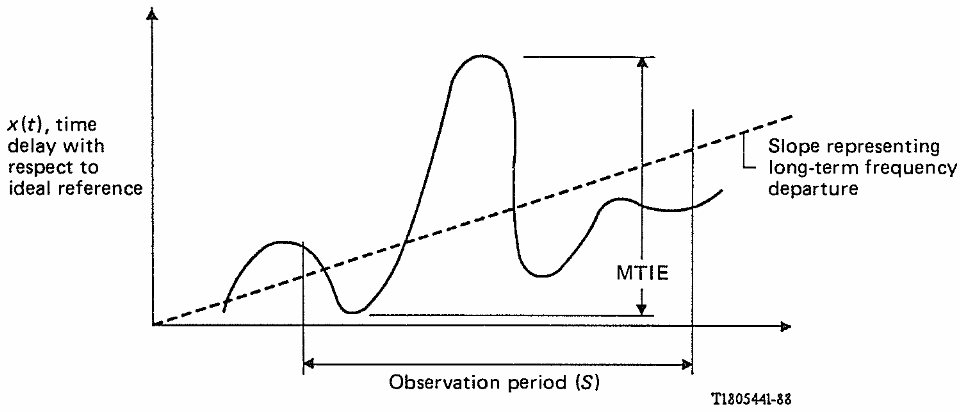


FIGURE 2/G.811
Definition of maximum time interval error

Long-term frequency departure ($\Delta f/f$) is determined by the MTIE divided by the observation interval S, as S increases.

Note – The rigorous definition and measurement of long-term frequency departure for clocks is a subject for further study.

2 Long-term frequency departure and phase stability of primary reference clocks

A primary reference clock controls the synchronization performance of the overall network. It is necessary to specify the long-term frequency departure and phase stability of a primary reference clock, and to provide guidance concerning issues associated with degradation and unavailability performance. The definition of a primary reference clock is given in Recommendation G.810.

2.1 *Long-term frequency departure*

A primary reference clock should be designed for a long-term frequency departure of not greater than 1×10^{-11}. The long-term frequency departure of 1×10^{-11} is about two orders of magnitude larger than the uncertainty of Coordinated Universal Time (UTC). Therefore UTC should be the reference for long-term frequency departure (see CCIR Report 898).

The theoretical long-term mean rate of occurrence of controlled frame or octet slips (i.e. the design rate of slips based on ideally undisturbed conditions) in any 64 kbit/s channel is consequently not greater than one in 70 days per digital international link (see Recommendation G.822).

Note 1 – Some Administrations support a primary reference clock long-term frequency departure of not greater than 7×10^{-12} based upon current primary reference clock technology.

Note 2 – Caesium-beam technology is suitable for primary reference clocks complying with the above specification.

2.2 *Phase stability*

The phase stability of a clock can be described by its phase variations, which in turn can be separated into a number of components:

– phase discontinuities due to transient disturbances;

– long-term phase variations (wander and integrated frequency departure);

– short-term phase variations (jitter).

A phase stability model for primary reference clocks is described in the annex to this Recommendation.

2.2.1 *Phase discontinuities*

Primary reference clocks need a very high reliability and are likely to include replication of the equipment in order to ensure the continuity of output. However, any phase discontinuity, due to internal operations within the clock, should only result in a lengthening or shortening of the timing signal interval and must not cause a phase discontinuity in excess of 1/8 of a unit interval at the clock output. (This refers to output signals at 1544 kbit/s or 2048 kHz, see § 4. Specification of other interfaces is under study.)

2.2.2 *Long-term phase variations*

The maximum permissible long-term phase variation of the output of a primary reference clock (whether sinusoidal or pulse) is expressed in MTIE.

The MTIE over a period of S seconds shall not exceed the following limits:

a) $100\ S$ ns for the interval $0.05 < S \leq 5$

b) $(5\ S + 500)$ ns for the interval $5 < S \leq 500$

c) $(0.01\ S + X)$ ns for values of $S > 500$.

The asymptote designated 10^{-11} refers to the long-term frequency departure specified in § 2.1.

The value of X is under study. It is provisionally recommended that X = 3000 ns. Certain Administrations support a value of 1000 ns.

Note 1 – For measurement of long-term phase variations, the use of a 10 Hz low-pass filter is suggested.

Note 2 – The MTIE Recommendation requires further study.

Note 3 – The overall specification is illustrated in Figure 3/G.811.

2.2.3 *Short-term phase variations*

Clock implementations exist today which may have some high-frequency phase instability components. The specification of maximum permissible short- term phase variation of a primary reference clock due to jitter is under study.

3 Degradation of the performance of a primary reference clock

To achieve the required high reliability a primary reference clock includes redundancy, i.e. by incorporating several (caesium beam) oscillators, the output of only one of these being used at any given time. If a clock frequency departs significantly from its nominal value, this should be detected and switching to an undegraded oscillator should then be effected. This switching should be accomplished before the MTIE specification is exceeded.

With current technology, the performance of a primary reference clock is statistically well below the MTIE specification of Figure 3/G.811.

4 Interfaces

The preferred interface for the timing output is in accordance with Recommendation G.703, § 10, i.e. an interface at 2048 kHz. By agreement between operators or manufacturers of equipment, the timing signal may also be delivered at various other physical interfaces (e.g., 1544 kbit/s primary rate signal, 1 MHz, 5 MHz, or 10 MHz).

5 Use of satellite systems in an international plesiochronous digital network

It is recommended that the link be operated in a plesiochronous mode using high accuracy (1×10^{-11}) source for the satellite TDMA timing. The international satellite links will be terminated on network nodes whose timing is in accordance with Recommendations G.823 and G.824.

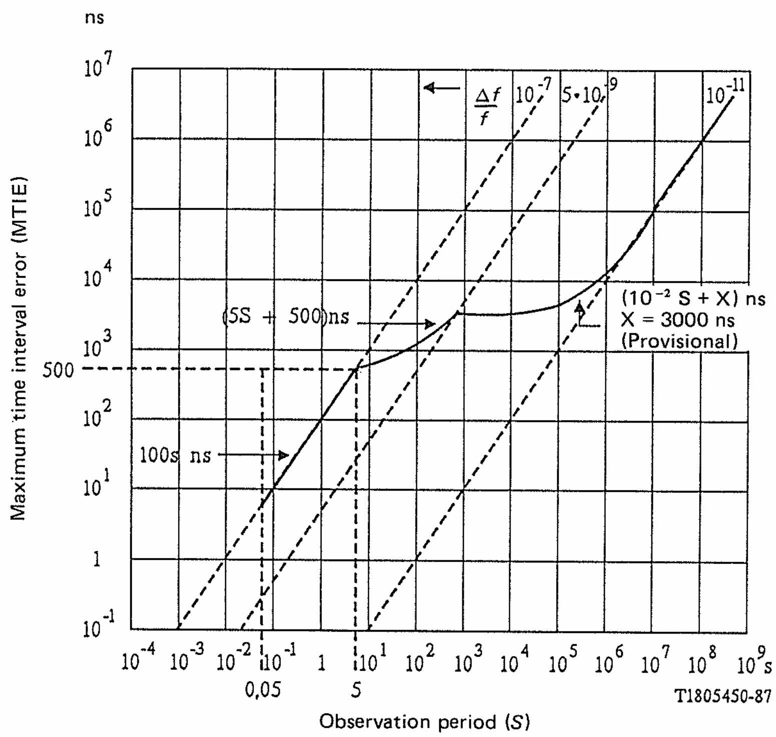


FIGURE 3/G.811

Permissible maximum time interval error (MTIE) due to long-term phase variation as a function of observation period *S* for a primary reference clock

6 Guidelines concerning the measurement of jitter and wander

Verification of compliance with jitter and wander specifications requires standardized measurement methodologies to eliminate ambiguities in the measurements and in interpretation and comparison of measurement results. Guidelines concerning the measurement of jitter and wander are contained in Supplement No. 3.8 (O-Series) and Supplement No. 35 at the end of this Fascicle.

ANNEX A

(to Recommendation G.811)

Characterization of primary reference clock phase stability

The following phase stability model may be employed to characterize primary reference clocks. Let $x(t)$ represent the time interval error of a clock synchronized at $t = 0$, and free-running against UTC thereafter. $x(t)$ may be defined as:

$$x(t) = y_0 + \left(\frac{D}{2}\right) t^2 + e(t)$$

where:

D is the normalized linear frequency drift per unit time (ageing),

y_0 is the initial frequency departure with respect to UTC, and

$e(t)$ is the random error component.

The estimate of the standard deviation of $x(t)$ may be obtained, and used for characterization of phase instability.

$$\sigma_x(t) = \left(\frac{D}{2}\right) t^2 + t\sqrt{\sigma_{y_0}^2 + \sigma_y^2\ (\tau = t)}$$

where:

σ_y^2 is the two-sample variance of the initial frequency departure, and

$\sigma_y^2(\tau)$ is the two-sample Allan variance describing the random frequency instability of the clock.

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