INTERNATIONAL TELECOMMUNICATION UNION

CCITT

THE INTERNATIONAL
TELEGRAPH AND TELEPHONE
CONSULTATIVE COMMITTEE

G.812

(11/1988)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Design objectives for digital networks

Timing requirements at the outputs of slave clocks suitable for plesiochronous operation of international digital links

Reedition of CCITT Recommendation G.812 published in the Blue Book, Fascicle III.5 (1989)

NOTES

1 CCITT Recommendation G.812 was published in Fascicle III.5 of the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Recommendation G.812

TIMING REQUIREMENTS AT THE OUTPUTS OF SLAVE CLOCKS SUITABLE FOR PLESIOCHRONOUS OPERATION OF INTERNATIONAL DIGITAL LINKS

(Melbourne, 1988)

1 General

1.1 *Purpose of this Recommendation*

The purpose of this Recommendation is to specify requirements for slave clocks, and promote understanding of associated timing requirements for plesiochronous operation of international digital links.

Note – Administrations may apply this Recommendation, at their own discretion, to slave clocks other than those used in connection with international traffic. Supplement No. 35 gives guidance on one suitable method for the measurement of clock performance with respect to this Recommendation.

1.2 *Maximum relative time interval error*

The concept of maximum relative time interval error (MRTIE) is useful in specifying slave clock performance. MRTIE is analogous to MTIE as defined in Recommendation G.811 but with reference to a practical high-performance oscillator instead of UTC.

2 Phase stability of slave clocks

The phase stability of a slave clock can be described by its phase variations which in turn can be separated into a number of components:

– phase discontinuities due to transient disturbances;

– long-term phase variations (wander and integrated frequency departure);

– short-term phase variations (jitter).

A phase stability model for slave clocks is described in Annex A to this Recommendation.

2.1 *Phase discontinuity*

In cases of infrequent internal testing or rearrangement operations within the slave clock, the following conditions should be met:

– the phase variation over any period up to 2^{11} UI should not exceed 1/8 of a UI;

– for periods greater than 2^{11} UI in the phase variation for each interval or 2^{11} UI should not exceed 1/8 UI up to a total amount of 1 μs,

Where the UI corresponds to the reciprocal of the bit rate of the interface.

2.2 *Long-term phase variations*

Slave clock phase stability requirements must account for clock behaviour in real network environments. Impairments such as jitter, error bursts, and outages are intrinsic characteristics of timing distribution facilities. The following specifications are based on the slave clock phase stability model contained in the Annex. This model characterizes actual clock performance, reflecting the stress conditions in real networks under which clocks should perform acceptably. There are three categories of clock operation which require specification:

i) ideal,

ii) stressed, and

iii) holdover.

2.2.1 *Ideal operation*

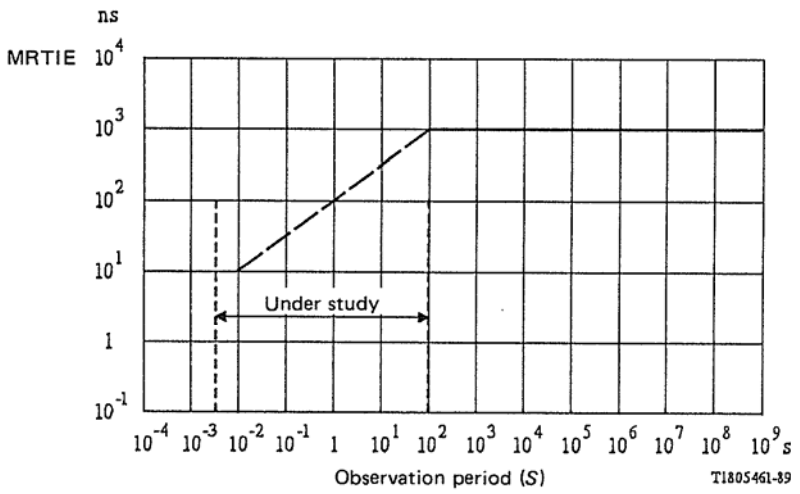
This category of operation reflects the performance of a clock under conditions in which there are no impairments on the input timing reference(s).

The MRTIE at the output of the slave clock should not, over any period of *S* seconds, exceed the following provisional limits:

1) $0.05 < S < 100$: this region requires further study;

2) 1000 ns for $S \geq 100$.

The resultant overall specification is summarized in Figure 1/G.812.



Note – For measurement of long-term variations the use of a 10 Hz low-pass filter with a 20 dB/dec roll-off is suggested.

FIGURE 1/G.812

Permissible maximum relative time interval error (MRTIE) due to long-term phase variations vs. observation period *S* for a slave clock under ideal operation

2.2.2 *Stressed operation*

This category of operation reflects the actual performance of a clock considering the impact of real operating (stressed) conditions. Stressed conditions include the effects of jitter, protection switching activity, and error bursts. The result of such stressed conditions is timing impairments, as discussed in the Annex.

The requirements for stressed operation are under study.

2.2.3 *Holdover operation*

This category of operation reflects the performance of a clock for the infrequent times when a slave clock will lose reference for a significant period of time.

The MRTIE (see § 1.2 and Recommendation G.811) at the output of the slave clock should not, over any period of *S* seconds, exceed the following provisional limits.

$$\text{For } S \geq 100,\ \text{MRTIE}\ (S) = (aS + 1/2\ bS^2 + c)\ \text{ns}$$

where parameters a, b, c are proposed provisionally in Table 1/G.812 (Note 5):

TABLE 1/G.812

	Transit node clock [a] (stratum 2 clock)	Local node clock [a] (stratum 3 clock)
a	0.5 (Note 1)	10.0 (Note 3)
b	1.16×10^{-5} (Note 2)	2.3×10^{-4} (Note 4)
c	1000 (Note 6)	1000 (Note 6)

[a] See Recommendation G.810 for definitions.

Note 1 – Corresponds to un initial frequency offset of 5×10^{-10}.

Note 2 – Corresponds to a frequency drift of 1×10^{-9}/day.

Note 3 – Corresponds to an initial frequency offset of 1×10^{-8}.

Note 4 – Corresponds to a frequency drift of 2×10^{-8}/day.

Note 5 – Temperature effects: the effect of changes in environmental temperature on the performance of a slave clock in holdover mode requires further study.

Note 6 – Takes care of any MRTIE that might have existed at the beginning of holdover operation, and of effects of internal configuration, etc. in the clock (and timing distribution, if applicable). In any case, a smooth transition between "ideal" and "holdover" operations is stipulated.

The resultant overall specification is summarized in Figure 2/G.812.

2.3 *Short-term phase variations*

Clock implementations exist which may have some high frequency phase instability components. The maximum permissible short-term phase variation of a slave clock due to jitter is under study.

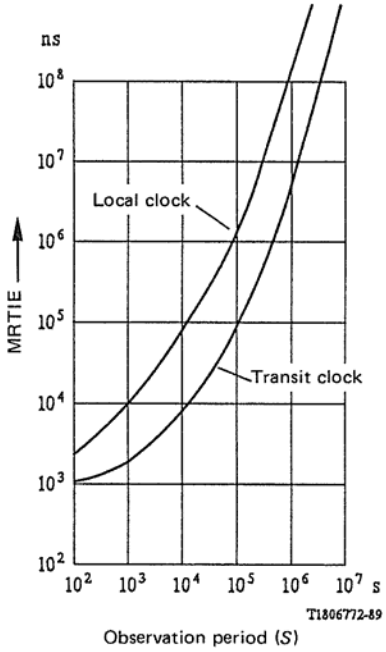


FIGURE 2/G.812

Permissible maximum relative time interval error (MRTIE) due to long-term phase variations vs. observation period *S* for a slave clock under holdover operation

ANNEX A

(to Recommendation G.812)

Characterization of slave clock phase stability

A.1 The slave clock model is described by the following equation:

$$x(t) = y_{bias} \cdot t + \left(\frac{D}{2}\right) t^2 + e_{mp}(t) + \int_{\tau=0}^{\tau=t} e_{mf}(\tau)\, d\tau$$

where,

$x(t)$ is the phase-time output relative to the reference input (dimension time);

y_{bias} is a residual fractional frequency offset which can arise from disruption events on the reference input (dimensionless);

D is the linear frequency drift component when the clock is in holdover condition (dimension 1/time);

$e_{mp}(t)$ is a white noise phase modulation (PM) component associated with the short-term instability of the clock (dimension time);

$e_{mf}(\tau)$ is a white noise fractional frequency modulation (FM) component associated with the disruption process of the reference (dimensionless).

The clock model is best understood by considering the three categories of clock operation:

– ideal operation;

– stressed operation;

– holdover operation.

A.1.1 *Ideal operation*

For short observation intervals outside the tracking bandwidth of the PLL, the stability of the output timing signal is determined by the short term stability of the local synchronizer time base. In the absence of reference disruptions, the stability of the output timing signal behaves asymptotically as a white noise PM process as the observation period is increased to be within the tracking bandwidth of the PLL. The output of the clock can be viewed as a superposition of the high frequency noise of the local oscillator riding on the low frequency portion of the input reference signal. In phase locked operation the high frequency noise must be bounded, and is uncorrelated (white) for large observation periods relative to the bandwidth of the phase locked loop.

Under ideal conditions, the only non-zero parameter of the model is the white noise PM component.

A.1.2 *Stressed operation*

In the presence of interruptions, the stability of the output timing signal behaves as a white noise FM process as the observation period is increased to be within the tracking bandwidth of the PLL. The presence of white noise FM can be justified based on the simple fact that in general, network clocks extract time interval, rather than absolute time from the time reference. An interruption is by nature a short period during which the reference time interval is not available. When reference is restored there is some ambiguity regarding the actual time difference between the local clock and the reference. Depending on the sophistication of the clock phase build-out there can be various levels of residual phase error which occur for each interruption. There is a random component which is independent from one interruption event to the next which results in a random walk in phase, i.e. a white noise FM noise source.

In addition to the white noise FM component, interruption events can actually result in a frequency offset between the clock and its reference. This frequency offset (y_{bias}) results from a bias in the phase build-out when reference is restored. This is a critical point. The implications of this effect are that in actual network environments there is some accumulation of frequency offset through a chain of clocks. Thus, clocks controlled by the same primary reference clock are actually operating plesiochronously to some degree.

To summarize, under stress conditions the non-zero parameters of the clock model are the white noise FM component (e_{mf}) and the frequency offset component (y_{bias}). The stressed category of operation reflects a realistic characterization of what “normal” operation of a clock is.

A.1.3 *Holdover operation*

In holdover, the key components of the clock model are the frequency drift (D) and the initial frequency offset (y_{bias}). The drift term accounts for the significant ageing associated with quartz oscillators. The initial frequency offset is associated with the intrinsic setability of the local oscillator frequency.

A.2 *Relationship of slave clock model to TIE performance*

It is useful to consider the relationship between the clock model and the Time Interval Error (TIE) that would be expected. It is proposed that the two sample Allan variance be used to describe the stochastic portion of the clock model. The following equations apply for the three categories of operation:

Ideal

$$\sigma_{EIT} = \sqrt{3\sigma_{,}^{2}\,(\tau = t)\cdot t}$$

Stressed

$$\sigma_{EIT} = \sqrt{\sigma_{bias}^{2} + \sigma_{,}^{2}\,(\tau = t)\cdot t}$$

Holdover

$$\sigma_{EIT} = \left(\frac{D}{2}\right) t^{2} + \sqrt{\sigma_{bias}^{2} + \sigma_{,}^{2}\,(\tau = t)\cdot t}$$ where,

σ_{EIT} is the standard deviation of the relative time interval error of the clock output compared to the reference over the observation time *t*;

$\sigma,\ (\tau)$ is the two sample standard deviation describing the random frequency fluctuation of the clock, and

σ_{bias} describes the two sample standard deviation of the frequency bias.

A.3. *Guidelines concerning the measurement of jitter and wander*

Verification of compliance with jitter and wander specifications requires standardized measurement methodologies to eliminate ambiguities in the measurements and in the interpretation and comparison of measurement results. Guidance concerning the measurement of jitter and wander is contained in Supplement No. 35.

ITU-T RECOMMENDATIONS SERIES

Series A	Organization of the work of the ITU-T
Series B	Means of expression: definitions, symbols, classification
Series C	General telecommunication statistics
Series D	General tariff principles
Series E	Overall network operation, telephone service, service operation and human factors
Series F	Non-telephone telecommunication services
Series G	**Transmission systems and media, digital systems and networks**
Series H	Audiovisual and multimedia systems
Series I	Integrated services digital network
Series J	Transmission of television, sound programme and other multimedia signals
Series K	Protection against interference
Series L	Construction, installation and protection of cables and other elements of outside plant
Series M	TMN and network maintenance: international transmission systems, telephone circuits, telegraphy, facsimile and leased circuits
Series N	Maintenance: international sound programme and television transmission circuits
Series O	Specifications of measuring equipment
Series P	Telephone transmission quality, telephone installations, local line networks
Series Q	Switching and signalling
Series R	Telegraph transmission
Series S	Telegraph services terminal equipment
Series T	Terminals for telematic services
Series U	Telegraph switching
Series V	Data communication over the telephone network
Series X	Data networks and open system communications
Series Y	Global information infrastructure and Internet protocol aspects
Series Z	Languages and general software aspects for telecommunication systems

Printed in Switzerland

Geneva, 2006