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Digital networks – Design objectives for digital networks

Timing requirements of slave clocks suitable for use as node clocks in synchronization networks

ITU-T Recommendation G.812

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ITU-T Recommendation G.812

Timing requirements of slave clocks suitable for use as node clocks in synchronization networks

Summary

This Recommendation outlines minimum requirements for timing devices used as node clocks in synchronization networks. The requirements relate to frequency deviation; pull-in, hold-in and pull-out range; noise generation, tolerance and transfer; transient response and holdover performances. The node clocks are suitable for use in SDH and PSTN network applications.

This Recommendation includes specifications for three types of clocks. The Type I clock is primarily intended for use in networks optimized for the 2048 kbit/s hierarchy. The Types II and III clocks are primarily intended for use in networks optimized for the particular 1544 kbit/s hierarchy that includes the rates 1544 kbit/s, 6312 kbit/s and 44 736 kbit/s.

Additionally, this Recommendation includes specifications for three other clocks in Annex A. Type IV is typically deployed in existing networks that support the 1544 kbit/s. The Types V and VI clocks were defined for transit and local node applications in the 1988 version of this Recommendation.

Source

ITU-T Recommendation G.812 was approved on 13 June 2004 by ITU-T Study Group 15 (2001-2004) under the ITU-T Recommendation A.8 procedure. The typo corrected by G.812 (2004) Erratum 1 is included in the electronic version of this Recommendation.

Keywords

Clock performance objectives, clock performance parameters, jitter performance, node clock, wander performance.

FOREWORD

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The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

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In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

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CONTENTS

ITU-T Recommendation G.812

Timing requirements of slave clocks suitable for use as node clocks in synchronization networks

1 Scope

This Recommendation outlines minimum requirements for timing devices used as node clocks in synchronization networks. The function of a node clock is to select one of the external synchronization links coming into a telecommunication station as the active synchronization reference, to attenuate its jitter and wander and subsequently to distribute the reference to the telecommunication equipment in the station. The requirements in this Recommendation apply under the normal environmental conditions specified for telecommunications equipment.

This Recommendation specifies node clocks suitable for use in SDH and PSTN network applications. They may provide acceptable performance for other applications, but that has to be investigated for each case individually.

In normal operation, a node clock is operating as a slave clock, traceable to a primary reference clock. For purposes of redundancy, a node clock will in general have multiple reference inputs. In the event that all links between the master(s) and the node clock fail, the node clock should be capable of maintaining operation within prescribed performance limits (the hold-over mode of operation).

A node clock can be a separate piece of equipment called a Stand Alone Synchronization Equipment (SASE) or it can be a part of another equipment such as a telephony exchange or an SDH cross-connect.

This Recommendation defines six Types of clocks. Applications for each clock Type are described in clause 2.

2 Node clock types and applications

2.1 Synchronization network considerations

Design of synchronization networks in general is not standardized. Principles for synchronization of SDH networks are outlined in ITU-T Rec. G.803. Some of these principles can be taken as general design rules for synchronization networks.

Synchronization requirements for node clocks in a PSTN environment can in principle be derived from the controlled slip rate objectives in ITU-T Rec. G.822. There are three elements that determine whether G.822 objectives can be achieved:

- the hold-over stability of the clocks;
- the network topology (i.e., length, routing and redundancy of the references); and
- the operational practices of the operator (i.e., mean time to repair).

Only the first element is covered in this Recommendation. Network providers can choose to use particular clock Types in their synchronization planning in order to match their network topology and operational practices.

Synchronization requirements for node clocks in an SDH environment are mainly driven by the jitter and wander specifications in ITU-T Recs G.823, G.824 and G.825. Given that SDH equipment clocks (as specified in ITU-T Rec. G.813) have only limited filtering capabilities and at the same time need to maintain their STM-N and PDH outputs in conformance with ITU-T Recs G.823,

G.824 and G.825, the phase transients at the output of node clocks must meet specifications that are more stringent than what is strictly needed for pure PDH transport equipment.

NOTE – Since the bandwidths of SDH equipment clocks are wider in networks based on the 2048 kbit/s hierarchy compared to those based on the 1544 kbit/s hierarchy (as described in ITU-T Rec. G.813 option 1 and option 2, respectively), the output phase transient requirements are correspondingly more stringent for node clocks deployed in 2048 kbit/s hierarchy environments.

2.2 Node clock types and applications

This Recommendation includes specifications for three clocks. The Type I clock is primarily intended for use in networks optimized for the 2048 kbit/s hierarchy. The Types II and III clocks are primarily intended for use in networks optimized for the particular 1544 kbit/s hierarchy that includes the rates 1544 kbit/s, 6312 kbit/s and 44 736 kbit/s.

The Type I clock can be used at all levels of the synchronization hierarchy in 2048 kbit/s based networks. The wander generation and bandwidth of Type I clocks are limited to values that allow the deployment of the maximum number of node clocks according to the synchronization network reference chain as defined in ITU-T Rec. G.803. Although a Type I clock is primarily intended for use in networks supporting the 2048 kbit/s hierarchy, a Type I clock can also be deployed in 1544 kbit/s based networks as long as at least its pull-in range, noise generation and noise tolerance (see clauses 7, 8 and 9) comply with the more stringent requirements that apply to Types II and III clocks in order to be compatible with SDH equipment clocks built according to ITU-T Rec. G.813 option 2.

The Type II clock has a more stringent hold-over stability specification than a Type I clock. It is typically deployed at distribution hubs in networks that support the 1544 kbit/s hierarchy mentioned above. Type II clocks have a hold-over stability specification sufficient to operate with a single reference at the highest levels of the synchronization hierarchy. Although a Type II clock is primarily intended for use in networks supporting the 1544 kbit/s hierarchy, a clock with Type II hold-over specifications can also be deployed in 2048 kbit/s based networks as long as at least its noise generation, noise tolerance and transient behaviour (see clauses 8, 9, 11.1 and 11.4) comply with the more stringent requirements that apply to Type I clocks in order to be compatible with SDH equipment clocks built according to ITU-T Rec. G.813 option 1.

The Type III clock has a less stringent hold-over stability requirement than Type I and Type II. It is typically deployed in end offices in networks that support the 1544 kbit/s hierarchy mentioned above. Like a Type II clock, a clock with Type III hold-over stability may also be deployed in 2048 kbit/s based networks as long as at least its noise generation, noise tolerance and transient behaviour (see clauses 8, 9, 11.1 and 11.4) comply to the more stringent requirements that apply to Type I when it is used to synchronize SDH equipment.

Additionally, this Recommendation includes specifications for three clocks in Annex A.

The Type IV clock is typically deployed in existing networks that support the 1544 kbit/s hierarchy mentioned above. If clocks with Type IV hold-over performance are embedded in SDH equipment in this hierarchy, the requirements in ITU-T Rec. G.813 option 2 should be met as well.

The Type V clock is typically deployed in existing transit nodes of networks based on both 1544 kbit/s and 2048 kbit/s hierarchies according to the specifications of the 1988 version of this Recommendation. It should be noted that these clocks are perfectly suitable for the synchronization of 2048 kbit/s based SDH networks provided they conform at least to the noise generation and short-term stability requirements (clauses 8, 11.1 and 11.4) of Type I clocks.

The Type VI clock is typically deployed in existing local nodes of networks based on the 2048 kbit/s hierarchy according to the specifications of the 1988 version of this Recommendation. Like Type V, clocks with Type VI hold-over stability characteristics may be used for the

synchronization of SDH networks as long as the clock at least meets the noise generation and short-term stability requirements (clauses 8, 11.1 and 11.4) of the Type I clock.

3 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[1] ITU-T Recommendation G.703 (2001), *Physical/electrical characteristics of hierarchical digital interfaces*.

[2] ITU-T Recommendation G.783 (2004), *Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks*.

[3] ITU-T Recommendation G.801 (1988), *Digital transmission model*s.

[4] ITU-T Recommendation G.803 (2000), *Architecture of transport networks based on the synchronous digital hierarchy (SDH)*.

[5] ITU-T Recommendation G.810 (1996), *Definitions and terminology for synchronization networks*.

[6] ITU-T Recommendation G.811 (1997), *Timing requirements of primary reference clocks*.

[7] ITU-T Recommendation G.813 (2003), *Timing requirements of SDH equipment slave clocks (SEC).*

[8] ITU-T Recommendation G.822 (1988), *Controlled slip rate objectives on an international digital connection*.

[9] ITU-T Recommendation G.823 (2000), *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy*.

[10] ITU-T Recommendation G.824 (2000), *The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy*.

[11] ITU-T Recommendation G.825 (2000), *The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH)*.

[12] ITU-T Recommendation Q.551 (2002), *Transmission characteristics of digital exchanges*.

4 Definitions

The terms and definitions used in this Recommendation are contained in ITU-T Rec. G.810.

5 Abbreviations

This Recommendation uses the following abbreviations.

CMI	Coded Mark Inversion
MTIE	Maximum Time Interval Error
NE	Network Element
PDH	Plesiochronous Digital Hierarchy
ppm	parts per million

PRBS Pseudo Random Binary Sequence

PRC Primary Reference Clock

PSD Power Spectral Density

PSTN Public Switched Telephone Network

SASE Stand Alone Synchronization Equipment

SDH Synchronous Digital Hierarchy

SEC SDH Equipment Clock

SSU Synchronization Supply Unit

STM Synchronous Transport Module

TDEV Time Deviation

UI Unit Interval

6 Frequency accuracy

Under prolonged hold-over conditions, the output frequency accuracy of the different Types of node clocks should not exceed the values in Table 1 with regard to a reference traceable to a primary reference clock, over a time period T as reported in the same Table.

Table 1/G.812 – Output frequency accuracy requirements

	Type I	Type II	Type III
Accuracy	NA	1.6×10^{-8}	4.6×10^{-6}
Period T	NA	1 year	1 year
NA Not applicable NOTE – The time period T applies after 30 days of continuous synchronized operation.			

7 Pull-in, hold-in, and pull-out ranges

The minimum pull-in, hold-in and pull-out ranges for the different Types of node clocks should be according to Table 2, whatever the internal oscillator frequency offset may be.

Table 2/G.812 – Pull-in, hold-in, and pull-out requirements

	Type I	Type II	Type III
Pull-in	1×10^{-8}	1.6×10^{-8}	4.6×10^{-6}
Hold-in	NA	1.6×10^{-8}	4.6×10^{-6}
Pull-out	TBD	NA	NA
NA Not applicable TBD To be defined			

8 Noise generation

The noise generation of a slave clock represents the amount of phase noise produced at the output when there is an ideal input reference signal or the clock is in hold-over state (see 11.2). A suitable reference, for practical testing purposes, implies a performance level at least 10 times more stable than the output requirements. The ability of the clock to limit this noise is described by its

frequency stability. The measures MTIE and Time Deviation (TDEV) are useful for characterization of noise generation performance.

MTIE and TDEV are measured through an equivalent 10 Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 second. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\ \tau$).

8.1 Wander in locked mode

When the slave clock is in the locked mode of operation, the MTIE at constant temperature (within ±1 K) measured using the synchronized clock configuration defined in Figure 1-a/G.810 should have the limits in Tables 3 and 4 for the different Types of node clocks.

Table 3/G.812 – Wander generation (MTIE) for Type I node clock at constant temperature (within ±1 K)

MTIE limit (ns)	Observation interval τ (s)
24	$0.1 < \tau \leq 9$
$8 \times \tau^{0.5}$	$9 < \tau \leq 400$
160	$400 < \tau \leq 10\ 000$

Table 4/G.812 – Wander generation (MTIE) for Types II and III node clocks at constant temperature (within ±1 K)

MTIE limit (ns)	Observation interval τ (s)
40	$0.1 < \tau \leq 1$
$40 \times \tau^{0.4}$	$1 < \tau \leq 10$
100	$\tau > 10$

When temperature effects are included of which the limits and rate of change are to be defined, the allowance for the total MTIE contribution of a single Type I node clock is given by the values in Table 5.

Table 5/G.812 – Total wander generation (MTIE) for Type I node clock for variable temperature

MTIE limit (ns)	Observation interval τ (s)
$3.2\ \tau^{0.5}$	$2500 < \tau \leq 10\ 000$

NOTE – For observation periods greater than 10 000 s, the MTIE is expected not to exceed 1 µs.

The resultant requirements are shown in Figure 1.

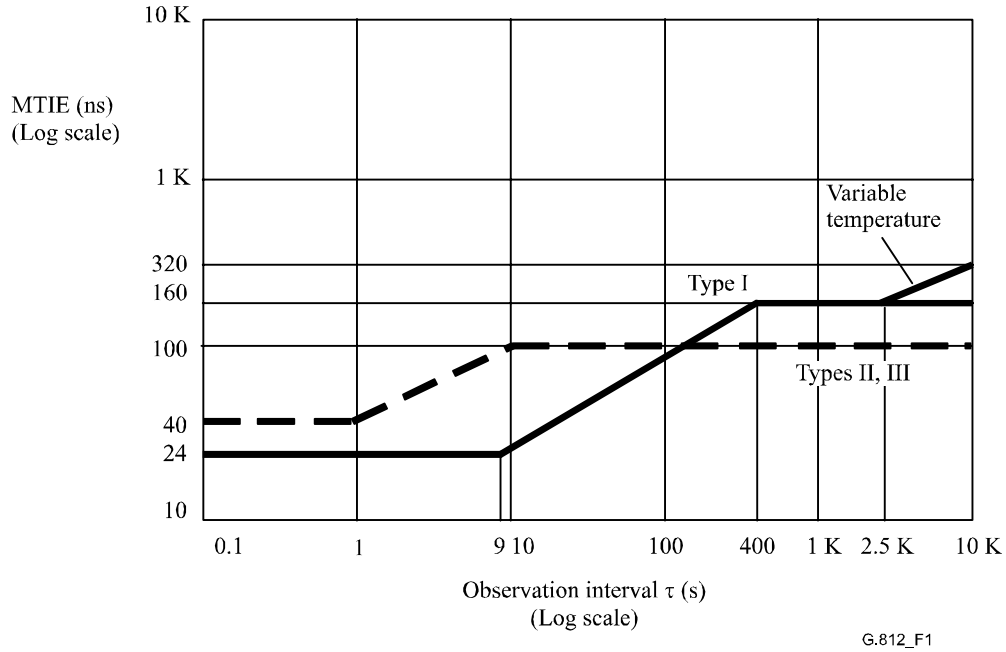

Figure 1/G.812 – Wander generation (MTIE)

When the node clock is in the locked mode of operation, the TDEV at constant temperature (within ±1 K) measured using the synchronized clock configuration defined in Figure 1-a/G.810 should have the limits in Tables 6 and 7 for the different Types of node clock.

Table 6/G.812 – Wander generation (TDEV) for Type I node clock at constant temperature (within ±1 K)

TDEV limit (ns)	Observation interval τ (s)
3	$0.1 < \tau \leq 25$
$0.12\ \tau$	$25 < \tau \leq 100$
12	$100 < \tau \leq 10\,000$

Table 7/G.812 – Wander generation (TDEV) for Types II and III node clocks at constant temperature (within ±1 K)

TDEV limit (ns)	Observation interval τ (s)
$3.2 \times \tau^{-0.5}$	$0.1 < \tau \leq 2.5$
2	$2.5 < \tau \leq 40$
$0.32 \times \tau^{0.5}$	$40 < \tau \leq 1000$
10	$\tau > 1000$

The resultant requirements are shown in Figure 2.

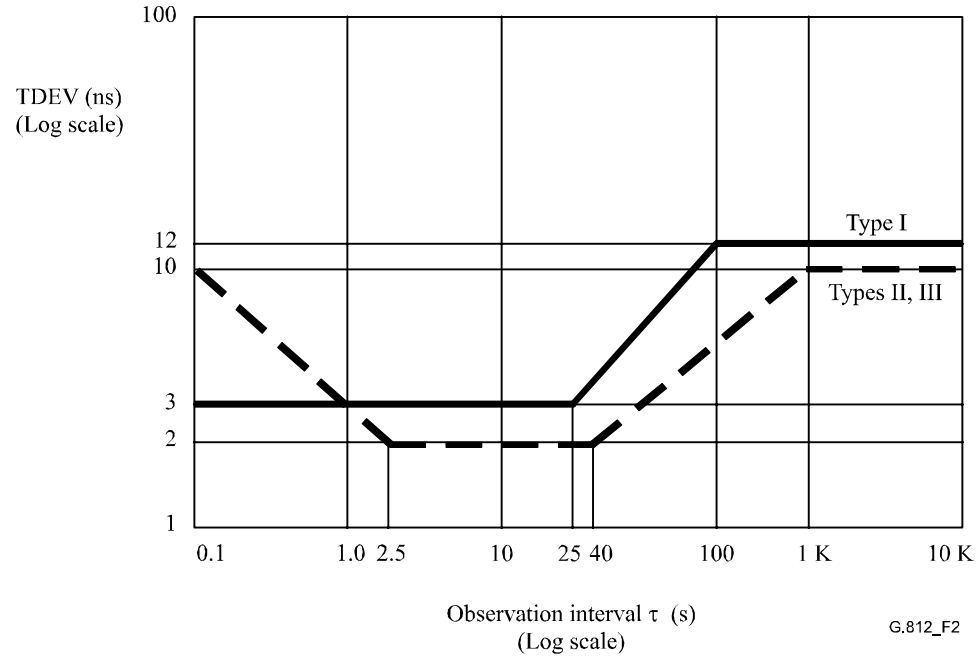

Figure 2/G.812 – Wander generation (TDEV) for constant temperature

8.2 Non-locked wander

When a clock is not locked to a synchronization reference, the random noise components are negligible compared to deterministic effects like initial frequency offset. Consequently, the non-locked wander effects are included in 11.2.

8.3 Jitter

While most requirements in this Recommendation are independent of the output interface at which they are measured, this is not the case for jitter production; jitter generation requirements utilize existing Recommendations that have different limits for different interface rates. These requirements are stated separately for the interfaces identified in clause 12. To be consistent with other jitter requirements, the values are in UI peak-peak, where the UI corresponds to the reciprocal of the bit rate of the interface.

Note that all filter values for STM-N interfaces specified in this clause have been harmonized with the filter values for the network limit as specified in ITU-T Rec. G.825.

NOTE – Due to the stochastic nature of jitter, the peak-peak values given in this clause eventually are exceeded. The requirements should therefore be fulfilled in at least 99% of all measurements made.

8.3.1 Output jitter at 2048 kHz and 2048 kbit/s interfaces

In the absence of input jitter, the intrinsic jitter at 2048 kHz and 2048 kbit/s output interfaces as measured over a 60-second interval should not exceed 0.05 UI peak-peak when measured through a single pole band-pass filter with corner frequencies at 20 Hz and 100 kHz.

8.3.2 Output jitter at a 1544 kbit/s interface

In the absence of input jitter, the intrinsic jitter at a 1544 kbit/s output interface should not exceed 0.05 UI peak-peak when measured through a single pole band-pass filter with corner frequencies at 10 Hz and 40 kHz. The measurement interval is for further study.

8.3.3 Output jitter at an STM-N interface

In the absence of input jitter at the synchronization interface, the intrinsic jitter at optical STM-N output interfaces as measured over a 60-second interval should not exceed the limits given in Table 8 below. The allowed jitter on an STM-1 electrical (CMI) interface is also given in Table 8 below.

The measurement filter roll-off at the lower cut-off frequency shall be 20 dB/decade and the roll-off at the upper cut-off frequency shall be 60 dB/decade. The characteristic of the upper cut-off filter roll-off is for further study.

Table 8/G.812 – STM-N jitter generation

Interface	Measuring filter (–3 dB frequencies)	Peak-peak amplitude (UI)
STM-1 electrical	500 Hz to 1.3 MHz	0.50
	65 kHz to 1.3 MHz	0.075
STM-1 optical	500 Hz to 1.3 MHz	0.50
	65 kHz to 1.3 MHz	0.10
STM-4	1000 Hz to 5 MHz	0.50
	250 kHz to 5 MHz	0.10
STM-16	5000 Hz to 20 MHz	0.50
	1 MHz to 20 MHz	0.10
For STM-1: 1 UI = 6.43 ns. For STM-4: 1 UI = 1.61 ns. For STM-16: 1 UI = 0.40 ns.		

9 Noise tolerance

The noise tolerance of a G.812 clock indicates the lower limit of the maximum phase noise level at the input of the clock that should be accommodated while:

- Maintaining the clock within prescribed performance limits. The exact performance limits are for further study.
- Not causing any alarms.
- Not causing the clock to switch reference.
- Not causing the clock to go into hold-over.

In general, the noise tolerance of a G.812 clock is the same as the network limit for the synchronization interface in order to maintain acceptable performance. However, the synchronization interface network limit may be different according to the application. Therefore, in order to determine the slave clock noise tolerance, the worst-case network limit should be used. An explanation of the different network limits for acceptable payload performance is given in Appendix I/G.813 for information.

The wander and jitter tolerances given in 9.1 and 9.2 represent the worst levels that a synchronization carrying interface should exhibit. The TDEV signal used for a conformance test should be generated by adding white, gaussian noise sources, each of which has been filtered to obtain the proper type of noise process with the proper amplitude. Guidance is provided in Appendix II.

MTIE and TDEV are measured through an equivalent 10 Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 second. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\ \tau$).

9.1 Wander tolerance

9.1.1 MTIE wander tolerance

The G.812 clock input wander tolerance expressed as an MTIE limit is given in Table 9 for Type I node clocks and in Table 10 for Types II and III node clocks.

Table 9/G.812 – Input wander tolerance (MTIE) for Type I node clock

MTIE limit (μs)	Observation interval τ (s)
0.75	$0.1 < \tau \leq 7.5$
0.1 τ	$7.5 < \tau \leq 20$
2	$20 < \tau \leq 400$
0.005 τ	$400 < \tau \leq 1000$
5	$1000 < \tau \leq 10\ 000$

Table 10/G.812 – Input wander tolerance (MTIE) for Types II and III node clocks

MTIE limit (μs)	Observation interval τ (s)
0.3 + 0.002 5 τ	$0.05 < \tau \leq 280$
0.997 + 0.000 01 τ	$\tau > 280$

The resultant requirements are shown in Figure 3.

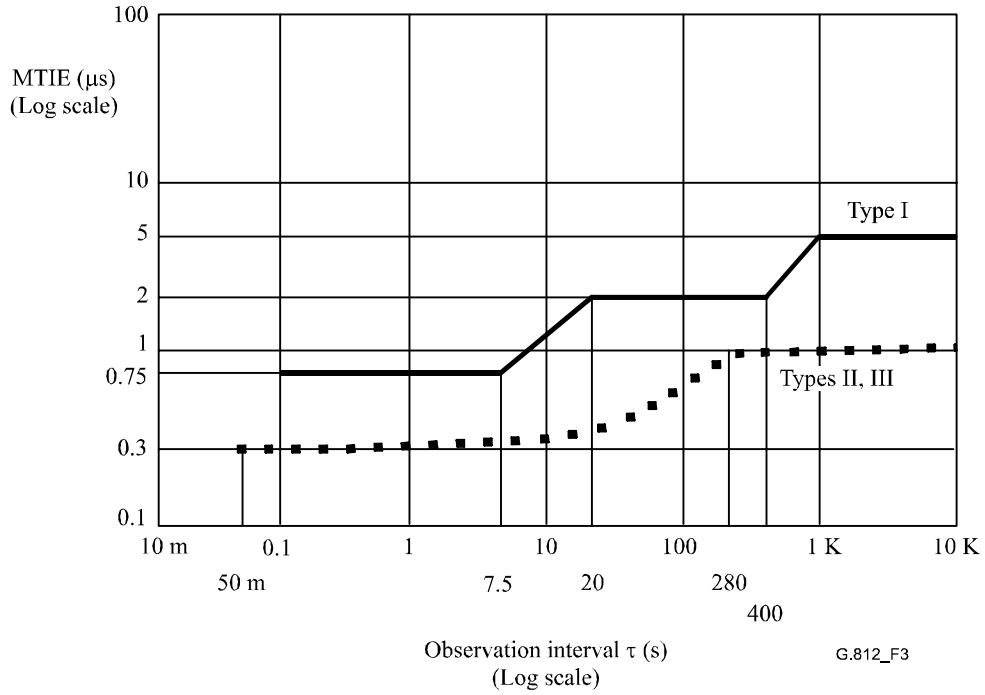

Figure 3/G.812 – Input wander tolerance (MTIE)

9.1.2 TDEV wander tolerance

The G.812 clock input wander tolerance expressed as a TDEV limit is given in Table 11 for Type I node clocks and in Table 12 for Types II and III node clocks.

Table 11/G.812 – Input wander tolerance (TDEV) for Type I node clock

TDEV limit (ns)	Observation interval τ (s)
34	$0.1 < \tau \leq 20$
$1.7 \times \tau$	$20 < \tau \leq 100$
170	$100 < \tau \leq 1000$
$5.4 \times \tau^{0.5}$	$1000 < \tau \leq 10\,000$

Table 12/G.812 – Input wander tolerance (TDEV) for Types II and III node clocks

TDEV limit (ns)	Observation interval τ (s)
FFS	$\tau \leq 0.05$
100	$0.05 < \tau \leq 10$
$31.6\ \tau^{0.5}$	$10 < \tau \leq 1000$
FFS	$\tau > 1000$
FFS For further study	

The resultant requirements are shown in Figure 4.

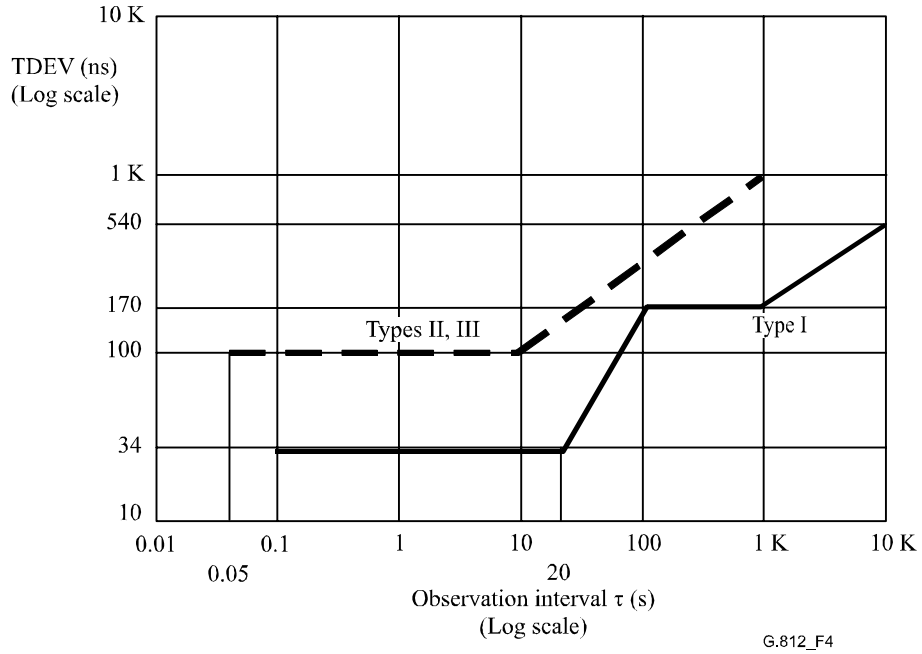

Figure 4/G.812 – Input wander tolerance (TDEV)

9.1.3 Sinusoidal wander tolerance

While suitable test signals that check conformance to the mask in Figure 3 are being studied, test signals with a sinusoidal phase variation can be used. The requirements for Type I node clocks are shown in Table 13. The requirements for Types II and III are shown in Table 14.

Table 13/G.812 – Lower limit of maximum tolerable sinusoidal input wander for Type I node clocks

Peak-peak wander amplitude (μs)	Frequency f (Hz)
5	$0.000\,012 < f \leq 0.000\,32$
$0.001\,6 \times f^{-1}$	$0.000\,32 < f \leq 0.000\,8$
2	$0.000\,8 < f \leq 0.016$
$0.032 \times f^{-1}$	$0.016 < f \leq 0.043$
0.75	$0.043 < f \leq 1$

Table 14/G.812 – Lower limit of maximum tolerable sinusoidal input wander for Types II and III node clocks

Peak-peak wander amplitude (μs)	Frequency f (Hz)
$0.997 + [4 \times 10^{-6}/f]$	$0.000\,031\,8 < f \leq 0.001\,43$
$0.3 + [0.001/f]$	$0.001\,43 < f \leq 10$

The resultant requirements are shown in Figure 5.

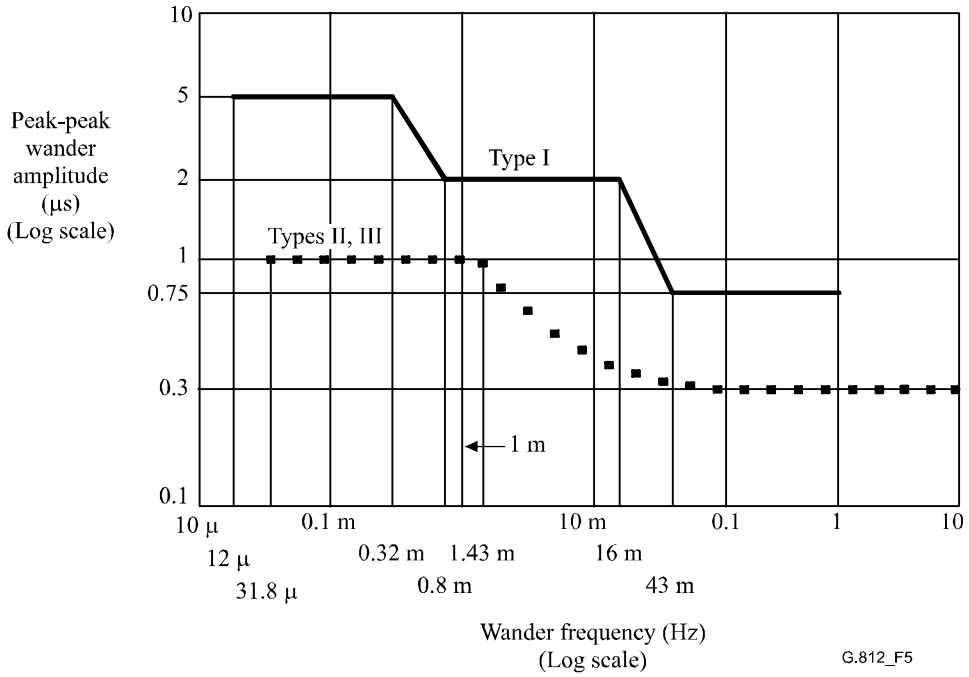

Figure 5/G.812 – Lower limit of maximum tolerable sinusoidal input wander

9.2 Jitter tolerance

9.2.1 Jitter tolerance at 2048 kHz and 2048 kbit/s interfaces

The lower limit of maximum tolerable sinusoidal input jitter for a Type I node clock is given in Table 15 and Figure 6 for both 2048 kHz and 2048 kbit/s input ports.

Table 15/G.812 – Lower limit of maximum tolerable sinusoidal input jitter for Type I node clock

Peak-peak jitter amplitude (ns)	Frequency f (Hz)
750	$1 < f \leq 2400$
$1.8 \times 10^6 f^{-1}$	$2400 < f \leq 18\,000$
100	$18\,000 < f < 100\,000$

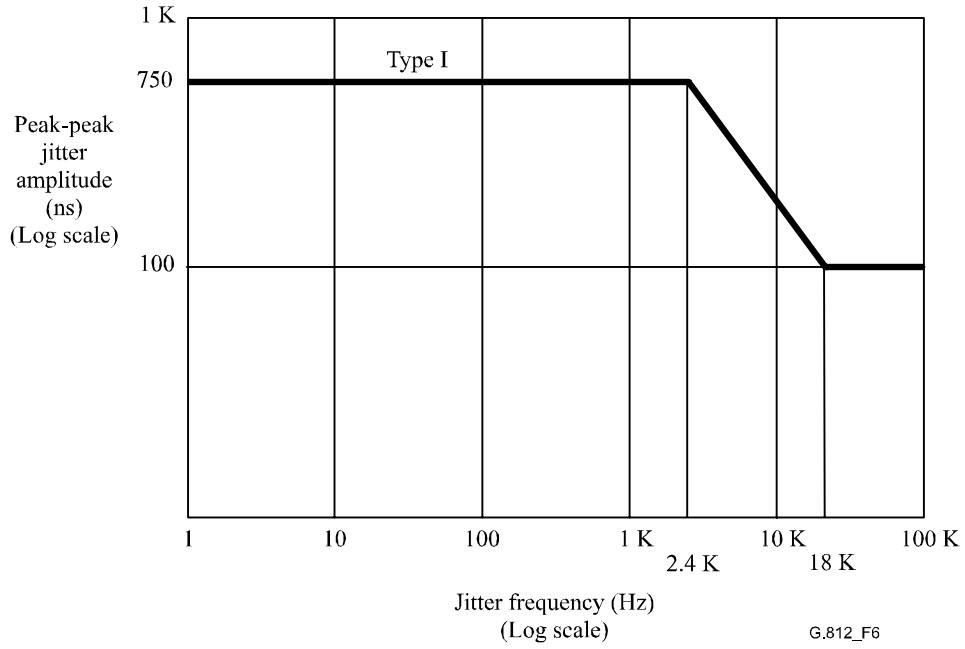

Figure 6/G.812 – Lower limit of maximum tolerable sinusoidal input jitter for Type I node clocks

9.2.2 Jitter tolerance at a 1544 kbit/s interface

The lower limit of maximum tolerable sinusoidal input jitter for Types II and III node clocks is given in Table 16 and Figure 7 for 1544 kbit/s input ports.

Table 16/G.812 – Lower limit of maximum tolerable sinusoidal input jitter for Types II and III node clocks

Peak-peak jitter amplitude (UI)	Frequency f (Hz)
5	$10 < f \leq 500$
$5 \times [500/f]^{1.411}$	$500 < f \leq 8000$
0.1	$8000 < f \leq 40\,000$

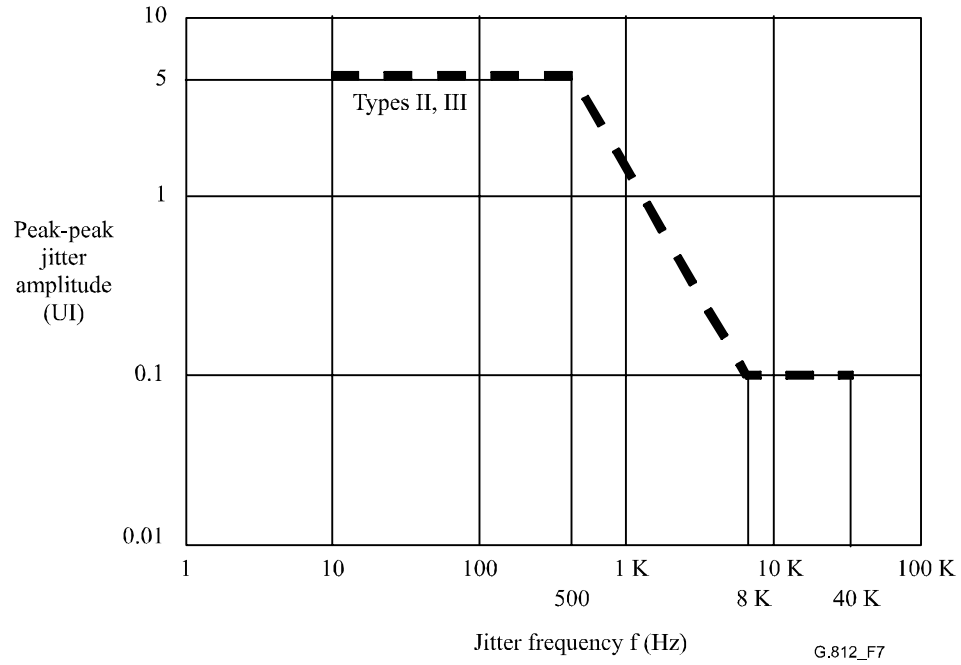

Figure 7/G.812 – Lower limit of maximum tolerable sinusoidal input jitter for Types II and III node clocks

9.2.3 Jitter tolerance at an STM-N interface

Jitter tolerance for STM-N interfaces is given in ITU-T Rec. G.825.

10 Noise transfer

The transfer characteristic of a slave clock determines its properties with regard to the transfer of excursions of the input phase relative to the phase modulation. Noise transfer can be described in two ways:

a) The slave clock can be viewed as a low-pass filter for the differences between the actual input phase and the ideal input phase of the reference. The maximum allowed bandwidth for this low-pass filter behaviour is defined in Table 17 below, along with the maximum allowed gain in the passband.

Table 17/G.812 – Noise transfer requirements

	Type I	Type II	Type III
Maximum bandwidth (mHz)	3	1	1
Maximum gain (dB)	0.2	0.2	0.2

The above applies to a linear G.812 clock model. However, this model should not restrict implementations.

b) Noise transfer describes the amount of noise observed at the output, as a result of noise introduced at the input of the clock. The slave clock, when subjected to a wideband noise signal shaped as described in 9.1 (i.e., the TDEV input tolerance specification) shall produce an output signal lying below the limit specified in Table 18 for Type I node clocks and in Table 19 for Types II and III node clocks. The resultant requirements are shown in Figure 8. These masks should not be used to verify phase gain peaking.

Table 18/G.812 – Output wander mask (TDEV) for Type I node clock

TDEV limit (ns)	Observation interval τ (s)
3	$0.1 < \tau \leq 13.1$
$0.017\ 6\ \tau^2$	$13.1 < \tau \leq 100$
176	$100 < \tau \leq 1000$
$5.58\ \tau^{0.5}$	$1000 < \tau \leq 10\ 000$

NOTE – The values in Table 18 include the effects of gain peaking and intrinsic noise.

Table 19/G.812 – Output wander mask (TDEV) for Types II and III node clocks

TDEV limit (ns)	Observation interval τ (s)
$3.2\ \tau^{-0.5}$	$0.1 < \tau \leq 1.44$
$1.86\ \tau$	$1.44 < \tau \leq 300$
$32.2\ \tau^{0.5}$	$300 < \tau \leq 1000$

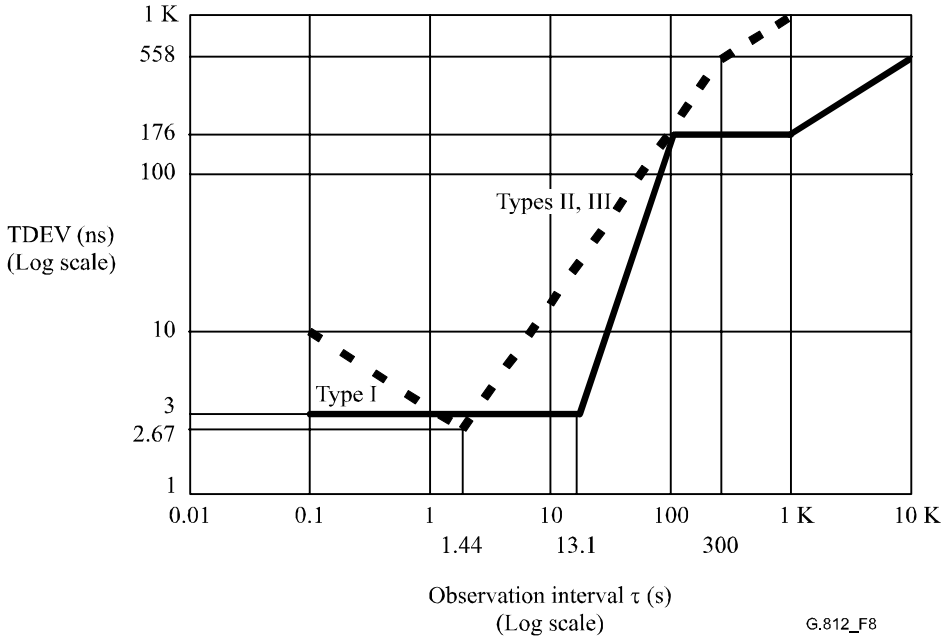

Figure 8/G.812 – Output wander mask (TDEV)

Guidance on the measurement techniques for these requirements is given in Appendix II.

MTIE and TDEV are measured through an equivalent 10 Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 second. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\ \tau$).

11 Transient response and hold-over performance

The requirements in this clause apply to situations where the input signal is affected by disturbances or transmission failures (e.g., short interruptions, switching between different synchronization signals, loss of reference, etc.) that result in phase transients at the G.812 output (see clause 12). The ability to withstand disturbances is necessary to avoid transmission defects or failures. Transmission failures and disturbances are common stress conditions in the transmission environment.

To ensure transmission integrity, it is recommended that all the phase movements at the output of the G.812 clock stay within the level described in the following subclauses.

11.1 Short-term phase transient response

This requirement reflects the performance of the clock in cases when the (selected) input reference is lost due to a failure in the reference path and a second reference input signal, traceable to the same reference clock, is available simultaneously or shortly after the detection of the failure (e.g., in cases of autonomous restoration).

The output jitter limit in 8.3 should be met.

11.1.1 Transient for Type I node clocks (2048 kHz and 2048 kbit/s interfaces)

The MTIE of the phase error should not exceed the limits given in Table 20 and illustrated by the dashed curve in Figure 9.

Table 20/G.812 – Transient for Type I node clocks (2048 kHz and 2048 kbit/s interfaces)

MTIE limit (ns)	Observation interval τ (s)
25	$0.001 < \tau \leq 0.003\ 3$
$7500\ \tau$	$0.003\ 3 < \tau \leq 0.016$
$120 + 0.5\ \tau$	$0.016 < \tau \leq 240$
240	$240 < \tau \leq 1000$

11.1.2 Transient for Type I node clocks (STM-N interfaces)

The MTIE of the phase error should not exceed the limits given in Table 21 and illustrated by the solid curve in Figure 9.

Table 21/G.812 – Transient for Type I node clocks (STM-N interfaces)

MTIE limit (ns)	Observation interval τ (s)
$7500\ \tau$	$0.001 < \tau \leq 0.016$
$120 + 0.5\ \tau$	$0.016 < \tau \leq 240$
240	$240 < \tau \leq 10\ 000$

11.1.3 Transient for Types II and III node clocks (1544 kbit/s interfaces)

The MTIE of the phase error should not exceed the limits given in Table 22 and illustrated by the dashed curve in Figure 9.

Table 22/G.812 – Transient for Types II and III node clocks (1544 kbit/s interfaces)

MTIE limit (ns)	Observation interval τ (s)
40 + 885 τ	0.014 < τ ≤ 0.16
182	0.16 < τ ≤ 280

11.1.4 Transient for Types II and III node clocks (STM-N interfaces)

The MTIE of the phase error should not exceed the limits given in Table 23 and illustrated by the solid curve in Figure 9.

Table 23/G.812 – Transient for Types II and III node clocks (STM-N interfaces)

MTIE limit (ns)	Observation interval τ (s)
7.6 + 885 τ	0.014 < τ ≤ 0.16
150	0.16 < τ ≤ 280

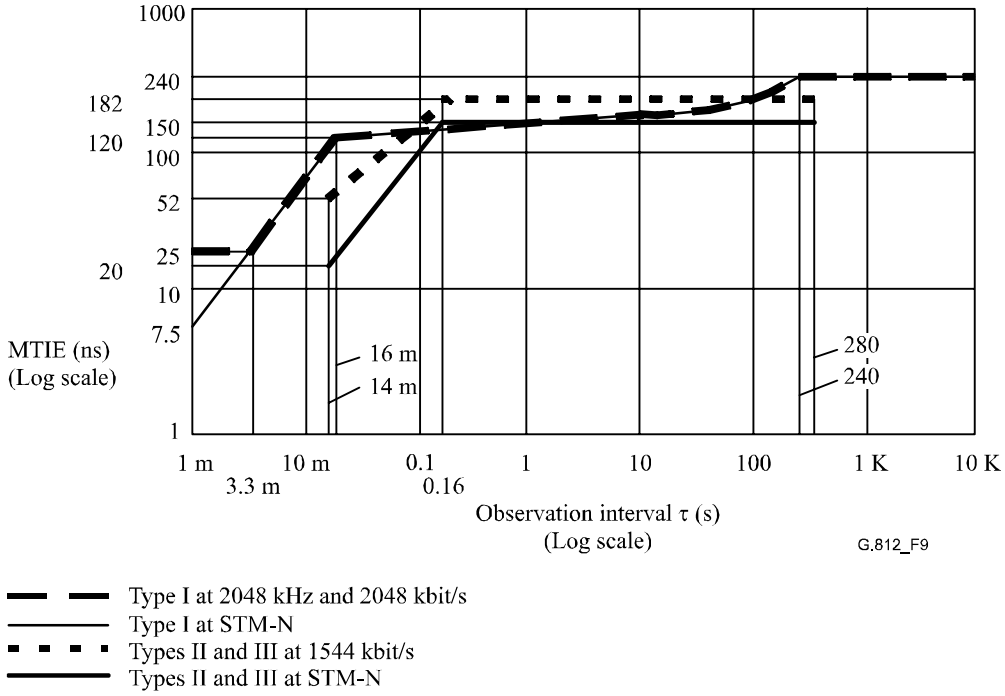

Figure 9/G.812 – Short-term phase transient mask (MTIE)

11.2 Long-term phase transient response (hold-over)

When a G.812 clock loses all its references, it enters the hold-over state. This requirement bounds the maximum excursions in the output timing signal. Additionally, it restricts the accumulation of the phase movement during input signal impairments or internal disturbances.

11.2.1 Clock Types I and III

The Phase Error, Δx, at the output of the slave clock from the moment of loss of reference should, over any period of S seconds, meet the following:

$$|\Delta x(S)| \leq \{(\mathbf{a}_1 + \mathbf{a}_2)S + 0.5\,\mathbf{b}\,S^2 + \mathbf{c}\}[\text{ns}]$$

The derivative of Δx(S), the fractional frequency offset, should, over any period of S seconds, meet the following:

$$|d(\Delta x(S))/dS| \leq \{\mathbf{a_1} + \mathbf{a_2} + \mathbf{b}S\}[\text{ns/s}]$$

The second derivative of Δx(S), the fractional frequency drift, should, over any period of S seconds, meet the following:

$$\left|d^2(\Delta x(S))/dS^2\right| \leq \mathbf{d}\left[\text{ns/s}^2\right]$$

In applying the above requirements for the derivative of Δx(S) and the second derivative of Δx(S), the period S must begin after any transient associated with entry into hold-over is over. During this transient period, the transient requirements of 11.1 apply.

NOTE 1 – $\mathbf{a}_1$ represents an initial frequency offset under constant temperature conditions (±1 K).

NOTE 2 – $\mathbf{a}_2$ accounts for temperature variations after the clock went into hold-over. If there are no temperature variations, the term $\mathbf{a}_2$ S should not contribute to the phase error.

NOTE 3 – **b** represents the average frequency drift caused by aging. This value is derived from typical aging characteristics after 60 days of continuous operation. It is not intended to measure this value on a per day basis, as the temperature effect will dominate.

NOTE 4 – The phase offset **c** takes care of any additional phase shift that may arise during the transition at the entry of the hold-over state.

NOTE 5 – **d** represents the maximum temporary frequency drift rate at constant temperature allowed during hold-over. However, it is not required that **d** and **b** be equal.

The permissible phase error specifications for different G.812 clock Types are shown in Table 24.

Table 24/G.812 – Transient response specifications during hold-over

	Type I	**Type III**
$\mathbf{a}_1$ (ns/s)	0.5	1.0
$\mathbf{a}_2$ (ns/s)	2	10
b (ns/s^2)	2.3×10^{-6}	1.16×10^{-5}
c (ns)	60	150
d (ns/s^2)	NA	1.16×10^{-5}
NA Not applicable		

During the transition at the entry of hold-over state, the temporary frequency offset on SDH output interfaces of Type I node clocks should not exceed 7.5 ppm.

11.2.2 Clock Type II

The derivative of the phase Δx(S), the fractional frequency offset, should, over any period of S seconds, meet the following:

$$\left|d(\Delta x(S))/dS\right| \leq Y(S)$$

where Y(S) is the maximum fractional frequency offset as given in Table 25 and shown in Figure 10 below. Y(S) begins 5000 s after entry into hold-over, i.e., Y(S) is not defined for S less than 5000 s, to ensure that any transient associated with entry into hold-over is over. During the first 5000 s, the transient requirements of 11.1 (Table 22 and Figure 9) apply.

Table 25/G.812 – Maximum fractional frequency offset Y(S) for Type II hold-over

Maximum fractional frequency offset Y(S) (ns/s)	Time S (s)
ND	$0 < S \leq 5000$
0.1	$5000 < S \leq 86\,400$
1.16×10^{-6} S	$86\,400 < S \leq 1.38 \times 10^{7}$
16	$1.38 \times 10^{7} < S \leq 3.2 \times 10^{7}$
ND Not defined	

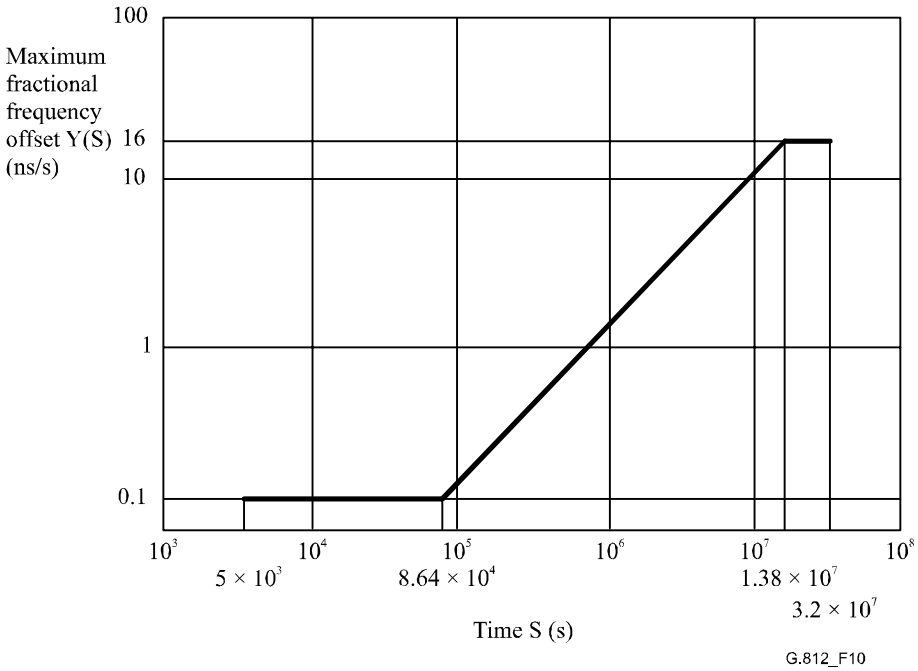

Figure 10/G.812 – Maximum fractional frequency offset Y(S) for Type II hold-over

11.3 Phase response to input signal interruptions

For short-term interruptions on synchronization input signals, that do not cause reference switching, the output phase variation is for further study.

11.4 Phase discontinuity

In cases of infrequent internal testing or rearrangement operations within the slave clock, the phase transient at the output of G.812 clocks should meet the MTIE specifications in Table 26 for Type I node clock and Table 27 for Types II and III node clocks.

Table 26/G.812 – Output phase transient (MTIE) for Type I node clock

MTIE limit (ns)	Observation interval τ (s)
60	$\tau \leq 0.001$
120	$0.001 < \tau \leq 4$
240	$\tau > 4$

In case the G.812 Type I clock is built-in into an SDH equipment, the temporary frequency offset at any STM-N output interface should never exceed 7.5 ppm.

Table 27/G.812 – Output phase transient (MTIE) for Types II and III node clocks

MTIE limit (ns)	Observation interval τ (s)
61 000 τ	$0.001\ 33 < \tau \leq 0.016\ 4$
1000	$0.016\ 4 < \tau$

The resultant requirements are shown in Figure 11.

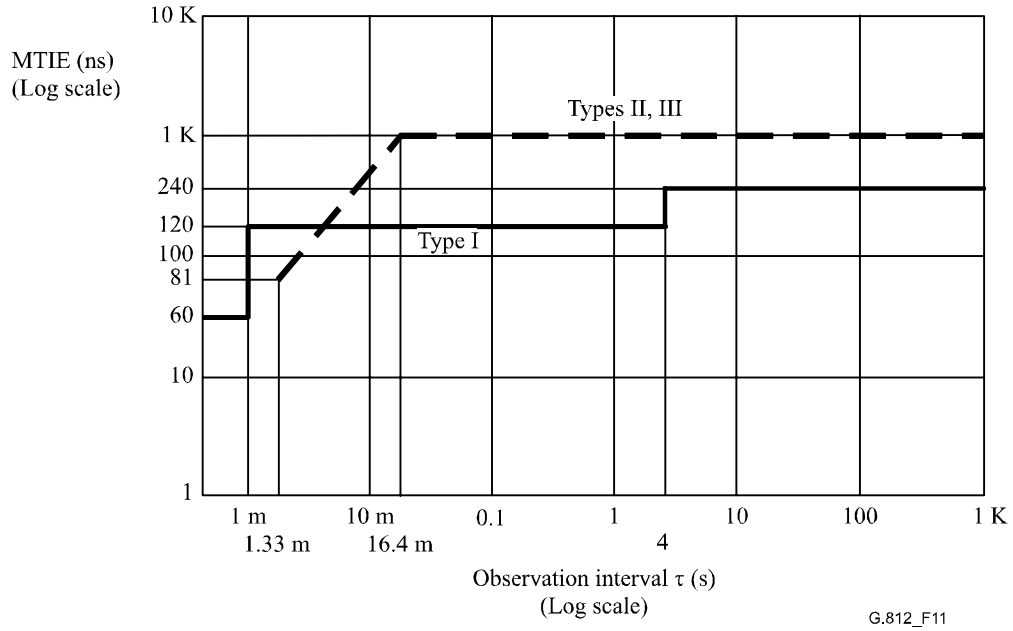

Figure 11/G.812 – Output phase transient requirements (MTIE)

12 Interfaces

The requirements in this Recommendation are related to reference points internal to the Network Elements (NEs) in which the clock is embedded and are therefore not necessarily available for measurement or analysis by the user. Therefore the performance of the G.812 clock is not defined at these internal reference points, but rather at the external interfaces of the equipment. The external input and output are:

- 1544 kbit/s interfaces according to ITU-T Rec. G.703.
- 2048 kHz external interfaces according to ITU-T Rec. G.703.
- 2048 kbit/s interfaces according to ITU-T Rec. G.703.
- STM-N traffic interfaces according to ITU-T Recs G.703 and G.957.

Note that all of the above interfaces may not be implemented on all equipment. These interfaces should comply with the additional jitter and wander requirements as defined in this Recommendation.

Annex A

Specifications for Types IV, V and VI clocks

The Type V clock is the transit node clock from the 1988 version of this Recommendation; the Type VI clock is the local node clock from the 1988 version of this Recommendation.

A.1 Frequency accuracy

Under prolonged hold-over conditions, the output frequency accuracy of the different Types of node clocks should not exceed the values in Table A.1 with regard to a reference traceable to a primary reference clock, over a time period T as reported in the same Table.

Table A.1/G.812 – Output frequency accuracy requirements

	Type IV	Type V	Type VI
Accuracy	4.6×10^{-6}	NA	NA
Period T	1 year	NA	NA
NA Not applicable NOTE – The time period T applies after 30 days of continuous synchronized operation.			

A.2 Pull-in, hold-in and pull-out ranges

The minimum pull-in, hold-in and pull-out ranges for the different Types of node clocks should be according to Table A.2, whatever the internal oscillator frequency offset may be.

Table A.2/G.812 – Pull-in, hold-in, and pull-out requirements

	Type IV	Type V	Type VI
Pull-in	4.6×10^{-6}	ND	ND
Hold-in	4.6×10^{-6}	ND	ND
Pull-out	NA	ND	ND
NA Not applicable ND Not defined			

A.3 Noise generation

The noise generation of a slave clock represents the amount of phase noise produced at the output when there is an ideal input reference signal or the clock is in hold-over state (see A.6.2). A suitable reference, for practical testing purposes, implies a performance level at least 10 times more stable than the output requirements. The ability of the clock to limit this noise is described by its frequency stability. The measures MTIE and Time Deviation (TDEV) are useful for characterization of noise generation performance.

MTIE and TDEV are measured through an equivalent 10 Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 second. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\ \tau$).

A.3.1 Wander in locked mode

When the slave clock is in the locked mode of operation, the MTIE at constant temperature (within ±1 K) measured using the synchronized clock configuration defined in Figure 1-a/G.810 should have the limits given in Tables A.3 and A.4 for the different Types of node clocks.

Table A.3/G.812 – Wander generation (MTIE) for Type IV node clock at constant temperature (within ±1 K)

MTIE limit (ns)	Observation interval τ (s)
40	$0.1 < \tau \leq 1$
$40 \times \tau^{0.4}$	$1 < \tau \leq 10$
100	$\tau > 10$

Table A.4/G.812 – Wander generation (MTIE) for Types V and VI node clocks at constant temperature (within ±1 K)

MTIE limit (ns)	Observation interval τ (s)
FFS	$0.05 < \tau \leq 100$
1000	$\tau > 100$
FFS For further study	

The resultant requirements are shown in Figure A.1.

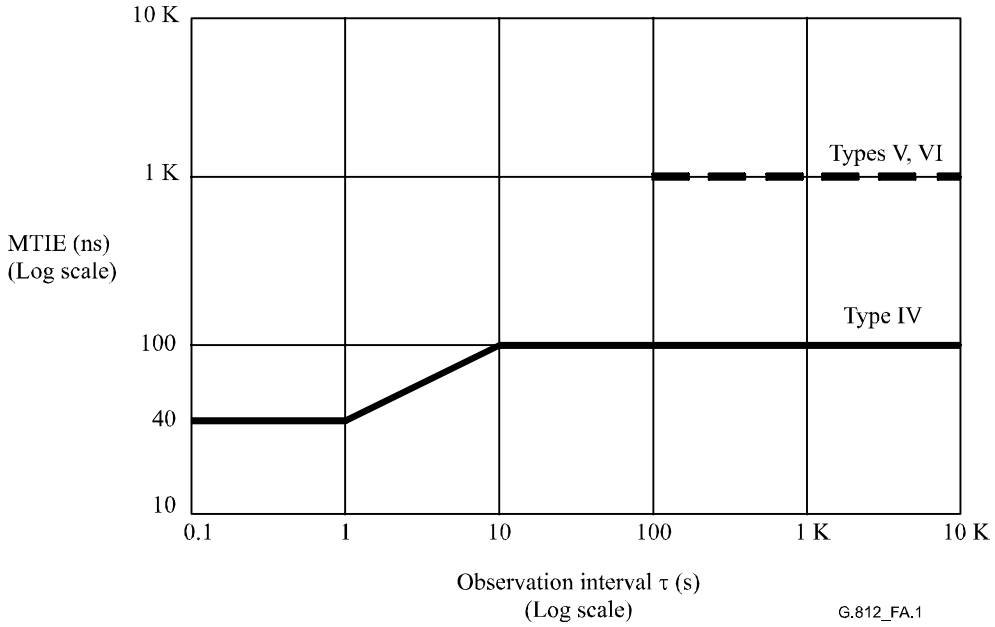

Figure A.1/G.812 – Wander generation (MTIE) at constant temperature (within ±1 K)

When the node clock is in the locked mode of operation, the TDEV at constant temperature (within ±1 K) measured using the synchronized clock configuration defined in Figure 1-a/G.810 should have the limits given in Tables A.5 and A.6 for the different Types of node clock.

Table A.5/G.812 – Wander generation (TDEV) for Type IV node clock at constant temperature (within ±1 K)

TDEV limit (ns)	Observation interval τ (s)
$3.2\ \tau^{-0.5}$	$0.1 < \tau \leq 2.5$
2	$2.5 < \tau \leq 40$
$0.32\ \tau^{0.5}$	$40 < \tau \leq 1000$
10	$\tau > 1000$

Table A.6/G.812 – Wander generation (TDEV) for Types V and VI node clocks at constant temperature (within ±1 K)

TDEV limit (ns)	Observation interval τ (s)
FFS	$0.1 < \tau < 10\ 000$
FFS For further study	

The resultant requirements are shown in Figure A.2.

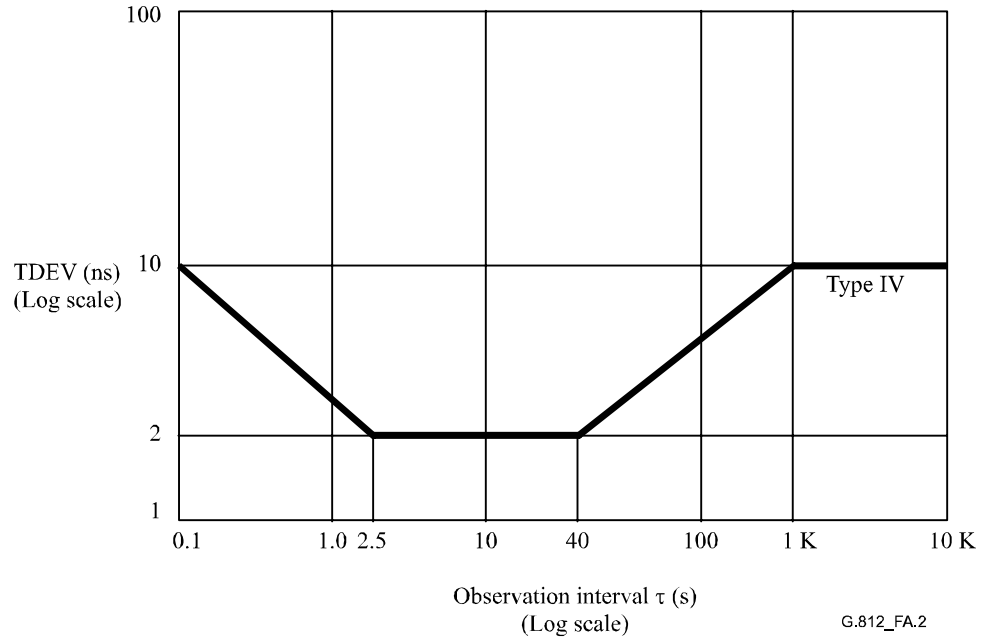

Figure A.2/G.812 – Wander generation (TDEV) for constant temperature

A.3.2 Non-locked wander

When a clock is not locked to a synchronization reference, the random noise components are negligible compared to deterministic effects like initial frequency offset. Consequently the non-locked wander effects are included in A.6.2.

A.3.3 Jitter

While most requirements in this Recommendation are independent of the output interface at which they are measured, this is not the case for jitter production; jitter generation requirements utilize existing Recommendations that have different limits for different interface rates. These requirements are stated separately for the interfaces identified in A.7. To be consistent with other jitter requirements, the values are in UI peak-peak, where the UI corresponds to the reciprocal of the bit rate of the interface.

Note that all filter values specified in this generation clause for STM-N interfaces have been harmonized with the filter values for the network limit as specified in ITU-T Rec. G.825.

NOTE – Due to the stochastic nature of jitter, the peak-peak values given in this clause eventually are exceeded. The requirements should therefore be fulfilled in at least 99% of all measurements made.

A.3.3.1 Output jitter at 2048 kHz and 2048 kbit/s interfaces

In the absence of input jitter, the intrinsic jitter at 2048 kHz and 2048 kbit/s output interfaces as measured over a 60-second interval should not exceed 0.05 UI peak-peak when measured through a single pole band-pass filter with corner frequencies at 20 Hz and 100 kHz.

A.3.3.2 Output jitter at a 1544 kbit/s interface

In the absence of input jitter, the intrinsic jitter at a 1544 kbit/s output interface should not exceed 0.05 UI peak-peak when measured through a single pole band-pass filter with corner frequencies at 10 Hz and 40 kHz (the measurement interval is for further study).

A.3.3.3 Output jitter at an STM-N interface

In the absence of input jitter at the synchronization interface, the intrinsic jitter at optical STM-N output interfaces as measured over a 60-second interval should not exceed the limits given in Table A.7 below. The allowed jitter on an STM-1 electrical (CMI) interface is also given in Table A.7 below.

The measurement filter roll-off at the lower cut-off frequency shall be 20 dB/decade and the roll-off at the upper cut-off frequency shall be 60 dB/decade. The characteristic of the upper cut-off filter roll-off is for further study.

Table A.7/G.812 – STM-N jitter generation

Interface	Measuring filter (–3 dB frequencies)	Peak-peak amplitude (UI)
STM-1 electrical	500 Hz to 1.3 MHz	0.50
	65 kHz to 1.3 MHz	0.075
STM-1 optical	500 Hz to 1.3 MHz	0.50
	65 kHz to 1.3 MHz	0.10
STM-4	1000 Hz to 5 MHz	0.50
	250 kHz to 5 MHz	0.10
STM-16	5000 Hz to 20 MHz	0.50
	1 MHz to 20 MHz	0.10
For STM-1: 1 UI = 6.43 ns. For STM-4: 1 UI = 1.61 ns. For STM-16: 1 UI = 0.40 ns.		

A.4 Noise tolerance

The noise tolerance of a G.812 clock indicates the lower limit of the maximum phase noise level at the input of the clock that should be accommodated while:

- Maintaining the clock within prescribed performance limits. The exact performance limits are for further study.
- Not causing any alarms.
- Not causing the clock to switch reference.
- Not causing the clock to go into hold-over.

In general, the noise tolerance of a G.812 clock is the same as the network limit for the synchronization interface in order to maintain acceptable performance. However, the synchronization interface network limit may be different according to the application. Therefore, in order to determine the slave clock noise tolerance, the worst-case network limit should be used. An explanation of the different network limits for acceptable payload performance is given in Appendix I/G.813 for information.

The wander and jitter tolerances given in A.4.1 and A.4.2 represent the worst levels that a synchronization carrying interface should exhibit. The TDEV signal used for a conformance test should be generated by adding white, gaussian noise sources, each of which has been filtered to obtain the proper type of noise process with the proper amplitude. Guidance is provided in Appendix II.

MTIE and TDEV are measured through an equivalent 10 Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 second. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\ \tau$).

A.4.1 Wander tolerance

The G.812 clock input wander tolerance expressed as an MTIE limit is given in Table A.8 for Type IV node clocks.

Table A.8/G.812 – Input wander tolerance (MTIE) for Type IV node clocks

MTIE limit (μs)	Observation interval τ (s)
$0.3 + 0.002\ 5\ \tau$	$0.05 < \tau \leq 280$
$0.997 + 0.000\ 01\ \tau$	$\tau > 280$

The resultant requirement is shown in Figure A.3.

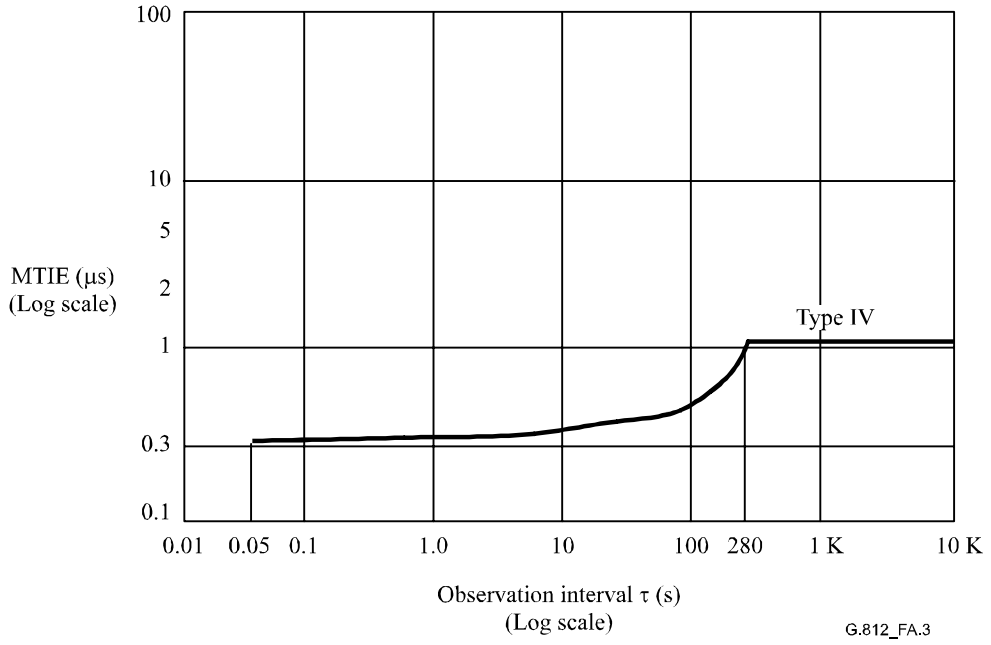

Figure A.3/G.812 – Input wander tolerance (MTIE) for Type IV node clocks

Input wander tolerance in terms of MTIE for Types V and VI is not defined.

The G.812 clock input wander tolerance expressed as a TDEV limit is given in Table A.9 for Type IV node clocks.

Table A.9/G.812 – Input wander tolerance (TDEV) for Type IV node clocks

TDEV limit (ns)	Observation interval τ (s)
FFS	$\tau \leq 0.05$
100	$0.05 < \tau \leq 10$
$31.6\ \tau^{0.5}$	$10 < \tau \leq 1000$
FFS	$\tau > 1000$
FFS For further study	

The resultant requirements are also shown in Figure A.4.

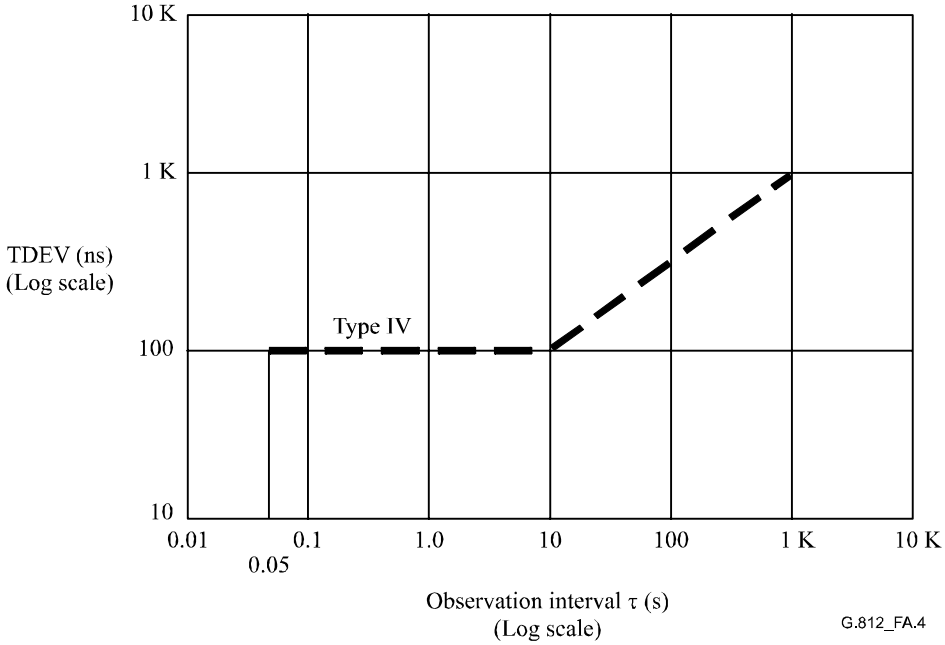

Figure A.4/G.812 – Input wander tolerance for Type IV node clocks (TDEV)

Input wander tolerance in terms of TDEV for Types V and VI is not defined.

While suitable test signals that check conformance to the mask in Figure A.3 are being studied, test signals with a sinusoidal phase variation can be used. The requirements for Type IV node clocks are shown in Table A.10.

Table A.10/G.812 – Lower limit of maximum tolerable sinusoidal input wander for Type IV node clocks

Peak-peak wander amplitude (μs)	Frequency f (Hz)
$0.997 + [4 \times 10^{-6}/f]$	$0.000\ 031\ 8 < f \leq 0.001\ 43$
$0.3 + [0.001/f]$	$0.001\ 43 < f \leq 10$

The resultant requirements are also shown in Figure A.5.

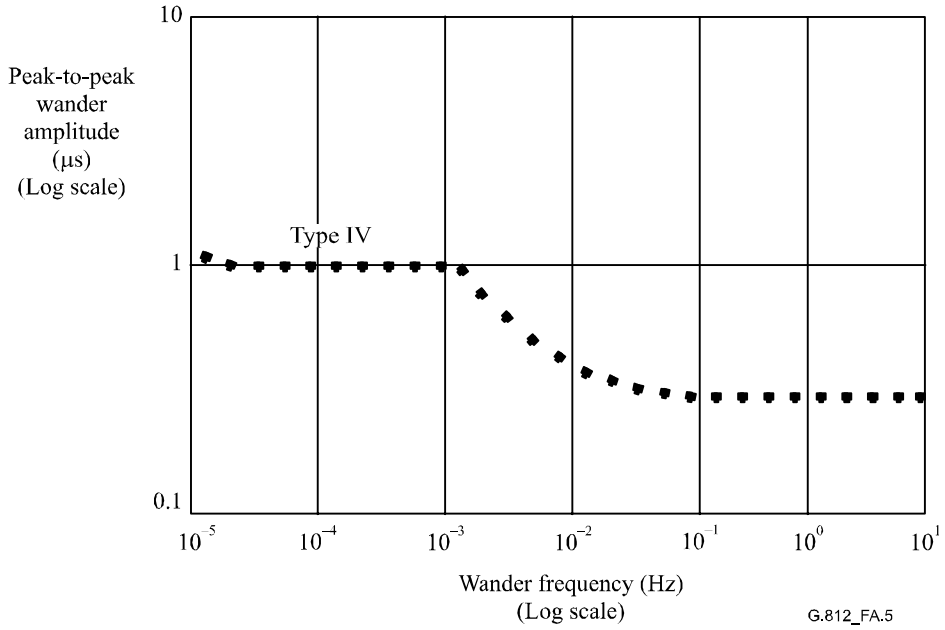

Figure A.5/G.812 – Lower limits of maximum tolerable sinusoidal input wander for Type IV node clocks

Lower limits of maximum tolerable sinusoidal input wander for Types V and VI are not defined.

A.4.2 Jitter tolerance

The lower limit of maximum tolerable sinusoidal input jitter for a Type IV node clock is given in Table A.11 and Figure A.6, for 1544 kbit/s input ports.

Table A.11/G.812 – Lower limit of maximum tolerable sinusoidal input jitter for Type IV node clocks

Peak-peak jitter amplitude (UI)	Frequency f (Hz)
5	$10 < f \leq 500$
$5 \times [500/f]^{1.411}$	$500 < f \leq 8000$
0.1	$8000 < f \leq 40\,000$

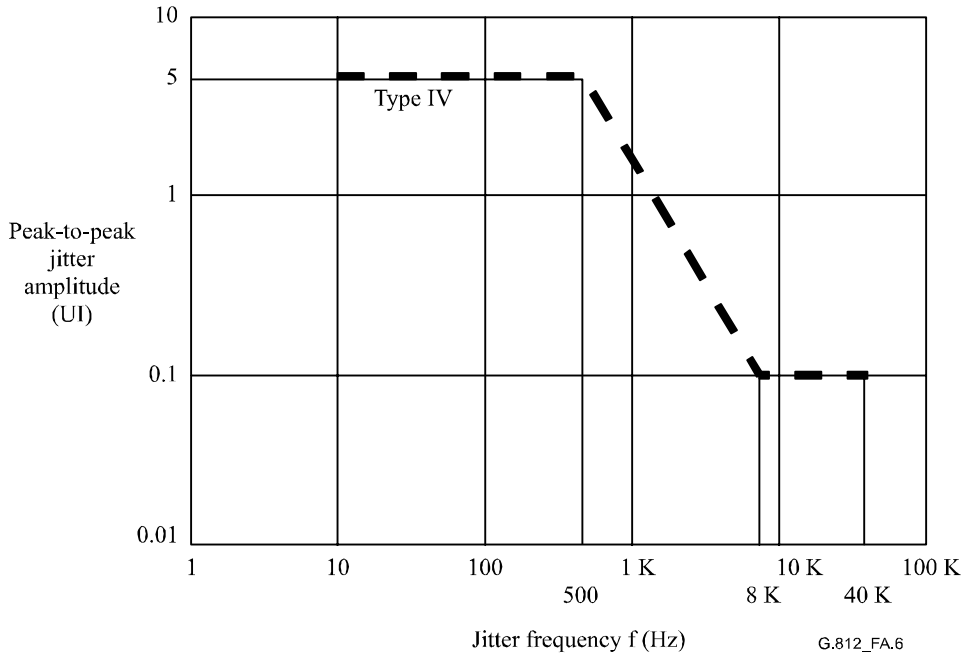

Figure A.6/G.812 – Lower limits of maximum tolerable sinusoidal input jitter for Type IV node clocks

The lower limits of maximum tolerable sinusoidal input jitter for Types V and VI node clocks are not defined.

A.5 Noise transfer

The transfer characteristic of a slave clock determines its properties with regard to the transfer of excursions of the input phase relative to the phase modulation. Noise transfer can be described in two ways:

a) The slave clock can be viewed as a low-pass filter for the differences between the actual input phase and the ideal input phase of the reference. The maximum allowed bandwidth for this low-pass filter behaviour is defined in Table A.12 below, along with the maximum allowed gain in the passband.

Table A.12/G.812 – Noise transfer requirements

	Type IV	Type V	Type VI
Maximum bandwidth (Hz)	3	0.1 (Note)	0.1 (Note)
Maximum gain (dB)	0.2	0.2 (Note)	0.2 (Note)
NOTE – These values are taken from ITU-T Rec. Q.551.			

The above applies to a linear G.812 clock model. However, this model should not restrict implementations.

b) Noise transfer describes the amount of noise observed at the output, as a result of noise introduced at the input of the clock. The slave clock, when subjected to a wideband noise signal shaped as described in A.4 (i.e., the TDEV input tolerance specification), shall produce an output signal lying below the limit specified in Table A.13 for Type IV node clocks. Wander transfer in terms of TDEV for Types V and VI node clocks is not defined. The resultant requirements are shown in Figure A.7. This mask should not be used to verify phase gain peaking.

Table A.13/G.812 – Output wander mask (TDEV) for Type IV node clocks

TDEV limit (ns)	Observation interval τ (s)
1020 τ	$0.05 < \tau \leq 0.1$
102	$0.1 < \tau \leq 10$
$32.2\ \tau^{0.5}$	$10 < \tau \leq 1000$

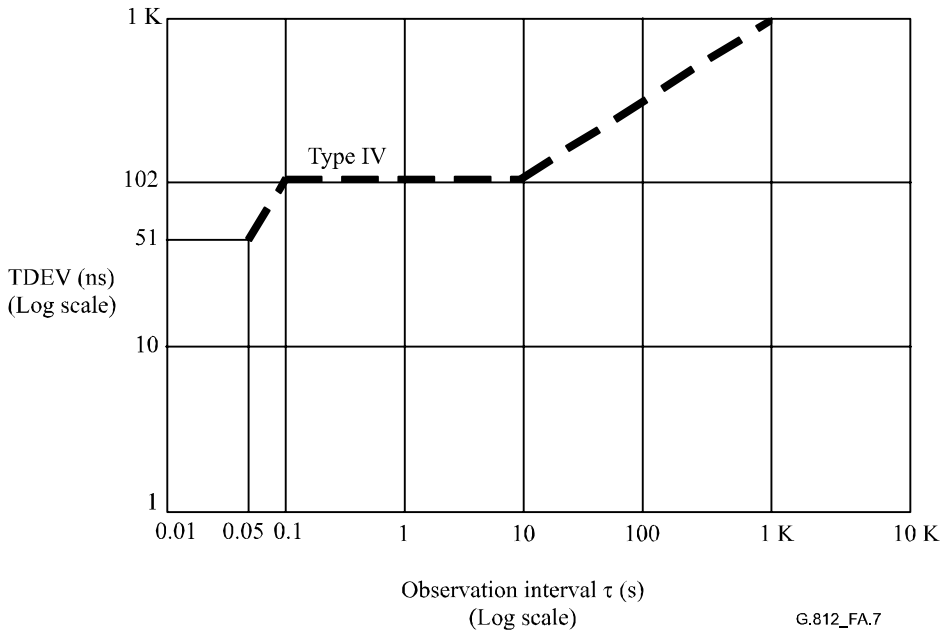

Figure A.7/G.812 – Output wander mask (TDEV)

Guidance on the measurement techniques for these requirements is given in Appendix II.

MTIE and TDEV are measured through an equivalent 10 Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 second. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\ \tau$).

A.6 Transient response and hold-over performance

The requirements in this clause apply to situations where the input signal is affected by disturbances or transmission failures (e.g., short interruptions, switching between different synchronization signals, loss of reference, etc.) that result in phase transients at the G.812 output (see A.7). The ability to withstand disturbances is necessary to avoid transmission defects or failures. Transmission failures and disturbances are common stress conditions in the transmission environment.

To ensure transmission integrity, it is recommended that all the phase movements at the output of the G.812 clock stay within the level described in the following subclauses.

A.6.1 Short-term phase transient response

This requirement reflects the performance of the clock in cases when the (selected) input reference is lost due to a failure in the reference path and a second reference input signal, traceable to the same reference clock, is available simultaneously or shortly after the detection of the failure (e.g., in cases of autonomous restoration).

The output jitter limit in A.3.3 should be met.

A.6.1.1 Transient for Type IV node clocks (1544 kbit/s interfaces)

The MTIE of the phase error should not exceed the limits given in Table A.14 and illustrated by the dashed curve in Figure A.8.

Table A.14/G.812 – Transient for Type IV node clocks (1544 kbit/s interfaces)

MTIE limit (ns)	Observation interval τ (s)
61 000 τ	0.001 33 ≤ τ ≤ 0.016 4
1000	τ > 0.016 4

A.6.1.2 Transient for Type IV node clocks (STM-N interfaces)

The MTIE of the phase error should not exceed the limits given in Table A.15 and illustrated by the solid curve in Figure A.8.

Table A.15/G.812 – Transient for Type IV node clocks (STM-N interfaces)

MTIE limit (ns)	Observation interval τ (s)
7.6 + 885 τ	0.014 < τ ≤ 0.5
300 + 300 τ	0.5 < τ ≤ 2.33
1000	2.33 < τ ≤ 280

A.6.1.3 Transient for Types V and VI node clocks (2048 kHz and 2048 kbit/s interfaces)

The MTIE of the phase error should not exceed the limits given in Table A.16 and illustrated by the dashed curve in Figure A.8.

Table A.16/G.812 – Transient for Types V and VI node clocks (2048 kHz and 2048 kbit/s interfaces)

MTIE limit (ns)	Observation interval τ (s)
25	0.001 < τ ≤ 0.003 3
7500 τ	0.003 3 < τ ≤ 0.016
120 + 0.5 τ	0.016 < τ ≤ 240
240	240 < τ ≤ 10 000

A.6.1.4 Transient for Types V and VI node clocks (STM-N interfaces)

The MTIE of the phase error should not exceed the limits given in Table A.17 and illustrated by the solid curve in Figure A.8.

Table A.17/G.812 – Transient for Types V and VI node clocks (STM-N interfaces)

MTIE limit (ns)	Observation interval τ (s)
7500 τ	0.001 < τ ≤ 0.016
120 + 0.5 τ	0.016 < τ ≤ 240
240	240 < τ ≤ 10 000

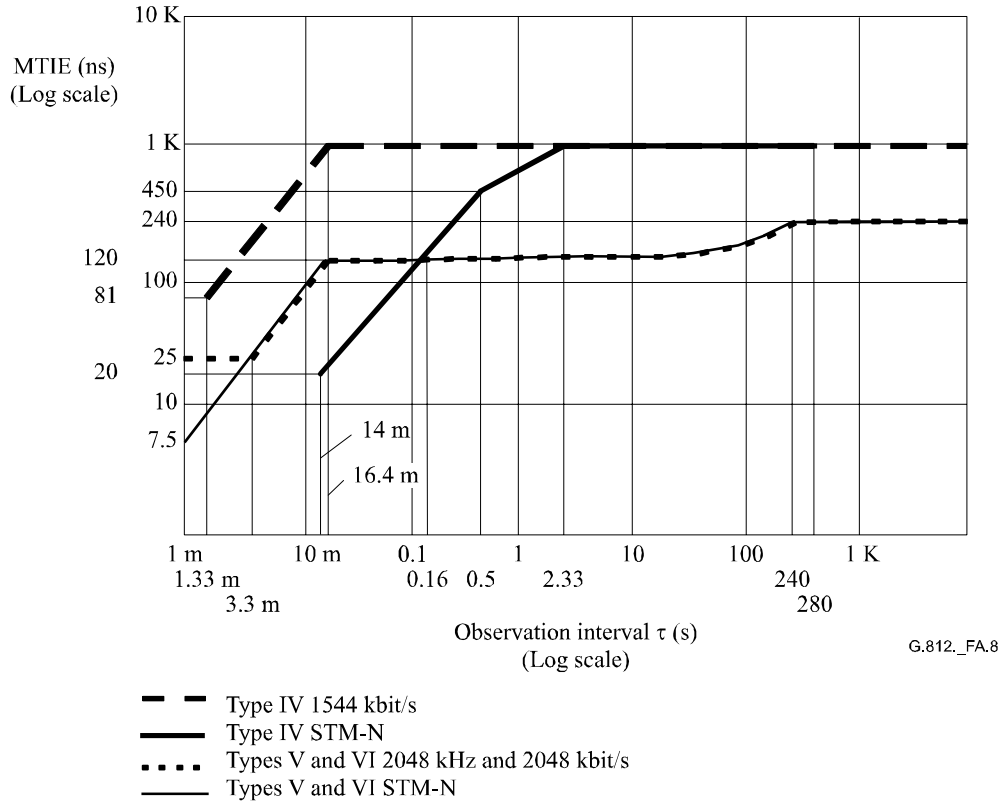

Figure A.8/G.812 – Short-term phase transient mask (MTIE)

A.6.2 Long-term phase transient response (hold-over)

This requirement bounds the maximum excursions in the output timing signal. Additionally, it restricts the accumulation of the phase movement during input signal impairments or internal disturbances.

When a G.812 clock loses all its references, it enters the hold-over state. The Phase Error, Δx, at the output of the slave clock from the moment of loss of reference, should, over any period of S seconds, meet the following:

$$\left|\Delta x(S)\right| \le \left\{(\mathbf{a}_1 + \mathbf{a}_2)S + 0.5\,\mathbf{b}\,S^2 + \mathbf{c}\right\}[\text{ns}]$$

The derivative of Δx(S), the fractional frequency offset, should, over any period of S seconds, meet the following:

$$\left|d\left(\Delta x(S)\right)/dS\right| \le \left\{\mathbf{a}_1 + \mathbf{a}_2 + \mathbf{b}S\right\}[\text{ns/s}]$$

The second derivative of Δx(S), the fractional frequency drift, should, over any period of S seconds, meet the following:

$$\left|d^2\left(\Delta x(S)\right)/dS^2\right| \le \mathbf{d}\left[\text{ns/s}^2\right]$$

In applying the above requirements for the derivative of Δx(S) and the second derivative of Δx(S), the period S must begin after any transient associated with entry into hold-over is over. During this transient period, the transient requirements of A.6.1 apply.

NOTE 1 – $\mathbf{a}_1$ represents an initial frequency offset under constant temperature conditions (±1 K).

NOTE 2 – $\mathbf{a}_2$ accounts for temperature variations after the clock went into hold-over. If there are no temperature variations, the term $\mathbf{a}_2$ S should not contribute to the phase error.

NOTE 3 – **b** represents the average frequency drift caused by aging. This value is derived from typical aging characteristics after 60 days of continuous operation. It is not intended to measure this value on a per day basis, as the temperature effect will dominate.

NOTE 4 – The phase offset **c** takes care of any additional phase shift that may arise during the transition at the entry of the hold-over state.

NOTE 5 – **d** represents the maximum temporary frequency drift rate at constant temperature allowed during hold-over. However, it is not required that **d** and **b** be equal.

The permissible phase error specifications for different G.812 clock Types are shown in Table A.18.

Table A.18/G.812 – Transient response specifications during hold-over

	Type IV	**Type V**	**Type VI**
Applies for	TBD	S > 100 s	S > 100 s
$\mathbf{a}_1$ (ns/s)	50	0.5	10
$\mathbf{a}_2$ (ns/s)	300	NA	NA
b (ns/s^2)	4.63×10^{-4}	1.16×10^{-5}	2.3×10^{-4}
c (ns)	1000	1000	1000
d (ns/s^2)	4.63×10^{-4}	NA	NA
NA Not applicable TBD To be defined			

A.6.3 Phase response to input signal interruptions

For short-term interruptions on synchronization input signals, that do not cause reference switching, the output phase variation is for further study.

A.6.4 Phase discontinuity

In cases of infrequent internal testing or rearrangement operations within the slave clock, the phase transient at the output of G.812 clocks should meet the MTIE specifications in Table A.19 for Type IV node clock and in Table A.20 for Types V and VI clocks and illustrated for all these clocks in Figure A.9.

Table A.19/G.812 – Output phase transient (MTIE) for Type IV node clocks

MTIE limit (ns)	Observation interval τ (s)
NA	$\tau \leq 0.001\ 33$
61 000 τ	$0.001\ 33 < \tau \leq 0.016\ 4$
1000	$\tau > 0.016\ 4$
NA Not applicable	

Table A.20/G.812 – Output phase transient (MTIE) for Types V and VI node clocks

MTIE limit (ns)	Observation interval τ (s)
61	$\tau \leq 0.001$
61 000 τ	$0.001 < \tau \leq 0.016\ 4$
1000	$\tau > 0.016\ 4$

The resultant requirements are shown in Figure A.9.

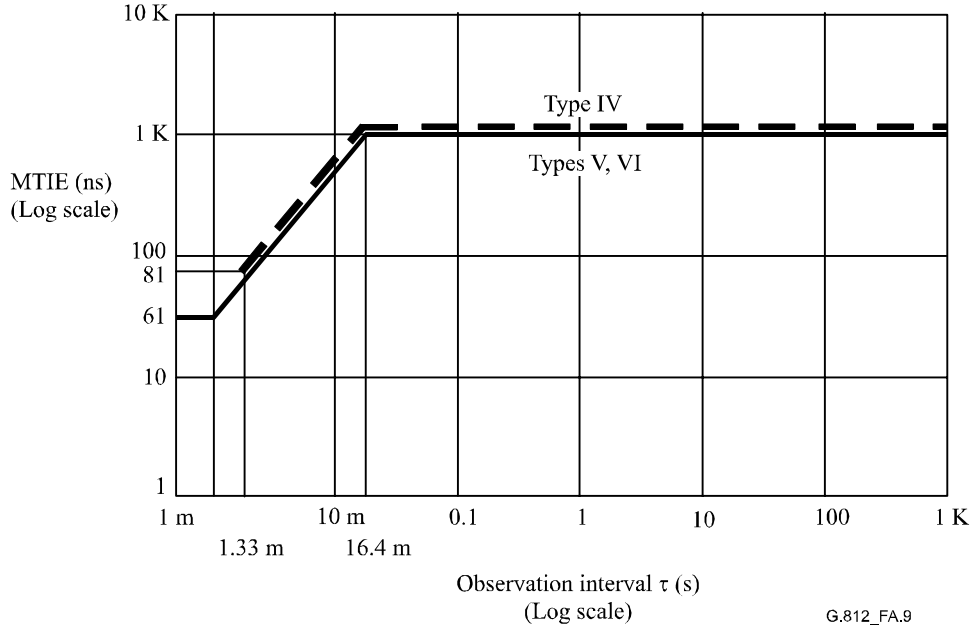

Figure A.9/G.812 – Output phase transient requirements (MTIE)

A.7 Interfaces

The requirements in this Recommendation are related to reference points internal to the Network Elements (NEs) in which the clock is embedded and are therefore not necessarily available for measurement or analysis by the user. Therefore the performance of the G.812 clock is not defined at these internal reference points, but rather at the external interfaces of the equipment. The external input and output are:

- 1544 kbit/s interfaces according to ITU-T Rec. G.703.
- 2048 kHz external interfaces according to ITU-T Rec. G.703.

- 2048 kbit/s interfaces according to ITU-T Rec. G.703.
- STM-N traffic interfaces according to ITU-T Recs G.703 and G.957.

Note that all of the above interfaces may not be implemented on all equipment. These interfaces should comply with the additional jitter and wander requirements as defined in this Recommendation.

Appendix I

Relationship between TDEV and power spectral density

This appendix is provided for information and shows that the power spectral density of phase is given approximately in terms of the TDEV of the phase by $S_x(f) \approx \frac{0.75}{f}\left(\mathrm{TDEV}\left(\frac{0.3}{f}\right)\right)^2$

From II.3/G.810:

$$\mathrm{TDEV}(\tau) = \sqrt{\frac{2}{3(\pi \nu_{nom} n)^2}\int_0^{f_h} S_\varphi(f)\frac{\sin^6(\pi n \tau_0 f)}{\sin^2(\pi \tau_0 f)}\,df}$$

where ν_{nom} is the nominal frequency (in Hz) of the reference with wander, and $n\tau_0 = \tau$, and $S_\varphi(f)$ is the Power Spectral Density (PSD) of phase $\varphi(t)$ in radians. Let:

$$S_x(f) = \frac{1}{(2\pi \nu_{nom})^2} S_\varphi(f)$$

be the power spectral density of the time interval error $x(t) = \varphi(t) / (2\pi\nu_{nom})$ in seconds. If the largest f is $f = 10$ Hz and the largest τ_0 is $\tau_0 = 20$ ms, then $\pi\tau_0 f < 0.628$, and $n \cdot \sin(\pi\tau_0 f) \approx n \cdot \pi\tau_0 f = \pi\tau f$, and:

$$\mathrm{TDEV}(\tau) = \sqrt{\frac{8}{3}\int_0^{f_h} S_x(f)\frac{\sin^6(\pi\tau f)}{(\pi\tau f)^2}\,df} = \sqrt{\int_0^{f_h} S_x(f) H^2(\tau, f)\,df} \qquad \text{(I-1)}$$

where:

$$H(\tau, f) = \sqrt{\frac{8}{3}}\frac{\sin^3(\pi\tau f)}{\pi\tau f}$$

The term $S_x(f)\, H^2(\tau, f)$ is the power spectral density of the phase $x(t)$. Therefore, TDEV can be seen as the rms of the phase filtered by a band-bass filter $H(\tau, f)$. Figure I.1 shows $H(\tau, f)^2$ for the values $\tau = 0.5$ s and $\tau = 1.0$ s. Since $H(\tau, f)^2$ has only 0.85% of its area beyond $20/\tau$ in practice, one can use $f_h = 20/\tau$ with little effect on the calculated value of TDEV.

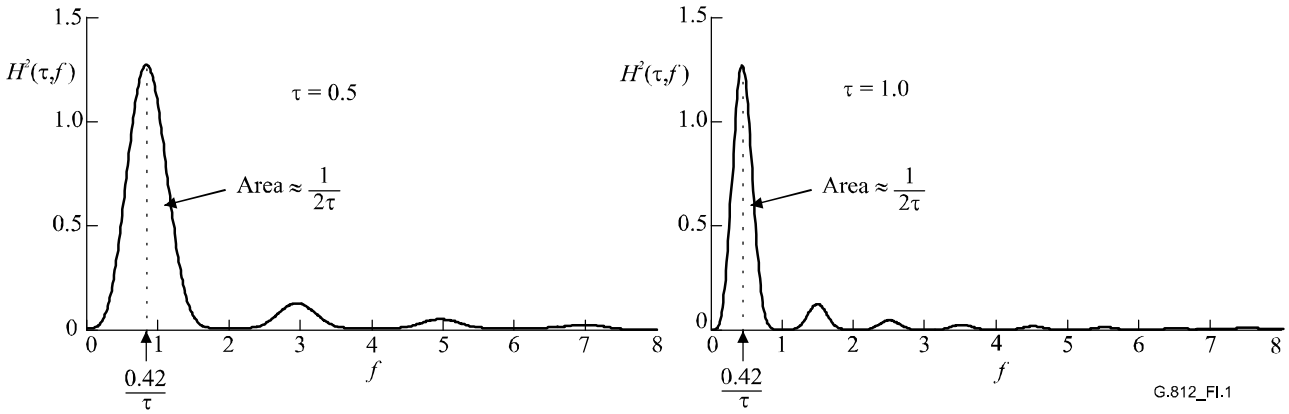

Figure I.1/G.812 – Frequency response of filter $H(\tau, f)$ that is part of TDEV calculation

Note that the response peaks at $f = 0.42/\tau$, and the area under the curve is $1/(2\tau)$. If the passband were very narrow, we would expect $\int_0^\infty S_x(f)H(\tau,f)^2 df \approx (1/2\tau)S_x(0.42/\tau)$. But because the filter has substantial bandwidth, and because phase tends to have stronger spectral components at low frequencies, a better approximation is:

$$\int_0^\infty S_x(f)H(\tau,f)^2 df \approx (1/2.5\tau)S_x(0.3/\tau)$$

Then TDEV is approximated by:

$$\mathrm{TDEV}(\tau) \approx \sqrt{\frac{1}{2.5\tau} S_x\left(\frac{0.3}{\tau}\right)} \tag{I-2}$$

We can get the inverse relationship – the PSD from TDEV – by substituting $0.3/f$ for τ and solving for $S_x(f)$:

$$S_x(f) \approx \frac{0.75}{f}\left(\mathrm{TDEV}\left(\frac{0.3}{f}\right)\right)^2 \tag{I-3}$$

In particular, if TDEV(τ) has a break at $\tau = \tau_{\mathrm{break}}$, then $S_x(f)$ has a break at $f = f_{\mathrm{break}}$, where $f_{\mathrm{break}} \approx 0.3/\tau_{\mathrm{break}}$.

Appendix II

Measurement method for noise transfer

The measurement method recommended here directly tests conformance with the noise transfer specification of clause 10 part b) by applying the TDEV input noise tolerance limit, Figure 4, as the test signal. The output TDEV characteristic is then directly compared against the specification limit, Figure 8.

II.1 Measurement set-up

The measurement set-up is shown in Figure II.1.

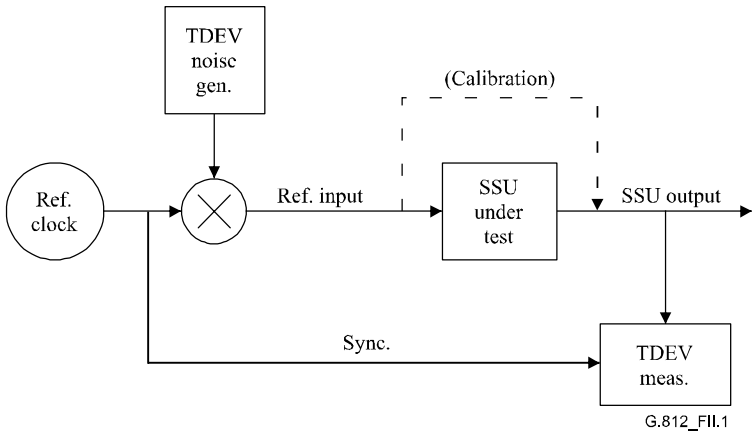

Figure II.1/G.812 – Measurement set-up for TDEV noise transfer characteristics

To ensure sufficiently accurate, robust and consistent measurements, the following principles should be applied:

1) The test signal should be deterministic, yet sufficiently noise-like over a short observation interval.

2) The noise generator should produce a test signal within ±20% of the input noise tolerance specification – clause 9, Figure 4.

3) At large values of τ, the TDEV results should match the TDEV output mask within ±2% of the specification – clause 10, Figure 8.

In order to achieve the above levels of accuracy, normalization and calibration techniques should be applied. In general, the following procedure is recommended:

1) Perform a calibration measurement sequence, without the slave clock under test – TDEV(cal). This obtains the raw test signal characteristics.

2) Calculate a correction factor with respect to the required input wander tolerance specification – TDEV(ref). This now represents the ideal test signal.

3) Measure TDEV(dat) of the slave clock under test under the same conditions as the calibration sequence.

4) Normalize TDEV(dat) using TDEV(ref) – obtaining TDEV(meas).

5) TDEV(meas) may now be directly compared with the noise transfer specification limit.

II.2 Functional model of TDEV noise generator

The noise generator shown in Figure II.1 can be described by the functional diagram in Figure II.2. It does not imply a specific implementation, but defines the key characteristics that should be observed in order to meet the measurement objectives above. A suitable noise generator can, for example, be constructed with a PRBS sequence of $2^{31} - 1$, generated at 6.4 kHz.

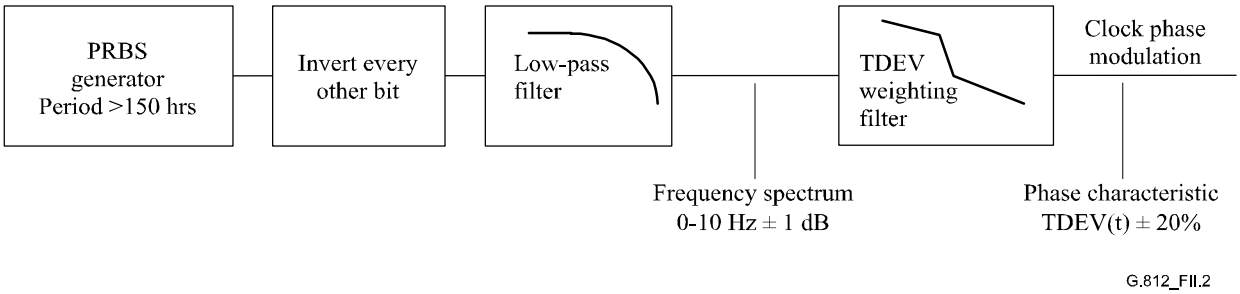

Figure II.2/G.812 – Functional model of TDEV noise generator

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