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TELECOMMUNICATION
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Ethernet over Transport aspects – Quality and availability targets

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Timing and synchronization aspects in packet networks

ITU-T Recommendation G.8261/Y.1361

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ITU-T Recommendation G.8261/Y.1361

Timing and synchronization aspects in packet networks

Summary

This Recommendation defines synchronization aspects in packet networks. It specifies the maximum network limits of jitter and wander that shall not be exceeded. It specifies the minimum equipment tolerance to jitter and wander that shall be provided at the boundary of these packet networks at TDM interfaces. It also outlines the minimum requirements for the synchronization function of network elements.

The requirements for the jitter and wander characteristics that are specified in this Recommendation must be adhered to in order to ensure interoperability of equipment produced by different manufacturers and a satisfactory network performance.

This edition incorporates the modifications introduced by Corrigendum 1 approved on 14 December 2006 by ITU-T Study Group 15.

Source

ITU-T Recommendation G.8261/Y.1361 was approved on 22 May 2006 by ITU-T Study Group 15 (2005-2008) under the ITU-T Recommendation A.8 procedure.

Keywords

Clock, jitter, synchronization, wander.

FOREWORD

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ITU-T Recommendation G.8261/Y.1361

Timing and synchronization aspects in packet networks

1 Scope

This Recommendation defines synchronization aspects in packet networks. It specifies the maximum network limits of jitter and wander that shall not be exceeded. It specifies the minimum equipment tolerance to jitter and wander that shall be provided at the boundary of these packet networks at TDM interfaces. It also outlines the minimum requirements for the synchronization function of network elements.

In particular, it focuses on the transport of synchronization information of TDM signals over packet networks.

NOTE – The application of the transport of SDH signals is for further study.

The packet networks that are in the scope of this Recommendation are currently limited to the following scenarios:

- Ethernet (IEEE 802.3™ [15], IEEE 802.1D™ [14], IEEE 802.1 ad™ [32], IEEE 802.1Q-REV™ [29]).

The following scenarios are planned to be covered in a future release of this Recommendation:

- MPLS (IETF RFC 3031 [B12], ITU-T Rec. G.8110/Y.1370 [22]);
- IP (IETF RFC 791 [B13], and RFC 2460 [B9]).

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[1] ITU-T Recommendation G.703 (2001), *Physical/electrical characteristics of hierarchical digital interfaces.*

[2] ITU-T Recommendation G.783 (2006), *Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks*.

[3] ITU-T Recommendation G.801 (1988), *Digital transmission models*.

[4] ITU-T Recommendation G.803 (2000), *Architecture of transport networks based on the synchronous digital hierarchy (SDH)*.

[5] ITU-T Recommendation G.810 (1996), *Definitions and terminology for synchronization networks.*

[6] ITU-T Recommendation G.811 (1997), *Timing characteristics of primary reference clocks*.

[7] ITU-T Recommendation G.812 (2004), *Timing requirements of slave clocks suitable for use as node clocks in synchronization networks*.

[8] ITU-T Recommendation G.813 (2003), *Timing characteristics of SDH equipment slave clocks (SEC).*

[9] ITU-T Recommendation G.822 (1988), *Controlled slip rate objectives on an international digital connection.*

[10] ITU-T Recommendation G.823 (2000), *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy.*

[11] ITU-T Recommendation G.824 (2000), *The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy.*

[12] ITU-T Recommendation G.825 (2000), *The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH).*

[13] IEEE Standard 802™-2001, *IEEE standard for Local and Metropolitan Area Networks: Overview and Architecture*.

[14] IEEE Standard 802.1D™-2004, *IEEE Standard for Local and Metropolitan Area Networks: Media Access Control (MAC) Bridge*s.

[15] IEEE Standard 802.3™-2005, *Part 3*, *CSMA/CD access method and physical layer specifications*.

[16] ITU-T Recommendation G.702 (1988), *Digital hierarchy bit rates.*

[17] ITU-T Recommendation O.171 (1997), *Jitter and wander measuring equipment for digital systems which are based on the plesiochronous digital hierarchy (PDH).*

[18] ITU-T Recommendation O.172 (2005), *Timing jitter and wander measuring equipment for digital systems which are based on the synchronous digital hierarchy (SDH).*

[19] ITU-T Recommendation V.90 (1998), *A digital modem and analogue modem pair for use on the Public Switched Telephone Network (PSTN) at data signalling rates of up to 56 000 bit/s downstream and up to 33 600 bit/s upstream.*

[20] ITU-T Recommendation T.4 (2003), *Standardization of Group 3 facsimile terminals for document transmission.*

[21] ITU-T Recommendation G.8010/Y.1306 (2004), *Architecture of Ethernet layer networks.*

[22] ITU-T Recommendation G.8110/Y.1370 (2005), *MPLS layer network architecture.*

[23] ITU-T Recommendation G.701 (1993), *Vocabulary of digital transmission and multiplexing, and pulse code modulation (PCM) terms.*

[24] ITU-T Recommendation Y.1411 (2003), *ATM-MPLS Network interworking – Cell mode user plane interworking.*

[25] ITU-T Recommendation Y.1540 (2002), *Internet protocol data communication service – IP packet transfer and availability performance parameters.*

[26] ITU-T Recommendation Y.1560 (2003), *Parameters for TCP connection performance in the presence of middleboxes.*

[27] ITU-T Recommendation Y.1561 (2004), *Performance and availability parameters for MPLS networks.*

[28] ITU-T Recommendation Y.1731 (2006), *OAM functions and mechanisms for Ethernet based networks*.

[29] IEEE Standard 802.1Q-REV™-2005, *IEEE Standard for Local and Metropolitan Area Networks: Virtual Bridged Local Area Network*s.

[30] ITU-T Recommendation G.705 (2000), *Characteristics of plesiochronous digital hierarchy (PDH) equipment functional blocks*.

[31] ITU-T Recommendation I.363.1 (1996), *B-ISDN ATM Adaptation Layer specification: Type 1 AAL*.

[32] IEEE Standard 802.1ad™-2005, *IEEE Standard for Local and Metropolitan Area Networks: Provider Bridges.*

3 Definitions

This Recommendation defines the following terms:

3.1 asynchronous interface: See ITU-T Rec. G.823 [10].

3.2 circuit emulation services (CES) island: Segment of a network, based on packet-switched technologies that emulates either the characteristics of a circuit-switched network or of a PDH/SDH transport network, in order to carry CBR services (e.g., E1).

3.3 interworking function (IWF): See ITU-T Rec. Y.1411 [24].

3.4 network-synchronous operation: Synchronization of the physical layer (usually by a timing distribution of a timing signal traceable to a Primary Reference Clock (PRC), see ITU-T Rec. G.811).

3.5 stabilization period: The period beginning at the point in time when a validated timing source has been selected by the IWF and ending when the output timing characteristics are within the output jitter and wander requirements.

3.6 synchronous interface: See ITU-T Rec. G.823.

3.7 time division multiplex (TDM): A term that conventionally refers to the isochronous bit streams used in telephony networks; in particular those belonging to PDH (plesiochronous digital hierarchy) as described in ITU-T Rec. G.705 [30]. The bit rates traditionally used in various regions of the world are detailed in ITU-T Rec. G.702 [16]. Examples of the signals covered by the TDM definition are those belonging to PDH and SDH hierarchies.

3.8 traffic interface: See ITU-T Rec. G.823.

4 Abbreviations

This Recommendation uses the following abbreviations:

3GPP	Third Generation Partnership Project
ATM	Asynchronous Transfer Mode
BS	Base Station
CBR	Constant Bit Rate
CDMA	Code Division Multiple Access
CE	Customer Equipment
CES	Circuit Emulation Service
FE	Fast Ethernet
GE	Gigabit Ethernet
GPS	Global Positioning System
GSM	Global System for Mobile communications
IEEE	Institute of Electrical and Electronics Engineers
IP	Internet Protocol

IWF InterWorking Function

MAC Medium Access Control

MRTIE Maximum Relative Time Interval Error

MTIE Maximum Time Interval Error

NTP Network Time Protocol

OTN Optical Transport Network

PDH Plesiochronous Digital Hierarchy

PRC Primary Reference Clock

PSTN Public Switched Telephone Network

SLA Service Level Agreement

SASE Stand Alone Synchronization Equipment

SDH Synchronous Digital Hierarchy

SEC SDH Equipment Clock

SRTS Synchronous Residual Time Stamp

SSM Synchronization Status Message

SSU Synchronization Supply Unit

STM Synchronous Transfer Mode

TDEV Time Deviation

TDM Time Division Multiplex

UI Unit Interval

UTC Universal Time Coordinated

5 Conventions

The terms "packets" and "frames" are used interchangeably throughout this Recommendation.

6 General

Packet switching was originally introduced to handle asynchronous data.

However, for new applications such as the transport of TDM service and the distribution of synchronization over packet networks, the strict synchronization requirements of those applications must be considered.

The ongoing evolution in telecommunications increases the likelihood of hybrid packet/circuit environments for voice and voiceband data services. These environments combine packet technologies (e.g., ATM, IP, Ethernet) with traditional TDM systems. Under these conditions, it is critical to ensure that an acceptable level of quality is maintained (e.g., limited slip rate).

Synchronization in TDM networks is well understood and implemented. Typically, a TDM circuit service provider will maintain a timing distribution network, providing synchronization traceable to a Primary Reference Clock (i.e., clock compliance with ITU-T Rec. G.811 [6]).

The timing and synchronization aspects addressed in this Recommendation are initially concerned with Ethernet-based networks with protocol layers as defined in IEEE 802 (see clause 1, Scope).

Functional architecture for Ethernet networks are defined in ITU-T Rec. G.8010/Y.1306 [21].

In the context of this Recommendation, the highest layers (e.g., layer 7 in OSI model) refer to applications transported over the packet networks. Real-time applications have relatively tight timing requirements concerning delay and delay variation. Some applications might resolve their timing issues within higher layers (e.g., MPEG-2); other applications rely on the timing support provided by one or more of the lower layers (e.g., physical layer).

This Recommendation aims at describing different methods to obtain the synchronization-related requirements.

Additionally, the requirements for interfaces and equipment that are part of the Ethernet network are described. It also gives recommendations when to apply different types of synchronization methods.

Some considerations on applicable synchronization requirements in a packet-based network are summarized in the following clauses.

This Recommendation primarily deals with CES in public network environments. In some private network applications involving circuit emulation, it may be sufficient to distribute a non-PRC quality level common clock towards CES IWF nodes. However, the use of synchronization timing below PRC quality level could result in internetworking difficulties between different network domains, such as interconnection involving multiple public network providers.

The use of a non-PRC quality level common clock is for further study.

6.1 Packet network synchronization requirements

The nodes involved in packet-oriented transmission technology (e.g., ATM network nodes) do not require any synchronization for the implementation of the packet switching function. In fact, at any entrance point of a packet switch, an individual device shall provide packet timing adaptation (for instance cell timing adaptation in case of ATM switch) of the incoming signal to the internal timing. For instance, in the case of ATM networks, the principle to cater for frequency differences is to use idle cell stuffing. Transmission links, in principle, need not be synchronized with each other.

However, as the packet network evolves to integrate TDM-based applications, i.e., when transporting a CBR stream over a packet network and when interworking with PSTN networks, the packet network shall provide correct timing at the traffic interfaces.

This means that the requirements on synchronization functions in packet networks, especially on the boundary of the packet networks, are dependent on the services carried over the network. For TDM-based services, the IWF may require network-synchronous operation in order to provide acceptable performance.

6.2 TDM timing requirements

The transport of TDM signals through packet networks requires that the signals at the output of the packet network comply with TDM timing requirements; this is crucial to enable interworking with TDM equipment.

These requirements are independent of the type of information (voice or data) transported by the TDM signal.

The adaptation of TDM signals into the packet network is called Circuit Emulation Services (CES).

The timing requirements that are applicable are: jitter and wander limits at traffic and/or synchronization interfaces, long-term frequency accuracy (which can influence the slip performance) and total delay (which is critical for real-time services, such as the voice service).

6.2.1 PDH timing requirements

The PDH timing requirements for traffic interfaces are mainly related to jitter, wander and slip performance.

At the input of the network element at the boundary of a packet network, jitter and wander tolerance requirements apply. At the output of the network element at the egress of the packet network, jitter and wander generation requirements apply.

These values are specified in ITU-T Rec. G.823 for the network based on 2048 kbit/s hierarchy and ITU-T Rec. G.824 for the network based on 1544 kbit/s hierarchy.

In addition, ITU-T Rec. G.822 specifies the applicable slip rate objectives. This is the case when the clock of the equipment that generates the TDM signal and the clock used in the equipment recovering the TDM signal from the packets are different and the slip buffer is needed in the application.

6.2.2 Synchronization interfaces requirements

In the case where the PDH signals are defined as synchronization interfaces, the synchronization requirements are more stringent than for 2048 kbit/s and 1544 kbit/s traffic interfaces. The synchronization interface requirements for PDH interfaces are also defined in ITU-T Recs G.823 [10] and G.824 [11].

6.2.3 SDH timing requirements

Any STM-N signal must be compliant with ITU-T Rec. G.825 [12]. The relevant requirements refer to the jitter and wander tolerance applicable at the input of the network element at the boundary of a packet network that receives the STM-N data and jitter and wander generation applicable at the output of the network element generating STM-N traffic at the other end of the packet network.

In the case of STM-N signals, there are no distinctions between traffic and synchronization interfaces as all STM-N signals are defined as synchronization interfaces.

6.3 Synchronization network engineering in packet networks

The driving force for much of this work is to cater for the synchronization needs of the application or in general the need of certain technologies (for instance, Base Stations in GSM and WCDMA networks). In order to achieve such goal, operators have therefore to distribute a reference timing signal of suitable quality to the network elements processing the application.

One approach is to follow a distributed PRC strategy (for instance, by means of GPS technologies). An alternative approach is based on a master-slave strategy. The engineering rules for designing the synchronization network in these cases are well understood and documented (see for example ITU-T Rec. G.803 [4]) when the underlying transport of the packets (e.g., Ethernet frames) will run over the existing synchronous technologies (PDH or SDH networks). On the other hand, when the underlying transport is based on non-synchronous technologies (i.e., Ethernet), alternative approaches shall be considered. This will be further analysed in clause 8.

6.4 Timing requirements at edge versus timing requirements in core networks

Different performance can be requested in case the packet network is part of an access network or is the underlying layer of the core network.

The distribution of a synchronization reference over a portion of a core network may be requested to comply with strict jitter and wander requirements (i.e., ITU-T Recs G.823, and G.824 for synchronization interfaces, and ITU-T Rec. G.825).

On the other hand, in the access network, requirements may be relaxed to allow a distribution of a timing reference signal with performance sufficient (e.g., lower than PRC quality level) to support

the timing requirements of the end node (for instance, a Base Station, or a V90 modem). More information is provided in Appendix IV.

7 Network limits

The jitter and wander network limits currently specified in the relevant ITU-T Recommendations (i.e., ITU-T Recs G.823 and G.824) have to be fulfilled in all the scenarios that are relevant for this Recommendation.

This clause describes three different deployment scenarios for a CES segment or island. The jitter and wander limits for TDM traffic interfaces (excluding STM-N signals) carried over the CES segment in each of these scenarios are defined in this clause.

The network limits applicable to synchronization interfaces (as specified in clause 6/G.823 and clause 6/G.824) and to STM-N signals carried over packet networks, are for further study.

It should be noted that in some cases, signals with quality according to clause 5/G.823 and clause 5/G.824 (traffic interfaces) when traceable to a PRC, can be used as reference timing signals towards end equipment able to tolerate these signals and to correctly operate (model for Deployment Case 2 is an example of this scenario).

NOTE – The network limits provided by this clause shall be valid under normal conditions (e.g., when failure conditions or maintenance actions are not present). It is out of the scope of this Recommendation to specify the proportion of time during which these limits apply.

7.1 Network model underlying the network limits

For the transport of PDH signals, the models in Figure A.1/G.823 and in Figure A.1/G.824 are the starting point to consider the insertion of a CES segment. The wander budget allocation for the CES segment must be only a portion of the entire wander budget as specified in ITU-T Recs G.823 or G.824, since the total wander budget has to be shared with the rest of the network.

Depending on where the CES segment is located, different wander requirements may apply. Several models of CES deployment have been identified; the models are defined in 7.1.1, 7.1.2 and 7.1.3.

NOTE 1 – The figures in this clause do not show the details on how the timing is recovered by the IWF or how the timing is distributed in the packet network. For further details, refer to clauses 8 and 9.

NOTE 2 – Only one CES island is presented in these models since it aims at allocating wander budget only for the CES technology segment. There might be several CES systems as long as their accumulated wander generation is within the budget allocated for CES.

The wander accumulation through multiple islands is for further study.

7.1.1 Deployment Case 1

When the CES segment is located at an island between the two switches of the G.823 reference model, the wander budget is calculated based on the model in Figure 1 below. The model is based on Figures A.1/G.823 and A.1/G.824 where one of the SDH islands is replaced by the CES network.

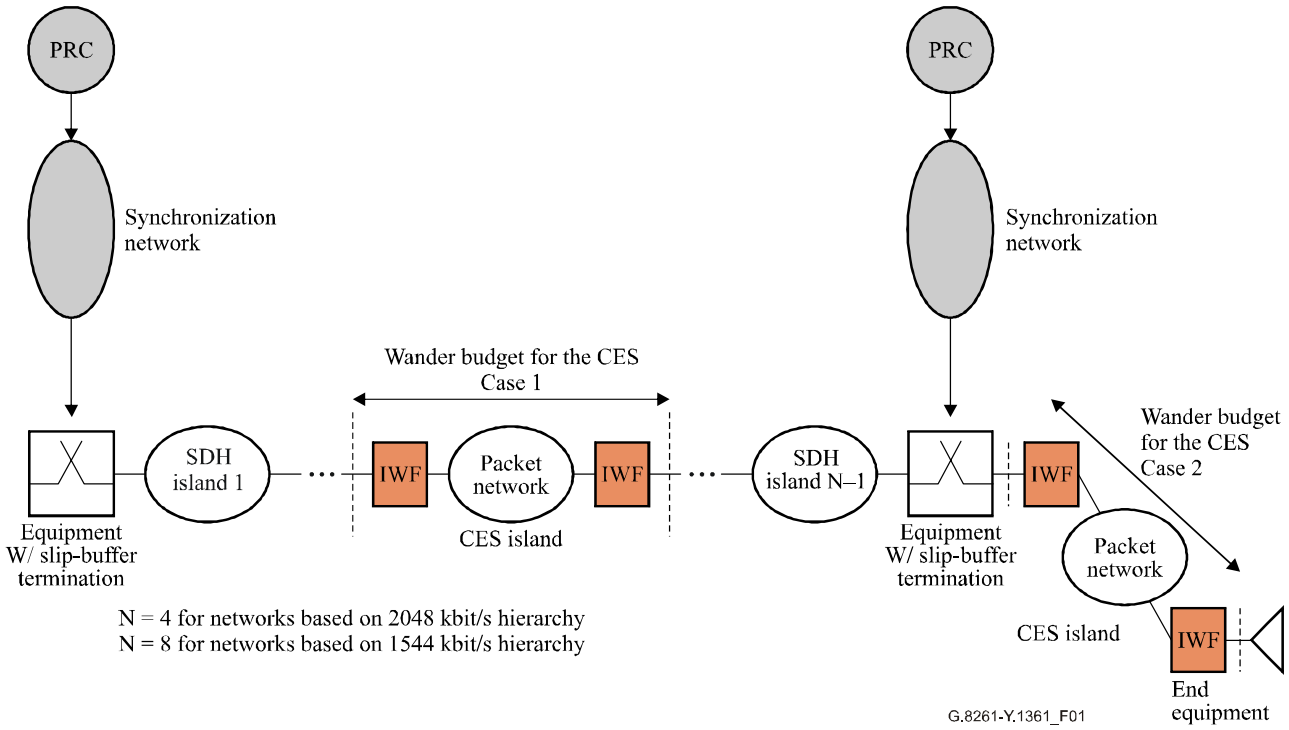


Figure 1/G.8261/Y.1361 – Network models for traffic and clock wander accumulation: Deployment Case 1 and Case 2

The wander budget for 2048 kbit/s signal is defined in Table 1.

Table 1/G.8261/Y.1361 – Deployment Case 1: 2048 kbit/s interface output wander limit

Observation interval, τ [s]	**MRTIE requirement [µs]**
$0.05 < \tau \leq 0.2$	$10.75\ \tau$
$0.2 < \tau \leq 32$	$9 * 0.24 = 2.15$
$32 < \tau \leq 64$	$0.067\ \tau$
$64 < \tau \leq 1000$	$18 * 0.24 = 4.3$
NOTE – For the asynchronous configuration, the maximum observation interval to be considered is 80 s. The specification between 80 s and 1000 s for the asynchronous interfaces is for further study.	

The 2048 kbit/s jitter network limits shall comply with 5.1/G.823.

The wander budget for 1544 kbit/s signal is defined in Table 2.

Table 2/G.8261/Y.1361 – Deployment Case 1: Wander limit for 1544 kbit/s interface

Observation interval, τ [s]	MTIE [µs]
$\tau \leq 0.1$	No requirement (See Note)
$0.1 < \tau \leq 0.47$	$4.5\ \tau$
$0.47 < \tau \leq 900$	2.1
$900 < \tau \leq 1930$	$2.33 * 10e\text{-}3\ \tau$
$1930 < \tau \leq 86\ 400$	4.5
NOTE – This region is covered by jitter requirements	

The 1544 kbit/s jitter network limits shall comply with 5.1/G.824.

NOTE – The network limits for the other PDH signals (i.e., 34 368 kbit/s, 44 736 kbit/s and 139 264 kbit/s signals) carried over the CES segments are for further study.

7.1.2 Deployment Case 2

7.1.2.1 Application A

When the CES segment is located outside the network elements containing the slip buffers (see Figure 1), the retiming effect of the switch has to be considered. At the output of this equipment, the timing of the traffic signal will meet the network limit for a synchronization signal which is tighter than for a traffic signal.

The jitter and wander budget of the CES segment in this case is the difference between the 2048 kbit/s network limit (see Figure 1/G.823) and the 2048 kbit/s synchronization interface network limit (see Figure 10/G.823). The limit is provided in Table 3.

Table 3/G.8261/Y.1361 – Case 2A: 2048 kbit/s interface output wander limit

Observation interval, τ [s]	MRTIE requirement [µs]
$0.05 < \tau \leq 0.2$	$40\ \tau$
$0.2 < \tau \leq 32$	8
$32 < \tau \leq 64$	$0.25\ \tau$
$64 < \tau \leq 1000$ (Note)	16
NOTE – For the asynchronous configuration, the maximum observation interval to be considered is 80 s. The specification between 80 s and 1000 s for the asynchronous interfaces is for further study.	

In case of 1544 kbit/s interfaces, the jitter and wander budget of the CES segment is the difference between the 1544 kbit/s network limit (see Table 2/G.824) and the 1544 kbit/s synchronization interface network limit (see Figure 3/G.824). The actual values are for further study.

NOTE – The network limits for the other PDH signals (i.e., 34 368 kbit/s, 44 736 kbit/s and 139 264 kbit/s signals) carried over the CES segments are for further study.

7.1.2.2 Application B

In this case the application recovers timing through the TDM signal; therefore, there is no differential jitter and wander between the clock and the data other than within the bandwidth of the clock recovery since the data and clock are extracted from the same signal. The wander budget of

the CES segment is only limited by the timing quality requested by the application (e.g., Base Station requirements) and not by the G.823 specification.

NOTE – This application is valid only for application with a single signal; if two signals are received, there might exist a differential jitter and wander between one signal and the clock extracted from the other signal.

7.1.3 Deployment Case 3

When retiming is implemented at the output of the SDH islands as shown in Figure 2, the amplitude of noise on the PDH output is that of a synchronization interface. This allows an increase in the wander budget up to that of Case 2 Application A in some configurations. It should be noted that the service clock is not preserved end-to-end in this case.

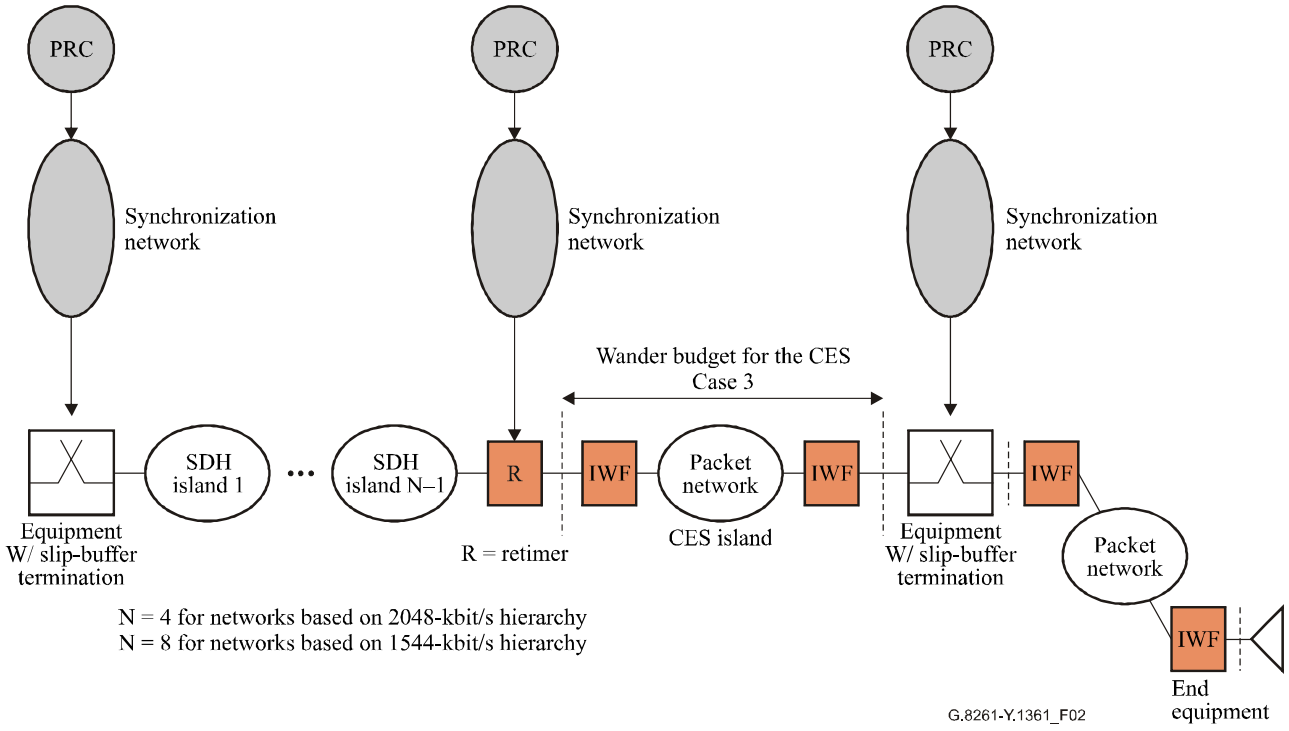


Figure 2/G.8261/Y.1361 – Deployment Case 3 scenario

8 Reference timing signal distribution over packet networks

In order to fulfil the applicable synchronization requirements, it should be possible to distribute a reference timing signal with proper phase stability and frequency accuracy characteristics.

Two main classes of methods are identified in this Recommendation:

- plesiochronous and network synchronous methods;
- packet-based methods.

8.1 Plesiochronous and network-synchronous methods

The first class of methods refers to PRC distributed method (for instance, based on GPS), or Master-Slave method using a synchronous physical layer (e.g., STM-N); see Figure 3. These methods are widely implemented to synchronize the TDM networks.

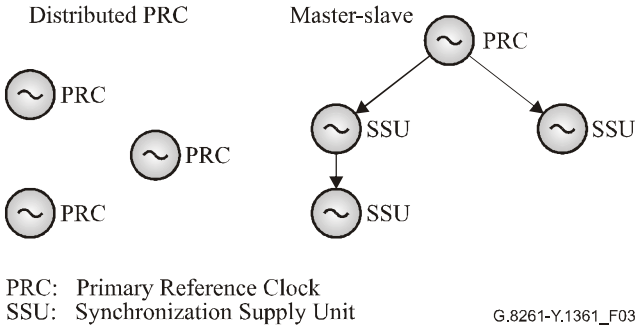


Figure 3/G.8261/Y.1361 – Distributed PRC and master-slave methods

It has been recognized that when G.811 traceability is required, it would be an advantage to be able to distribute timing via a synchronous Ethernet as well as traditional means.

Traditional Ethernet networks are free-running (± 100 ppm). However, all the key elements exist within Ethernet technology in order to make it synchronous and allow a master-slave synchronization architecture to be introduced at the physical layer. The Ethernet physical layer can then be used to provide reference timing signal distribution over packet networks, from backbone level to access level. This method can also be used to provide timing recovery at the IWFs for CBR services transported over packet networks. It could also be used to provide a timing reference signal down to edge access equipment in a pure Ethernet network.

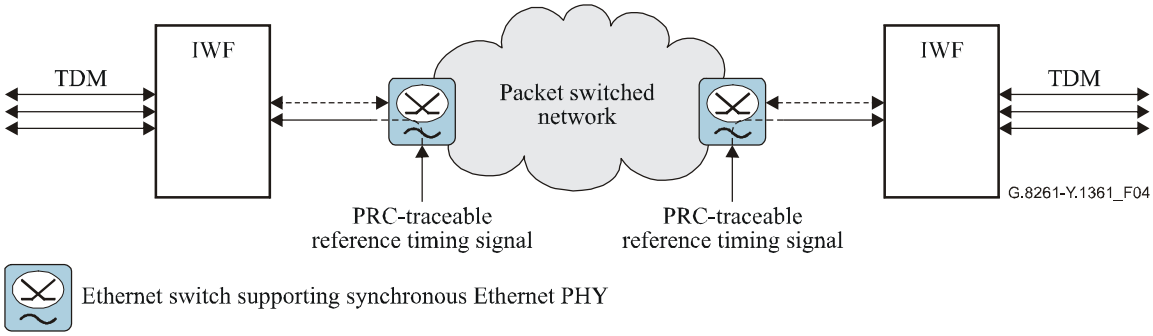
It should be noted that there are a number of technical issues to be solved before this technique can be widely used: traceability for quality management, jitter and wander interface specifications, protection of networks, etc.

Clause 8.1.1 details a high-level method of achieving a synchronous Ethernet network.

8.1.1 Synchronous Ethernet networks

8.1.1.1 General architecture

The general concept of delivering a physical layer clock from the Ethernet switch to the IWF is given in Figure 4.



NOTE – The two PRC-traceable reference timing signals may originate from the same source.

Figure 4/G.8261/Y.1361 – Timing to Ethernet IWF provided over Ethernet PHY

A reference timing signal traceable to a PRC is injected into the Ethernet switch using an external clock port. This signal is extracted and processed via a synchronization function before injecting timing onto the Ethernet bit stream. The synchronization function provides filtering and may require holdover. These requirements are for further study.

Clearly, there may be a number of Ethernet switches between the element where the reference timing signal is injected and the IWF. In such cases the synchronization function within the Ethernet switch must be able to recover synchronization "line timing" from the incoming bit stream.

As part of the architecture, a distinction should be made between the network clock and the service clock as described below.

8.1.1.2 Network clock

The network clock is the clock used to discipline the synchronization function within the Ethernet switch and therefore the bit rate leaving the Ethernet switch. The clock injected into the synchronization function will be synchronous, i.e., locked to the network clock.

NOTE – In the network clocking case, the production of jitter and wander will need to be limited through the use of a network clock. The specification of such a clock (this specification may include clock accuracy, filtering function, holdover performance and noise generation) is for further study.

8.1.1.3 Service clock

Within existing Ethernet technology, the service is effectively asynchronous. In synchronous Ethernet, existing Ethernet services will continue to be mapped into and out of the Ethernet physical layer at the appropriate rates.

A proposed architecture is described in Annex A.

8.2 Packet-based methods

The second class of methods relies on timing information carried by the packets (e.g., sending dedicated Time Stamp messages as shown in Figure 5; methods using two-way transfer of timing information are also possible such as NTP or similar protocols; it should be noted that two-way protocols can transport time information as well). In some cases this is the only alternative to a PRC-distributed approach.

Packet-based methods and related performances are under study.

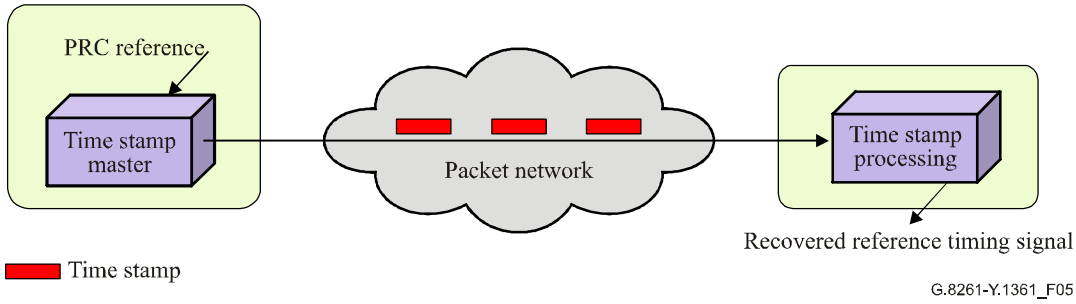


Figure 5/G.8261/Y.1361 – Example of packet-based method with timing distribution of the reference timing signal via time stamps

9 Timing recovery for constant bit rate services transported over packet networks

CBR (Constant Bit Rate) services (e.g., Circuit-Emulated TDM signal) require that the timing of the signal is similar on both ends of the packet network and is handled by the IWF responsible for delivering the constant bit rate stream. The notion of service clock preservation is that the incoming service clock frequency be replicated as the outgoing service clock frequency when considered in terms of a long-term average. It does not imply that wander on the incoming TDM signal be replicated on the outgoing TDM signal.

The operating methods identified within this Recommendation are described in the following clauses.

9.1 Network-synchronous operation

This method refers to the fully network-synchronous operation by using a PRC-traceable network derived clock or a local PRC (e.g., GPS) as the service clock (see Figure 6). This implies the availability of a PRC reference. It should be highlighted that this method does not preserve the service timing.

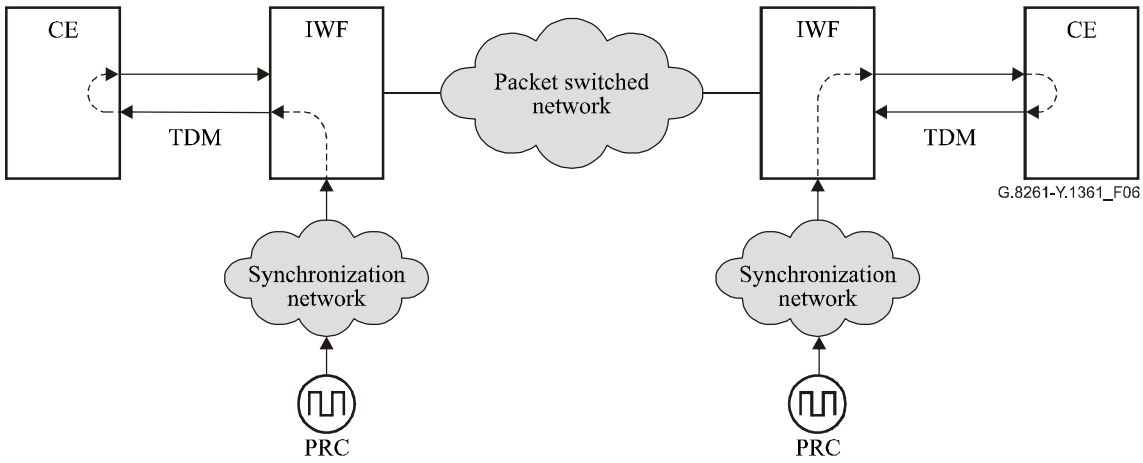


Figure 6/G.8261/Y.1361 – Example of network-synchronous operation

NOTE – The reference timing signal at the input to the IWF shall comply with synchronization interfaces as defined in ITU-T Recs G.823 and G.824.

9.2 Differential methods

According to the differential methods, the difference between the service clock and the reference clock is encoded and transmitted across the packet network (see Figure 7). The service clock is recovered on the far end of the packet network making use of a common reference clock. The Synchronous Residual Time Stamp (SRTS) method [31] is an example of this family of methods. It should be highlighted that the method can preserve the service timing.

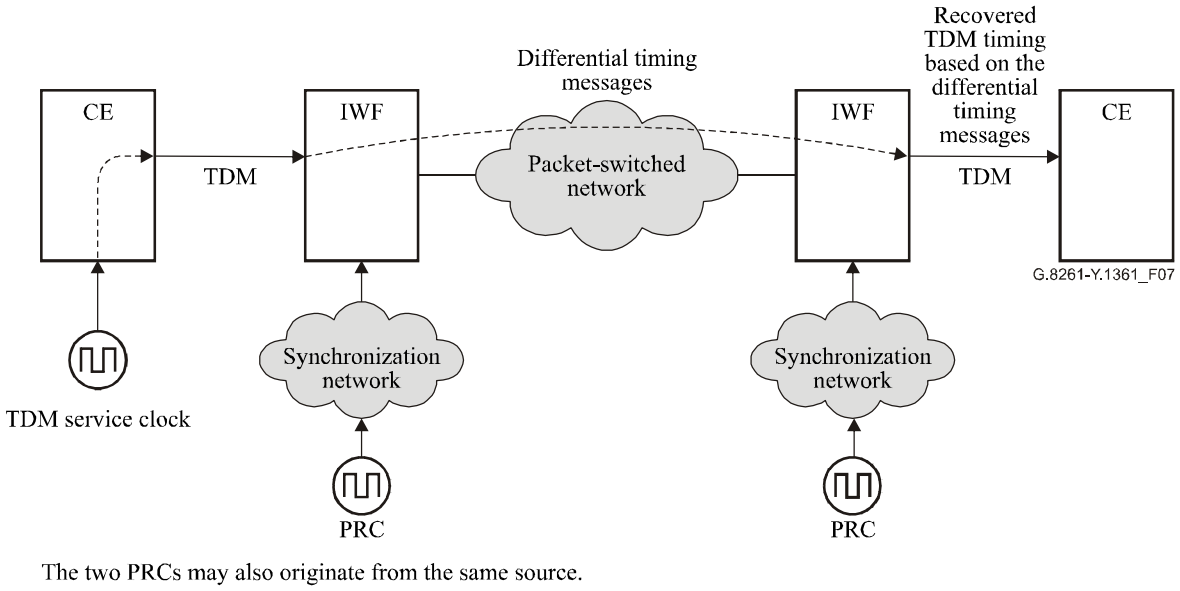


Figure 7/G.8261/Y.1361 – Example of timing recovery operation based on differential methods

NOTE 1 – Differential methods may work with IWF reference clocks that are not PRC traceable. The use of non-PRC traceable clocks is application dependent and is not within the scope of this Recommendation.

NOTE 2 – The reference timing signal at the input of the IWF shall comply with synchronization interfaces as defined in ITU-T Recs G.823 and G.824.

9.3 Adaptive methods

In the adaptive methods, the timing can be recovered based on the inter-arrival time of the packets or on the fill level of the jitter buffer. It should be highlighted that the method preserves the service timing (see Figure 8).

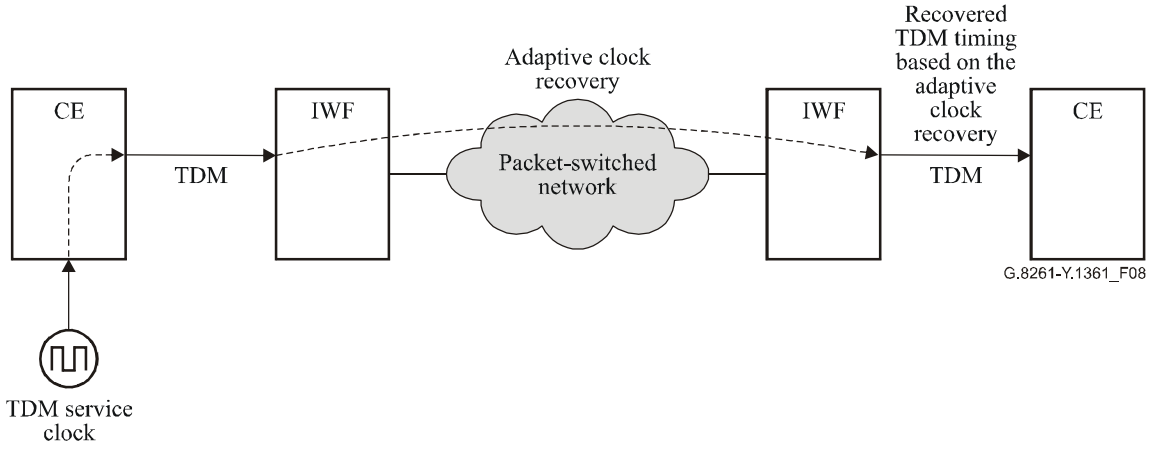


Figure 8/G.8261/Y.1361 – Example of adaptive method

9.4 Reference clock available at the TDM end systems

When the reference clock is available at the TDM end systems, this is a trivial case, since both the end systems have direct access to the timing reference, and will retime the signal leaving the IWF. Therefore, there is no need to recover the timing.

The use of loop timing in the IWF on the TDM interface is an example of the implementation of this method (see Figure 9). An example when this scenario might apply is when two PSTN domains are connected via a packet network.

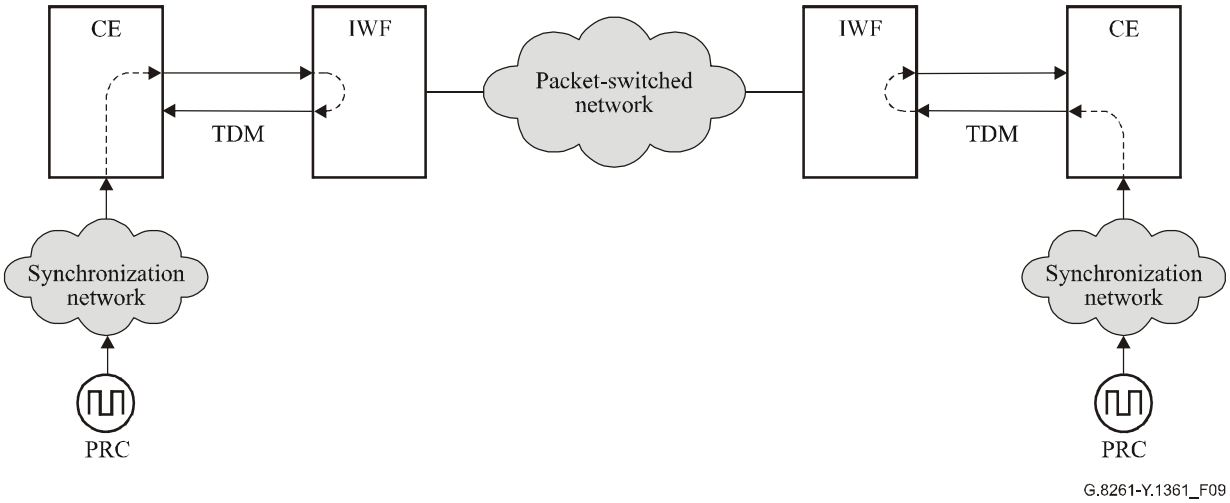


Figure 9/G.8261/Y.1361 – Example of PRC reference timing signal available at the TDM end systems

Note that Figure 9 shows the TDM transmitter and receiver being traceable to a common reference clock that may be a PRC. This is the case where transmitter and receiver are for example digital switches where there is a need to control slips. However, there are cases where the transmitter and receiver are not traceable to G.811 clocks, for example 34 368 kbit/s or 44 736 kbit/s multiplexers.

10 Impact of impairments in the packet network on timing distribution and service clock recovery

This clause discusses the different impairments impacting the traffic and its timing information in packet networks. It is understood that the requirements of emulated circuits and recovered clocks, which are specified in clause 7, are to be met under operational conditions.

Fundamentally, network synchronization is required in Layer 1 networks to manage buffers. Layer 1 buffers as present in PDH, SDH and OTN networks and its adaptation functions are simple structures, where the nominal ingress and egress rate is controlled within specific bounds as given in the related networking standards of these TDM networks. Mechanisms such as stuff bytes and pointers, together with system clocks, are the methods used to manage these buffers and accommodate different clocking domains. The network design constrains the buffer size to minimize latency. In Layer 1 networks, such as SDH, there is a direct linkage between the network clock and the level of wander or jitter that may be imparted on a client signal.

In the case of packet data networks transport, the data is delivered over the network in blocks (packets, frames), rather than being carried as a continuous stream of constant bit rate. Packets may be statistically multiplexed and are routed via packet switches which subject a packet to delay due to processing, buffering and retransmission at intermediate switches. Within a single switch, multiple packet streams may have to converge onto a single output buffer. The resulting buffer contention will introduce variable delay. In some cases, packets will be dropped. The clock used to drive the Layer 1 transmission links is likely to be asynchronous to the clock used within the switch. Any difference in the rate at which packets are presented for transmission and the actual transmission rate is accommodated by adding padding between packets or discarding packets.

Since packets may traverse different routes, a stream of packets from ingress to egress may exhibit significant packet delay variation. Additionally, packets may be misordered resulting in additional buffering. Services that utilize the packet network need to consider these impairments. For packet networks, large buffers are required to perform packet-level processing in which case only coarse levels of synchronization are required to support most services.

Unlike a Layer 1 network, such as SDH, there is no direct linkage between the network clock and the packet processing buffers. Thus, network timing cannot be used to control packet delay variation in these networks. The need to provide network synchronization to a packet switch is generally required only to meet any synchronization requirements for physical layer interfaces to the switch in accordance with the related TDM interface requirements as given by the particular networking standards as SDH/PDH.

Timing requirements of services carried at upper layers above the Layer 2 network (e.g., IPTV, MPEG-4) are specified to accommodate the variations of existing packet networks. Any service-specific timing is encoded at the service layer (e.g., H.264, MPEG-4).

However, there are cases when the physical layer of a packet network is synchronous (e.g., SDH) and may be utilized by the adaptation layer.

In most cases, the information carried across the packet network, i.e., the Characteristic Information (CI: see Appendix III), does not include timing information. This has certain ramifications when services require the transfer of accurate timing. For end-to-end services, the timing characteristics of the server layer need to support the synchronization requirements of the client. In traditional Layer 1 mechanisms (PDH, SDH and OTN), the network timing adaptation mechanisms are specifically designed to be compatible with the timing requirements of the client signal. When the server layer is incapable of supporting the timing of the client, alternate means of providing client timing may be required. This would be performed at the adaptation layer to the network. An example is ATM AAL1.

Impairments in the packet network may have a detrimental effect on the recovery of the service clock for constant bit rate services emulated over a packet network. This clause explores the levels of such impairments that a clock recovery process should be capable of withstanding while maintaining the clock within the relevant specifications.

The following performance parameters relating to packet network impairments are defined in ITU-T Recs Y.1540 [25] (for IP networks) and Y.1561 [27] (for MPLS networks). Similar performance measures for Ethernet networks are also defined in ITU-T Rec. Y.1731 [28].

1) Packet Transfer Delay and Delay Variation;
2) Packet Error Ratio;
3) Packet Loss Ratio;
4) Packet Severe Loss Block Outcomes.

10.1 Packet Transfer Delay and Delay Variation

10.1.1 Differential Methods

Packet transfer delay and delay variation should not affect clock recovery performance when a network reference clock is available at both ends and Differential Methods are used.

10.1.2 Adaptive Methods

Adaptive recovery of the service clock from a packet stream containing constant bit rate data is in general achieved by some computing function of the arrival rate or arrival times of the packets at the destination node.

If the delay through the packet network is constant, the frequency of arrival of packets at the destination node is not affected by the network. There may be a phase lag in the recovered clock due to the delay through the network, but there should be no frequency or phase wander.

If the delay varies, it may be perceived by a clock recovery process as a change in phase or frequency of the original service clock. Therefore, during the design of a clock recovery process, the causes of delay variation must be considered carefully.

There are several causes of delay variation on a packet network. These may include:

- random delay variation (e.g., queuing delays);
- low frequency delay variation (e.g., day/night patterns);
- systematic delay variation (e.g., store and forward mechanisms in the underlying transport layer);
- routing changes;
- congestion effects.

10.1.2.1 Random delay variation

Random variation in delay results from the behaviour of switches or routers in the packet network. The primary source of this is the output queuing delay, caused when a packet arrives at a switch or router when the exit port is blocked by other traffic, and the packet has to wait in a queue. Other factors caused by the internal operation of the switch or router may also delay the packet, as described in Appendix I.

It is not possible to predict with any certainty the delay of any packet through a switch or router, although it is likely that the delay will increase with load on the device. Therefore, there will be some correlation of delay between successive packets with the traffic load in the network.

10.1.2.2 Low frequency delay variation

As described above, the delay through a packet network, although unpredictable, is generally correlated with the load on the network at the time period in question. Load is a dynamic quantity, and may contain extremely low frequency components. For example, if a network is more heavily loaded during the day than at night, this gives a component to the load variation with a 24-hour period.

This extremely low frequency variation may lead to phase wander in a clock recovered from a packet stream with the same period. Since many of the relevant clock specifications limit the permissible phase wander over periods of 24 hours or more (e.g., G.824 [11]), this has to be compensated for during the design of a clock recovery process.

10.1.2.3 Systematic delay variation

Certain types of underlying transport networks can cause systematic variation in packet delay over time. For example, some types of transport use a "transmission window" or "timeslot", storing packets for transmission until the window opens. Examples of these include PON, xDSL and WiMAX.

The effect of the transmission window is to impose a systematic "sawtooth" delay profile onto a packet stream (see Figure 10). For regular rate packet streams, e.g., those containing constant bit rate data, the period of the transmission window may beat against the packet rate, causing a slow variation in delay over time. These effects are very similar to the waiting time jitter in TDM networks. In TDM networks it is possible to control the waiting time jitter, this is not the case in packet networks.

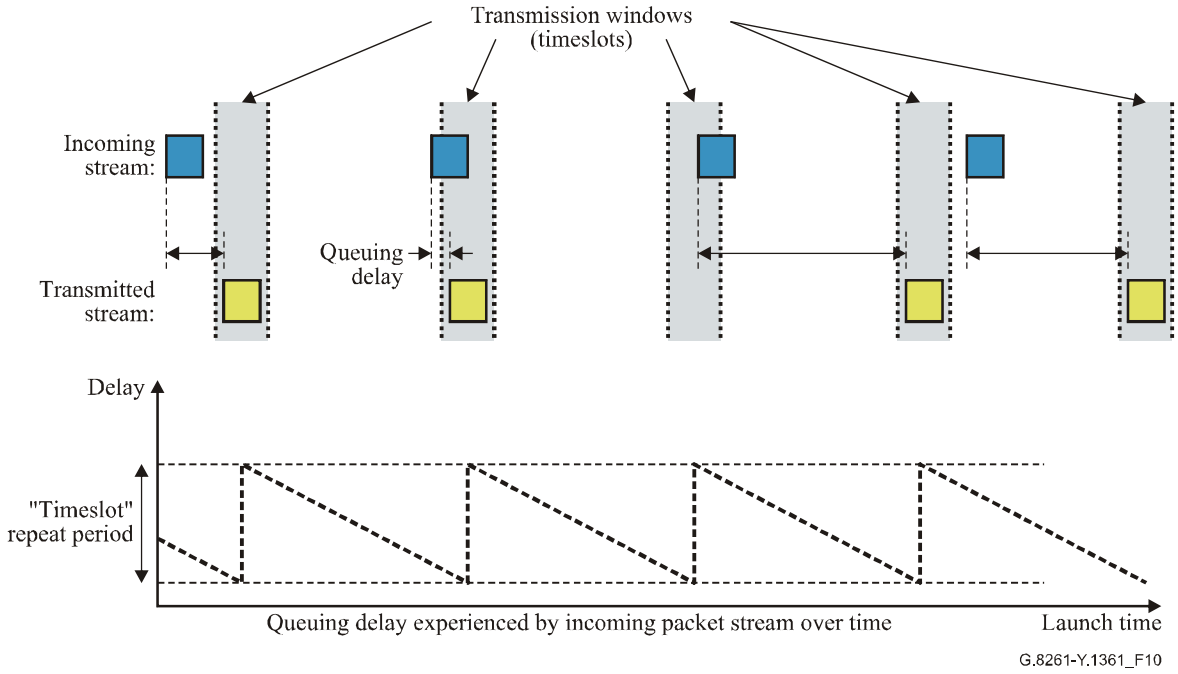


Figure 10/G.8261/Y.1361 – Systematic delay variation caused by network with timeslots

Another type of systematic delay variation that constant bit rate packet streams may be subject to is beating against other regular packet streams. Figure 11 shows what happens when two packet streams of almost the same frequency are combined onto a single packet link by a switch or router.

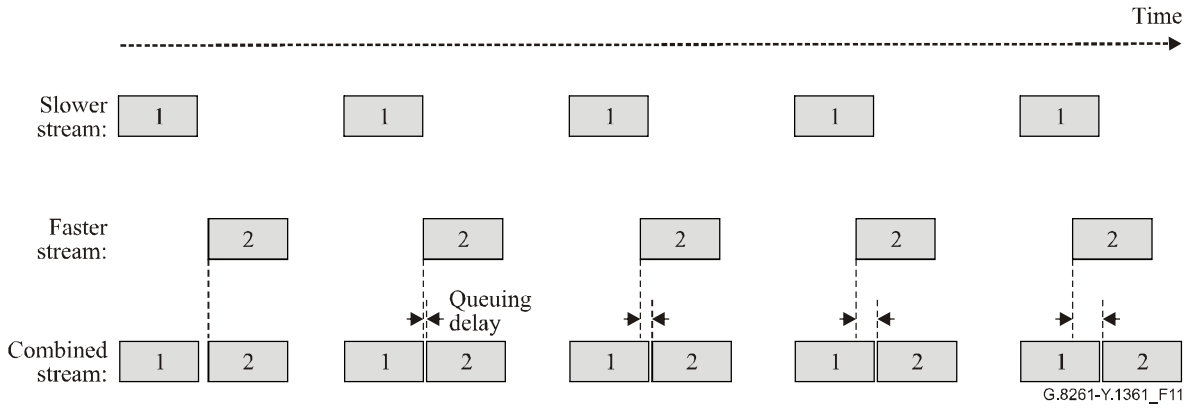


Figure 11/G.8261/Y.1361 – Beating between regular rate packet streams

Stream 1 is the slower stream, and for a time the packets in stream 1 arrive at the switch or router ahead of those in stream 2. However, the packets in stream 2 start to catch up. Since only one packet at a time can be output onto the packet link, the packets in stream 2 start to experience queuing delay (see Figure 12). This delay builds up to the point where it is equal to the transmission time of the packet on the link.

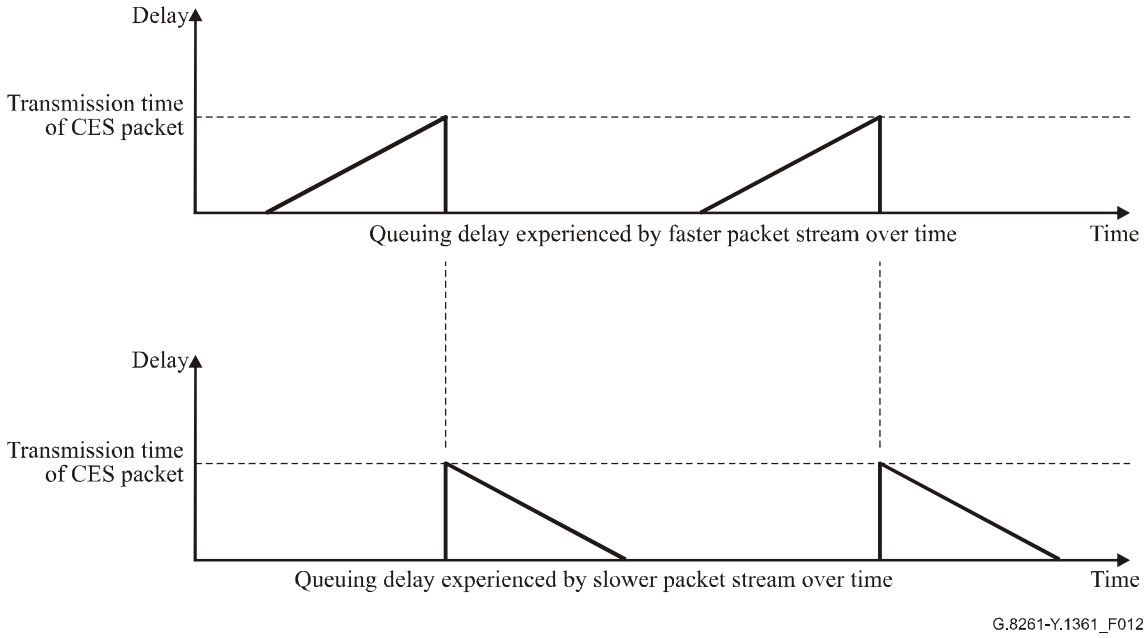


Figure 12/G.8261/Y.1361 – Delay profile experienced by beating packet streams

Eventually, the packets in stream 2 start to arrive at the switch or router ahead of those in stream 1, and the queuing delay is removed. At this point, it is stream 1 which now sees a queuing delay. This steadily declines until the packets in stream 1 arrive at the switch after the packets in stream 2 have completed transmission.

The duration of time that the packet streams experience queuing delay (i.e., the width of the triangles in Figure 12) is inversely proportional to the difference in rate between the two packet streams. Where the packet rates are very close, the duration may be extremely long. This long-term variation in the delay may cause a slow phase wander in any clock recovered from one of the packet streams.

Where multiple asynchronous constant bit rate streams share the same packet link, the effect may be additive. In the worst case, packets from all streams may line up exactly yielding the maximum queuing delay, although the frequency of this combined beat will reduce with the number of streams.

10.1.2.4 Routing changes

The route taken by a stream of packets through a packet network may change at certain instants in time. This may be due to network errors (e.g., routing around a failed or congested link), protection switching to use an alternative route, or network re-configuration.

The net effect of this is a step change in delay through the network. If uncompensated, this may be seen in the recovered clock as a phase change. Such changes must be detected and accounted for in the clock recovery process. In general, large changes in delay are relatively easy to detect and compensate for, but small changes may be masked by the general delay variation, or local oscillator drift at the clock recovery node.

10.1.2.5 Congestion effects

Congestion is the temporary increase in traffic load in all or part of a network. It may lead to all or part of the network becoming "overloaded", and packets becoming severely delayed or dropped. The duration of congestion events is variable, and may last for several seconds or minutes. If the network experiences frequent severe congestion events lasting longer than 5 minutes, it is an indication that the network is probably not suitable for running circuit emulation.

10.2 Impacts from packet impairments

10.2.1 Packet error and packet loss

Impairments within packet networks have an impact on three distinct elements within the delivery path: the IWF clock recovery process (note this may not be available to monitor), the service clock recovery; and the TDM service itself. Packet loss and packet misordering limits and their impact on the service and clock recovery processes are for further study.

Additional text discussing the relevant issues is given in the following clauses.

Packet loss and packet misordering do not significantly affect the IWF clock recovery performance for any of the methods presented in this Recommendation. Specifically, at levels at which the TDM transport service remains useable, packet loss (both uniform and bursty) and packet misordering have negligible effect on IWF clock recovery performance.

10.2.1.1 Impact on TDM service

TDM circuits carried over packet networks may be extremely vulnerable to bit errors caused by packet loss. One of the reasons for this is that bit errors are magnified by the packet transport – a single bit error in the packet leads to the whole packet being discarded, yielding a burst of consecutive bit errors in the recovered TDM stream. Hence, even moderate levels of packet loss (from the viewpoint of conventional packet network) may cause unavailability of a TDM circuit.

NOTE – The vulnerability of the TDM circuits would mainly depend upon the specific IWF characteristics. Some IWFs might employ different packet-loss concealment techniques to protect the application from packet loss.

10.2.1.2 Impact on IWF clock recovery process

The IWF clock recovery combines the packet to clock recovery algorithm, the embedded clock and the timing recovery method used (i.e., Adaptive or Differential). Performance of the IWF clock recovery process is a combination of packet network stress, the algorithm used to overcome network stress, the clock embedded within the IWF and the timing recovery method used.

NOTE – The packet loss and misordering limits for the preservation of IWF clock recovery and service clock recovery shall be specified to cover all possible packet loss scenarios; these limits are for further study.

10.2.1.3 Impact on service clock recovery

With respect to the service clock recovery process, it is required that the clock recovery has to withstand much higher packet losses than the TDM circuit itself, such that the service clock remains within specification beyond the point where the data is declared unavailable. The IWF clock recovery will directly influence the service clock recovery performance.

10.2.2 Packet severe loss block outcomes

ITU-T Recs Y.1540 [25] and Y.1561 [27] define a severe loss block outcome as occurring when, for a block of packets observed at an ingress interface during time interval T, the ratio of lost packets to total packets exceeds a threshold. Similar effects are expected in Ethernet networks.

During these impairments the timing recovery mechanism has to handle the total loss of packets as discussed in 10.2.1. This subject is for further study.

11 Impact of the reference clock impairment on timing distribution and service clock recovery

11.1 Impairments for the network-synchronous operation methods

The clocks involved in the transport of TDM signals through a packet network are shown in Figure 13.

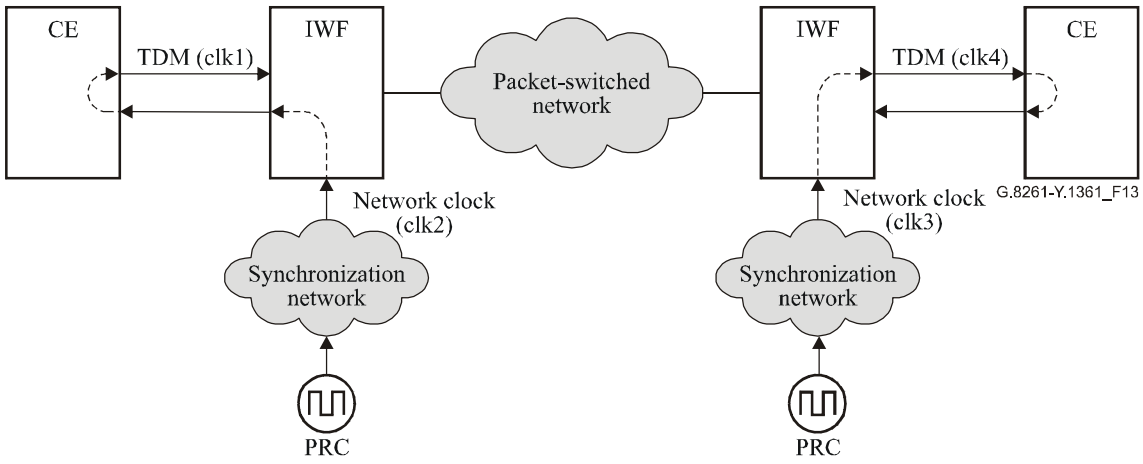


Figure 13/G.8261/Y.1361 – Clocks involved in the transport of TDM signals through a packet network for network-synchronous operation

In Figure 13, the clocks are:

– the clock that generates the TDM signal (clk1);

– the network reference clock used for de-packetization in the left hand IWF (clk2);

– the network reference clock used for de-packetization in the right hand IWF (clk3);

– the clock that generates the TDM signal after the packet network (clk4).

clk1 has to be traceable to a PRC; this can be either obtained by loop timing as shown in Figure 13, or by other means. If not, the use of a network clock reference in the de-packetizer (i.e., clk3 in the figure) will raise severe problems.

In order to have correct timing in the output TDM signal, the clocks generating (i.e., clk1) and retiming (i.e., clk4) the TDM signals must have the same long-term frequency (or within the PRC limits); otherwise an unacceptable rate of slips will be generated (the short-term noise shall be kept within the applicable limits).

In normal operation the network reference clock at the TDM source (clk1) and the network reference clock at the de-packetizer are both locked to a reference timing signal that is traceable to a PRC. However, during failures conditions in the synchronization network, these clocks may be locked to a reference timing signal that is traceable to a clock operating in holdover mode. During failure conditions, these clocks shall provide a suitable holdover that is based on the G.822 slip performance objectives.

The clock providing this holdover function during failures in the synchronization network may be either integrated in the equipment itself or available in the site (for instance, integrated in a transmission network element or in a SASE). It is the responsibility of the network planner to provide the most suitable solution.

In summary, the network synchronous mode of operation requires either the introduction of precise clocks in the sink IWF or a system that allows to switch to another suitable clock in case of loss of synchronization from the network clock (PRC).

In order to detect the periods of loss of synchronization, some kind of supervision of the traceability is needed (e.g., SSM).

11.2 Impairments for the differential method

The clocks involved in the transport of TDM signals through a packet network are shown in Figure 14.

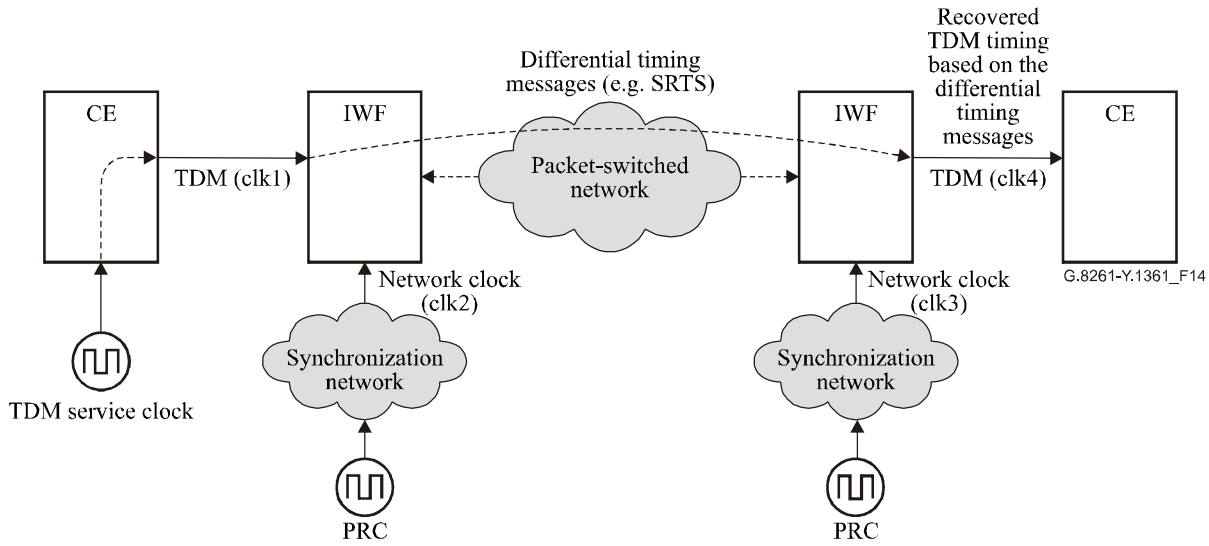


Figure 14/G.8261/Y.1361 – Clocks involved in the transport of TDM signals through a packet network for the differential method

In Figure 14 these are:

– the clock that generates the TDM signal, PDH or SDH (clk1). This clock may be plesiochronous although it is considered that most signals are now synchronous;

– the network clock that is used to generate the differential timing messages (clk2);

– the network clock (clk3) that is used to regenerate the TDM clock (clk4) based on the differential timing messages.

Any phase noise on these clocks will cause phase noise on the timing of the output TDM signal.

In order to have correct timing in the output TDM signal, the clocks generating (i.e., clk1) and retiming (i.e., clk4) the TDM signals must have the same long-term frequency (or within the PRC limits); otherwise an unacceptable rate of slips will be generated (the short-term noise shall be kept within the applicable limits).

In normal operation, the network clocks generating the differential timing messages and regenerating the TDM clock (clk2 and clk3) are locked to a reference timing signal that is traceable to a PRC. However, during failure conditions in the synchronization network, these clocks may be locked to a reference timing signal that is traceable to a clock operating in holdover mode. During failure conditions, these clocks shall provide a suitable holdover that is based on the G.822 slip performance objectives.

The clock providing this holdover function during failures in the synchronization network may be either integrated in the IWF itself or available in the site (for instance integrated in a transmission network element or in a SASE). It is the responsibility of the network planner to provide the most suitable solution.

In order to detect the periods of loss of synchronization, some kind of supervision of the traceability is needed (e.g., SSM).

12 IWF synchronization-related requirements

12.1 Traffic interfaces

The following requirements have been taken from existing Recommendations (e.g., ITU-T Recs G.823, G.824, etc.).

NOTE – The SDH interfaces are mentioned in the following clauses only for information purposes as the transport of the SDH signals over packet network is for further study.

12.1.1 Physical, electrical and optical characteristics

Physical and electrical characteristics of E0 (64 kbit/s), E11 (1544 kbit/s), E12 (2048 kbit/s) interfaces, all PDH interfaces, 51 840 kbit/s (STM-0) and ES1 (STM-1) interfaces shall comply with requirements of ITU-T Rec. G.703.

Physical and optical characteristics of STM-1, STM-4, STM-16 interfaces shall comply with requirements of the relevant physical interface Recommendation, e.g., G.957, G.691, G.959.1, etc.

12.1.2 Jitter and wander tolerance

The input jitter and wander tolerance for networks based on 2048 kbit/s hierarchy at E0, E12, E22, E31, E4 traffic interfaces shall comply with requirements of 7.1/G.823.

The input jitter and wander tolerance for networks based on 1544 kbit/s hierarchy at E11, E21, 32 064 kbit/s, E32, 97 728 kbit/s traffic interfaces shall comply with requirements of 7.2/G.824.

The input jitter tolerance for SDH-based networks at STM-1e, STM-1, STM-4, STM-16 traffic interfaces shall comply with requirements of 6.1.2/G.825. The input jitter tolerance at 51 840 kbit/s traffic interface shall comply with requirements of 16.3/G.703.

The input wander tolerance for SDH-based networks – at 51 840 kbit/s, STM-1e, STM-1, STM-4, STM-16 traffic interfaces – according to 6.1.1/G.825, shall comply with requirements of 9.1/G.812 and 8.1/G.813, whichever is applicable. These requirements are defined for synchronization interfaces (SSU and SEC respectively) because STM-N traffic interfaces are considered as synchronization interfaces.

Measurement methods are defined in ITU-T Rec. O.171 [17] and ITU-T Rec. O.172 [18].

12.2 Synchronization interfaces

The following requirements have been taken from existing Recommendations (e.g., ITU-T Rec. G.703, etc.).

12.2.1 Physical and electrical characteristics

Physical and electrical characteristics of T12 (2048 kHz) synchronization interface shall comply with requirements of clause 13/G.703.

Physical and electrical characteristics of E12 (2048 kbit/s) synchronization interface shall comply with requirements of clause 9/G.703.

Physical and electrical characteristics of E11 (1544 kbit/s) synchronization interface shall comply with requirements of clause 5/G.703.

12.2.2 Jitter and wander tolerance

The input jitter tolerance at T12, E12 synchronization interfaces, according to 7.2/G.823, shall comply with requirements of 9.2/G.812 (Type I) for SSU interfaces and of 8.2/G.813 (Option 1) for SEC interfaces, whichever is applicable.

The input jitter tolerance at E11 synchronization interface, according to 7.3/G.824, shall comply with requirements of 9.2/G.812 (Types II and III) for SSU interfaces and of 8.2/G.813 (Option 2) for SEC interfaces, whichever is applicable.

The input wander tolerance at T12, E12 synchronization interfaces, according to 7.2/G.823 shall comply with requirements of 9.1/G.812 (Type I) for SSU interfaces and of 8.1/G.813 (Option 1) for SEC interfaces, whichever is applicable.

The input wander tolerance at E11 synchronization interface, according to 7.3/G.824, shall comply with requirements of 9.1/G.812 (Types II and III) for SSU interfaces and of 8.1/G.813 (Option 2) for SEC interfaces, whichever is applicable.

12.3 IWF synchronization function

In the context of this Recommendation, the IWF provides the necessary adaptations between TDM and packet streams.

With reference to Figure 15, the possible supported timing options for the Tx clock are:

- timing from recovered source clock carried by the TDM input (loop-timing or line-timing);
- timing from the network clock (the network clock can be derived either from the physical layer of the traffic links from the packet network or through an external physical timing interface, e.g., 2048 kHz);
- timing from a free-running clock (it shall provide an accuracy according to relevant TDM/CBR service interface, e.g., 2048 kbit/s shall comply with ITU-T Rec. G.703, ±50 ppm);
- differential methods;
- adaptive timing (including clock recovery using dedicated time stamps).

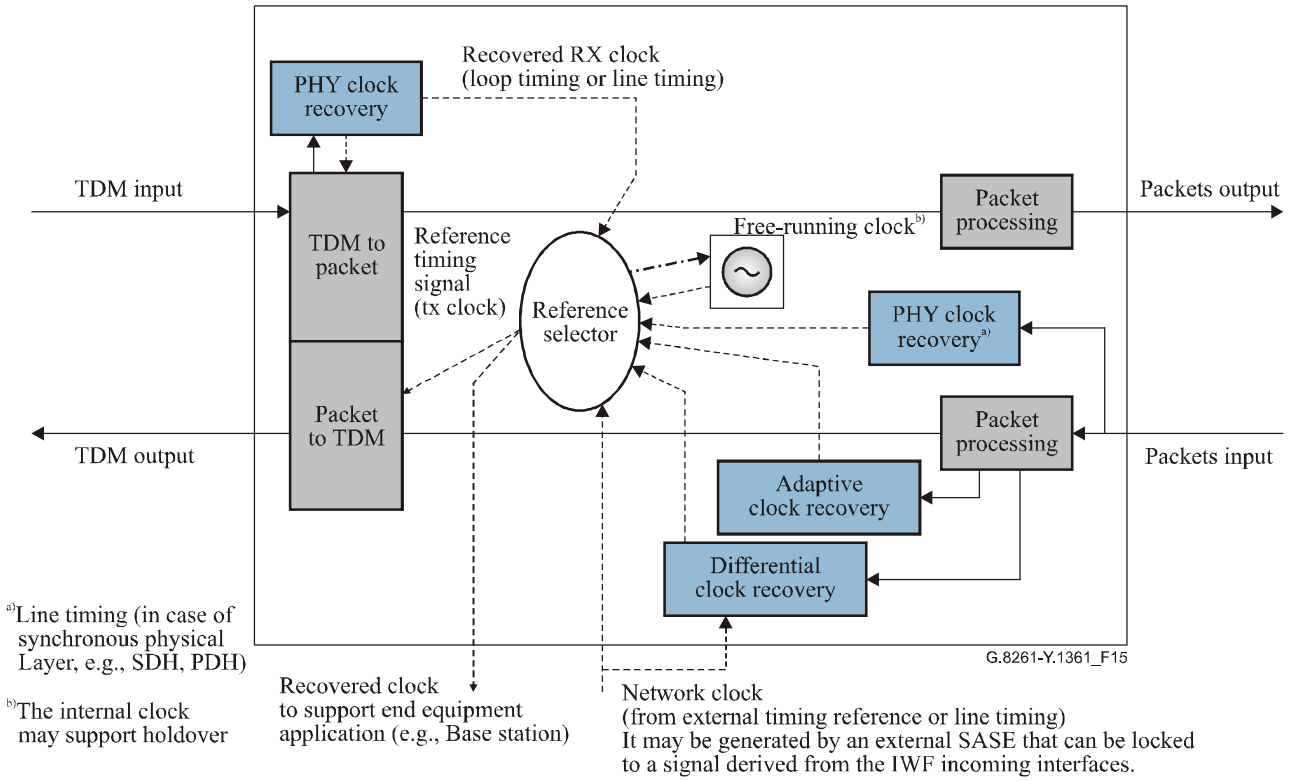


Figure 15/G.8261/Y.1361 – IWF synchronization functions (Packet to TDM direction)

Depending on the services to be provided, a suitable subset of the listed timing options shall be supported.

It is recommended to have slip control in the TDM Tx direction to control possible over/underflow in the playout buffer. Slips shall be performed on n × 125 μs frames.

When TDM transmitter and/or receiver clocks are in holdover or are traceable to clocks in holdover, and a synchronous clock recovery technique (Differential method or network-synchronous operation) is used, slips (most likely uncontrolled) will occur.

NOTE – Clock requirements are for further study.

In the TDM-to-packet direction, the synchronization-related requirements are mainly depending on the synchronization requirements of the physical layer, or to support differential timing method (these aspects are not detailed in the figure).

It shall be noted that Figure 15 provides only a functional view and is not meant to restrict implementation.

When selecting a new timing source, the output wander may temporarily exceed the output wander limit. However, the output wander must be within the output wander limit by the end of a period called the "Stabilization Period". The requirements for the stabilization period are for further study; more information is provided in Appendix II.

Another characteristic that is relevant for the IWF is the latency. The latency requirements are normally defined on the network level specifying the total latency in the end-to-end connection. Requirements on IWF contribution on the total latency is for further study.

The noise transfer characteristics can be specified on the total CES segment, including the IWFs pair that adapts the TDM flow into the packet network. The specification of the total noise transfer of a CES segment is for further study.

13 Results and consequences of the different synchronization methods over packet network reference models

The recommendations on the methodology to distribute synchronization references and to recover the timing of a TDM service differ according to the network scenarios and to the synchronization requirements that are relevant for the specific application.

The following scenarios have been identified within the scope of this Recommendation (with reference to the network models in clause 7).

13.1 Recommendations for Deployment Case 1

13.1.1 Recommendation for the timing recovery of a TDM service

The network limits for PDH signals in this case are defined in clause 7 for Deployment Case 1.

The timing recovery of PDH signals carried over packet network can be performed by means of:

- network-synchronous operation when a signal traceable to PRC is available at the IWFs and it is not required to preserve the service clock;
- differential methods when a PRC traceable reference is available at the IWF. With this method it is possible to preserve the service clock;
- adaptive methods when the delay variation in the network can be controlled. With this method it is possible to preserve the service clock.

  NOTE – In these scenarios, the network limits are quite stringent. However, it is assumed that when the network can be modelled according to Model A (at least Scenario 2 and Scenario 3, see Appendix V), the adaptive methods should allow the compliance with the network limits as defined in clause 7.

It is for further study if the adaptive method can be used in network that can be modelled according to Model B (see Appendix V).

The transport of SDH signals in this scenario is for further study. It should be noted that the clock recovery for SDH signals shall fulfil the quality level as per synchronization interfaces according to ITU-T Rec. G.823 for networks based on the 2048 kbit/s hierarchy, and in ITU-T Rec. G.824 for networks based on the 1544 kbit/s hierarchy. The use of the methods as described in 8.1 can guarantee that these requirements are fulfilled.

13.1.2 Recommendation to distribute a reference timing signal

The distribution of reference timing signals according to clause 6/G.823 and clause 6/824 is not possible to be modelled by means of Deployment Case 1 model (e.g., using methods as described in 8.2). It should be noted that the methods as described in 8.1 could be used to distribute a reference timing signal to the end IWF fulfilling the synchronization interface requirements.

Reference timing signals of lower quality are normally not applicable in these scenarios (e.g., backbone network).

13.2 Recommendations for Deployment Case 3

13.2.1 Recommendation for the timing recovery of a TDM service

The Network limits for PDH signals in this case are defined in clause 7 for Deployment Case 3.

The timing recovery of PDH signals carried over packet network can be performed by means of:

- network Synchronous operation when a signal traceable to PRC is available at the IWFs and it is not required to preserve the service clock;
- differential methods when a PRC traceable reference is available at the IWF. With this method it is possible to preserve the service clock;
- adaptive methods when the delay variation in the network can be controlled. With this method it is possible to preserve the service clock.

  NOTE – In these scenarios the network limits are less stringent than in the scenarios in 13.1. It is assumed that when the network can be modelled according to Model A, the adaptive methods should allow the compliance with the network limits as defined in clause 7.

  It is for further study if the adaptive method can be used in a network that can be modelled according to Model B.

The transport of SDH signals in this scenario is for further study. It should be noted that the clock recovery for SDH signals shall fulfil the quality level as per synchronization interfaces according to ITU-T Rec. G.823 for networks based on the 2048 kbit/s hierarchy, and in ITU-T Rec. G.824 for networks based on the 1544 kbit/s hierarchy. The use of the methods as described in 8.1 can guarantee that these requirements are fulfilled.

13.2.2 Recommendation to distribute a reference timing signal

The distribution of reference timing signals according to clause 6/G.823 and clause 6/G.824 is not possible to be modelled by means of Deployment Case 3 model (e.g., using methods as described in 8.2). It should be noted that the methods as described in 8.1 could be used to distribute a reference timing signal to the end IWF fulfilling the synchronization interface requirements.

Reference timing signals of lower quality are normally not applicable in these scenarios (e.g., backbone network).

13.3 Recommendations for Deployment Case 2 Application A

13.3.1 Recommendation for the timing recovery of a TDM service

The network limits for PDH signals in this case are defined in clause 7 for Deployment Case 2 Application A.

The timing recovery of PDH signals carried over packet network in this case can be performed by means of:

- network-Synchronous operation when a signal traceable to PRC is available at the IWFs and it is not required to preserve the service clock;
- differential methods when a PRC traceable reference is available at the IWF. With this method it is possible to preserve the service clock;
- adaptive methods when the delay variation in the network can be controlled. With this method it is possible to preserve the service clock.

  NOTE – In these scenarios the network limits are less stringent than in the scenarios in 13.1. It is assumed that when the network can be modelled according to Model A, the adaptive methods should allow the compliance with the network limits as defined in clause 7.

  It is for further study if the adaptive method can be used in network that can be modelled according to Model B.

The transport of SDH signals in this scenario is for further study. It should be noted that the clock recovery for SDH signals shall fulfil the quality level as per synchronization interfaces according to ITU-T Rec. G.823 for networks based on the 2048 kbit/s hierarchy, and in ITU-T Rec. G.824 for networks based on the 1544 kbit/s hierarchy. The use of the methods as described in 8.1 can guarantee that these requirements are fulfilled.

13.3.2 Recommendation to distribute a reference timing signal

The distribution of reference timing signals according to clause 6/G.823 and clause 6/G.824 is not possible to be modelled by means of Deployment Case 2 model (e.g., using methods as described in 8.2). It should be noted that the methods as described in 8.1 could be used to distribute a reference timing signal to the end IWF fulfilling the synchronization interface requirements.

It should be noted that normally the end equipment does not require to be synchronized to reference timing signal compliant to a synchronization interfaces as described in ITU-T Recs G.823 and G.824 and reference timing signals of lower quality could be considered in Deployment Case 2 Application A.

In this case, the timing distribution over packet network can be performed by means of:

- network-Synchronous operation when a signal traceable to PRC is available at the IWFs (by means of methods described in 8.1);
- via packet-based methods (see 8.2) when the delay variation in the network can be controlled.

  In case the required quality shall be according to the ITU-T Rec. G.823 and ITU-T Rec. G.824 traffic interface limits, it is assumed that when the network can be modelled according to Model A, these methods should allow the compliance.

  It is for further study if the packet-based methods can be used in network that can be modelled according to Model B.

13.4 Recommendations for Deployment Case 2 Application B

13.4.1 Recommendation for the timing recovery of a TDM service

The network limits for PDH signals in this case are defined in clause 7 for Deployment Case 2 Application B.

The timing recovery of PDH signals carried over packet network in this case can be performed by means of:

- network-Synchronous operation when a signal traceable to PRC is available at the IWFs and it is not required to preserve the service clock;
- differential methods when a PRC traceable reference is available at the IWF. With this method it is possible to preserve the service clock;
- adaptive methods when the delay variation in the network can be controlled. With this method it is possible to preserve the service clock.

  NOTE – In these scenarios the network limits are dependent on the characteristics of the end equipment that normally is able to tolerate the G.823 and G.824 traffic interface limits. It is assumed that when the network can be modelled according to Model A, adaptive methods should allow compliance to ITU-T Recs G.823 or G.824 as appropriate.

  It is for further study if the adaptive method can be used in network that can be modeled according to Model B.

The transport of SDH signals in this scenario is for further study. It should be noted that the clock recovery for SDH signals shall fulfil the quality level as per synchronization interfaces according to ITU-T Rec. G.823 for networks based on the 2048 kbit/s hierarchy, and in ITU-T Rec. G.824 for networks based on the 1544 kbit/s hierarchy. The use of the methods as described in 8.1 can guarantee that these requirements are fulfilled.

13.4.2 Recommendation to distribute a reference timing signal

The distribution of reference timing signals according to clause 6/G.823 and clause 6/G.824 is not possible to be modelled by means of Deployment Case 2 model (e.g., using methods as described in 8.2). It should be noted that the methods as described in 8.1 could be used to distribute a reference timing signal to the end IWF fulfilling the synchronization interface requirements.

It should be noted that normally the end equipment does not require to be synchronized to reference timing signal compliant to a synchronization interfaces as described in ITU-T Recs G.823 and G.824 and reference timing signals of lower quality could be considered in Deployment Case 2 Application B.

In this case, the timing distribution over packet network can be performed by means of:

- network-Synchronous operation when a signal traceable to PRC is available at the IWFs (by means of methods described in 8.1);
- via packet-based methods (see 8.2) when the delay variation in the network can be controlled.

  In case the required quality shall be according to the ITU-T Rec. G.823 and ITU-T Rec. G.824 traffic interface limits, it is assumed that when the network can be modelled according to Model A, these methods should allow the compliance.

  It is for further study if the packet based-methods can be used in network that can be modelled according to Model B.

Annex A

Proposed network architecture for synchronous Ethernet PHY

A.1 PRC location

A typical synchronous Ethernet architecture will have a PRC located in one of three positions dependent on the overall architecture that the network operator wishes to follow. However, these can be summarized into three generic locations. As shown in Figure A.1, these are either:

- Case A: Core-located – The PRC will be located at the core node, location "A". This architecture suggests a few PRC nodes, i.e., centrally located with some form of distribution to the IWF; or
- Case B: Access-located – The PRC will be located at some point further back within the network (geographically separate to the IWF) typically at the multi-service access point, location "B". This architecture suggests a greater number of PRC nodes to that required for Case A, i.e., the PRCs are centrally located with some form of distribution to the IWF; or
- Case C: IWF-located – The PRC will be located geographically with the IWF and there will be a direct synchronization connection to the IWF, location "C". This suggests many PRC nodes, i.e., one PRC per IWF.

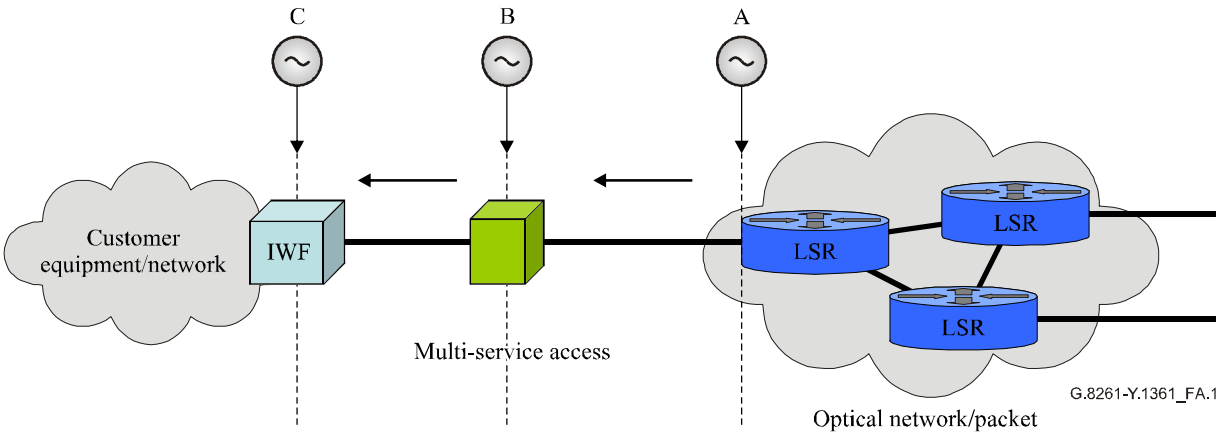


Figure A.1/G.8261/Y.1361 – Reference clock location

Referring to Figure A.1, the synchronization flow is provided from the Core Network to the IWF. It is not intended to distribute the timing from customer equipment towards the Core Network.

A.2 Synchronization Status Messaging

Synchronization Status Messaging (SSM) provides a mechanism for downstream Ethernet switches to determine the traceability of the synchronization distribution scheme back to the PRC or highest quality clock that is available. The synchronization function processes the SSM.

Under upstream network failure conditions, the synchronization function takes appropriate action based on the SSM and pre-set priorities and selects an alternate synchronization feed. This may be another network feed or an external feed.

Further details are provided in Appendix VIII.

A.3 Limiting jitter and wander of synchronous Ethernet

Limiting the jitter and wander production of the synchronous Ethernet solution in a wide area network environment will be a requirement to meet the network limits.

The synchronization function within the synchronous Ethernet switch should be based upon the performance characteristics of an embedded clock. Such a clock will ensure proper network operation occurs when such a clock is synchronized from another similar synchronous Ethernet clock or a higher-quality clock. For consistency with existing synchronization networks, the embedded clock may be based upon the ITU-T Rec. G.813 SEC. However, the precise detail of this clock is for further study. Use of such a network clock would ensure synchronization interworking compliance when such a synchronous Ethernet solution is combined with ITU-T Rec. G.812 SSU or SASE and hence to an ITU-T Rec. G.811 PRC, as specified in master-slave synchronization modes of operation. It would also allow interworking between existing TDM networks and new packet network architectures.

It should also be noted that this work does not impact any existing IEEE 802.3 specifications for frequency tolerance, etc., but refers to the new additional network element clock functionality.

Appendix I

Characteristics of Ethernet switches and networks

I.1 Delay characteristics of Ethernet switches

I.1.1 Functional operations within an Ethernet switch

From a "black box" perspective, an Ethernet frame passes through four functional operations in a typical Ethernet switch. These are shown in Figure I.1:

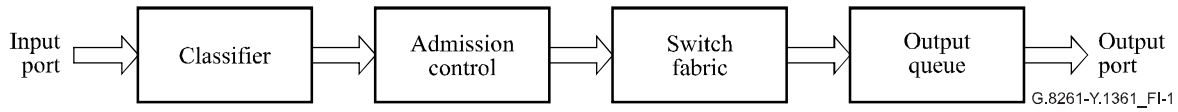


Figure I.1/G.8261/Y.1361 – Typical functions within an Ethernet switch

- Classification – Identification of the flow to which the frame belongs, and determination of the output port and priority;
- Admission control – Application of traffic management for the flow (policing, shaping, marking);
- Switching – Forwarding to the appropriate output port;
- Output queue – Waiting for a transmission slot on the output port. Typically, queuing policies such as strict priority, weighted fair queuing or round robin are applied.

The following clauses discuss the delay properties of the various functions within a switch.

I.1.2 Input stage delay

The time required for the classification and admission control stages should be approximately constant in most cases. However, depending on the switch design and the traffic loading on the switch, the delay through these functions may vary. For example, in some switches, both classification and admission control may be performed in software on a network processor. At full load, the software may not be able to keep up with the number of frames to be processed, hence the

delay may increase, and some frame dropping may occur. The same may also be true of some hardware-based designs.

Figure I.2 shows a simplistic view of the variation of input stage delay with switch loading. Under low traffic loads, the switch can cope with the number of frames passing through it without adding to the delay. As the frame rate increases, while the overall processing capacity of the switch is not exceeded, the instantaneous frame rate may exceed the available processing rate. This will cause frames to be buffered awaiting processing, and some extra delay to be incurred. Finally at some point the mean incoming frame rate may exceed the processing capacity, causing the delay to be increased further, and in some cases frames to be dropped due to lack of buffering capacity.

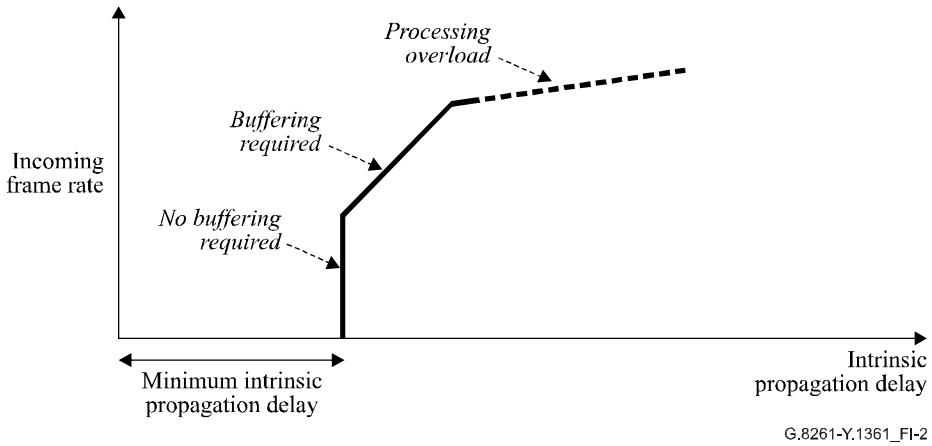


Figure I.2/G.8261/Y.1361 – Variation of input stage delay with loading

I.1.3 Switch fabric delay

The delay through the switch fabric itself is also dependent on both switch architecture and traffic loading. For example, many switches operate scheduling algorithms for switching of frames from input ports through to output ports, and this may cause a small variation in delay to the frames, depending on their arrival time relative to the scheduler "tick". However, in most cases this variation in delay is small due to the high frequency at which the scheduler works.

At very high incoming data rates, the switch fabric itself may be overloaded, and unable to cope with the full volume of traffic requiring switching. This will result in frames being dropped.

I.1.4 Output queuing delay

The amount of delay added by the output queue will depend on the queuing policy employed, and the priority of the traffic flow. For example, a high-priority flow (such as might be used for a packet timing flow) in conjunction with a strict priority policy might experience "head-of-line blocking" delay. This is where, although a frame has highest priority, it arrives at the output port just after a low-priority frame has started to be transmitted. The high-priority frame then has to wait until the other frame has finished transmitting.

Figure I.3 shows the delay profile experienced by a population of high-priority frames in conjunction with a strict priority queuing policy. For the purposes of simplicity, this diagram assumes frames experience an approximately constant delay through the other switch functions, here termed "intrinsic propagation delay through switch". A proportion of frames arrive at the output queue at a time when there are no other frames currently being transmitted. These frames are transmitted immediately. The remainder have to wait in the queue while the current transmission completes. There may also be an additional delay due to other high-priority packets also in the queue.

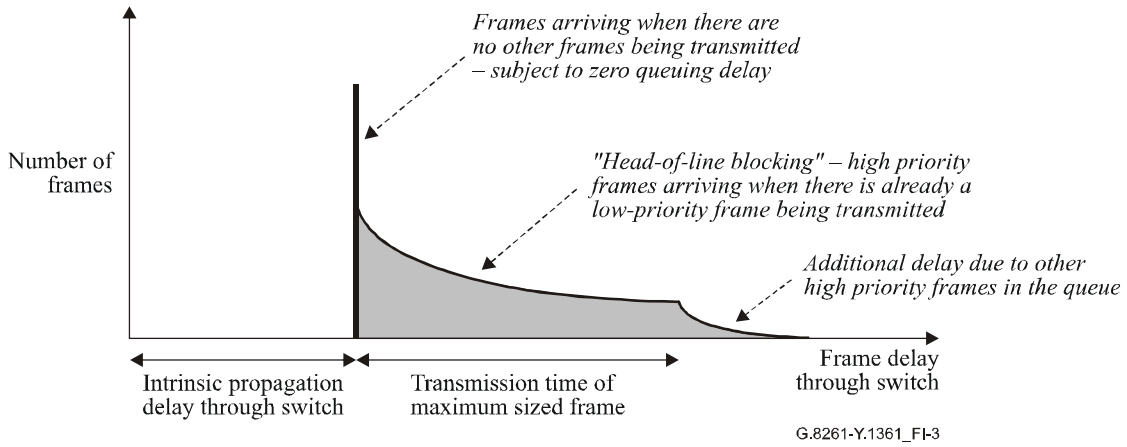


Figure I.3/G.8261/Y.1361 – Strict priority queuing: Head-of-line blocking

I.1.5 Typical delays in the Ethernet switches

Based on the model described in I.1, it is possible to provide a simplified modelling of the delays caused by an Ethernet switch, identifying two main contributions.

The first type of contributions is related to the classification, admission control and switching operations; the second type of contribution is related to the output queue and transmission.

The first type of the delay is then mainly related to the processing capacity of the switch while the second one depends on the bit rate of the outgoing line (e.g., 1 Gbit/s) and on the queuing policy/priorities that are implemented.

Assuming that the design of the Ethernet network will not implement Ethernet switches where the bottleneck is the processing capacity of the Ethernet switch, one could assume that the processing capacity should contribute with values below 10 µs (in fact a 1500-byte packet in the output queue takes 12 µs on 1 Gbit/s link) and in addition the processing overload or processing buffering should not be an issue (see Figure I.2).

With respect to the second type of delay, these can be calculated according to the model provided in Appendix V.

The simplified model is shown in Figure I.4.

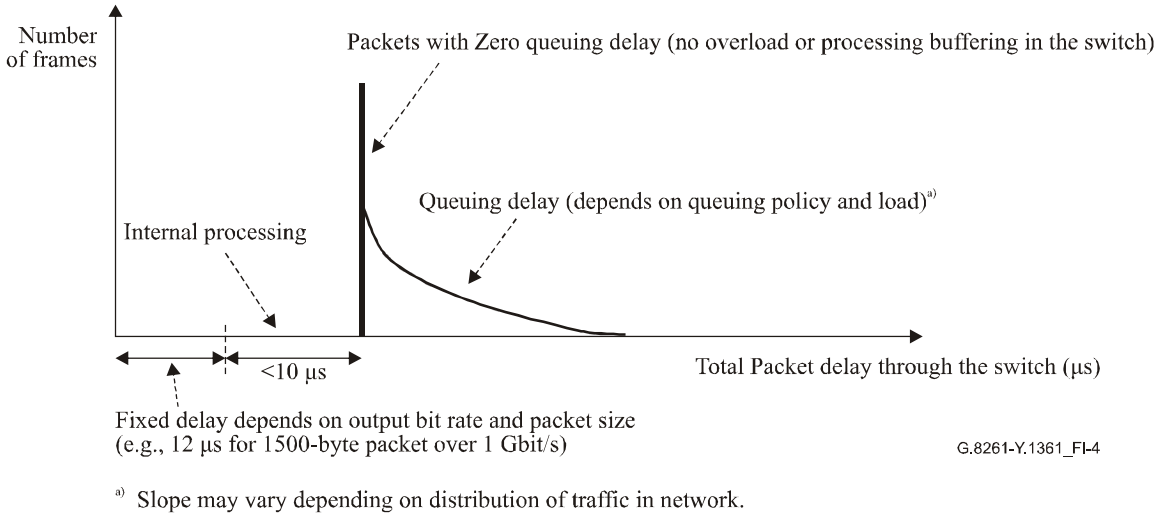


Figure I.4/G.8261/Y.1361 – Simplified model of the delays in the Ethernet switch

Referring to Figure I.4, it shall be noted that the queue processing may also impact the shape of the delay distribution.

I.2 Characteristics of switched Ethernet networks

I.2.1 Topology of Ethernet networks

Although there are many different possible network topologies, for the purpose of considering a particular flow through a network, it can be modelled as a chain of Ethernet switches as shown in Figure I.5. At each switch in the chain, an Ethernet frame has the potential to be delayed due to the mechanisms described in I.1. This delay will be affected by the other traffic flowing through the switch. Traffic directed to the same output port will affect the output queuing delay, while the sum total of all traffic flowing through the switch (including that flowing to other ports) will affect the processing and switch fabric delays.

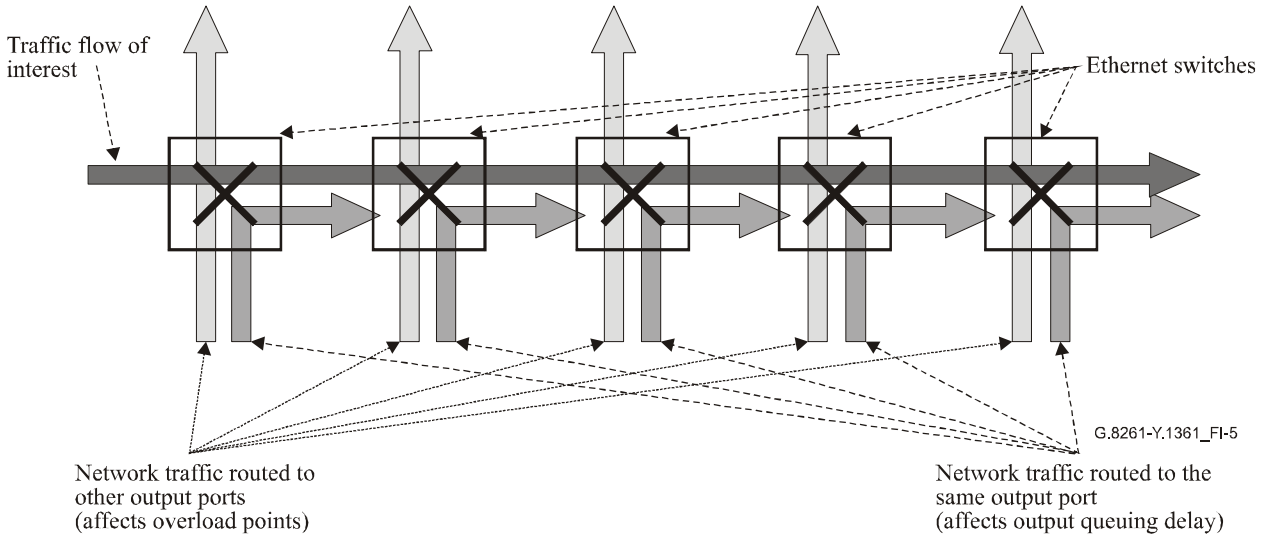


Figure I.5/G.8261/Y.1361 – Data flows within an Ethernet network

The length of the chain affects the total delay of the system; clearly the more switches there are, the greater the total delay, also the greater the delay variation. However, in many Ethernet networks, the length of the chain may be quite small. For example, in a hierarchical network, there may often be only two or three levels of hierarchy, yielding a chain length of up to five switches.

In some instances, a ring topology may be employed. Typically, these may contain around ten switches, giving a maximum "distance" around the ring of five switches. Occasionally, interconnected rings may be used, which could double the "distance" to around ten.

I.2.2 Traffic patterns and levels

With the exception of constant bit rate and real-time traffic, most network traffic is extremely bursty in nature. It has been observed that on almost any level one cares to look, traffic variation can be observed. For example, at a very small level there is bursting due to the opening and closing of the TCP window size. At a larger level, there may be bursting due to the nature of the application (e.g., downloads of large files), while at a larger level still there may be bursting due to the time of day (e.g., higher activity levels during the day than at night).

When considering the delay performance of a TDM transport flow, the effects of other traffic in the network have to be considered. For example, in Figure I.5, each of the network traffic flows may be varying in some form, independently of the other flows.

ITU-T Rec. G.1020 proposes the use of four-state Markov models for modelling packet loss distribution. A similar technique could be applied to burst lengths in each flow, allowing bursts and groups of bursts to be modelled. The longer term (e.g., diurnal variation) could then be applied as a gradual variation in burst densities.

I.2.3 Disruptive events in Ethernet networks

There are several types of "disruptive events" that may cause sudden changes in delay in an Ethernet network. The resulting delay changes may be permanent or temporary. These disruptive events include:

- routing change, causing a permanent step change in delay;
- temporary network overload, causing a significant but temporary delay change;
- temporary loss of service, causing all packets to be lost for a period.

Appendix II

Stabilization period

The stabilization period is a parameter that may be important during the start-up phase (in order to get a quick installation of the Equipment) or when switching between timing references (in order to limit the phase transient). In case the Equipment has been operating in holdover for long periods (e.g., hours), the phase error when selecting a new clock reference would be largely dominated by the phase error caused by the frequency error of the clock in holdover.

In case the adaptive method is used, the requirement on the stabilization period may depend on the actual phase noise in the packet network. In fact, a high packet delay variation in the packet network may require a long period before the clock can lock to the timing reference.

The filter implementation and the characteristics of the internal oscillator are important as well. In fact, depending on the holdover characteristics (e.g., G.812 Type II vs. Type III), longer time could be accepted when switching from a reference to a second reference, as a good holdover can allow longer locking periods (the main requirement is to limit the total phase error during reference switching).

The requirements on the stabilization period are under study.

For the purpose of the tests detailed in Appendix VI, a stabilization period of at least 900 s is proposed for the adaptive methods as, in order to properly characterize the packet delay variation statistics in a network, a sufficiently long period might be required.

Appendix III

Functional models based on ITU-T Recs G.805 and G.809

NOTE – This Appendix provides the current view on the development of synchronization modelling using some of the basic concepts provided in ITU-T Rec. G.805/Y.1306.

This version of the Recommendation deals with circuit emulation over Ethernet networks. The architecture of the Ethernet networks is specified in ITU-T Rec. G.8010/Y.1306 which defines the architecture in G.805 and G.809 terms. ITU-T Recs G.805 and G.809 are modeling methods developed by the ITU-T that allow formal specification of network architectures and equipment.

This Recommendation includes a brief description of the interworking function that is necessary to carry TDM payloads over packet-based networks (see clause 12). This Appendix provides details of certain components needed to carry emulated PDH services over packet networks. This version of the Recommendation does not describe the interworking function in terms of current G.805 modeling constructs as certain aspects related to synchronization cannot be described in terms of G.805 modeling methods. Extensions to the G.805 models are needed in this regard. This Appendix provides preliminary functional models.

The interworking function described in Figure 14 contains a number of key elements necessary to adapt TMD signals to packet-based transport.

These functions include:

- TDM-to-packet conversion;
- packet-to-TDM conversion;
- packet-related functions (e.g., addition of overhead);
- physical layer transport.

Critical to synchronization of the IWF various clocks are needed. For example:

- TDM clock recovery and generation;
- Physical layer clock recovery;
- Packet-based clock recovery.

In the case of packet-based clock recovery, this Recommendation describes two general methods: differential and adaptive.

III.1 Application of ITU-T Rec. G.805 to the IWF

ITU-T Rec. G.805 contains a number of architectural constructs that allow specification of layer networks. A key property of G.805 is the notion of client server relationships within a network architecture. A specific network may have multiple layers, each layer interacting in a client server relationship. Examples of layer networks include SDH, OTN and Ethernet. In the case of SDH, the three layers are the Path Layer, Multiplex section layer and the Regenerator section layer. The path layer is a client of the multiplex layer, the multiplex layer is a client of the regenerator layer. In the case of Ethernet, ITU-T Rec. G.8010/Y.1306 defines two layers, the ETH layer and the ETY layer. The ETH layer is analogous to Layer 2 in the OSI Reference Model (the data link layer) and provides packet type functions. The ETY layer is analogous the OSI physical layer (Layer 1).

ITU-T Rec. G.805 describes functional blocks that provide the ability to describe the properties of the individual network layers. The two key functional blocks are Adaptation functions and Trail Termination functions. Interaction between layers is provided by adaptation functions. Trail Termination functions add necessary overhead to carry the signal through the server layer network. A client layer network is carried over a server layer network by adapting the client to the server

using an adaptation function. The information that is carried over a given layer is termed the characteristic information (CI). For further information, see ITU-T Rec. G.805.

With regard to the CES IWF in this Recommendation, and with application to Ethernet ETH and ETY layers, Figure 12 contains packet layer and physical layer functions and thus both the Ethernet ETH and ETY layers are implemented within the IWF. The PDH-to-packet conversion is not part of the Ethernet layers, but can be considered as an adaptation function in terms of ITU-T Rec. G.805. The basic IWF function in the PDH-to-packet direction (PDH input to IWF) can be viewed functionally as in Figure III.1 (a), and the packet-to-TDM direction (PDH output) can be viewed as in Figure III.1 (b). Note that some clock components of the IWF are not explicitly shown on this figure (e.g., clocks, clock reference selectors), while others may be contained within specific functions. For example, PDH clock recovery may be considered as part of the PDH-to-packet layer adaptation function as it is related to adapting client layer clock information to the underlying server layer (see III.2, below). In addition, the functional blocks contained in Figure III.1 are described in ways that do not restrict implementation and may be applied to various equipment topologies.

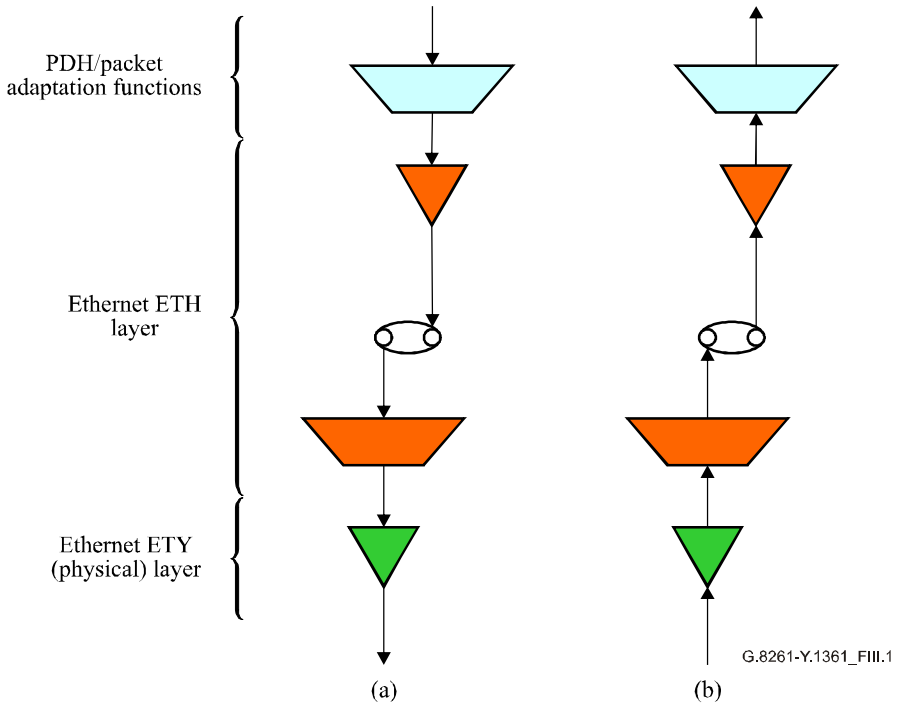


Figure III.1/G.8261/Y.1361 – Functional blocks within CES IWF

III.2 Timing information transported over layer networks

The layer network modeling methodology allows the transport of information from a client layer over a server layer network. The information that is transported is called the characteristic information (CI). The CI is defined for a specific layer network and will vary for different layer networks. For example, the characteristic information of a PDH signal consists of the data and clock information.

With respect to clock information, the PDH layer network and the ETY layer network have timing information as part of the CI while the ETH layer does not. The characteristic information of a PDH signal into the IWF consists of data and clock information (the service clock). The function of the IWF is to transport this data and clock information.

As noted above, adaptation functions are used to adapt the client information to be carried over a server layer network. In this case, the CI of the client layer network is now called Adapted Information (AI). In all cases, server layer networks can transport the data portion of the client CI, but not all server layer networks can inherently transport timing information. In such a case, where timing is required to be transported, alternative means of providing timing are required.

With respect to packet server layer networks, this Recommendation describes two methods that are intended to allow timing information of the client layer PDH signal to be carried over a packet based server layer network. Clause 9 describes differential and adaptive mechanisms to accomplish this.

III.3 Functional model of Ethernet physical layer timing

Figure 14 shows that the IWF may be timed via the "packet physical interface". In terms of the Ethernet architecture model, only the ETY trail termination function and the ETH/ETY adaptation function are used. For a point-to-point link, the functional model is shown in Figure III.2. The timing flow is shown on this figure. Timing to the ETH/ETY adaptation function may be either from an external source or from an internal free-running oscillator.

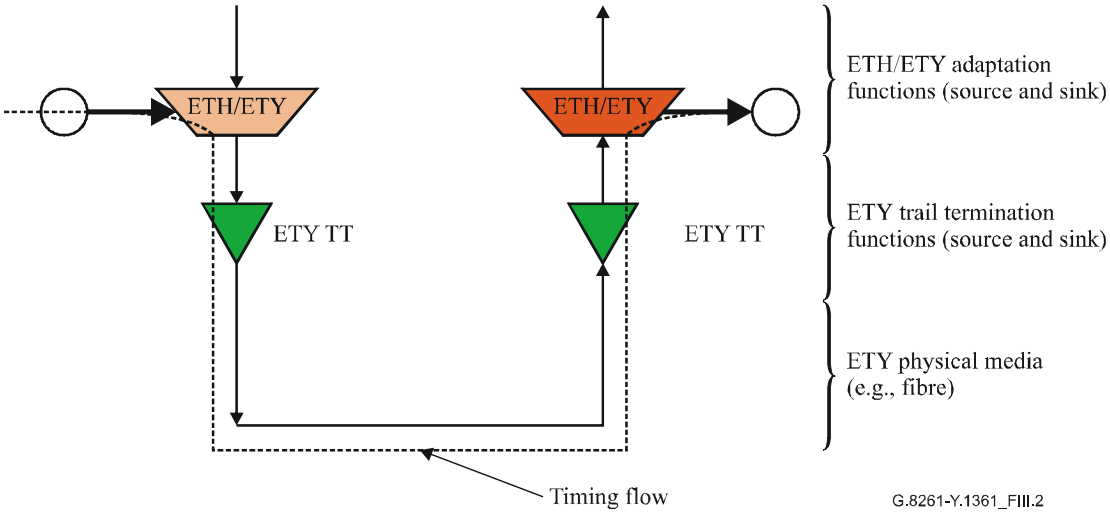


Figure III.2/G.8261/Y.1361 – Functional model for Ethernet timing (synchronous Ethernet PHY)

Figure III.3 provides an example of how physical layer timing may time a sink PDH/ETH adaptation function.

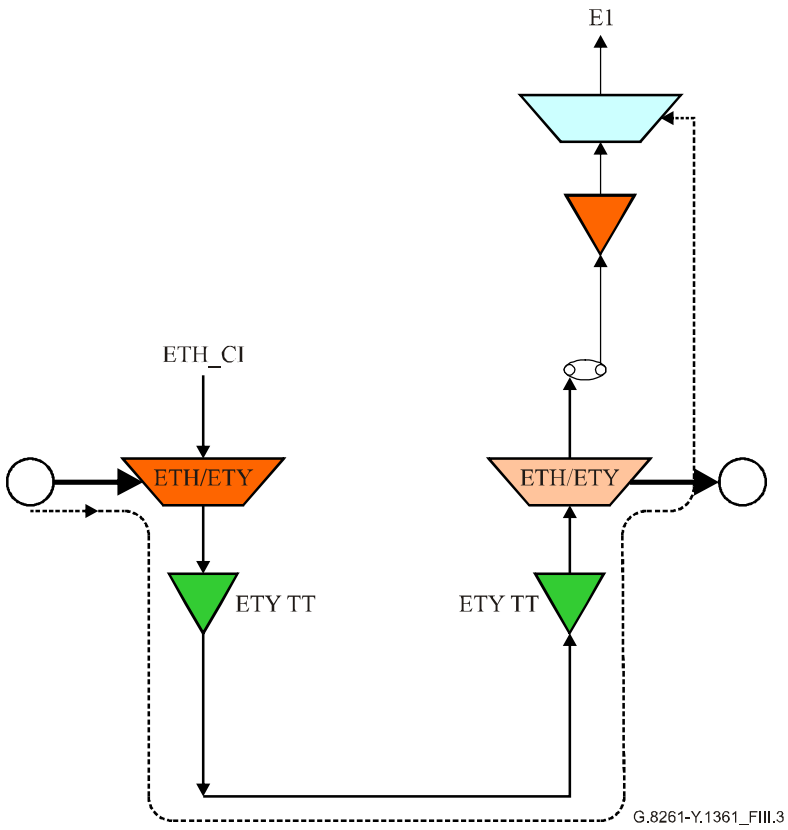


Figure III.3/G.8261/Y.1361 – Example of using physical layer timing to provide timing to an ETH/PDH adaptation function

III.4 Functional model for differential and adaptive methods

Differential and adaptive mechanisms to transfer timing based on packet methods are described in this Recommendation. In both cases, these functions reside in the PDH/ETH adaptation functions (see Figure III.1). The main difference between these two techniques is that the differential method requires a timing reference to be provided to both the sink and the source PDH/ETH function. Adaptive methods are generally based on the average packet reception rate on the sink IWF (usually accomplished either by measuring packets inter-arrival time or monitoring buffer fill level; some adaptive clock recovery mechanisms may also use time stamps) and thus do not need to be supplied with an external reference. The functional models for differential and adaptive methods are shown in Figures III.4 and III.5 respectively.

NOTE – In this appendix, two separate functions are defined for Differential and for Adaptive to allow implementation flexibility.

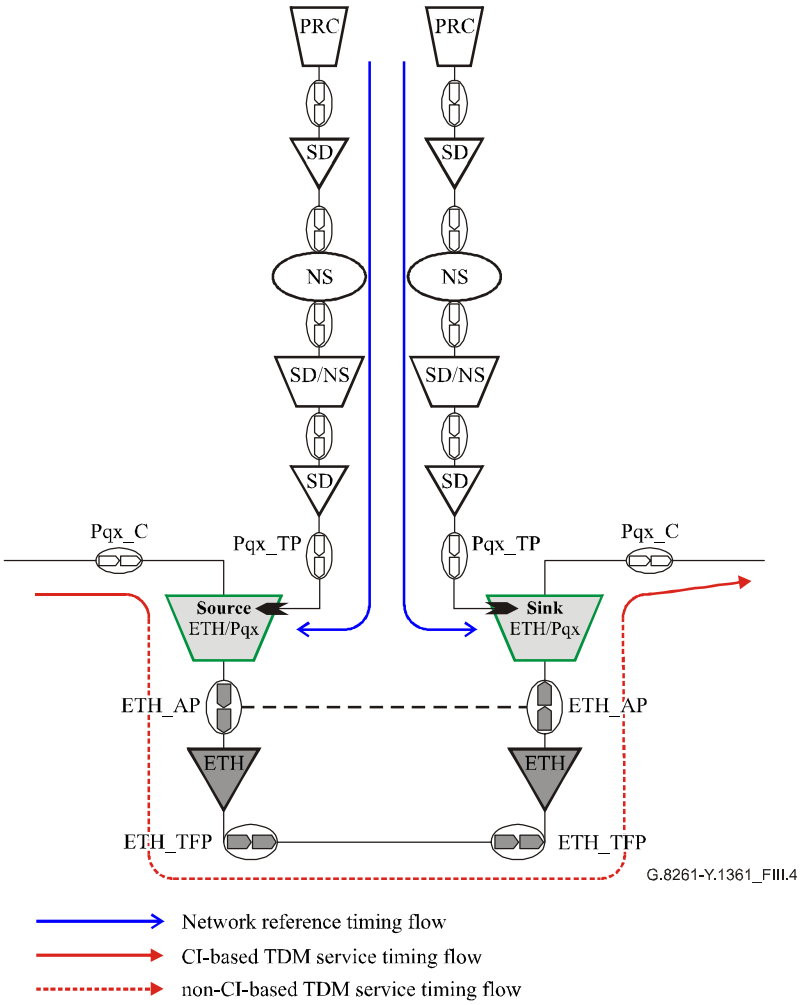


Figure III.4/G.8261/Y.1361 – Functional models for differential timing

In the case of differential mode, both source and sink IWFs (ETH/Pqx adaptation functions) are fed with a PRC-traceable reference clock (blue timing flows). At the source IWF, the difference between the timing of the service (solid red timing flow) and the external reference is encoded in the form of timestamps. This information is transferred over the Ethernet network (dashed red timing flow). At the sink IWF, the timestamps together with the external reference are used to recreate the service clock (solid red timing flow). Hence, the same reference (traceable to PRC) is required at both ends.

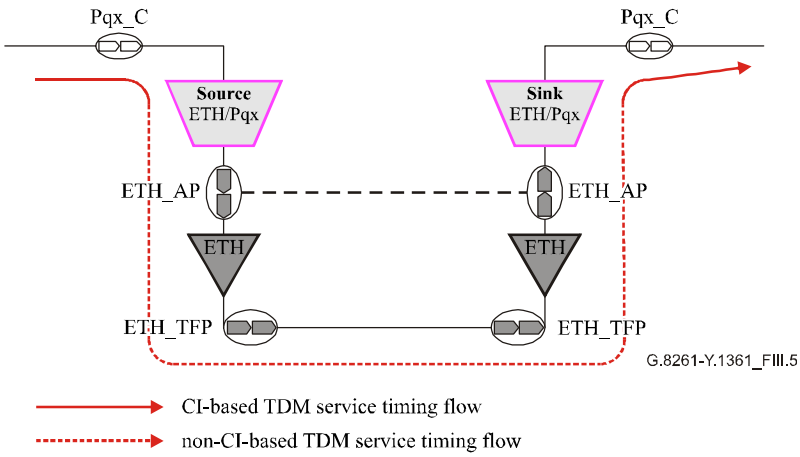


Figure III.5/G.8261/Y.1361 – Functional models for Adaptive timing

In the case of adaptive mode, the clock recovery at the sync end is based on the average packet reception rate on the sink IWF, usually accomplished either by measuring packets inter-arrival time or monitoring buffer fill level (some adaptive clock recovery mechanisms may also use timestamps). In this timing distribution mode, the use of an external reference is not required.

Details of adaptive and differential methods functions are for further study.

Appendix IV

Synchronization aspects at the edge of the network

IV.1 Synchronization requirements for GSM, WCDMA and CDMA2000 Base Stations

The timing requirements applicable to the GSM radio interface can be found in the ETSI technical specification TS 145 010 [B3]. The basic requirement is to fulfil 50 ppb frequency accuracy on the radio interface.

The timing requirements applicable to the WCDMA radio interface can be found in the technical specifications TS 125 104 (FDD mode) [B4] and TS 125 105 (TDD mode) [B5]. Also, for the WCDMA, the basic requirement is to fulfil 50 ppb frequency accuracy on the radio interface.

In order to fulfil the basic requirement, the structure and standards applicable for Layer 1 at the input of the BTS/Node B are presented in technical specifications TS 100 594 [B10] for GSM, and TS 125 402 [B6] and TS 125 431 [B10] for WCDMA.

Synchronization requirements on input signals are expressed in terms of output wander masks presented in ITU-T Recs G.823 and G.824, and traceability to a PRC source.

Technical specification TS 125 402 [B6] puts additional requirements on the phase accuracy in WCDMA TDD mode: the requirement on the relative phase difference between B nodes is to not exceed 2.5 µs.

It should be noted that in case of GSM and WCDMA radio access network there are not so strict frequency accuracy requirements related to limit the slip rate.

In fact, in these cases the data of a single user is stored in relatively large buffer (from 10 to 30 ms) and also assuming 50 ppb frequency accuracy the data would be lost (buffer empty or full) after long times, much longer if compared with classical switching network elements where buffers handling the data are much smaller (125 µs).

The relevant CDMA2000 standard is the 3GPP2 C.S0010-B. Concerning synchronization requirements, it states that:

- the timing of the base station shall be within 10 µs of UTC;
- the average frequency difference between the actual CDMA transmit carrier frequency and specified CDMA transmit frequency assignment shall be less than ±50 ppb.

In addition, according to 3GPP2 C.S0002-B specification, in order to support the CDMA System Time, all the base station digital transmissions are referenced to a common CDMA system-wide time-scale that uses the Global Positioning System (GPS) time-scale, which is traceable to, and synchronous with, Universal Coordinated Time (UTC).

Appendix V

Packet networks reference models

The packet network reference models that have been used to characterize the performance of the packet networks in terms of packet delay variations are shown in the following figures: model A in Figure V.1 is related to applications with very strict delay and delay variation requirements; model B in Figure V.2 refers to scenarios with less strict packet delay variation requirements.

These models do not describe how packet networks have to be designed. The purpose of the models is purely to get a general understanding of the characteristics of typical packet networks.

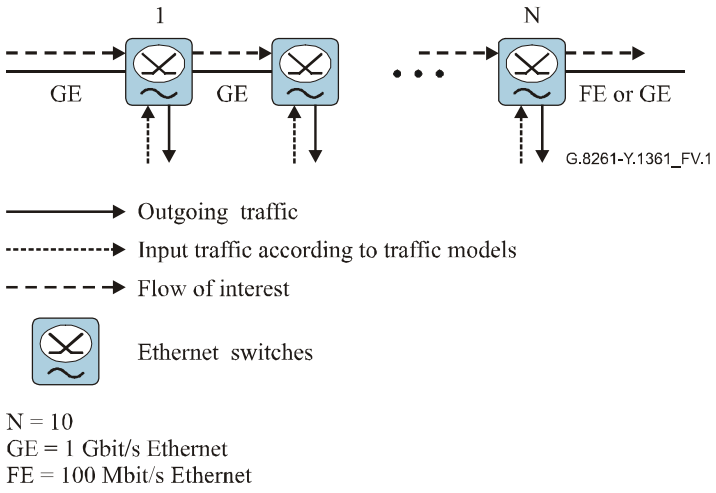


Figure V.1/G.8261/Y.1361 – Packet network reference model A (switched Ethernet network)

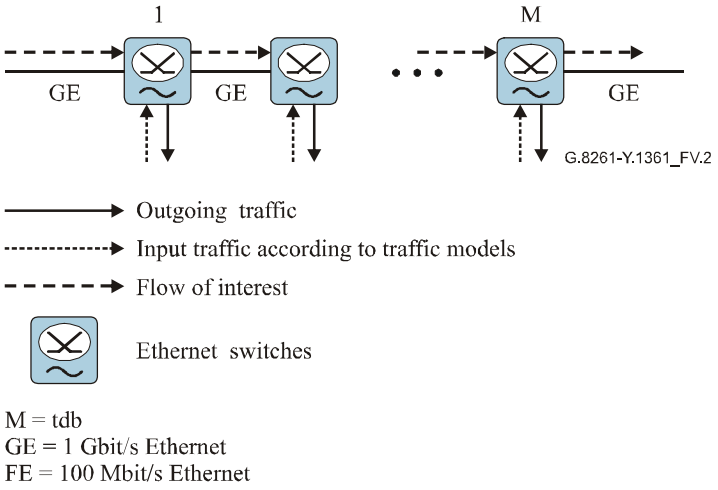


Figure V.2/G.8261/Y.1361 – Packet network reference model B (switched Ethernet network)

NOTE 1 – With respect to the number of Ethernet switches ("M") in Figure V.2, there is a common agreement that 20 is a reasonable number. This has to be confirmed.

NOTE 2 – 10 Gbit/s links could be considered in new models.

The following cases have been considered:

- Scenario 1: Switched Ethernet network – Best effort with over-provisioning (single queue);
- Scenario 2: Switched Ethernet network – Quality of service according to IEEE 802.1q, IEEE 802.1p (at least 2 queues, with one dedicated queue for handling real-time data and Weighted Fair Queuing (WFQ), discipline);
- Scenario 3: Switched Ethernet network – Quality of service according to IEEE 802.1q, IEEE 802.1p (with one queue dedicated for the handling of data used for timing recovery, e.g., timestamps).

NOTE 3 – In order to understand the applicability of the models in Figures V.1 and V.2, a simple approach could be to define two main classes of network scenarios: a backbone network, that can also be used to carry services in the access network (e.g., leasing bandwidth), and a dedicated access network. Model B (Figure V.2), could be the reference model mainly applicable for the first type of packet network (backbone), while Model A (Figure V.1) could be the reference model mainly applicable to an access network (e.g., wireless access network).

Referring to the models described in clause 7, this means that in general (most of the cases) the CE island in Case 1 and Case 3 could be characterized by packet network reference Model B, while the CE island in Case 2 could be characterized by packet network reference Model A. A third case is when bandwidth is leased by an operator to connect two end points connected via Ethernet switches (e.g., 100 Mbit/s guaranteed bandwidth over 1 Gbit/s transport). Also in this case, models in this appendix could be used. With a proper service level agreement between the customer and the Ethernet network operator, one could assume that the interfering traffic in the intermediate nodes could be considered as traffic with lower priority. The SLA in this case could guarantee bandwidth and increase priority, since both will be key elements of a premium SLA such as for instance the cellular operators will require from their Ethernet providers. This could then be considered as a scenario with traffic handling characteristics between scenario 2 and scenario 3. With respect to the expected result, when leasing bandwidth in a packet network, better performance could then normally be achieved if compared with scenarios 1 and 2.

These are the conditions considered as basis for the characterization of a packet network:

- Traffic load: 60% static;
- Packet rate: 10 packets per second;
- Observation intervals: 60 minutes;
- Traffic models according to Appendix VI;
- Packet length: 90 octets.

With respect to the conditions listed above the characteristics of 2 Mbit/s signals may also be considered: i.e., packets with a payload of 256 octets and packet rate of 1000 p/s.

Based on the above models, the parameters in Table V.1 describe the typical behaviour of the packet network in the different cases:

Table V.1/G.8261/Y.1361 – Parameters for the relevant network models

Network model		Average delay (μs)	min delay + threshold[a)] (x%) (μs)
Model A	Scenario 1	1400	800 + 1700 (95%) 800 + 800 (50%) 800 + 20 (10%) 800 + 1 (1%)
	Scenario 2	For further study	For further study
	Scenario 3	For further study	For further study
Model B	Scenario 1	For further study	For further study
	Scenario 2	For further study	For further study
	Scenario 3	For further study	For further study

a) This value is the maximum delay variation for x% of the packets (95%, 50%, 10% and 1% are the reference values).

NOTE 4 – The values are based on a configuration with only 100 Mbit/s links. This provides a conservative scenario, especially for packet with higher delay variation. Further work is needed in order to confirm and complete the table.

Details on the test cases that are needed to test the network also in non-static or failure conditions are provided in Appendix VI.

Different packet rates may be used in order to test different applications and to improve the performance of the filtering algorithms (this is relevant for adaptive methods, or more in general when the synchronization is carried over packets).

NOTE 5 – Spectral distribution should also be considered in the characterization of the packet networks. This item is for further study.

NOTE 6 – The definition of other scenarios is under study. These models should allow the study of other meaningful network scenarios (e.g., traffic concentration forming bottleneck situations as shown in Figure V.3).

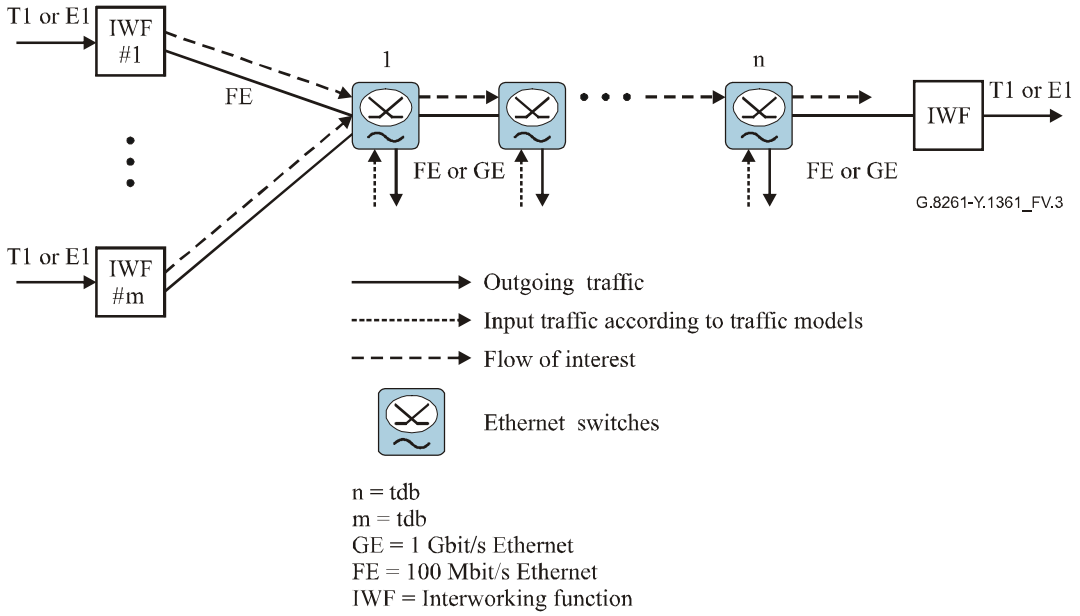


Figure V.3/G.8261/Y.1361 – Bottleneck configuration

Appendix VI

Measurement guidelines

VI.1 Measurement reference points

The measurement reference points are provided in Figure VI.1 (differential clock recovery method) and Figure VI.2 (adaptive clock recovery method). These figures provide two of the most relevant test scenarios. Additional scenarios may be identified in future versions of this Recommendation.

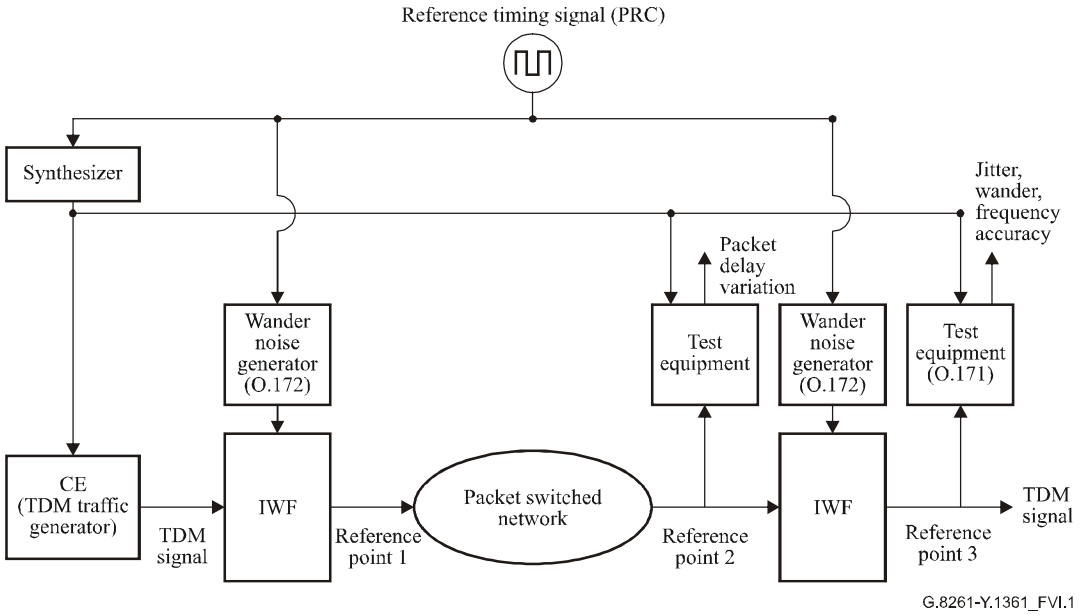
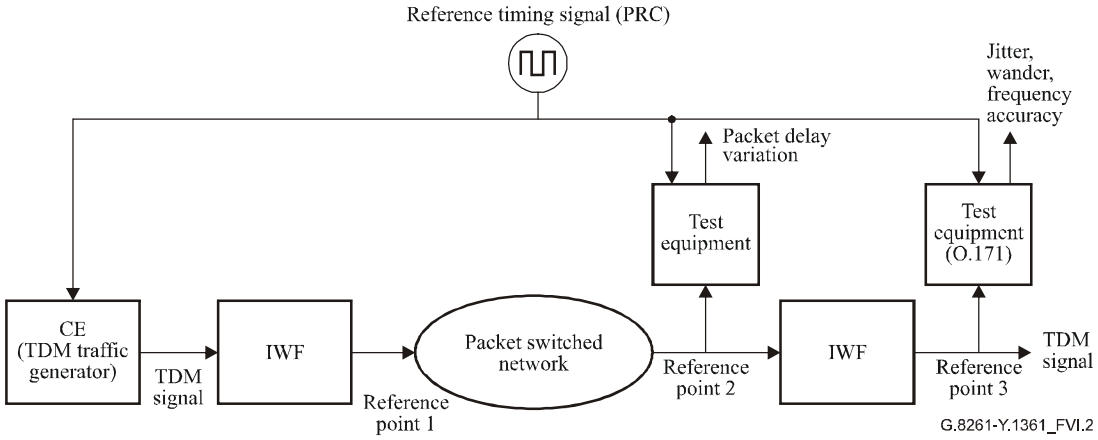


Figure VI.1/G.8261/Y.1361 – Measurement reference points in the differential clock recovery method



NOTE – The reference timing signal (PRC) is used to represent the TDM service clock.

Figure VI.2/G.8261/Y.1361 – Measurement reference points in the adaptive clock recovery method

NOTE 1 – The "Wander noise generator" in Figure VI.1 is inserted to simulate the noise generated by the synchronization network (as specified in ITU-T Rec. O.172). The output of the wander noise generator should comply with the synchronization interface as specified in ITU-T Recs G.824 and G.823.

NOTE 2 – The synthesizer in Figure VI.1 is needed to change the frequency of the asynchronous TDM signals (within the G.703 limits).

NOTE 3 – This appendix contains a suite of tests to evaluate the performance of adaptive clock recovery under different kinds of network topologies, traffic characteristics and impairments. However, the tests defined here are not exhaustive, and do not cover all possible impairments that may be caused by the packet network. Further tests may be defined in future, for example:

- Clock recovery under the presence of link aggregation such as 802.1ad;
- Clock recovery under the presence of QoS;
- Clock recovery under the presence of flow control such as 802.3x pause frames.

NOTE 4 – Tests for the differential clock recovery method still need to be defined.

NOTE 5 – Measurement methodologies for the asynchronous signals are provided in Appendix II/G.823.

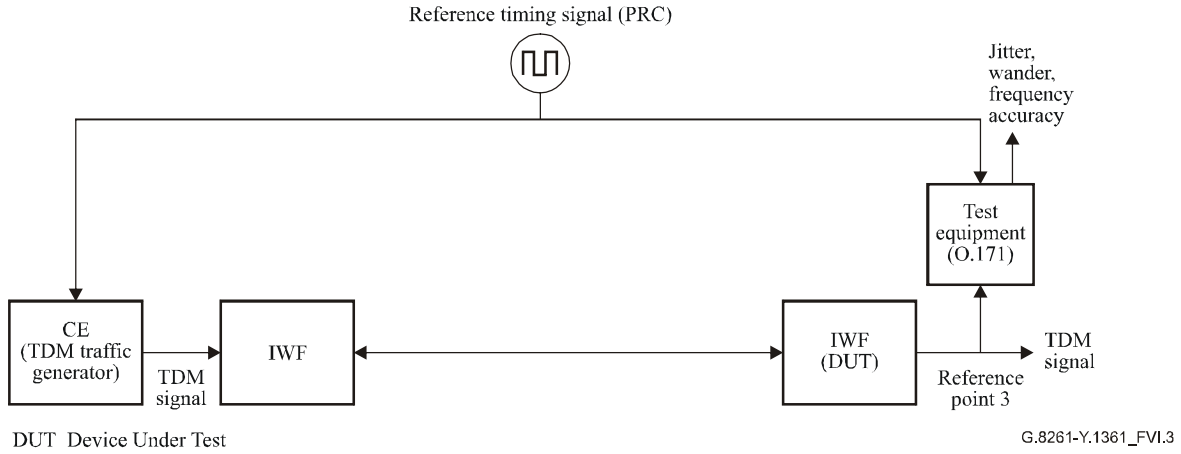
VI.2 Test topologies

The testing topologies described herein include methods for testing the synchronization methods applicable to this Recommendation.

These tests have been defined in a controlled environment (i.e., not in the field).

VI.2.1 Baseline test

Baseline test topology is shown in Figure VI.3.



NOTE – The reference timing signal (PRC) is used to represent the TDM service clock.

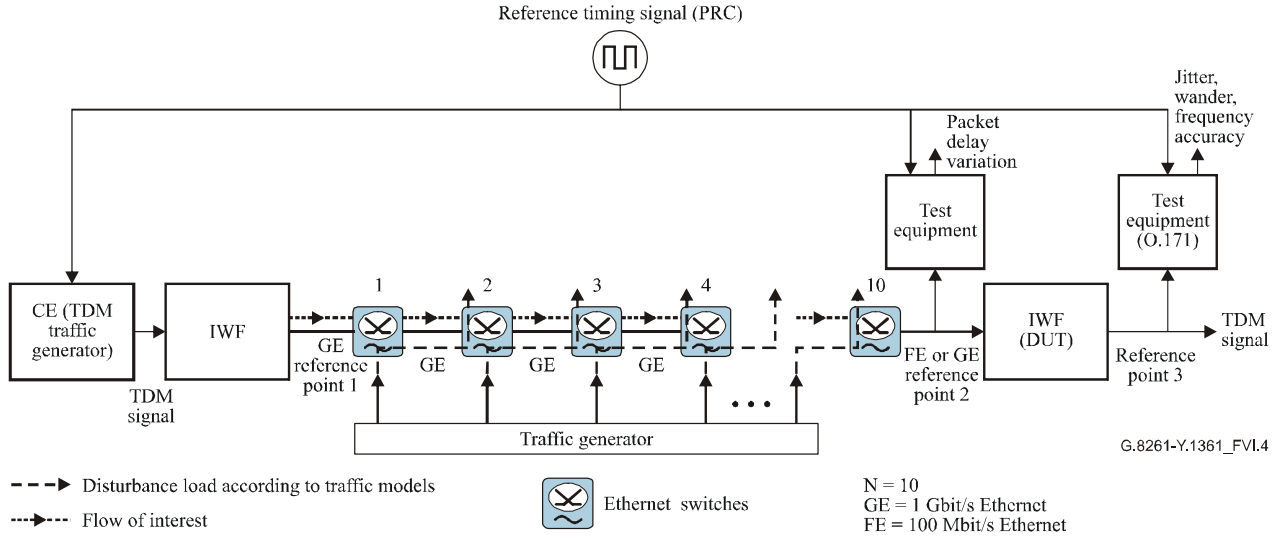
Figure VI.3/G.8261/Y.1361 – Baseline test topology

The baseline test should be done under the following conditions:

- no packet load;
- test measurements:
  - Measure TIE, MTIE, and MRTIE (as described in ITU-T Recs G.823 and G.824);
  - Measure frequency accuracy (the value for the frequency accuracy measurement integration-time is dependent upon the relevant end equipment);
  - Performance should meet the network limits for the relevant cases as defined in clause 7.

VI.2.2 Performance test

The performance test is equivalent to Model A in Appendix V, composed with either 10-gigabit Ethernet switches or 9-gigabit Ethernet switches and 1 fast Ethernet switch. The test topology is shown in Figure VI.4.



NOTE – The reference timing signal (PRC) is used to represent the TDM service clock.

Figure VI.4/G.8261/Y.1361 – Performance test topology

The DUT must be tested for stability of operation under disruptive events that may cause the synchronization to fail or go out of specification. Test Cases 1 to 6 are performed to test the DUT under load variation, network changes and packet loss.

For each of the test cases described in VI.2.2.2 to VI.2.2.7, the following measurements should be performed:

- Measure TIE, MTIE, and MRTIE (as described in ITU-T Recs G.823 and G.824).
- Measure frequency accuracy (the value for the frequency accuracy measurement integration-time is dependent upon the relevant end equipment).
- Measure packet delay variation.

Performance should meet the network limits for the relevant cases as defined in clause 7.

NOTE – The test set up as described in Figure VI.4 provides the starting point towards a common test scenario.

However, in order to get a test environment that will be simpler to be implemented and in order to remove any risk for getting different results when using Ethernet switches of different technologies, the proposal is under discussion to replace the specification as defined in Figure VI.4, with a new test set-up where, in place of the Ethernet switches and the traffic generator, the delay variation could be created by a test equipment with a delay variation profile as input.

This delay variation profile could be expressed in terms of delay variation "test vectors" (test sequence) of duration 15 min, 60 min, and 24 hours. The delay variation shall be expressed with the proper timing resolution.

The test sequences would be based on the results from the tests performed using the tests topology as described in Figure VI.4.

VI.2.2.1 Input traffic characteristics

To be able to account for different traffic types in the network, two types of disturbance traffic models are defined as described in VI.2.2.1.1 and VI.2.2.1.2.

The Network Traffic Model 1 is intended to model the traffic in the access network where the majority of the traffic is voice. The Network Traffic Model 2 is intended to model the traffic on networks where the majority of the traffic is data.

It should be noted that the CES traffic is in addition to the disturbance traffic.

VI.2.2.1.1 Network Traffic Model 1

According to 3GPP, the access traffic is composed by conversational (voice), streaming (audio-video), interactive (e.g., http) and background (sms, e-mail). It is known that in wireless network, 80% to 90% of the traffic is conversational, with the average call lasting from 1 minute to 2 minutes. To be able to model this traffic, 80% of the packets should be fixed small-size constant bit rate packets, and 20% of packets with a mix of medium and maximum size packets.

The packet size profile is:

- 80% of the load must be minimum size packets (64 octets);
- 15% of the load must be maximum size packets (1518 octets);
- 5% of the load must be medium size packets (576 octets).

Maximum size packets will occur in bursts lasting between 0.1 s and 3 s.

VI.2.2.1.2 Network Traffic Model 2

Bigger packets compared with the Network Traffic Model 1 compose the network that handles more data traffic. To be able to model this traffic, 60% of the packets must be maximum size, and 40% of packets with a mix of minimum and medium size packets.

The packet size profile is:

- 60% of the load must be maximum size packets (1518 octets);
- 30% of the load must be minimum size packets (64 octets);
- 10% of the load must be medium size packets (576 octets).

Maximum size packets will occur in bursts lasting between 0.1 s and 3 s.

VI.2.2.2 Test Case 1

Test case 1 models the "Static" Packet load. Test Case 1 must use the following network conditions:

- Network disturbance load with 80% for 1 hour assuming that the clock recovery is in a stable condition. Allow a stabilization period according to Appendix II for the clock recovery process to stabilize before doing the measurements. The packets to load the network must use Network Traffic Model 2 as defined in VI.2.2.1.2.

VI.2.2.3 Test Case 2

Test Case 2 models sudden large, and persistent changes in network load. It demonstrates stability on sudden large changes in network conditions, and wander performance in the presence of low frequency PDV.

Test Case 2 must use the following network conditions:

- The packets to load the network must use Network Traffic Model 1 as defined in VI.2.2.1.1.
- Allow a stabilization period according to Appendix II for the clock recovery process to stabilize before doing the measurements.
- Start with network disturbance load at 80% for 1 hour, drop to 20% for an hour, increase back to 80% for an hour, drop back to 20% for an hour, increase back to 80% for an hour, drop back to 20% for an hour (see Figure VI.5).

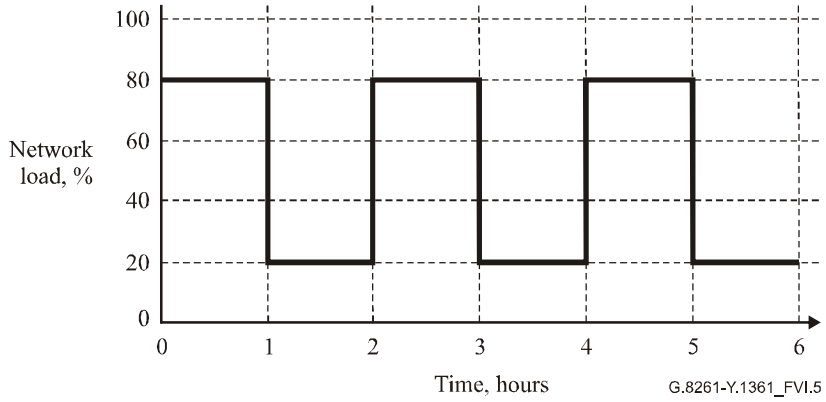


Figure VI.5/G.8261/Y.1361 – Sudden network disturbance load modulation

- Repeat the test using the Network Traffic Model 2 as defined in VI.2.2.1.2 to load the network.

VI.2.2.4 Test Case 3

Test Case 3 models the slow change in network load over an extremely long time-scale. It demonstrates stability with very slow changes in network conditions, and wander performance in the presence of extremely low frequency PDV.

Test Case 3 must use the following network conditions:

- The packets to load the network must use Network Traffic Model 1 as defined in VI.2.2.1.1.
- Allow a stabilization period according to Appendix II for the clock recovery process to stabilize before doing the measurements.
- Vary network disturbance load smoothly from 20% to 80% and back over a 24-hour period (see Figure VI.6).

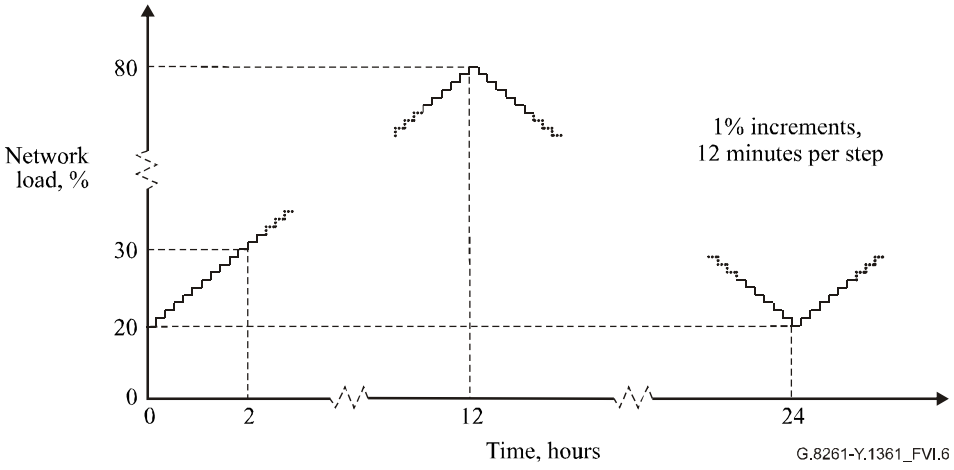


Figure VI.6/G.8261/Y.1361 – Slow network load modulation

- Repeat the test using the Network Traffic Model 2 as defined in VI.2.2.1.2 to load the network.

VI.2.2.5 Test Case 4

Test Case 4 models temporary network outages and restoration for varying amounts of time. It demonstrates ability to survive network outages and to recover on restoration. It should be noted that MTIE over the 1000 s interruption will largely be governed by the quality of the local oscillator, and should not be taken as indicative of the quality of the clock recovery process.

Test Case 4 must use the following network conditions:

- The packets to load the network must use Network Traffic Model 1 as defined in VI.2.2.1.1.
- Start with 40% of network disturbance load. After a stabilization period according to Appendix II, remove network connection for 10 s, then restore. Allow a stabilization period according to Appendix II for the clock recovery process to stabilize. Repeat with network interruptions of 100 s.
- Repeat the test using the Network Traffic Model 2 as defined in VI.2.2.1.2 to load the network.

VI.2.2.6 Test Case 5

Test Case 5 models temporary network congestion and restoration for varying amounts of time. It demonstrates ability to survive temporary congestion in the packet network.

Test Case 5 must use the following network conditions:

- The packets to load the network must use Network Traffic Model 1 as defined in VI.2.2.1.1.
- Start with 40% of network disturbance load. After a stabilization period according to Appendix II, increase network disturbance load to 100% (inducing severe delays and packet loss) for 10 s, then restore. Allow a stabilization period according to Appendix II for the clock recovery process to stabilize. Repeat with a congestion period of 100 s.
- Repeat the test using the Network Traffic Model 2 as defined in VI.2.2.1.2 to load the network.

VI.2.2.7 Test Case 6

Test Case 6 models routing changes.

Test Case 6 must use the following network conditions:

- Change the number of switches between the DUTs, causing a step change in packet network delay.
  - The packets to load the network must use Network Traffic Model 1 as defined in VI.2.2.1.1.
  - Start with 40% of network disturbance load. After a stabilization period according to Appendix II, re-route the network to bypass one switch. Allow a stabilization period according to Appendix II for the clock recovery process to stabilize, and then restore the original path.
  - Start with 40% of network disturbance load. After a stabilization period according to Appendix II, re-route the network to bypass five switches. Allow a stabilization period according to Appendix II for the clock recovery process to stabilize, and then restore the original path.
- Repeat the test using the Network Traffic Model 2 as defined in VI.2.2.1.2 to load the network.

Appendix VII

Wander limits in Deployment Case 1

VII.1 Limits for the 2048 kbit/s interface

Table 1 has been calculated based on the following considerations with reference to Annex A/G.823.

The wander budget can be split into 3 main components:

- diurnal wander;
- asynchronous mapping of 2048 kbit/s;
- wander caused by clock noise and transients.

Diurnal wander

There is no reason to change it, and its amplitude is small: 1 μs.

Asynchronous mapping of 2048 kbit/s

An RMS law has been used to calculate the accumulation of the 2UI per island, 3 island will accumulate √3 *2UI, i.e., 1.7 μs, instead of 2 μs in the original network model.

Wander caused by clock noise and transients

According to I.1.5/G.823, the accumulation process may be different, depending on the magnitude of frequency offset, which may result in correlated or uncorrelated effects. It has been agreed an RMS noise accumulation. This means that each of the 4 islands is responsible for half of the wander budget, as currently indicated in this Recommendation. In the new network model, the 3 SDH islands are responsible for √3 of one SDH island budget according to the RMS accumulation law.

The total amount of wander allocated by ITU-T Rec. G.823 is 15 µs, and simulations reported 12.6 µs.

The accumulation law between SDH and CES is different from that between SDH islands.

The noise generated in the SDH island is the result of VC-12 pointer events, which are infrequent, at least for a frequency offset in the range of 10^{-9} to 10^{-10}, as stated in I.1.5/G.823. This results in a very low probability that pointers occur at the same time in several islands.

As for the noise in a CES island, it looks very different from the one observed in SDH islands. This noise results from PDV.

As it has not been demonstrated that the RMS accumulation law applies between CES and SDH islands, it is proposed that the new model is assumed to have an RMS accumulation law for the 3 SDH islands and a linear accumulation for the CES.

Thus, the wander budget that can be allocated to CES would be:

18 – (1(diurnal wander) + √3 * 2UI(3 VC-12 mapping) + 12.6/2 * √3(3 SDH islands)) = 4.3 µs

A wander of 4.3 µs is then allocated to the CES for a period of 24 hours, and the wander template is reduced by a factor of 4.3/18 (0.24), for the other plateau derived from Table 2/G.823.

VII.2 Limits for the 1544 kbit/s interface

The wander reference model and budget for 1544 kbit/s is specified in ITU-T Rec. G.824 and consists of eight SDH islands. The wander budget components include switch synchronization, DS1 to DS3 mapping, DS1 to VC-11 mapping, Diurnal wander (Temperature effects on fibre), NE synchronization noise and wander due to random pointers. The total budget of 18 µs (over 24 hours) allows 14.3 µs of wander between switches (refer to Figure A.1/G.824) and this has been subdivided to accommodate the replacement of one SDH island with a CES island. The procedure followed assumes that accumulation of mapping wander, synchronization noise and wander due to pointers is based on RMS addition. Based on RMS addition, the portion of the 18 µs available (i.e., 12.7 – see Table VII.1) to each of the eight islands is now 4.5 µs (12.7/sqrt(8)).

Table VII.1/G.8261/Y.1361 – 1544 kbit/s wander budget component allocation

Budget component	Allocation	Portion available for subdividing
Switch synchronization	3.7	
E11-E31 mapping	0.3	
E11 to VC-11 mapping	2.6	2.6
Diurnal wander (Temp)	1.3	
NE sync noise/pointers	10.1	10.1
Total	18.0	12.7

The resulting wander for each island in terms of MTIE over all observation times up to 24 hours is given in Table 2. That table is based on a uniform reduction of the interface specification in Table 2/G.824. Note that that table also considers the mapping jitter requirements for a single VC-11 island, 0.7 UIpp, as specified in ITU-T Rec. G.783 (see Table 15-3/G.783).

The wander accumulation studies that were performed to derive the SDH wander components were based on extensive simulations to verify that the 18-microsecond requirement could be met over the SDH reference model. Future simulation work may be required when the CES network models and mappings are specified in greater detail. These numbers may be revised based on the results of that work.

Appendix VIII

Synchronization Status Messaging in synchronous Ethernet PHY

NOTE – The following text is waiting for formal allocation of an OUI from IEEE. Once this is allocated, this Appendix will become an Annex.

VIII.1 Synchronization Operations & Maintenance

OAM functionality is achieved by using OAM Protocol Data Units (OAMPDUs) which are identified by specific header fields in the Ethernet frame.

OAMPDUs are standard Ethernet MAC frames but are then identified through both the Length/Type as Slow Protocol frames (value 8809) and then specifically by a Subtype (value 0x03) as OAMPDUs. A code field is used to specify which type of OAMPDU the frame is. There are 8 possible values for the code field. A specific value (FE) is reserved for organization-specific extensions. The organization-specific extension is located in the first 3 octets of the data field and will consist of values XX, YY, ZZ (these values are to be defined by IEEE) leaving a minimum of 39 octets for OAM user data. The code field, organization-specific extension and user data portion is given in Figure VIII.1 and illustrated in Figure VIII.2.

Field description

Function	Size	Notes
Destination Address	6 octets	
Source Address	6 octets	
OAMPDU Length / Type	2 octets	Slow protocol type field value 8809
OAMPDU Subtype	1 octet	Identification of slow protocol being encapsulated for OAMPDU = 0x03
Flags	2 octets	
Code	1 octet	Identifies specific OAMPDU type set to FE
Synchronization Functionality i.e., User Data [OUI & Synchronization function]	42 octets	NOTE – The first 3 octets of user data include the OUI
Frame Check Sequence (FCS)	4 octets	

8	7	6	5	4	3	2	1	Octets
Destination address								1-6
Source address								7-12
OAMPDU Length/Type								13-14
OAMPDU subtype								15
Flags								16-17
Code								18
OUI								19-21
SSM (see Note 1)								22
Reserved (see Note 2)								23-60
Frame Check Sequence (FCS)								61-64

NOTE 1 – The entire octet is reserved for SSM use. See Figures VIII.3 and VIII.4 for details.

NOTE 2 – This table specifies the minimum requirement for the frame length of 64 octets to ensure that 802.3 frames are valid frames. As a minimum, 39 octets of padding data of an undefined nature are used to achieve this minimum length. The maximum length of the synchronization functionality field is for further study.

Figure VIII.1/G.8261/Y.1361 – Encapsulation of OAMPDU Data field section

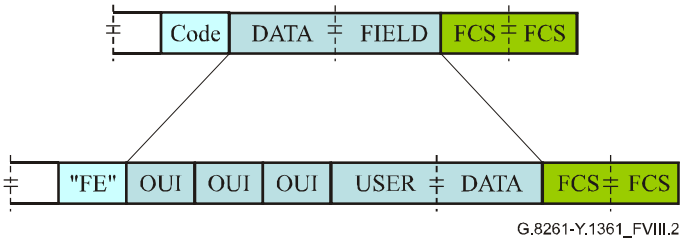


Figure VIII.2/G.8261/Y.1361 – General layout of OAMPDU Data Field section

Format, function and structure of the remaining part of the OAMPDU are given in the following clause.

However, the actual length of the data field – up to the maximum length specified by IEEE – before the Frame Check Sequence (FCS) is for further study.

VIII.2 Synchronization Status Messaging

Synchronization Status Messaging (SSM) provides a mechanism for downstream Ethernet switches to determine the traceability of the synchronization distribution scheme back to the PRC or highest quality clock that is available. The synchronization function process the SSM. Under upstream

network failure conditions, the synchronization function takes appropriate action based on the SSM and preset priorities and selects an alternate synchronization feed. This may be another network feed or an external feed.

The SSM is defined in ITU-T Recs G.707/Y.1322 and G.781 [B15]. Guidelines for SSM usage in Ethernet networks are for further study.

The general layout of the SSM section of the User Data field is given in Figure VIII.3 and is illustrated in Figure VIII.4. The first octet of the User Data field is reserved for SSMs, with the least significant half of this octet containing the SSM message and the most significant half unused but reserved for SSM capability.

Synchronization Status Message (SSM)		**Description**
Bits 8-5	Bits 4-1	
Reserved for future use	Existing SSM Status as given in ITU-T Recs G.707/Y.1322 and G.781	Existing SSM Status as given in ITU-T Recs G.707/Y.1322 and G.781

Figure VIII.3/G.8261/Y.1361 – Synchronization Status Message format

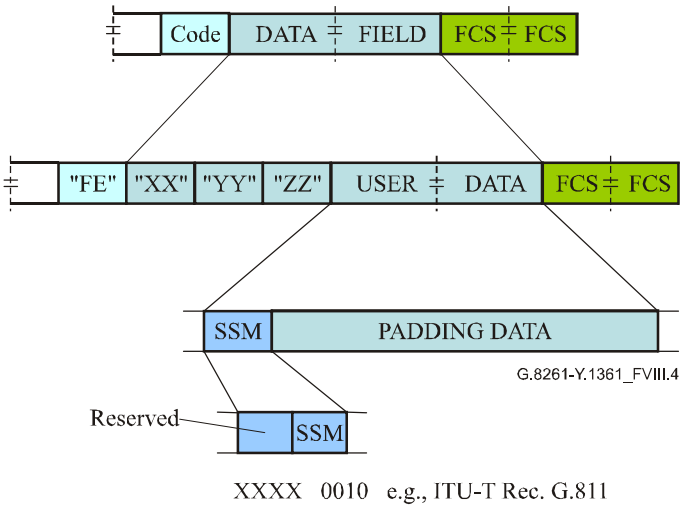


Figure VIII.4/G.8261/Y.1361 – OAMPDU Synchronization Status Message

The remaining space in the user data field is filled with padding data.

VIII.3 New Ethernet equipment

New Ethernet equipment which requires synchronization transport functionality shall support 802.3ah.

VIII.4 Legacy Ethernet equipment

It is not envisaged that Synchronous Ethernet will be used by legacy equipment as such equipment will not have the necessary changes implemented for synchronization transport.

Equipment that is not IEEE 802.3ah aware, i.e., legacy Ethernet equipment, will not recognize OAMPDU frames; any such frames will be seen as normal Ethernet MAC frames and transparently forwarded. Therefore, this function should be disabled on specific ports so it is not forwarded to unwanted networks or nodes.

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