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Timing characteristics of synchronous Ethernet equipment slave clock (EEC)

ITU-T Recommendation G.8262/Y.1362

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ITU-T Recommendation G.8262/Y.1362

Timing characteristics of synchronous Ethernet equipment slave clock (EEC)

Summary

ITU-T Recommendation G.8262/Y.1362 outlines requirements for timing devices used in synchronizing network equipment that uses synchronous Ethernet. This Recommendation defines the requirements for clocks, e.g., bandwidth, frequency accuracy, holdover and noise generation.

FOREWORD

The International Telecommunication Union (ITU) is the United Nations specialized agency in the field of telecommunications, information and communication technologies (ICTs). The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of ITU. ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

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NOTE

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As of the date of approval of this Recommendation, ITU had received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementers are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database at http://www.itu.int/ITU-T/ipr/.

CONTENTS

Introduction

The synchronous Ethernet method refers to the PRC distributed method (for instance, based on GPS), or the master-slave method using a synchronous physical layer (e.g., ETY, STM-N). These methods are widely implemented to synchronize the TDM networks.

ITU-T Recommendation G.8262/Y.1362

Timing characteristics of synchronous Ethernet equipment slave clock (EEC)

1 Scope

This Recommendation outlines minimum requirements for timing devices used in synchronizing network equipment that supports synchronous Ethernet. It supports clock distribution based on network-synchronous line-code methods (e.g., synchronous Ethernet).

This Recommendation allows for proper network operation when an EEC (Option 1 or 2) is timed from another network equipment clock or a higher-quality clock.

Included in this Recommendation are requirements for clock accuracy, noise transfer, holdover performance, noise tolerance, and noise generation. These requirements apply under the normal environmental conditions specified for the equipment.

This Recommendation contains two options for synchronous Ethernet. The first option, referred to as "EEC-Option 1", applies to synchronous Ethernet equipments that are designed to interwork with networks optimized for the 2048-kbit/s hierarchy. These networks allow the worst-case synchronization reference chain as specified in Figure 8-5 of [ITU-T G.803]. The second option, referred to as "EEC-Option 2", applies to synchronous Ethernet equipments that are designed to interwork with networks optimized for the 1544-kbit/s hierarchy. The synchronization reference chain for these networks is defined in clause II.3 of [ITU-T G.813].

A synchronous Ethernet equipment slave clock should comply with all of the requirements specific to one option and should not mix requirements between EEC-Options 1 and 2. In the clauses where one requirement is specified, the requirements are common to both options. It is the intention that EEC-Options 1 and 2 should be harmonized in the future. The intent of the synchronous Ethernet is to interoperate with existing synchronization networks based on [ITU-T G.813].

Careful consideration should be taken when interworking between networks with synchronous Ethernet based on EEC-Option 1 and networks with synchronous Ethernet based on EEC-Option 2.

Some synchronous Ethernet NEs may have a higher-quality clock. This Recommendation allows for proper network operation when a synchronous Ethernet equipment (EEC-Option 1 or 2) is timed from either another synchronous Ethernet equipment (like option), or from a SEC, or a higher-quality clock. Hierarchical timing distribution is recommended for synchronous Ethernet networks. Timing should not be passed from a synchronous Ethernet in free-run/holdover mode to a higher-quality clock since the higher-quality clock should not follow the synchronous Ethernet signal during fault conditions.

Certain Ethernet equipments such as regenerators/repeaters must provide through-timing capability to transmit timing via synchronous Ethernet. These equipments are for further study.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T G.703]	ITU-T Recommendation G.703 (2001), *Physical/electrical characteristics of hierarchical digital interfaces.*
[ITU-T G.781]	ITU-T Recommendation G.781 (1999), *Synchronization layer functions.*
[ITU-T G.783]	ITU-T Recommendation G.783 (2006), *Characteristics of Synchronous Digital Hierarchy (SDH) equipment functional blocks.*
[ITU-T G.801]	ITU-T Recommendation G.801 (1988), *Digital transmission models.*
[ITU-T G.803]	ITU-T Recommendation G.803 (2000), *Architecture of transport networks based on the synchronous digital hierarchy (SDH).*
[ITU-T G.810]	ITU-T Recommendation G.810 (1996), *Definitions and terminology for synchronization networks.*
[ITU-T G.811]	ITU-T Recommendation G.811 (1997), *Timing characteristics of primary reference clocks.*
[ITU-T G.812]	ITU-T Recommendation G.812 (2004), *Timing requirements of slave clocks suitable for use as node clocks in synchronization networks.*
[ITU-T G.813]	ITU-T Recommendation G.813 (2003), *Timing characteristics of SDH equipment slave clocks (SEC).*
[ITU-T G.822]	ITU-T Recommendation G.822 (1988), *Controlled slip rate objectives on an international digital connection.*
[ITU-T G.823]	ITU-T Recommendation G.823 (2000), *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy.*
[ITU-T G.824]	ITU-T Recommendation G.824 (2000), *The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy.*
[ITU-T G.825]	ITU-T Recommendation G.825 (2000), *The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH).*
[ITU-T G.8010]	ITU-T Recommendation G.8010/Y.1306 (2004), *Architecture of Ethernet layer networks.*
[ITU-T G.8261]	ITU-T Recommendation G.8261/Y.1361 (2006), *Timing and synchronization aspects in packet networks.*
[ITU-T Q.551]	ITU-T Recommendation Q.551 (2002), *Transmission characteristics of digital exchanges.*
[IEEE 802.3]	IEEE Standard 802.3 -2005, *Information technology – Telecommunications and information exchange between systems – Local and metropolitan area networks – Specific requirements Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications.*

3 Definitions

The terms and definitions used in this Recommendation are contained in [ITU-T G.810].

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

EEC   Ethernet Equipment Clock

ETH	Ethernet MAC layer network
ETY	Ethernet PHY layer network
MTIE	Maximum Time Interval Error
NE	Network Element
OAM	Operation, Administration and Maintenance
PRC	Primary Reference Clock
SDH	Synchronous Digital Hierarchy
SEC	SDH Equipment Clock
STM	Synchronous Transport Module
TDEV	Time Deviation
UI	Unit Interval
UTC	Coordinated Universal Time

5 Conventions

This clause is intentionally left blank.

6 Frequency accuracy

6.1 EEC-Option 1

Under free-running conditions, the EEC output frequency accuracy should not be greater than 4.6 ppm with regard to a reference traceable to a [ITU-T G.811] clock.

NOTE – The time interval for this accuracy is for further study. Values of 1 month and 1 year have been proposed.

6.2 EEC-Option 2

Under prolonged holdover conditions, the output frequency accuracy of the different types of node clocks should not exceed 4.6 ppm with regard to a reference traceable to a primary reference clock, over a time period T of 1 year.

NOTE – The time period T applies after 30 days of continuous synchronized operation.

7 Pull-in, hold-in, and pull-out ranges

7.1 Pull-in range

7.1.1 EEC-Option 1

The minimum pull-in range should be ±4.6 ppm, whatever the internal oscillator frequency offset may be.

7.1.2 EEC-Option 2

The minimum pull-in range should be ±4.6 ppm, whatever the internal oscillator frequency offset may be.

7.2   Hold-in range

7.2.1   EEC-Option 1

The hold-in range for EEC-Option 1 is not required.

7.2.2   EEC-Option 2

The hold-in range for EEC-Option 2 should be ±4.6 ppm, whatever the internal oscillator frequency offset may be.

7.3   Pull-out range

7.3.1   EEC-Option 1

The pull-out range is for further study. A minimum value of ±4.6 ppm has been proposed.

7.3.2   EEC-Option 2

The pull-out range is not applicable.

8   Noise generation

The noise generation of an EEC represents the amount of phase noise produced at the output when there is an ideal input reference signal or the clock is in holdover state. A suitable reference, for practical testing purposes, implies a performance level at least 10 times more stable than the output requirements. The ability of the clock to limit this noise is described by its frequency stability. The measures MTIE and Time Deviation (TDEV) are useful for characterization of noise generation performance.

MTIE and TDEV are measured through an equivalent 10-Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 seconds. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\tau$).

8.1   Wander in locked mode

8.1.1   EEC-Option 1

When the EEC is in the locked mode of operation synchronized to a wander-free reference, the MTIE measured using the synchronized clock configuration defined in Figure 1a of [ITU-T G.810] should have the limits in Table 1, if the temperature is constant (within ±1°K):

Table 1 – Wander generation (MTIE) for EEC-Option 1 with constant temperature

MTIE limit [ns]	Observation interval τ [s]
40	$0.1 < \tau \le 1$
$40\,\tau^{0.1}$	$1 < \tau \le 100$
$25.25\,\tau^{0.2}$	$100 < \tau \le 1000$

The resultant requirement is shown by the thick solid line in Figure 1.

When temperature effects are included, the allowance for the total MTIE contribution of a single EEC increases by the values in Table 2.

Table 2 – Additional wander generation (MTIE) for EEC-Option 1 with temperature effects

Additional MTIE allowance [ns]	Observation interval τ [s]
0.5 τ	$\tau \leq 100$
50	$\tau > 100$

The resultant requirements are shown by the thin solid line in Figure 1.
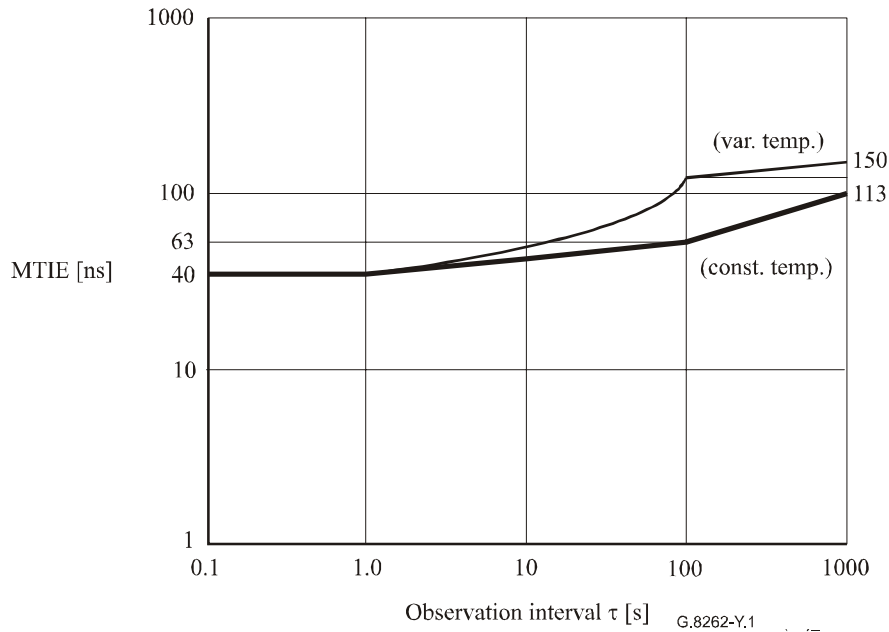
Figure 1 – Wander generation (MTIE) for EEC-Option 1

When the EEC is in the locked mode of operation, the TDEV measured using the synchronized clock configuration defined in Figure 1a of [ITU-T G.810] should have the limits in Table 3, if the temperature is constant (within ±1°K):

Table 3 – Wander generation (TDEV) for EEC-Option 1 with constant temperature

TDEV limit [ns]	Observation interval τ [s]
3.2	$0.1 < \tau \leq 25$
0.64 $\tau^{0.5}$	$25 < \tau \leq 100$
6.4	$100 < \tau \leq 1000$

The resultant requirements are shown in Figure 2.
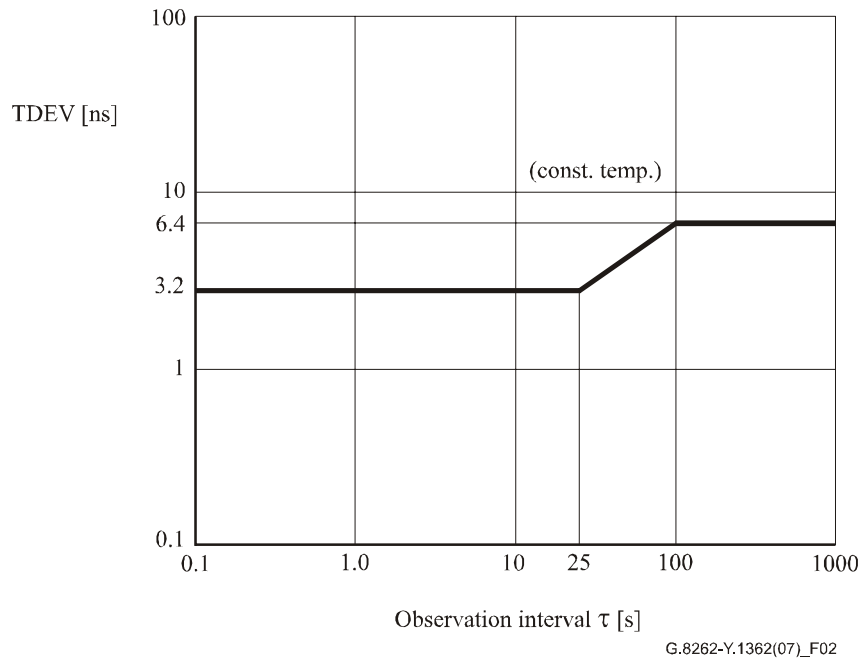
Figure 2 – Wander generation (TDEV) for EEC-Option 1 with constant temperature

The allowance for the total TDEV contribution of a single EEC when temperature effects are included is for further study.

8.1.2 EEC-Option 2

When the EEC clock is in the locked mode of operation synchronized to a wander-free reference, the MTIE and TDEV measured at the output under constant temperature (within ±1°K) shall be below the limits in Tables 4 and 5.

Table 4 – Wander generation (MTIE) for EEC-Option 2 with constant temperature

MTIE limit [ns]	Observation interval τ [s]
20	$0.1 < \tau \leq 1$
$20\,\tau^{0.48}$	$1 < \tau \leq 10$
60	$10 < \tau \leq 1000$

Table 5 – Wander generation (TDEV) for EEC-Option 2 with constant temperature

TDEV limit [ns]	Observation interval τ [s]
$3.2\,\tau^{-0.5}$	$0.1 < \tau \leq 2.5$
2	$2.5 < \tau \leq 40$
$0.32\,\tau^{0.5}$	$40 < \tau \leq 1000$
10	$1000 < \tau \leq 10\,000$

The resultant requirements are shown in Figures 3 and 4.
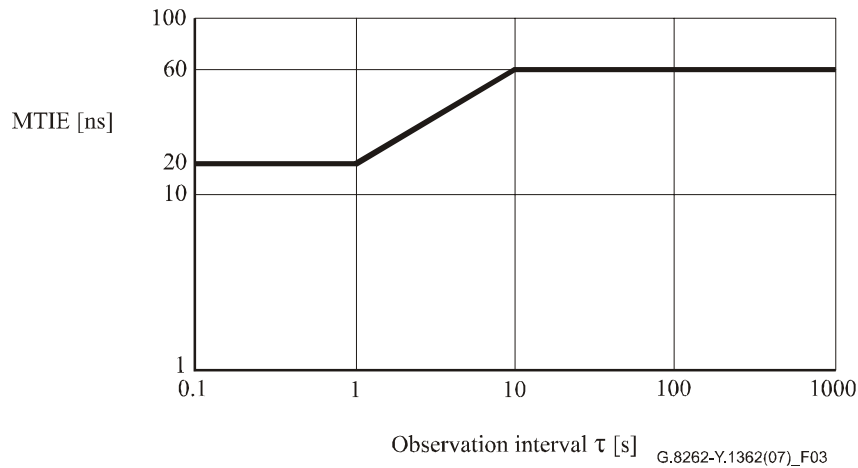
Figure 3 – Wander generation (MTIE) for EEC-Option 2 with constant temperature
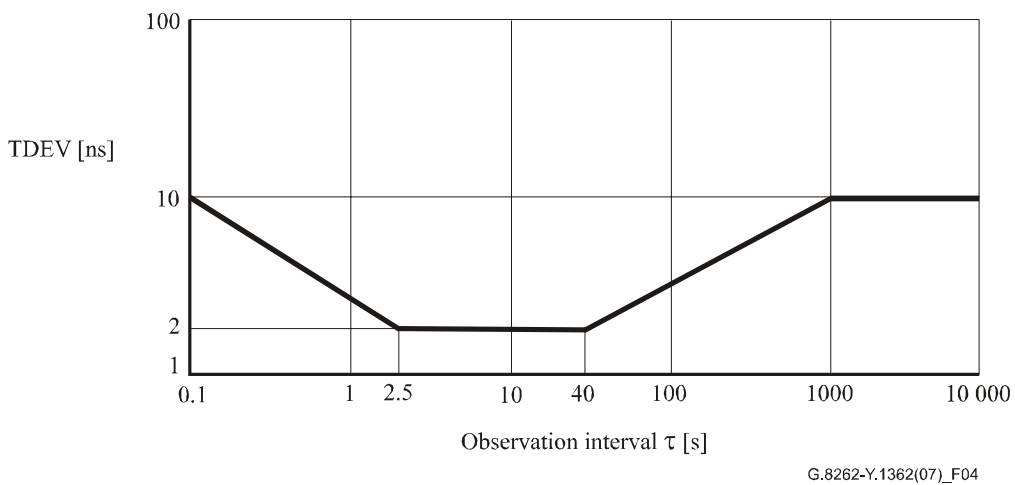
Figure 4 – Wander generation (TDEV) for EEC-Option 2 with constant temperature

8.2   Non-locked wander

When a clock is not locked to a synchronization reference, the random noise components are negligible compared to deterministic effects like initial frequency offset. Consequently, the non-locked wander effects are included in clause 11.2.

8.3   Jitter

While most requirements in this Recommendation are independent of the output interface at which they are measured, this is not the case for jitter production; jitter generation requirements utilize existing Recommendations that have different limits for different interface rates. These requirements are stated separately for the interfaces identified in clause 12.

8.3.1 EEC-Option 1

Jitter generation for Ethernet interfaces for EEC-Option 1 is specified in [IEEE 802.3].

Jitter generation for the 2048-kHz and 2048-kbit/s interface, and for the STM-N interface are defined in clause 7.3 for Option 1 in [ITU-T G.813].

NOTE – Measurement methodology for Ethernet is defined in [IEEE 802.3]. The applicability for the measurement in a synchronization network environment is for further study.

8.3.2 EEC-Option 2

Jitter generation for Ethernet interfaces for EEC-Option 2 is specified in [IEEE 802.3].

Jitter generation for the 1544-kbit/s interface and for the STM-N interfaces are defined in clause 7.3 for Option 2 in [ITU-T G.813].

NOTE – Measurement methodology for Ethernet is defined in [IEEE 802.3]. The applicability for the measurement in a synchronization network environment is for further study.

9   Noise tolerance

The noise tolerance of an EEC indicates the minimum phase noise level at the input of the clock that should be accommodated whilst:

–   maintaining the clock within prescribed performance limits. The exact performance limits are for further study;

–   not causing any alarms;

–   not causing the clock to switch reference;

–   not causing the clock to go into holdover.

In general, the noise tolerance of the EEC is the same as the network limit for the synchronization interface in order to maintain acceptable performance. However, the synchronization interface network limit may be different according to the application. Therefore, in order to determine the EEC noise tolerance, the worst-case network limit should be used. An explanation of the different network limits is given in Appendix I of [ITU-T G.813] for information.

The wander and jitter tolerances given in clauses 9.1 and 9.2 represent the worst levels that a synchronization carrying interface should exhibit. The TDEV signal used for a conformance test should be generated by adding white, Gaussian noise sources, of which each has been filtered to obtain the proper type of noise process with the proper amplitude.

MTIE and TDEV are measured through an equivalent 10-Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 seconds. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\ \tau$).

9.1   Wander tolerance

9.1.1   EEC-Option 1

The input wander tolerance expressed in MTIE and TDEV limits is given in Tables 6 and 7.

Table 6 – Input wander tolerance (MTIE) for EEC-Option 1

MTIE limit [μs]	Observation interval τ [s]
0.25	$0.1 < \tau \le 2.5$
$0.1\ \tau$	$2.5 < \tau \le 20$
2	$20 < \tau \le 400$
$0.005\ \tau$	$400 < \tau \le 1000$

Table 7 – Input wander tolerance (TDEV) for EEC-Option 1

TDEV limit [ns]	Observation interval τ [s]
12	$0.1 < \tau \le 7$
$1.7\,\tau$	$7 < \tau \le 100$
170	$100 < \tau \le 1000$

The resultant requirements are shown in Figures 5 and 6.

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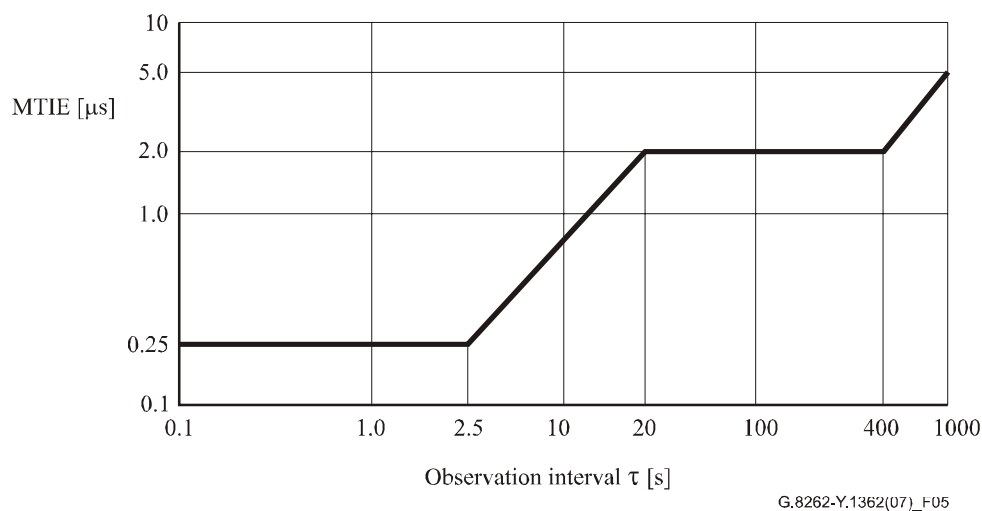
Figure 5 – Input wander tolerance (MTIE) for EEC-Option 1

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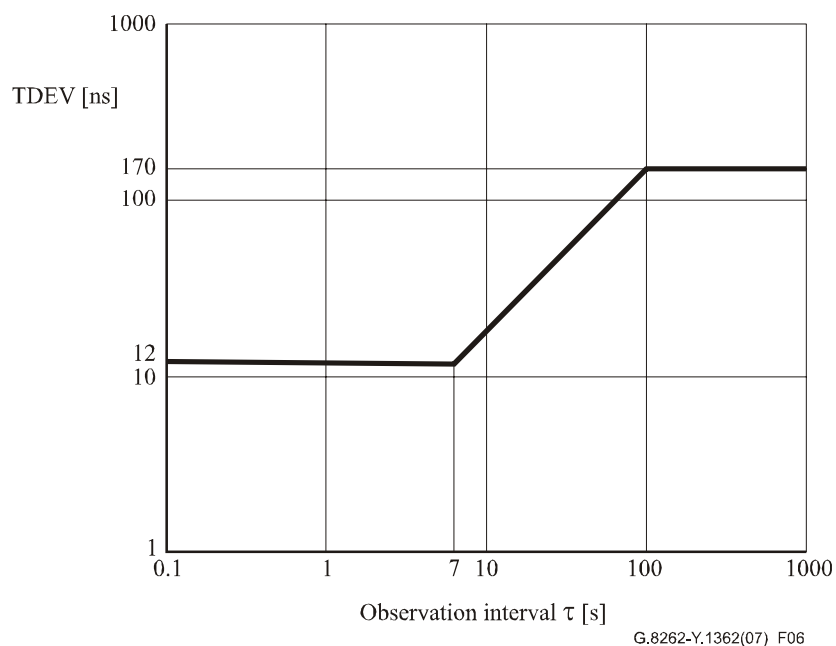
Figure 6 – Input wander tolerance (TDEV) for EEC-Option 1

While suitable test signals that check conformance to the mask in Figure 6 are being studied, test signals with a sinusoidal phase variation can be used, according to the levels in Table 8.

Table 8 – Lower limit of maximum tolerable sinusoidal input wander for Option 1

Peak-to-peak wander amplitude		Wander frequency				
A_1 [μs]	A_2 [μs]	f_4 [MHz]	f_3 [MHz]	f_2 [MHz]	f_1 [Hz]	f_0 [Hz]
0.25	2	0.32	0.8	16	0.13	10

The resultant requirements are shown in Figure 7.
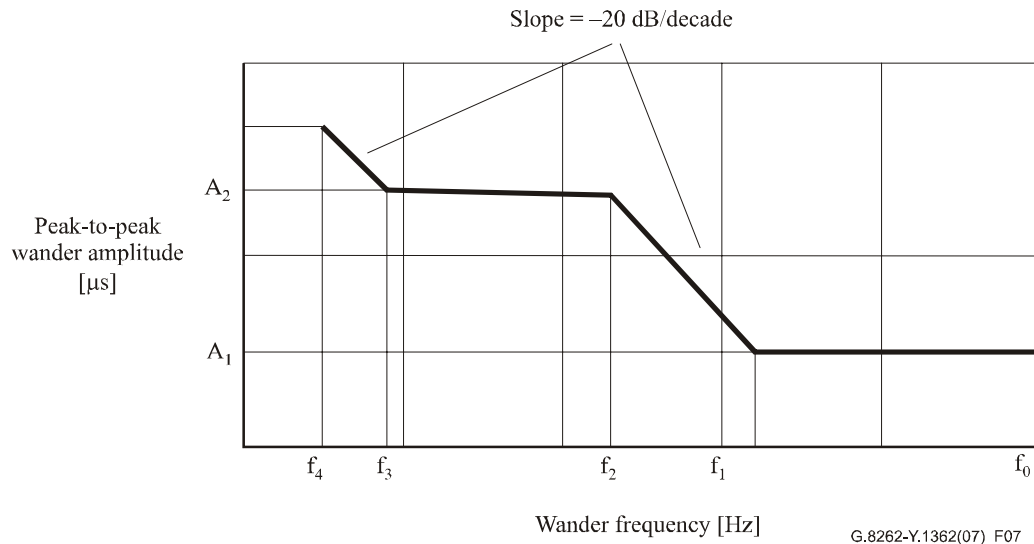
Figure 7 – Lower limit of max tolerable sinusoidal input wander for EEC-Option 1

9.1.2   EEC-Option 2

The EEC input wander tolerance expressed in TDEV is specified in Table 9.

Table 9 – Input wander tolerance (TDEV) for Option 2

TDEV limit [ns]	Observation interval τ [s]
17	$0.1 < \tau \le 3$
$5.77\,\tau$	$3 < \tau \le 30$
$31.6325\,\tau^{0.5}$	$30 < \tau \le 1000$

The resultant requirement is shown in Figure 8. A requirement expressed in MTIE is not defined.

Figure 8 – Input wander tolerance (TDEV) for Option 2

9.2 Jitter tolerance

9.2.1 EEC-Option 1

The lower limit of maximum tolerable input jitter for Ethernet interfaces for EEC-Option 1 is specified in [IEEE 802.3].

The lower limit of maximum tolerable input jitter for 2048-kHz and 2048-kbit/s signals is defined in clause 8.2, for Option 1 in [ITU-T G.813].

The lower limit of maximum tolerable input jitter for STM-N interfaces is defined in [ITU-T G.825].

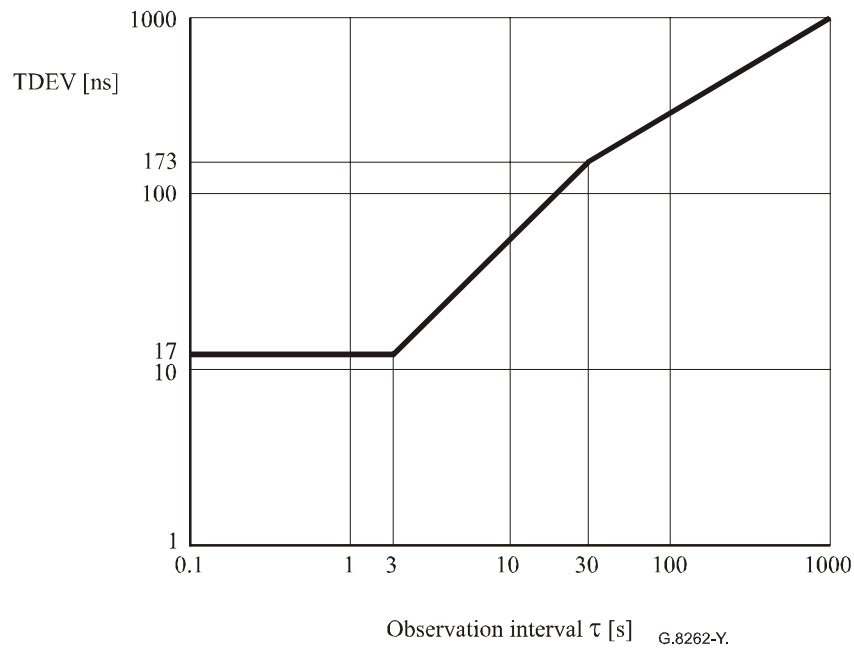NOTE – Measurement methodology for Ethernet is defined in [IEEE 802.3]. The applicability for the measurement in a synchronization network environment is for further study.

9.2.2 EEC-Option 2

The lower limit of maximum tolerable input jitter for Ethernet interfaces for EEC-Option 2 is specified in [IEEE 802.3].

The lower limit of maximum tolerable jitter for external 1544-kbit/s synchronization is defined in clause 8.2, for Option 2 in [ITU-T G.813].

The lower limit of maximum tolerable jitter for STM-N interfaces is defined in [ITU-T G.825].

NOTE – Measurement methodology for Ethernet is defined in [IEEE 802.3]. The applicability for the measurement in a synchronization network environment is for further study.

10 Noise transfer

The transfer characteristic of the EEC determines its properties with regard to the transfer of excursions of the input phase relative to the carrier phase. The EEC can be viewed as a low-pass filter for the differences between the actual input phase and the ideal input phase of the reference. The minimum and maximum allowed bandwidths for this low-pass filter behaviour are based on the considerations described in Appendix II of [ITU-T G.813] and are indicated below.

In the passband, the phase gain of the EEC should be smaller than 0.2 dB (2.3%). The above applies to a linear EEC model. However, this model should not restrict implementation.

10.1 EEC-Option 1

The minimum bandwidth requirement for an EEC is 1 Hz. The maximum bandwidth requirement for an EEC is 10 Hz.

10.2 EEC-Option 2

synchronous Ethernet or SDH NEs, when referenced to a synchronous Ethernet or a STM-N timing signal that meets the input TDEV mask in Figure 8 and Table 9, shall output signals that meet the output TDEV limits in Table 10.

Table 10 – Wander transfer for Option 2 (maximum output wander when input wander meets Table 9)

TDEV limit [ns]	Observation interval τ [s]
10	$0.1 < \tau \leq 1.7$
$5.77\,\tau$	$1.7 < \tau \leq 30$
$31.63\,\tau^{0.5}$	$30 < \tau \leq 1000$

The resultant requirement is shown in the mask of Figure 9. The purpose of these masks is to ensure that the maximum bandwidth of an EEC is 0.1 Hz. These masks should not be used to verify phase gain peaking. There is no requirement for a minimum bandwidth.

TDEV is measured through an equivalent 10-Hz, first-order, low-pass measurement filter at a maximum sampling time τ_0 of 1/30 seconds. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\,\tau$).

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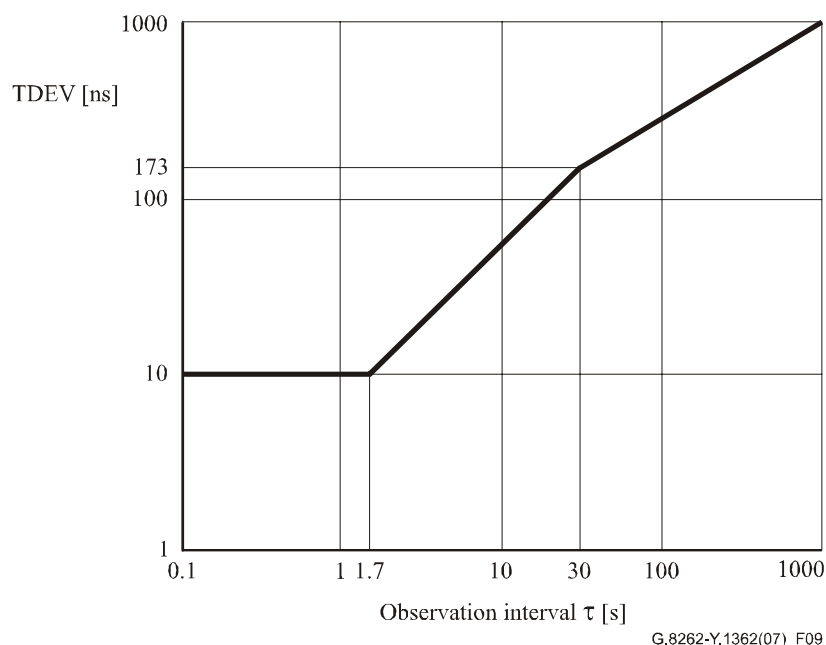
Figure 9 – Wander transfer for EEC-Option 2 (maximum output wander when input wander meets Figure 8)

11 Transient response and holdover performance

The requirements in this clause apply to situations where the input signal is affected by disturbances or transmission failures (e.g., short interruptions, switching between different synchronization signals, loss of reference, etc.) that result in phase transients at the EEC output (see clause 12). The ability to withstand disturbances is necessary to avoid transmission defects or failures. Transmission failures and disturbances are common stress conditions in the transmission environment.

It is recommended that all the phase movements at the output of the EEC stay within the level described in the following subclauses.

Measurements of MTIE for EEC-Option 2 clocks are measured through an equivalent 100-Hz, first-order, low-pass measurement filter.

11.1 Short-term phase transient response

11.1.1 EEC-Option 1

This requirement reflects the performance of the clock in cases when the (selected) input reference is lost due to a failure in the reference path and a second reference input signal, traceable to the same reference clock, is available simultaneously, or shortly after the detection of the failure (e.g., in cases of autonomous restoration). In such cases the reference is lost for at most 15 s. The output phase variation, relative to the input reference before it was lost, is bounded by the following requirements:

The phase error should not exceed $\Delta t + 5 \times 10^{-8} \times S$ seconds over any period S up to 15 seconds. Δt represents two phase jumps that may occur during the transition into and out of the holdover state which both should not exceed 120 ns with a temporary frequency offset of no more than 7.5 ppm.

The resultant overall requirement is summarized in Figure 10. This figure is intended to depict the worst-case phase movement attributable to an EEC reference clock switch. Clocks may change state more quickly than is shown here. Background information on the requirements that drove this requirement is provided in Appendix II of [ITU-T G.813].
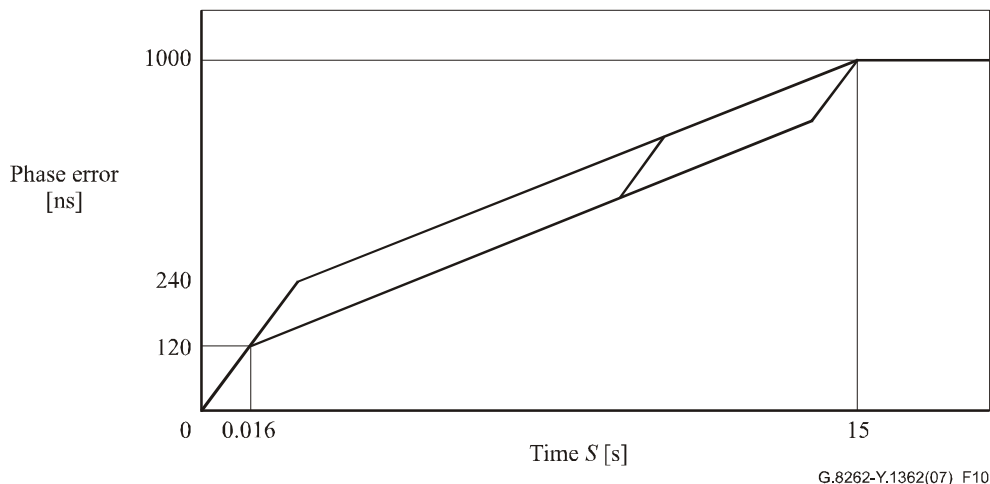
Figure 10 – Maximum phase transient at the output due to reference switching for EEC-Option 1

Figure 10 shows two phase jumps in the clock switching transient. The first jump reflects the initial response to a loss of the synchronization reference source and subsequent entry into holdover. The magnitude of this jump corresponds to a frequency offset less than 7.5 ppm for a duration less than 16 ms. After 16 ms, the phase movement is restricted to lie underneath the line with a slope of

5×10^{-8} in order to constrain pointer activity. The second jump, which is to take place within 15 s after entering holdover, accounts for the switching to the secondary reference. The same requirements are applicable for this jump. After the second jump, the phase error should remain constant and smaller than 1 µs.

NOTE – The output phase excursion, when switching between references which are not traceable to the same PRC, is for further study.

In cases where the input synchronization signal is lost for more than 15 s, the requirements in clause 11.2 apply.

11.1.2 EEC-Option 2

During clock rearrangement operations (e.g., reference switching), the output of the clock should meet the MTIE requirement as defined in clause 11.4.2.

11.2 Long-term phase transient response (Holdover)

This requirement bounds the maximum excursions in the output timing signal. Additionally, it restricts the accumulation of the phase movement during input signal impairments or internal disturbances.

11.2.1 EEC-Option 1

When an EEC loses all its references, it is said to enter the holdover state. The Phase Error, ΔT, at the output of the EEC relative to the input at the moment of loss of reference should not, over any period of $S > 15$ s, exceed the following limit:

$$\Delta T(S) = \left\{ (a_1 + a_2)S + 0.5bS^2 + c \right\} \qquad [ns]$$

where:

$\qquad a_1 = $ 50 ns/s (see Note 1)

$\qquad a_2 = $ 2000 ns/s (see Note 2)

$\qquad b = $ 1.16×10^{-4} ns/s^2 (see Note 3)

$\qquad c = $ 120 ns (see Note 4)

This limit is subject to a maximum frequency offset of ±4.6 ppm. The behaviour for $S < 15$ s is defined in clause 11.1.

NOTE 1 – The frequency offset a_1 represents an initial frequency offset corresponding to 5×10^{-8} (0.05 ppm).

NOTE 2 – The frequency offset a_2 accounts for temperature variations after the clock went into holdover and corresponds to 2×10^{-6} (2 ppm). If there are no temperature variations, the term a_2S should not contribute to the phase error.

NOTE 3 – The drift b is caused by ageing: 1.16×10^{-4} ns/s^2 corresponds to a frequency drift of 1×10^{-8}/day (0.01 ppm/day). This value is derived from typical ageing characteristics after 10 days of continuous operation. It is not intended to measure this value on a per day basis, as the temperature effect will dominate.

NOTE 4 – The phase offset c takes care of any additional phase shift that may arise during the transition at the entry of the holdover state.

The resultant overall requirement for constant temperature (i.e., when the temperature effect is negligible) is summarized in Figure 11.

$$\Delta T(S) = \left(a_1 S + \frac{b}{2} S^2 + c \right) \qquad [ns]$$
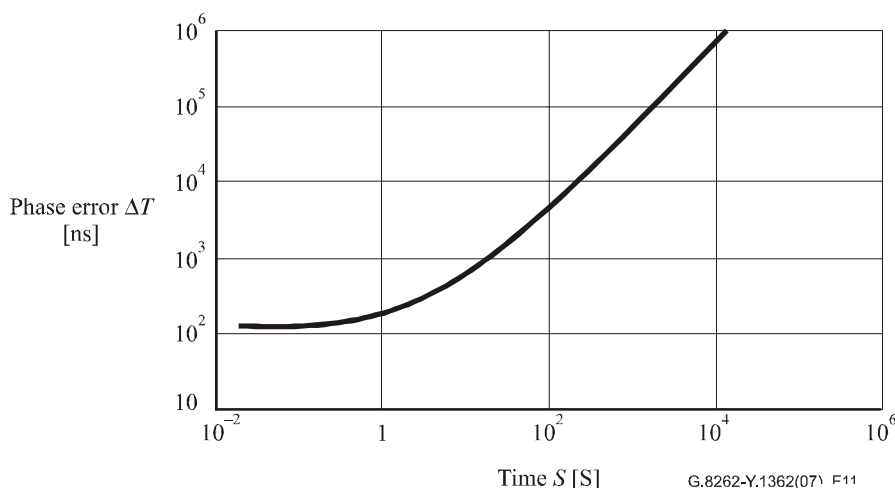
**Figure 11 – Permissible phase error for an EEC-Option 1
under holdover operation at constant temperature**

11.2.2 EEC-Option 2

When an EEC clock loses all its references, it enters the holdover state. The phase error, Δx, at the output of the slave clock from the moment of loss of reference, should, over any period of S seconds, meet the following:

$$\left|\Delta x(S)\right| \leq \left\{(a_1 + a_2)S + 0.5bS^2 + c\right\} \qquad [\text{ns}]$$

The derivative of $\Delta x(S)$, the fractional frequency offset, should, over any period of S seconds, meet the following:

$$\left|d(\Delta x(S))/dS\right| \leq \left\{a_1 + a_2 + bS\right\} \qquad [\text{ns/s}]$$

The second derivative of $\Delta x(S)$, the fractional frequency drift, should, over any period of S seconds, meet the following:

$$\left|d^2(\Delta x(S))/dS^2\right| \leq d \qquad \left[\text{ns/s}^2\right]$$

In applying the above requirements for the derivative of $\Delta x(S)$ and the second derivative of $\Delta x(S)$, the period S must begin after any transient associated with entry into holdover is over. During this transient period, the transient requirements of clause 11.4.2 apply.

NOTE 1 – a_1 represents an initial frequency offset under constant temperature conditions (±1 K).

NOTE 2 – a_2 accounts for temperature variations after the clock went into holdover. If there are no temperature variations, the term $a_2 S$ should not contribute to the phase error.

NOTE 3 – b represents the average frequency drift caused by aging. This value is derived from typical aging characteristics after 60 days of continuous operation. It is not intended to measure this value on a per day basis, as the temperature effect will dominate.

NOTE 4 – The phase offset c takes care of any additional phase shift that may arise during the transition at the entry of the holdover state.

NOTE 5 – d represents the maximum temporary frequency drift rate at constant temperature allowed during holdover. However, it is not required that d and b be equal.

The permissible phase error specifications for EEC-Option 2 is shown in Table 11.

Table 11 – Transient response specification during holdover

Applies for	EEC-Option 2 $S >$ TBD
a_1 (ns/s)	50
a_2 (ns/s)	300
b (ns/s^2)	4.63×10^{-4}
c (ns)	1000
d (ns/s^2)	4.63×10^{-4}
TBD To be defined	

11.3 Phase response to input signal interruptions

11.3.1 EEC-Option 1

For short-term interruptions on synchronization input signals that do not cause reference switching, the output phase variation should not exceed 120 ns, with a maximum frequency offset of 7.5 ppm for a maximum period of 16 ms.

11.3.2 EEC-Option 2

This is for further study.

11.4 Phase discontinuity

11.4.1 EEC-Option 1

In cases of infrequent internal testing or other internal disturbances (but excluding major hardware failures, e.g., those that would give rise to clock equipment protection switches) within the synchronous Ethernet equipment clock, the following conditions should be met:

–   The phase variation over any period S (ms) up to 16 ms should not exceed 7.5 S ns;

–   The phase variation over any period S (ms) from 16 ms up to 2.4 s should not exceed 120 ns;

–   For periods greater than 2.4 s, the phase variation for each interval of 2.4 s should not exceed 120 ns with a temporary offset of no more than 7.5 ppm up to a total amount of 1μs.

11.4.2 EEC-Option 2

In cases of infrequent internal testing or rearrangement operations within the slave clock, the phase transient at the output of EEC-Option 2 should meet the MTIE specifications as specified in Table 12.

Table 12 – MTIE at the output due to reference switching/ rearrangement operations for Option 2

MTIE limit [ns]	Observation interval τ [s]
Not specified	$\tau \le 0.014$
$(7.6 + 885\, \tau)$	$0.014 < \tau \le 0.5$
$(300 + 300\, \tau)$	$0.5 < \tau \le 2.33$
1000	$2.33 < \tau$

This MTIE requirement is illustrated in Figure 12.
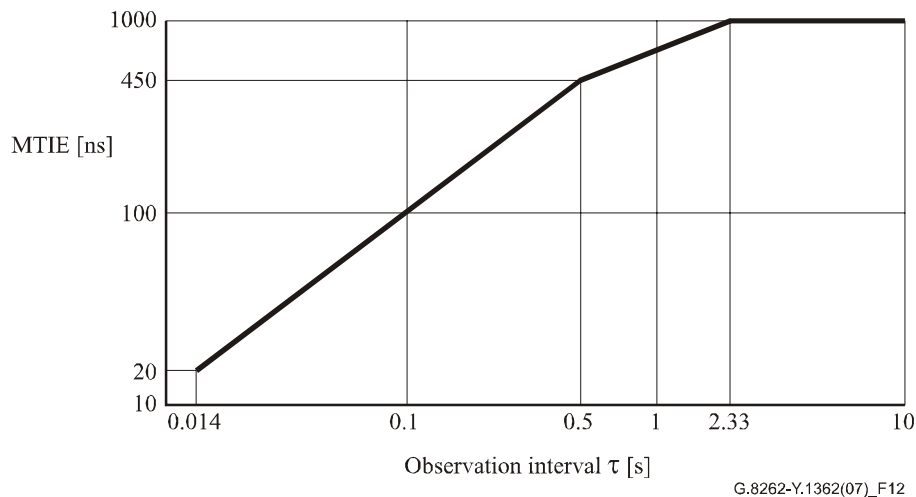
**Figure 12 – MTIE at the output due to reference switching/
rearrangement operations for Option 2**

12   Interfaces

The requirements in this Recommendation are related to reference points internal to the network elements (NEs) in which the clock is embedded and are, therefore, not necessarily available for measurement or analysis by the user. Therefore, the performance of the EEC is not defined at these internal reference points, but rather at the external interfaces of the equipment.

The synchronization input and output interfaces for Ethernet equipment in which the EEC may be contained are:

–   1544-kbit/s interfaces according to [ITU-T G.703];

–   2048-kHz external interfaces according to [ITU-T G.703];

–   2048-kbit/s interfaces according to [ITU-T G.703];

–   STM-N traffic interfaces (for hybrid NEs);

–   64-kHz interface according to [ITU-T G.703];

–   6312-kHz external interfaces according to [ITU-T G.703];

–   synchronous Ethernet interfaces.

All of the above interfaces may not be implemented on all equipment. These interfaces should comply with the jitter and wander requirements as defined in this Recommendation.

NOTE – To support interoperability with existing network equipment, interfaces to and from external network clocks may optionally support SSM.

12.1   External synchronization interfaces

Synchronization Ethernet equipment will require a range of interface types to be supported that will allow synchronization to be derived from an [ITU-T G.812] SSU/BITS clock, the output from an [ITU-T G.813] SEC or from another synchronous Ethernet equipment as specified in this Recommendation.

The primary objectives are:

–   to provide an easy migration path from existing synchronization distribution architectures based on SDH transmission to future synchronization architectures based on carrier scale Ethernet transport with an embedded EEC;

–   to ensure that synchronization (frequency) is transported at the physical layer where it is not subject to load impairments.

Table 13 shows the external interface type.

Table 13 – External interface type

External interface type	Supports
[ITU-T G.703]-based 2.048 MHz/2.048 Mbit/s 1.544 MHz/1.544 Mbit/s	Legacy/Initial architecture support for frequency NOTE – Allows transition from legacy architecture based on SDH to carrier scale initial synchronous Ethernet architecture reusing existing SSU functionality.
Synchronous Ethernet (rate TBD)	Initial requirement for frequency

Other external interface types are for further study.

NOTE – Synchronous Ethernet support for time transfer (i.e., both frequency and time) is for further study.

Annex A

Reference source selection mechanism

(This annex forms an integral part of this Recommendation)

Synchronous Ethernet equipment will require a reference source selection mechanism to provide traceability to upstream elements and ultimately the PRC with respect to frequency.

A.1 Requirements

The selection mechanism controls the physical timing flows within the equipment.

The selection mechanism must be able to select:

– an appropriate external reference source (see clause 12);
– an appropriate traffic reference source (see clause 12);
– internal clock (i.e., local oscillator).

A reference derived from an Ethernet traffic source that is not synchronous Ethernet shall not be selected.

A.2 Inputs

The node synchronization source can be:

– an external input reference;
– a recovered clock reference from the line.

A.3 Internal oscillator

This provides filtering and holdover.

A.4 Internal physical timing flows – Frequency ETY

A number of internal physical timing flows will be required to synchronize the ETY layer (Ethernet PHY).

A.5 Selection mechanism

Synchronous Ethernet equipment shall support a selection mechanism that allows synchronization to be derived from line, i.e., traffic carrying interfaces, from external synchronization interfaces, i.e., provided by co-located equipment or internally from the EEC. These will be supported by the SSM message set. Figure A.1 shows a high-level representation of synchronization sub-system selection mechanism for synchronous Ethernet equipment.
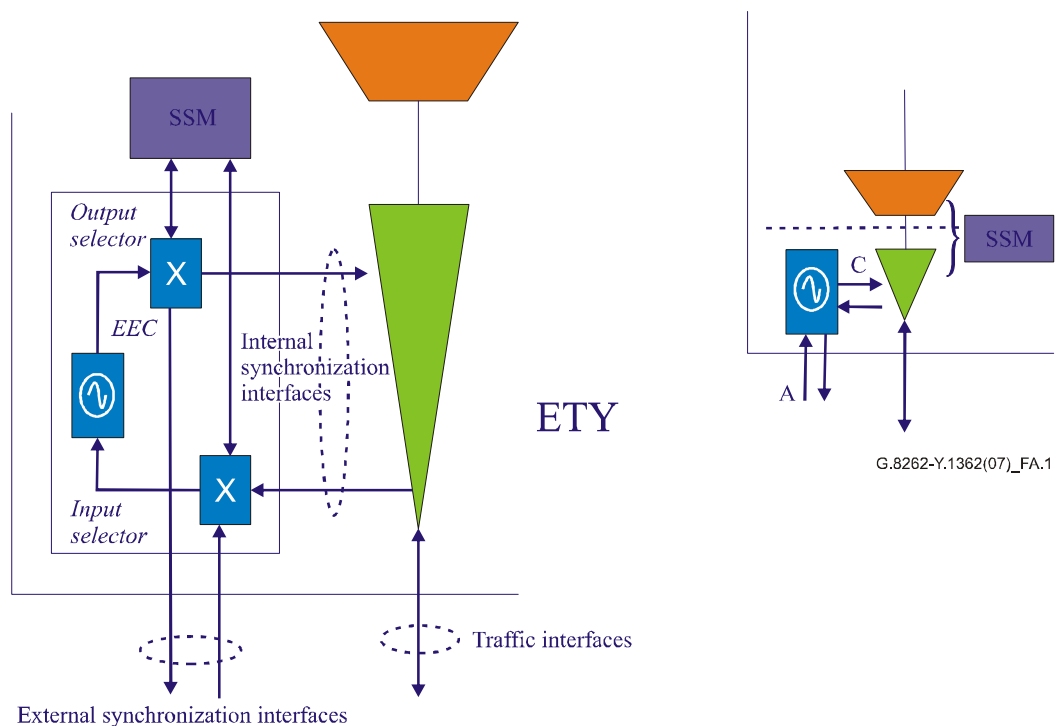
Figure A.1 – Synchronous Ethernet equipment – High-level representation of synchronization sub-system selection mechanism

The EEC within the internal synchronization sub-system shall comply with this Recommendation.

The synchronous Ethernet equipment shall have the ability to recover synchronization from the synchronization inputs either traffic interfaces via the "internal synchronization interfaces" and/or "external synchronization interfaces". These will be injected into an internal synchronization sub-system.

The internal synchronization sub-system shall provide the necessary filtering and holdover performance and shall perform any synchronization messaging functionality.

The internal synchronization sub-system shall be able to select an alternate synchronization source through the use of priority tables and synchronization status messaging (SSM).

The internal synchronization sub-system shall make use of the SSM to determine priority and clock traceability.

The internal synchronization sub-system shall provide clocks of the appropriate rates (internal synchronization interfaces) to lock the Ethernet PHY (ETY) of the traffic interface.

A.6 Synchronization status message selection

Synchronization status messaging is required to allow the downstream element that requires synchronization to know the quality of the upstream clock.

The synchronization message shall be "pushed" from device to device that supports synchronous Ethernet. At each device that supports synchronous Ethernet, the message shall be processed and acted upon. The message set shall then be remade and passed to the next downstream element.

The synchronization sub-system shall be able to select an alternate source based on priority and SSM.

The transport channel for SSM is for further study.

A.7 Hybrid equipment selection function

Figure A.2 (SDH/Synchronous Ethernet "SETS" function) shows the equivalent selection mechanism of an SDH SETS function that has been adapted to hybrid SDH/Synchronous Ethernet equipment having Ethernet and SDH interfaces. *ETY & STM-N* input (TE and T1) and output (T0) represent the various Ethernet traffic interfaces (100BASE-TX, 1000BASE-SX, etc.) and SDH traffic interfaces. The SETG has characteristics defined in this Recommendation for synchronous Ethernet and in [ITU-T G.813]/[ITU-T G.812] for SDH. Also, note that in North American networks, the use of the T4 interface is to provide network timing to a BITS/SSU only. Selection of line interfaces (e.g., TE or T1 in Figure A.2) is only provided via selector A. Selector C can only select the output from Selector A. T4 is not filtered by the SETG, as any filtering is done by the BITS/SSU.

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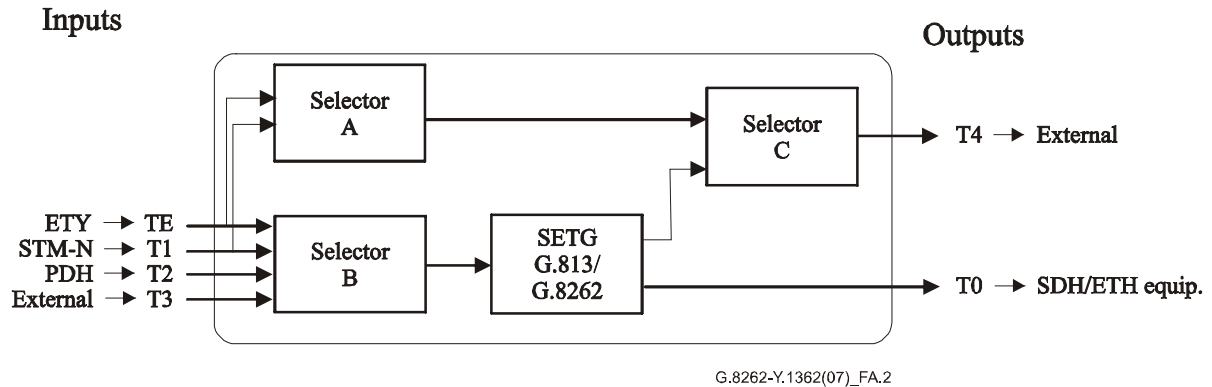
Figure A.2 – Hybrid SDH/synchronous Ethernet "SETS" function

Appendix I

Network applications and requirements for clocks
specified in ITU-T G.8262/Y.1362

(This appendix does not form an integral part of this Recommendation)

A current synchronization network uses of PRC(s), SSUs and SECs. The SSUs are often stand-alone equipment. The timing information is transferred via SDH NEs (SEC) from a PRC to an SSU or from an SSU to an SSU of a lower hierarchical level. Two or more routes are used for resilience. This is illustrated in Figure I.1a.

With the introduction of packet-switched NEs in the transport network, SDH NEs may be replaced by packet-switched NEs. In cases where the replaced SDH NEs were used in a synchronization chain, it is important that the new packet-switched NEs take over the timing transfer function without any modifications of the SSUs or the PRC. Figure I.1b shows two synchronization chains, one formed by SDH NE (circles with "S") and the other formed by packet-switched NEs using Ethernet interfaces (circles with E).

Hybrid NEs that offer both STM-N interfaces with associated SDH-VC cross-connect functions and Ethernet interfaces (ETY) with associated packet switching. Figure I.2 illustrates a hybrid NE and timing relations between the equipment clock (EC) and STM-N and ETY interfaces. It should be possible to use such hybrid NEs at any place in synchronization chains. An example is illustrated in Figure I.1c. The upper hybrid NE (circle with H) uses an STM-N interface at the ingress and an ETY interface at the egress. The lower hybrid NE uses an ETY interface at the ingress and an STM-N interface at the egress. Timing is transferred from STM-N to ETY and from ETY to STM-N, respectively.
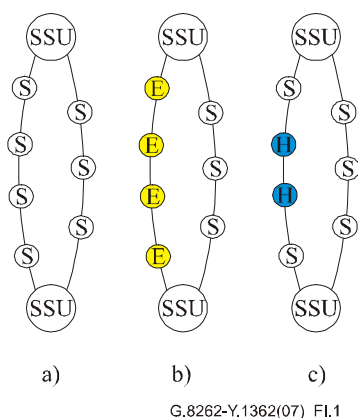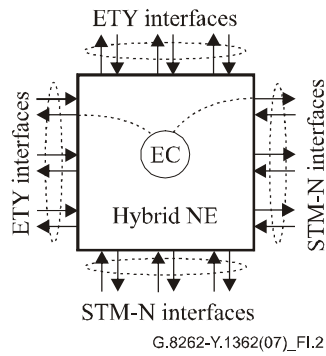

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Figure I.1 – Synchronization chains implemented with different types of NEs

G.8262-Y.1362(07)_FI.2

Figure I.2 – Hybrid NE using STM-N and Ethernet (ETY) interfaces

The clock characteristics of EECs may support the construction of timing distribution chains providing the same behaviour as chains of SECs (see Figure I.1b).

The EEC clocks may support the use of hybrid NEs at any place in a synchronization chain. Timing transfer may be supported from any type of input interface to any type of output interface as shown in Table I.1.

The use of ETY interfaces for timing distribution and the use of hybrid NEs should not require modifications of deployed SDH NEs or clocks (PRC, SSU), e.g., no new SSM code point for STM-N interfaces. Code point "0000" should also not be used.

Table I.1 – Combination of input and output ports for timing distribution

Timing input	Timing output
STM-N	STM-N
STM-N	ETY
STM-N	T4
ETY	STM-N
ETY	ETY
ETY	T4
T3	STM-N
T3	ETY

Appendix II

Relationship between requirements contained in this Recommendation and other key synchronization related Recommendations

(This appendix does not form an integral part of this Recommendation)

This appendix describes the relationship between the clock performance requirements contained within the body of this Recommendation and the key synchronization Recommendations that are under development, or have been developed within Question 13 (Network synchronization and time distribution performance) of ITU-T Study Group 15.

This Recommendation describes performance requirements for synchronous Ethernet clocks. The basic concept of synchronous Ethernet is described in [ITU-T G.8261], the first ITU-T Recommendation to detail network synchronization aspects applicable to packet-based networks.

The clocks described in this Recommendation, if embedded into Ethernet network elements, allow transfer of network traceable timing via the Ethernet physical layer. In this context, the Ethernet physical layer is defined by [IEEE 802.3].

The performance requirements in this Recommendation are derived from existing Recommendations. The EEC-Option 1 requirements are based on the [ITU-T G.813] Option 1 clock and the EEC-Option 2 is based on the Type IV clock from [ITU-T G.812], as deployed in an SDH NE.

Both EEC clocks offer similar performance, but are intended for use in networks optimized to either the 2-Mbit/s hierarchy (for Option 1) or to the 1544-kbit/s hierarchy (for Option 2). As the EEC clocks are consistent with existing SDH network element clocks used in the distribution of frequency, synchronization network engineering will not require any change to current network engineering practices.

Synchronization networks in general are based on SDH synchronization distribution as described in [ITU-T G.803]. Synchronization distribution may follow specific regional practices in order to meet the fundamental performance requirements and network interface limits from either [ITU-T G.823] or [ITU-T G.824] for the 2048-kbit/s or 1544-kbit/s hierarchy, respectively. Both [ITU-T G.823] and [ITU-T G.824] are traceable to the fundamental slip rate objectives in [ITU-T G.822].

The EEC clocks are purposely specified to perform in a manner consistent with existing synchronization networks. The Option-1 EEC can be deployed within the synchronization distribution network in exactly the same manner as a [ITU-T G.813] SEC, while the Option-2 EEC can be deployed as per existing [ITU-T G.812] Type IV clocks.

It is important to note that while the requirements in this Recommendation define the performance of synchronous Ethernet equipment clocks, additional work is ongoing to develop additional Recommendations to describe additional network element functionality necessary to completely integrate EEC clocks within existing SDH-based synchronization networks.

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