International Telecommunication Union

ITU-T G.8262/Y.1362

(07/2010)

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Timing characteristics of a synchronous Ethernet equipment slave clock

Recommendation ITU-T G.8262/Y.1362

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Recommendation ITU-T G.8262/Y.1362

Timing characteristics of a synchronous Ethernet equipment slave clock

Summary

Recommendation ITU-T G.8262/Y.1362 outlines requirements for timing devices used in synchronizing network equipment that uses synchronous Ethernet. This Recommendation defines the requirements for clocks, e.g., bandwidth, frequency accuracy, holdover and noise generation.

History

Edition	Recommendation	Approval	Study Group
1.0	ITU-T G.8262/Y.1362	2007-08-13	15
1.1	ITU-T G.8262/Y.1362 (2007) Amend. 1	2008-04-29	15
1.2	ITU-T G.8262/Y.1362 (2007) Amend.2	2010-01-13	15
2.0	ITU-T G.8262/Y.1362	2010-07-29	15

Keywords

Clock, jitter, synchronization, wander.

FOREWORD

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The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSA Resolution 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

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CONTENTS

Introduction

The synchronous Ethernet method refers to the primary reference clock (PRC) distributed method (for instance, based on the global navigation satellite system (GNSS)), or the master-slave method using a synchronous physical layer (e.g., ETY, STM-N). These methods are widely implemented to synchronize the TDM networks.

Recommendation ITU-T G.8262/Y.1362

Timing characteristics of a synchronous Ethernet equipment slave clock

1 Scope

This Recommendation outlines minimum requirements for timing devices used in synchronizing network equipment that supports synchronous Ethernet. It supports clock distribution based on network-synchronous line-code methods (e.g., synchronous Ethernet).

This Recommendation allows for proper network operation when an EEC (Option 1 or 2) is timed from another network equipment clock or a higher-quality clock.

Included in this Recommendation are requirements for clock accuracy, noise transfer, holdover performance, noise tolerance, and noise generation. These requirements apply under the normal environmental conditions specified for the equipment.

This Recommendation contains two options for synchronous Ethernet. The first option, referred to as "EEC-Option 1", applies to synchronous Ethernet equipments that are designed to interwork with networks optimized for the 2048-kbit/s hierarchy. These networks allow the worst-case synchronization reference chain as specified in Figure 8-5 of [ITU-T G.803]. The second option, referred to as "EEC-Option 2", applies to synchronous Ethernet equipments that are designed to interwork with networks optimized for the 1544-kbit/s hierarchy. The synchronization reference chain for these networks is defined in clause II.3 of [ITU-T G.813].

A synchronous Ethernet equipment slave clock should comply with all of the requirements specific to one option and should not mix requirements between EEC-Options 1 and 2. In the clauses where one requirement is specified, the requirements are common to both options. It is the intention that EEC-Options 1 and 2 should be harmonized in the future. The intent of the synchronous Ethernet is to interoperate with existing synchronization networks based on [ITU-T G.813].

Careful consideration should be taken when interworking between networks with synchronous Ethernet based on EEC-Option 1 and networks with synchronous Ethernet based on EEC-Option 2.

Some synchronous Ethernet NEs may have a higher-quality clock. This Recommendation allows for proper network operation when a synchronous Ethernet equipment (EEC-Option 1 or 2) is timed from either another synchronous Ethernet equipment (like option), or from a SEC, or a higher-quality clock. Hierarchical timing distribution is recommended for synchronous Ethernet networks. Timing should not be passed from a synchronous Ethernet in free-run/holdover mode to a higher-quality clock since the higher-quality clock should not follow the synchronous Ethernet signal during fault conditions.

Certain Ethernet equipments such as regenerators/repeaters must provide through-timing capability to transmit timing via synchronous Ethernet. These equipments are for further study.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T G.703] Recommendation ITU-T G.703 (2001), *Physical/electrical characteristics of hierarchical digital interfaces*.

[ITU-T G.781] Recommendation ITU-T G.781 (1999), *Synchronization layer functions*.

[ITU-T G.783] Recommendation ITU-T G.783 (2006), *Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks*.

[ITU-T G.801] Recommendation ITU-T G.801 (1988), *Digital transmission models*.

[ITU-T G.803] Recommendation ITU-T G.803 (2000), *Architecture of transport networks based on the synchronous digital hierarchy (SDH)*.

[ITU-T G.810] Recommendation ITU-T G.810 (1996), *Definitions and terminology for synchronization networks*.

[ITU-T G.811] Recommendation ITU-T G.811 (1997), *Timing characteristics of primary reference clocks*.

[ITU-T G.812] Recommendation ITU-T G.812 (2004), *Timing requirements of slave clocks suitable for use as node clocks in synchronization networks*.

[ITU-T G.813] Recommendation ITU-T G.813 (2003), *Timing characteristics of SDH equipment slave clocks (SEC)*.

[ITU-T G.822] Recommendation ITU-T G.822 (1988), *Controlled slip rate objectives on an international digital connection*.

[ITU-T G.823] Recommendation ITU-T G.823 (2000), *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy*.

[ITU-T G.824] Recommendation ITU-T G.824 (2000), *The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy*.

[ITU-T G.825] Recommendation ITU-T G.825 (2000), *The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH)*.

[ITU-T G.8010] Recommendation ITU-T G.8010/Y.1306 (2004), *Architecture of Ethernet layer networks*.

[ITU-T G.8261] Recommendation ITU-T G.8261/Y.1361 (2008), *Timing and synchronization aspects in packet networks*.

[ITU-T G.8264] Recommendation ITU-T G.8264/Y.1364 (2008), *Timing distribution through packet networks.*

[ITU-T Q.551] Recommendation ITU-T Q.551 (2002), *Transmission characteristics of digital exchanges*.

[IEEE 802.3] IEEE Standard 802.3-2008, *Information technology – Telecommunications and information exchange between systems – Local and metropolitan area networks – Specific requirements Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications.*

3 Definitions

The terms and definitions used in this Recommendation are contained in [ITU-T G.810].

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

EEC synchronous Ethernet Equipment Clock

ETH Ethernet MAC layer network

ETY Ethernet PHY layer network

GNSS Global Navigation Satellite System

MTIE Maximum Time Interval Error

NE Network Element

OAM Operation, Administration and Maintenance

PRC Primary Reference Clock

SDH Synchronous Digital Hierarchy

SEC SDH Equipment Clock

SSU Synchronization Supply Unit

STM Synchronous Transport Module

TDEV Time Deviation

UI Unit Interval

UTC Coordinated Universal Time

5 Conventions

This clause is intentionally left blank.

6 Frequency accuracy

6.1 EEC-Option 1

Under free-running conditions, the EEC output frequency accuracy should not be greater than 4.6 ppm with regard to a reference traceable to a [ITU-T G.811] clock.

NOTE – The time interval for this accuracy is for further study. Values of 1 month and 1 year have been proposed.

6.2 EEC-Option 2

Under prolonged holdover conditions, the output frequency accuracy of the different types of node clocks should not exceed 4.6 ppm with regard to a reference traceable to a primary reference clock, over a time period T of 1 year.

NOTE – The time period T applies after 30 days of continuous synchronized operation.

7 Pull-in, hold-in, and pull-out ranges

7.1 Pull-in range

7.1.1 EEC-Option 1

The minimum pull-in range should be ±4.6 ppm, whatever the internal oscillator frequency offset may be.

7.1.2 EEC-Option 2

The minimum pull-in range should be ±4.6 ppm, whatever the internal oscillator frequency offset may be.

7.2 Hold-in range

7.2.1 EEC-Option 1

The hold-in range for EEC-Option 1 is not required.

7.2.2 EEC-Option 2

The hold-in range for EEC-Option 2 should be ±4.6 ppm, whatever the internal oscillator frequency offset may be.

7.3 Pull-out range

7.3.1 EEC-Option 1

The pull-out range is for further study. A minimum value of ±4.6 ppm has been proposed.

7.3.2 EEC-Option 2

The pull-out range is not applicable.

8 Noise generation

The noise generation of an EEC represents the amount of phase noise produced at the output when there is an ideal input reference signal or the clock is in holdover state. A suitable reference, for practical testing purposes, implies a performance level at least 10 times more stable than the output requirements. The ability of the clock to limit this noise is described by its frequency stability. The measures maximum time interval error (MTIE) and time deviation (TDEV) are useful for characterization of noise generation performance.

MTIE and TDEV are measured through an equivalent 10-Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 seconds. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\tau$).

8.1 Wander in locked mode

8.1.1 EEC-Option 1

When the EEC is in the locked mode of operation synchronized to a wander-free reference, the MTIE measured using the synchronized clock configuration defined in Figure 1a of [ITU-T G.810] should have the limits in Table 1, if the temperature is constant (within ±1°K):

Table 1 – Wander generation (MTIE) for EEC-Option 1 with constant temperature

MTIE limit [ns]	Observation interval τ [s]
40	$0.1 < \tau \leq 1$
$40\ \tau^{0.1}$	$1 < \tau \leq 100$
$25.25\ \tau^{0.2}$	$100 < \tau \leq 1000$

The resultant requirement is shown by the thick solid line in Figure 1.

When temperature effects are included, the allowance for the total MTIE contribution of a single EEC increases by the values in Table 2.

Table 2 – Additional wander generation (MTIE) for EEC-Option 1 with temperature effects

Additional MTIE allowance [ns]	Observation interval τ [s]
0.5 τ	$\tau \leq 100$
50	$\tau > 100$

The resultant requirements are shown by the thin solid line in Figure 1.

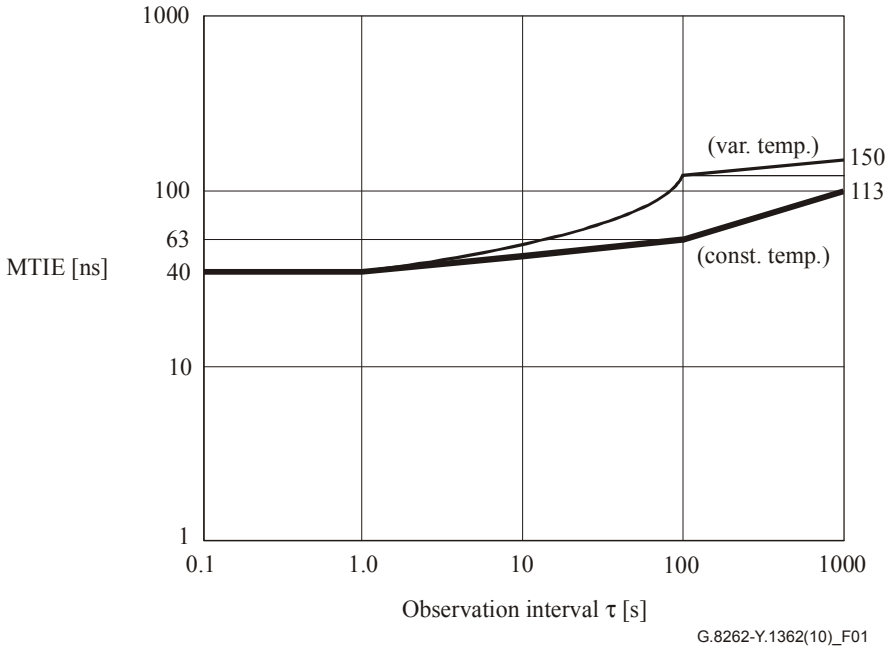

Figure 1 – Wander generation (MTIE) for EEC-Option 1

When the EEC is in the locked mode of operation, the TDEV measured using the synchronized clock configuration defined in Figure 1a of [ITU-T G.810] should have the limits in Table 3, if the temperature is constant (within ±1°K):

Table 3 – Wander generation (TDEV) for EEC-Option 1 with constant temperature

TDEV limit [ns]	Observation interval τ [s]
3.2	$0.1 < \tau \leq 25$
$0.64\ \tau^{0.5}$	$25 < \tau \leq 100$
6.4	$100 < \tau \leq 1000$

The resultant requirements are shown in Figure 2.

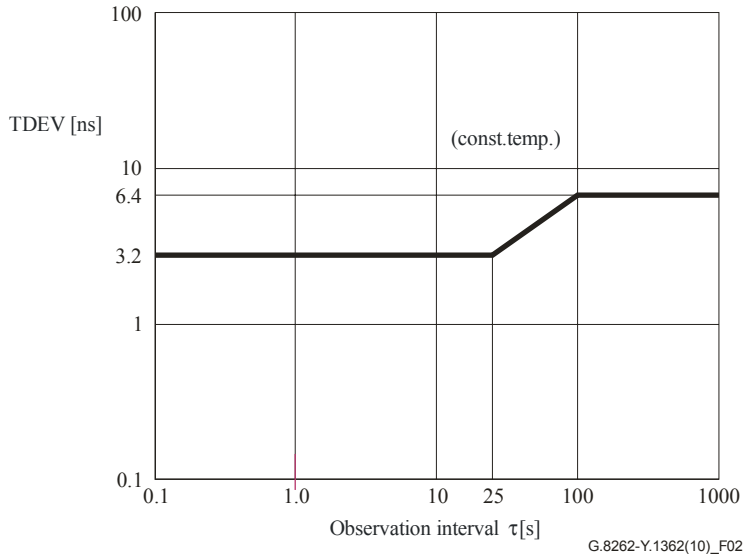

Figure 2 – Wander generation (TDEV) for EEC-Option 1 with constant temperature

The allowance for the total TDEV contribution of a single EEC when temperature effects are included is for further study.

8.1.2 EEC-Option 2

When the EEC clock is in the locked mode of operation synchronized to a wander-free reference, the MTIE and TDEV measured at the output under constant temperature (within ±1°K) shall be below the limits in Tables 4 and 5.

Table 4 – Wander generation (MTIE) for EEC-Option 2 with constant temperature

MTIE limit [ns]	Observation interval τ [s]
20	$0.1 < \tau \leq 1$
$20\ \tau^{0.48}$	$1 < \tau \leq 10$
60	$10 < \tau \leq 1000$

Table 5 – Wander generation (TDEV) for EEC-Option 2 with constant temperature

TDEV limit [ns]	Observation interval τ [s]
$3.2\ \tau^{-0.5}$	$0.1 < \tau \leq 2.5$
2	$2.5 < \tau \leq 40$
$0.32\ \tau^{0.5}$	$40 < \tau \leq 1000$
10	$1000 < \tau \leq 10\ 000$

The resultant requirements are shown in Figures 3 and 4.

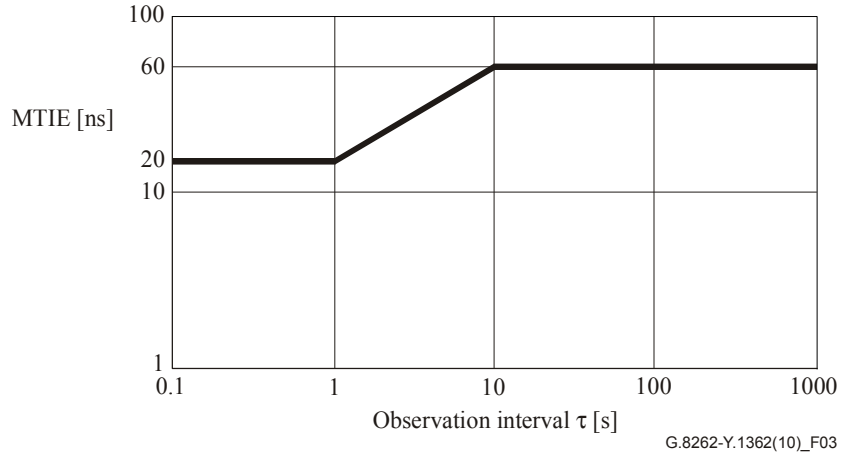

Figure 3 – Wander generation (MTIE) for EEC-Option 2 with constant temperature

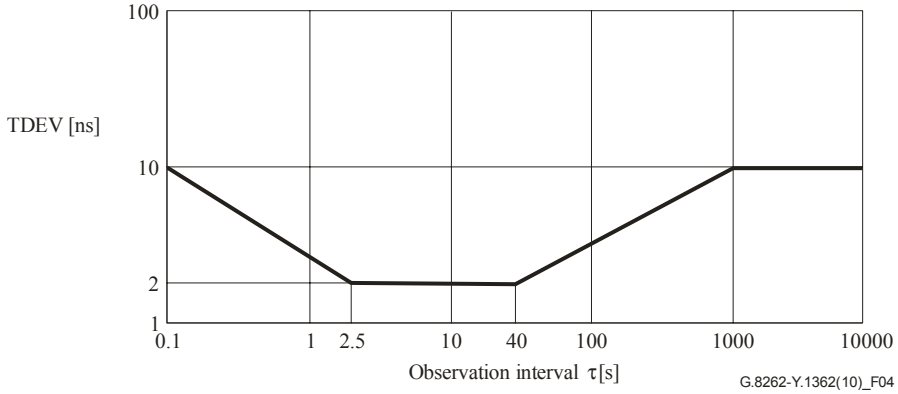

Figure 4 – Wander generation (TDEV) for EEC-Option 2 with constant temperature

8.2 Non-locked wander

When a clock is not locked to a synchronization reference, the random noise components are negligible compared to deterministic effects like initial frequency offset. Consequently, the non-locked wander effects are included in clause 11.2.

8.3 Jitter

While most requirements in this Recommendation are independent of the output interface at which they are measured, this is not the case for jitter production; jitter generation requirements utilize existing Recommendations that have different limits for different interface rates. These requirements are stated separately for the interfaces identified in clause 12.

8.3.1 EEC-Option 1 and EEC-Option 2

Output jitter at a synchronous Ethernet interface:

In the absence of input jitter at the synchronization interface, the intrinsic jitter at the synchronous Ethernet output interfaces, as measured over a 60-second interval, should not exceed the limits given in Table 6.

Table 6 – Synchronous Ethernet jitter generation for EEC-Option 1 and EEC-Option 2

Interface	Measuring filter	Peak-to-peak amplitude (UI)
1G (Notes 1, 2, 4)	2.5 kHz to 10 MHz	0.50
10G (Notes 1, 3, 4)	20 kHz to 80 MHz	0.50

NOTE 1 – There is no specific high-band jitter requirement for synchronous Ethernet. The relevant IEEE 802.3 jitter requirements shall be met in addition to the specific synchronous Ethernet wideband jitter requirements specified in this table. [IEEE 802.3] defines measurement methodologies. The applicability for those measurement methodologies in a synchronization network environment is for further study.

NOTE 2 – 1G includes 1000BASE-KX, -SX, -LX; multi-lane interfaces are for further study.

NOTE 3 – 10G includes 10GBASE-SR/LR/ER, 10GBASE-LRM, 10GBASE-SW/LW/EW; multi-lane interfaces are for further study.

NOTE 4 – 1G: 1 UI = 0.8 ns
10G (10GBASE-SR/LR/ER, -LRM): 1 UI = 96.97 ps
10G (10GBASE-SW/LW/EW): 1 UI = 100.47 ps

Output jitter at 2048 kHz, 2048 kbit/s, 1544 kbit/s and STM-N interfaces:

Jitter generation for the 2048 kHz and 2048 kbit/s interface, and for the STM-N interface are defined for Option 1 in clause 7.3 of [ITU-T G.813].

Jitter generation for the 1544-kbit/s interface and for the STM-N interfaces are defined for Option 2 in clause 7.3 of [ITU-T G.813].

9 Noise tolerance

The noise tolerance of an EEC indicates the minimum phase noise level at the input of the clock that should be accommodated whilst:

– maintaining the clock within prescribed performance limits. The exact performance limits are for further study;
– not causing any alarms;
– not causing the clock to switch reference;
– not causing the clock to go into holdover.

In general, the noise tolerance of the EEC is the same as the network limit for the synchronization interface in order to maintain acceptable performance. However, the synchronization interface network limit may be different according to the application. Therefore, in order to determine the EEC noise tolerance, the worst-case network limit should be used. An explanation of the different network limits is given in Appendix I of [ITU-T G.813], for information.

The wander and jitter tolerances given in clauses 9.1 and 9.2 represent the worst levels that a synchronization carrying interface should exhibit. The TDEV signal used for a conformance test should be generated by adding white, Gaussian noise sources, of which each has been filtered to obtain the proper type of noise process with the proper amplitude.

MTIE and TDEV are measured through an equivalent 10-Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 seconds. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\tau$).

9.1 Wander tolerance

9.1.1 EEC-Option 1

The input wander tolerance expressed in MTIE and TDEV limits is given in Tables 7 and 8.

Table 7 – Input wander tolerance (MTIE) for EEC-Option 1

MTIE limit [µs]	Observation interval τ [s]
0.25	$0.1 < \tau \leq 2.5$
0.1 τ	$2.5 < \tau \leq 20$
2	$20 < \tau \leq 400$
0.005 τ	$400 < \tau \leq 1000$

Table 8 – Input wander tolerance (TDEV) for EEC-Option 1

TDEV limit [ns]	Observation interval τ [s]
12	$0.1 < \tau \leq 7$
1.7 τ	$7 < \tau \leq 100$
170	$100 < \tau \leq 1000$

The resultant requirements are shown in Figures 5 and 6.

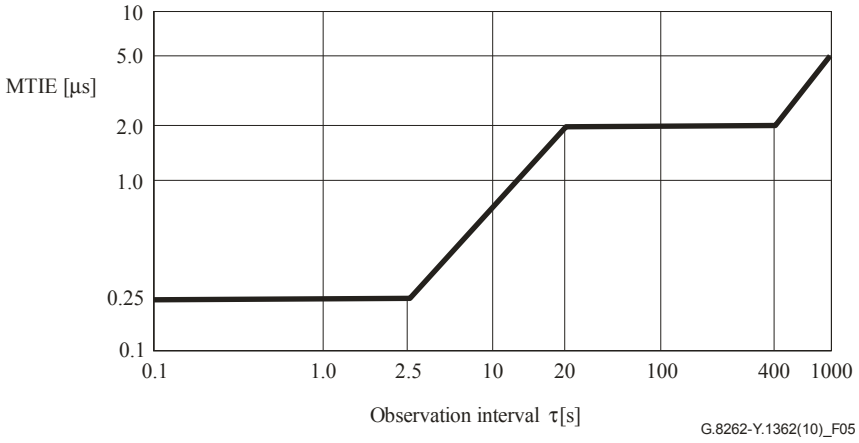

Figure 5 – Input wander tolerance (MTIE) for EEC-Option 1

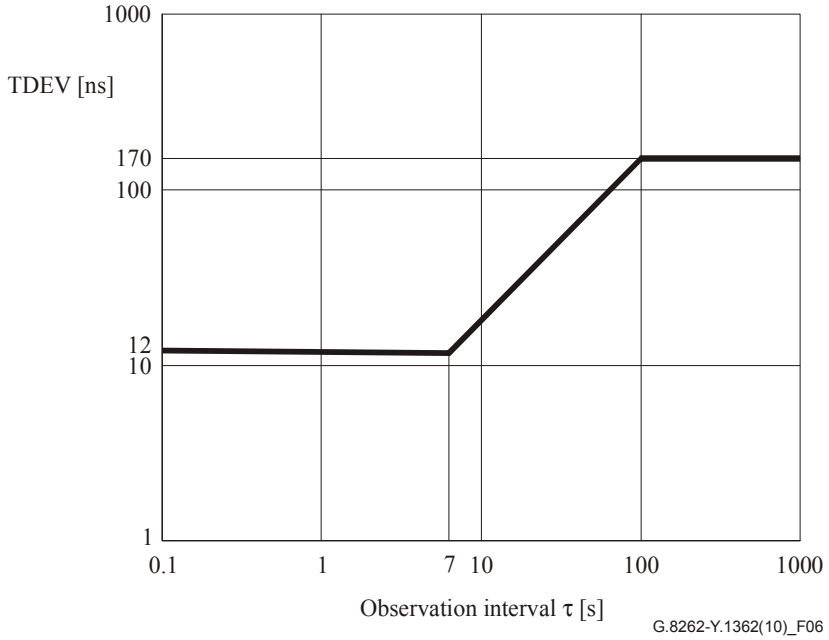

Figure 6 – Input wander tolerance (TDEV) for EEC-Option 1

Suitable test signals that check conformance to the mask in Figure 6 are being studied. Test signals with a sinusoidal phase variation can be used, according to the levels in Table 9, to check conformance to the mask in Figure 5.

Table 9 – Lower limit of maximum tolerable sinusoidal input wander for EEC-Option 1

Peak-to-peak wander amplitude			**Wander frequency**				
A_1 [µs]	A_2 [µs]	A_3 [µs]	f_4 [mHz]	f_3 [mHz]	f_2 [mHz]	f_1 [Hz]	f_0 [Hz]
0.25	2	5	0.32	0.8	16	0.13	10

The resultant requirements are shown in Figure 7.

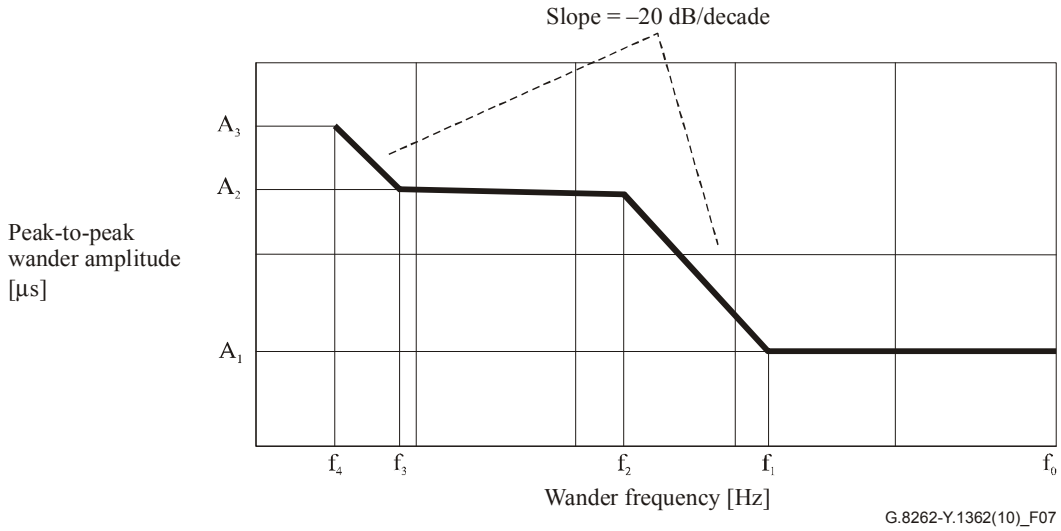

Figure 7 – Lower limit of maximum tolerable sinusoidal input wander for EEC-Option 1

9.1.2 EEC-Option 2

The EEC input wander tolerance expressed in TDEV is specified in Table 10.

Table 10 – Input wander tolerance (TDEV) for EEC-Option 2

TDEV limit [ns]	Observation interval τ [s]
17	$0.1 < \tau \leq 3$
$5.77\ \tau$	$3 < \tau \leq 30$
$31.6325\ \tau^{0.5}$	$30 < \tau \leq 1000$

The resultant requirement is shown in Figure 8. A requirement expressed in MTIE is not defined.

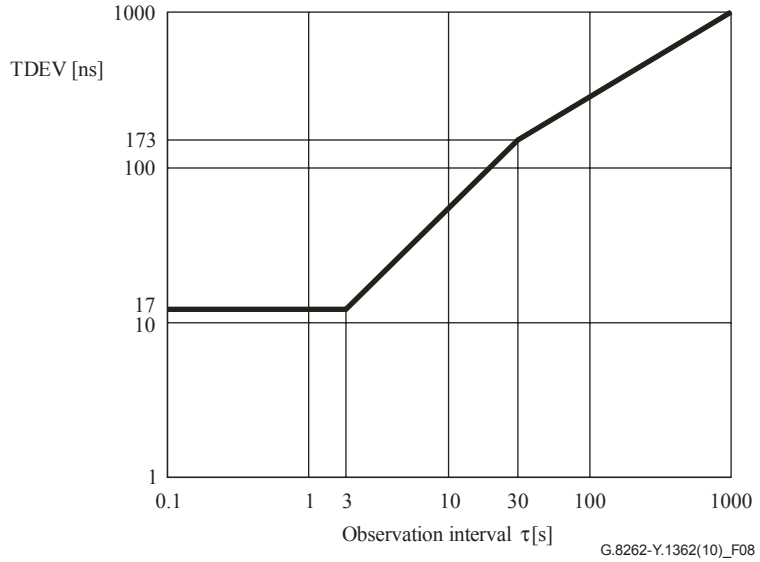

Figure 8 – Input wander tolerance (TDEV) for EEC-Option 2

9.2 Jitter tolerance

9.2.1 EEC-Option 1 and EEC-Option 2

Jitter tolerance at a synchronous Ethernet interface:

The lower limit of maximum tolerable input jitter for 1G Ethernet interfaces for EEC-Option 1 and EEC-Option 2 is given in Table 11 and Figure 9.

Table 11 – 1G synchronous Ethernet wideband jitter tolerance for EEC-Option 1 and EEC-Option 2

Peak-peak jitter amplitude (UI)	Frequency f (Hz)
312.5	$10 < f \leq 12.1$
$3750\ f^{-1}$	$12.1 < f \leq 2.5$ k
1.5	2.5 k $< f \leq 50$ k
NOTE – 1G includes 1000BASE-KX, -SX, -LX; multi-lane interfaces are for further study.	

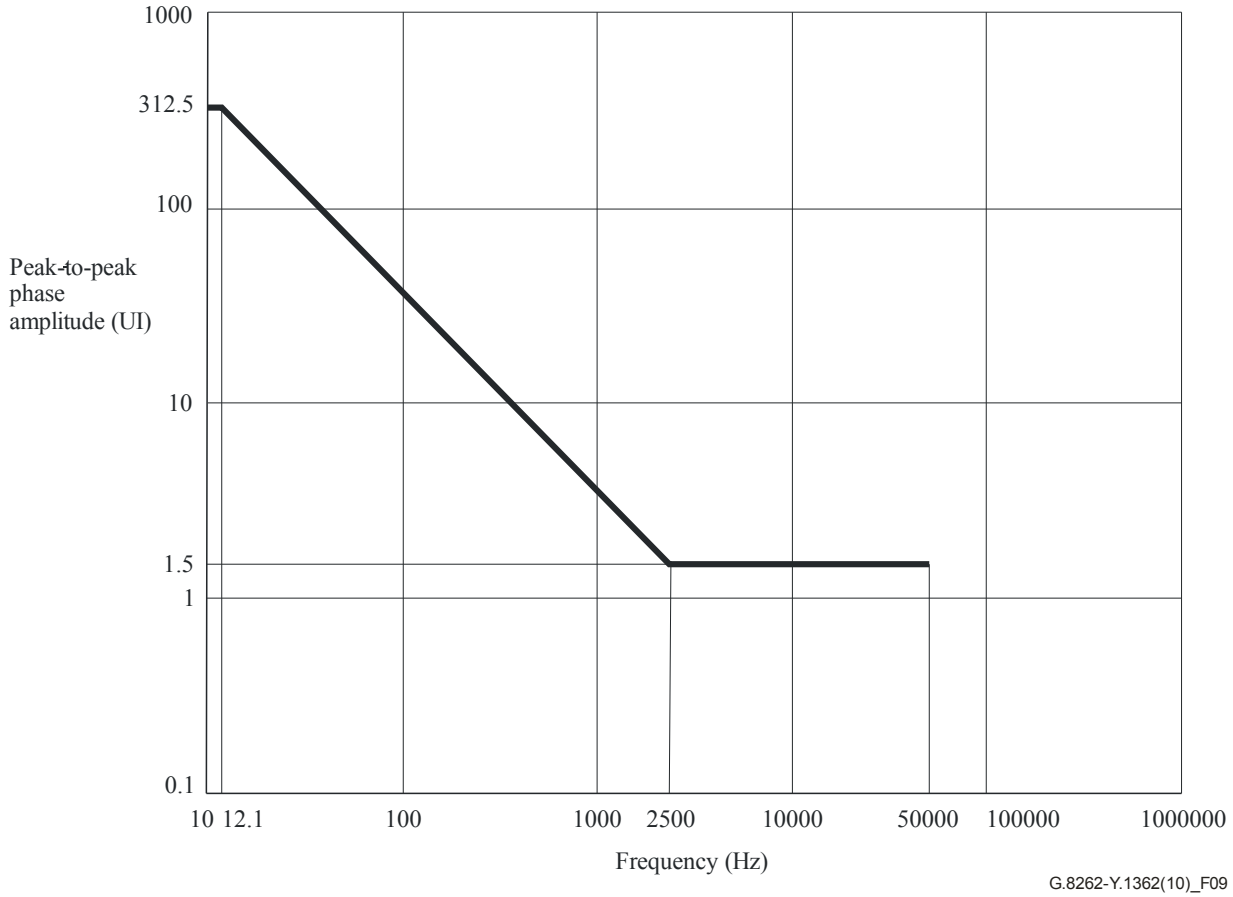

Figure 9 – 1G synchronous Ethernet wideband jitter tolerance for EEC-Option 1 and EEC-Option 2

NOTE 1 – The relevant IEEE 802.3 jitter tolerance requirements shall be met in addition to the specific synchronous Ethernet wideband jitter tolerance requirements.

NOTE 2 – For testing purposes, high frequency jitter tolerance and test signal generation for Ethernet traffic interfaces above 637 kHz are specified by [IEEE 802.3].

NOTE 3 – The slope above 50 kHz is 20 dB/decade. The actual values between 50 kHz and 637 kHz are for further study as the measurement methods between [IEEE 802.3] and ITU-T are not fully comparable. Information on the ITU jitter specification can be found in Appendix I of [ITU-T G.825].

The lower limit of maximum tolerable input jitter for 10G Ethernet interfaces for EEC-Option 1 and EEC-Option 2 is given in Table 12 and Figure 10.

Table 12 – 10G synchronous Ethernet wide-band jitter tolerance for EEC-Option 1 and EEC-Option 2

Peak-peak jitter amplitude (UI)	Frequency f (Hz)
2488	$10 < f \leq 12.1$
$30000\ f^{-1}$	$12.1 < f \leq 20$ k
1.5	20 k $< f \leq 40$ k
NOTE – 10G includes 10GBASE-SR/LR/ER, 10GBASE-LRM, 10GBASE-SW/LW/EW; multi-lane interfaces are for further study.	

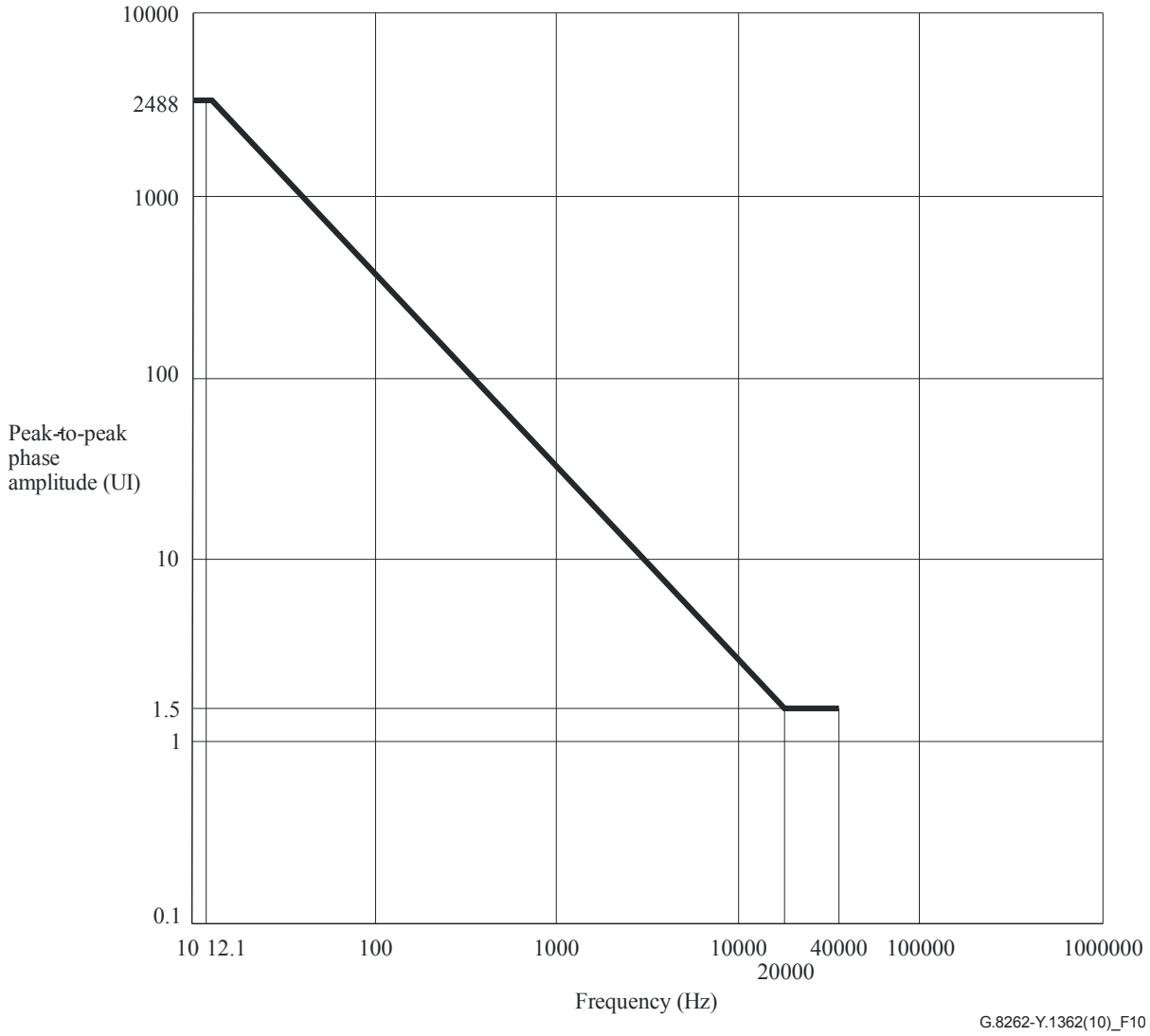

Figure 10 – 10G synchronous Ethernet wide-band jitter tolerance for EEC-Option 1 and EEC-Option 2

NOTE 4 – The relevant [IEEE 802.3] jitter tolerance requirements shall be met in addition to the specific synchronous Ethernet wideband and jitter tolerance requirements.

NOTE 5 – The measurements methods between [IEEE 802.3] and ITU-T are not fully comparable. Information on the ITU jitter specification can be found in Appendix I of [ITU-T G.825].

Jitter tolerance at 2048 kHz, 2048 kbit/s, 1544 kbit/s and STM-N interfaces:

The lower limit of maximum tolerable input jitter for 2048 kHz and 2048 kbit/s signals is defined for Option 1 in clause 8.2 of [ITU-T G.813].

The lower limit of maximum tolerable jitter for external 1544 kbit/s synchronization is defined for Option 2 in clause 8.2 of [ITU-T G.813].

The lower limit of maximum tolerable input jitter for STM-N interfaces is defined in [ITU-T G.825].

10 Noise transfer

The transfer characteristic of the EEC determines its properties with regard to the transfer of excursions of the input phase relative to the carrier phase. The EEC can be viewed as a low-pass filter for the differences between the actual input phase and the ideal input phase of the reference.

The minimum and maximum allowed bandwidths for this low-pass filter behaviour are based on the considerations described in Appendix II of [ITU-T G.813] and are indicated below.

In the passband, the phase gain of the EEC should be smaller than 0.2 dB (2.3%). The above applies to a linear EEC model. However, this model should not restrict implementation.

10.1 EEC-Option 1

The minimum bandwidth requirement for an EEC is 1 Hz. The maximum bandwidth requirement for an EEC is 10 Hz.

10.2 EEC-Option 2

Synchronous Ethernet or SDH NEs, when referenced to a synchronous Ethernet or a STM-N timing signal that meets the input TDEV mask in Figure 8 and Table 10, shall output signals that meet the output TDEV limits in Table 13.

Table 13 – Wander transfer for EEC-Option 2 (maximum output wander when input wander meets Table 10)

TDEV limit [ns]	Observation interval τ [s]
10	$0.1 < \tau \leq 1.7$
$5.77\ \tau$	$1.7 < \tau \leq 30$
$31.63\ \tau^{0.5}$	$30 < \tau \leq 1000$

The resultant requirement is shown in the mask of Figure 11. The purpose of these masks is to ensure that the maximum bandwidth of an EEC is 0.1 Hz. These masks should not be used to verify phase gain peaking. There is no requirement for a minimum bandwidth.

TDEV is measured through an equivalent 10-Hz, first-order, low-pass measurement filter at a maximum sampling time τ_0 of 1/30 seconds. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\tau$).

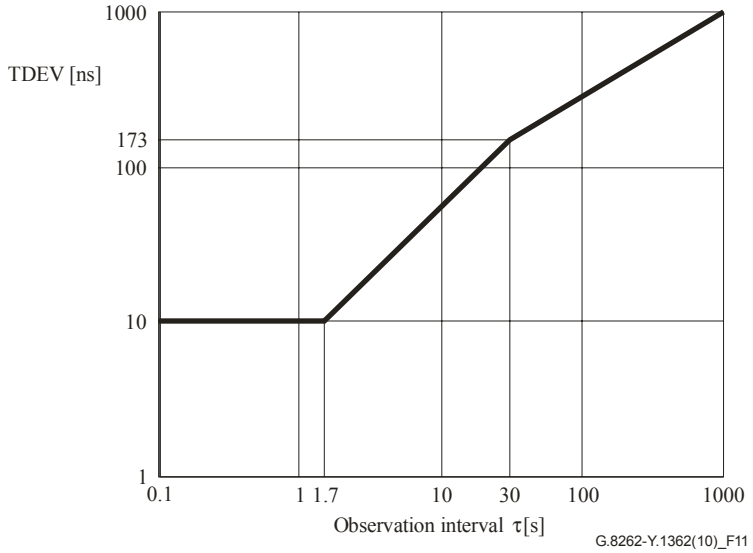

Figure 11 – Wander transfer for EEC-Option 2 (maximum output wander when input wander meets Figure 8)

The masks in Figures 8 and 11 are used to verify wander tolerance and measure TDEV transfer and they do not represent the network wander limit needed to be met for the payload wander

accumulation requirement. In practice, this will not cause loss of synchronization at an EEC, as the network wander tolerance limit in Figure 11 is within the pass band of the EEC-Option 2 clock. However, it will cause higher wander accumulation.

11 Transient response and holdover performance

The requirements in this clause apply to situations where the input signal is affected by disturbances or transmission failures (e.g., short interruptions, switching between different synchronization signals, loss of reference, etc.) that result in phase transients at the EEC output. The ability to withstand disturbances is necessary to avoid transmission defects or failures. Transmission failures and disturbances are common stress conditions in the transmission environment.

It is recommended that all the phase movements at the output of the EEC stay within the levels described in the following subclauses.

Measurements of MTIE for EEC-Option 2 clocks are carried out through an equivalent 100-Hz, first-order, low-pass measurement filter.

11.1 Short-term phase transient response

11.1.1 EEC-Option 1

This requirement reflects the performance of the clock in cases when the (selected) input reference is lost due to a failure in the reference path and a second reference input signal, traceable to the same reference clock, is available simultaneously, or shortly after the detection of the failure (e.g., in cases of autonomous restoration). In such cases the reference is lost for at most 15 seconds. The output phase variation, relative to the input reference before it was lost, is bounded by the following requirements:

The phase error should not exceed $\Delta t + 5 \times 10^{-8} \times S$ seconds over any period S up to 15 seconds. Δt represents two phase jumps that may occur during the transition into and out of the holdover state which both should not exceed 120 ns with a temporary frequency offset of no more than 7.5 ppm.

The resultant overall requirement is summarized in Figure 12. This figure is intended to depict the worst-case phase movement attributable to an EEC reference clock switch. Clocks may change state more quickly than is shown here. Background information on the requirements that drove this requirement is provided in Appendix II of [ITU-T G.813].

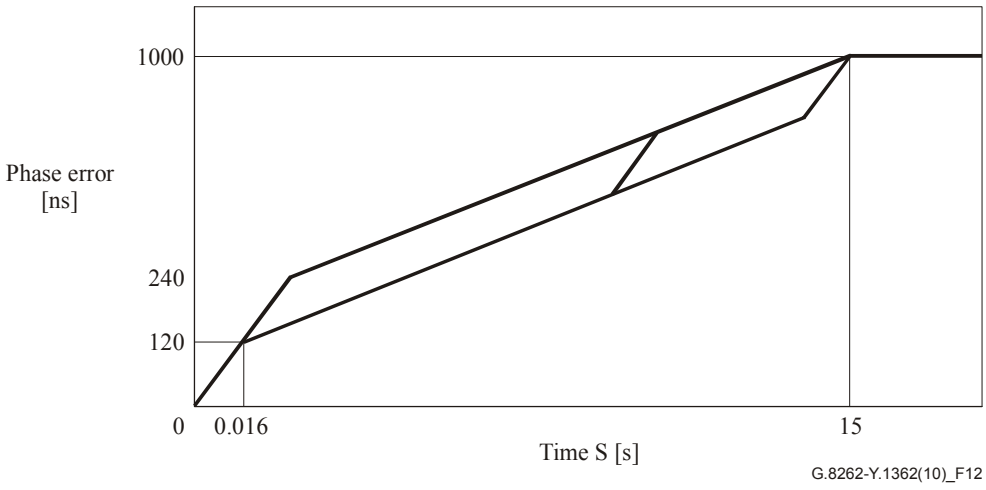

Figure 12 – Maximum phase transient at the output due to reference switching for EEC-Option 1

Figure 12 shows two phase jumps in the clock switching transient. The first jump reflects the initial response to a loss of the synchronization reference source and subsequent entry into holdover. The magnitude of this jump corresponds to a frequency offset less than 7.5 ppm for a duration less than 16 ms. After 16 ms, the phase movement is restricted to lie underneath the line with a slope of 5×10^{-8} in order to constrain pointer activity. The second jump, which is to take place within 15 seconds after entering holdover, accounts for the switching to the secondary reference. The same requirements are applicable for this jump. After the second jump, the phase error should remain constant and smaller than 1 µs.

NOTE – The output phase excursion, when switching between references which are not traceable to the same PRC, is for further study.

In cases where the input synchronization signal is lost for more than 15 seconds, the requirements in clause 11.2 apply.

11.1.2 EEC-Option 2

During clock rearrangement operations (e.g., reference switching), the output of the clock should meet the MTIE requirement as defined in clause 11.4.2.

11.2 Long-term phase transient response (Holdover)

This requirement bounds the maximum excursions in the output timing signal. Additionally, it restricts the accumulation of the phase movement during input signal impairments or internal disturbances.

11.2.1 EEC-Option 1

When an EEC loses all its references, it is said to enter the holdover state. The phase error, ΔT, at the output of the EEC relative to the input at the moment of loss of reference should not, over any period of $S > 15$ s, exceed the following limit:

$$\Delta T(S) = \{(a_1 + a_2)S + 0.5bS^2 + c\} \qquad \text{[ns]}$$

Where:

a_1 = 50 ns/s (see Note 1)

a_2 = 2000 ns/s (see Note 2)

b = 1.16×10^{-4} ns/s^2 (see Note 3)

c = 120 ns (see Note 4)

This limit is subject to a maximum frequency offset of ±4.6 ppm. The behaviour for $S < 15$ s is defined in clause 11.1.

NOTE 1 – The frequency offset a_1 represents an initial frequency offset corresponding to 5×10^{-8} (0.05 ppm).

NOTE 2 – The frequency offset a_2 accounts for temperature variations after the clock went into holdover and corresponds to 2×10^{-6} (2 ppm). If there are no temperature variations, the term a_2S should not contribute to the phase error.

NOTE 3 – The drift b is caused by ageing: 1.16×10^{-4} ns/s^2 corresponds to a frequency drift of 1×10^{-8}/day (0.01 ppm/day). This value is derived from typical ageing characteristics after 10 days of continuous operation. It is not intended to measure this value on a per day basis, as the temperature effect will dominate.

NOTE 4 – The phase offset c takes care of any additional phase shift that may arise during the transition at the entry of the holdover state.

The resultant overall requirement for constant temperature (i.e., when the temperature effect is negligible) is summarized in Figure 13.

$$\Delta T(S) = \left(a_1 S + \frac{b}{2} S^2 + c \right) \qquad [ns]$$

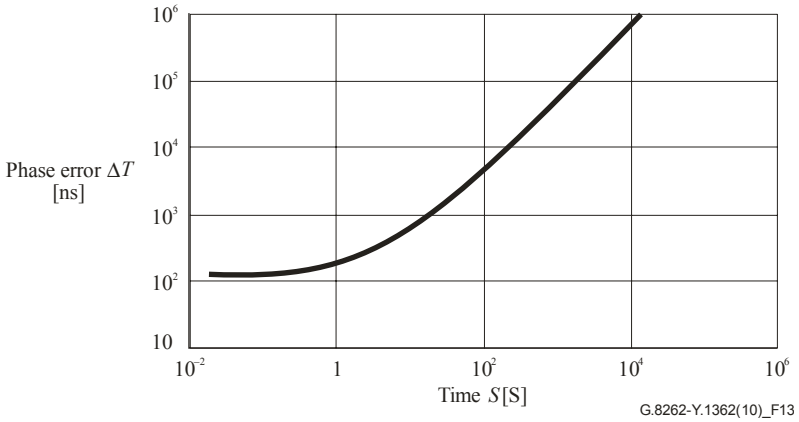

Figure 13 – Permissible phase error for an EEC-Option 1 under holdover operation at constant temperature

11.2.2 EEC-Option 2

When an EEC clock loses all its references, it enters the holdover state. The phase error, ΔT, at the output of the slave clock from the moment of loss of reference, should, over any period of S seconds, meet the following:

$$\left|\Delta T(S)\right| \le \left\{(a_1 + a_2)S + 0.5bS^2 + c\right\} \qquad [\text{ns}]$$

The derivative of $\Delta T(S)$, the fractional frequency offset, should, over any period of S seconds, meet the following:

$$\left|d(\Delta T(S))/dS\right| \le \left\{a_1 + a_2 + bS\right\} \qquad [\text{ns/s}]$$

The second derivative of $\Delta T(S)$, the fractional frequency drift, should, over any period of S seconds, meet the following:

$$\left|d^2(\Delta T(S))/dS^2\right| \le d \qquad \left[\text{ns/s}^2\right]$$

In applying the above requirements for the derivative of $\Delta T(S)$ and the second derivative of $\Delta T(S)$, the period S must begin after any transient associated with entry into holdover is over. During this transient period, the transient requirements of clause 11.4.2 apply.

NOTE 1 – a_1 represents an initial frequency offset under constant temperature conditions (±1 K).

NOTE 2 – a_2 accounts for temperature variations after the clock went into holdover. If there are no temperature variations, the term $a_2 S$ should not contribute to the phase error.

NOTE 3 – b represents the average frequency drift caused by aging. This value is derived from typical aging characteristics after 60 days of continuous operation. It is not intended to measure this value on a per day basis, as the temperature effect will dominate.

NOTE 4 – The phase offset c takes care of any additional phase shift that may arise during the transition at the entry of the holdover state.

NOTE 5 – d represents the maximum temporary frequency drift rate at constant temperature allowed during holdover. However, it is not required that d and b be equal.

The permissible phase error specification for EEC-Option 2 is shown in Table 14.

Table 14 – Transient response specification during holdover

	EEC-Option 2
Applies for	***S* > TBD**
a_1 [ns/s]	50
a_2 [ns/s]	300
b [ns/s^2]	4.63×10^{-4}
c [ns]	1000
d [ns/s^2]	4.63×10^{-4}
TBD: To be defined.	

11.3 Phase response to input signal interruptions

11.3.1 EEC-Option 1

For short-term interruptions on synchronization input signals that do not cause reference switching, the output phase variation should not exceed 120 ns, with a maximum frequency offset of 7.5 ppm for a maximum period of 16 ms.

11.3.2 EEC-Option 2

This is for further study.

11.4 Phase discontinuity

11.4.1 EEC-Option 1

In cases of infrequent internal testing or other internal disturbances (but excluding major hardware failures, e.g., those that would give rise to clock equipment protection switches) within the synchronous Ethernet equipment clock, the following conditions should be met:

– The phase variation over any period *S* (ms) up to 16 ms should not exceed 7.5*S* ns;

– The phase variation over any period *S* (ms) from 16 ms up to 2.4 s should not exceed 120 ns;

– For periods greater than 2.4 s, the phase variation for each interval of 2.4 s should not exceed 120 ns with a temporary offset of no more than 7.5 ppm up to a total amount of 1 µs.

11.4.2 EEC-Option 2

In cases of infrequent internal testing or rearrangement operations within the slave clock, the phase transient at the output of EEC-Option 2 should meet the MTIE specifications as specified in Table 15.

Table 15 – MTIE at the output due to reference switching/ rearrangement operations for EEC-Option 2

MTIE limit [ns]	Observation interval τ [s]
Not specified	$\tau \leq 0.014$
$7.6 + 885\ \tau$	$0.014 < \tau \leq 0.5$
$300 + 300\ \tau$	$0.5 < \tau \leq 2.33$
1000	$2.33 < \tau$

This MTIE requirement is illustrated in Figure 14.

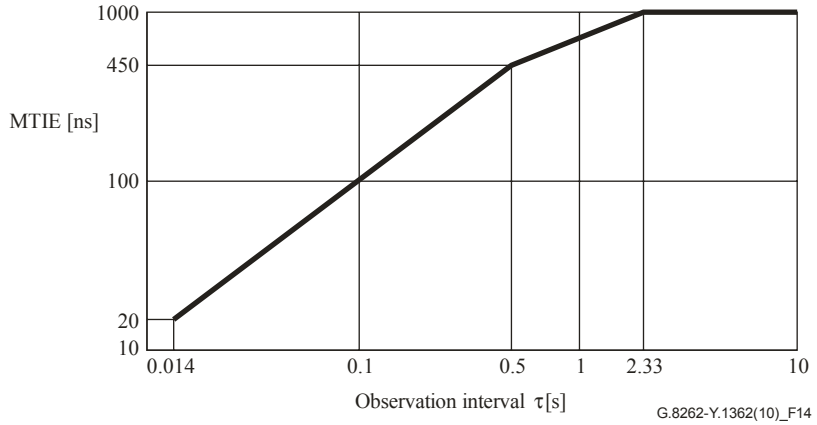

Figure 14 – MTIE at the output due to reference switching/ rearrangement operations for EEC-Option 2

12 Interfaces

The requirements in this Recommendation are related to reference points internal to the network elements (NEs) in which the clock is embedded and are, therefore, not necessarily available for measurement or analysis by the user. Therefore, the performance of the EEC is not defined at these internal reference points, but rather at the external interfaces of the equipment.

The synchronization input and output interfaces for Ethernet equipment in which the EEC may be contained are:

– 1544-kbit/s interfaces according to [ITU-T G.703];
– 2048-kHz external interfaces according to [ITU-T G.703];
– 2048-kbit/s interfaces according to [ITU-T G.703];
– STM-N traffic interfaces (for hybrid NEs);
– 64-kHz interface according to [ITU-T G.703];
– 6312-kHz external interfaces according to [ITU-T G.703];
– Synchronous Ethernet interfaces.

All of the above interfaces may not be implemented on all equipment. These interfaces should comply with the jitter and wander requirements as defined in this Recommendation.

Ethernet copper interfaces allow half-duplex mode and collisions on a line which could squelch the signals and destroy the timing, therefore synchronous Ethernet interfaces must work only in full-duplex and have a continuous bit stream.

NOTE – To support interoperability with existing network equipment, interfaces to and from external network clocks may optionally support SSM.

12.1 External synchronization interfaces

Synchronization Ethernet equipment will require a range of external synchronization interface types to be supported that will allow synchronization to be derived from an [ITU-T G.812] SSU/BITS clock, from the output of an [ITU-T G.813] SEC or from another synchronous Ethernet equipment as specified in this Recommendation.

The primary objectives are:

– to provide an easy migration path from existing synchronization distribution architectures based on SDH transmission to future synchronization architectures based on carrier scale Ethernet transport with an embedded EEC;

– to ensure that synchronization (frequency) is transported at the physical layer where it is not subject to load impairments.

Table 16 shows the external interface type.

Table 16 – External interface type

External interface type	Supports
[ITU-T G.703]-based 2.048 MHz/2.048 Mbit/s 1.544 MHz/1.544 Mbit/s	Legacy/Initial architecture support for frequency NOTE – Allows transition from legacy architecture based on SDH to carrier scale initial synchronous Ethernet architecture reusing existing SSU functionality.
Synchronous Ethernet (rate TBD)	Initial requirement for frequency

Other external interface types are for further study.

NOTE – Synchronous Ethernet support for time transfer (i.e., both frequency and time) is for further study.

Appendix I

Hybrid network elements (NEs) using STM-N and Ethernet (ETY) interfaces

(This appendix does not form an integral part of this Recommendation)

The EEC clocks may support the use of hybrid NEs at any place in a synchronization chain as shown in Appendix XII of [ITU-T G.8261]. Figure I.1 illustrates a hybrid NE and timing relations between the equipment clock (EC) and STM-N and ETY interfaces.

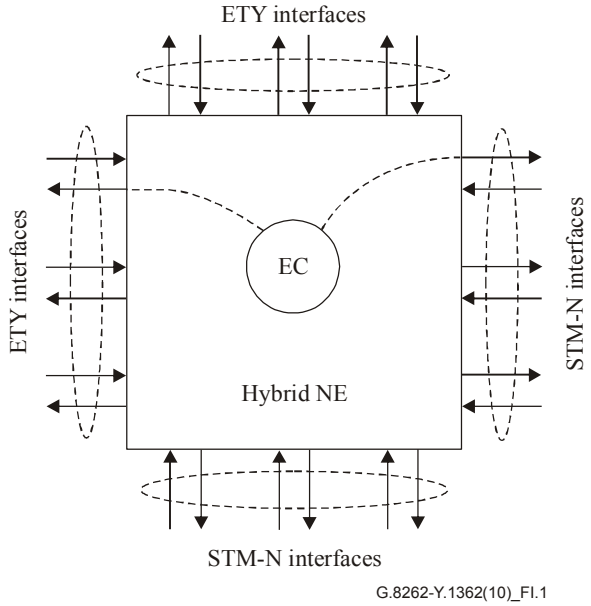

Figure I.1 – Hybrid NE using STM-N and Ethernet (ETY) interfaces

For hybrid NEs, timing transfer may be supported from any type of input interface to any type of output interface as shown in Table I.1.

Table I.1 – Combination of input and output ports for timing distribution

Timing input	Timing output
STM-N	STM-N
STM-N	ETY
STM-N	T4
ETY	STM-N
ETY	ETY
ETY	T4
T3	STM-N
T3	ETY

The use of ETY interfaces for timing distribution and the use of hybrid NEs should not require modifications of deployed SDH NEs or clocks (PRC, SSU), e.g., no new SSM code point for STM-N interfaces. Code point "0000" should also not be used.

Appendix II

Relationship between requirements contained in this Recommendation and other key synchronization-related Recommendations

(This appendix does not form an integral part of this Recommendation)

This appendix describes the relationship between the clock performance requirements contained within the body of this Recommendation and the key synchronization Recommendations that are under development, or have been developed within Question 13 (Network synchronization and time distribution performance) of ITU-T Study Group 15.

This Recommendation describes performance requirements for synchronous Ethernet clocks. The basic concept of synchronous Ethernet is described in [ITU-T G.8261], the first ITU-T Recommendation to detail network synchronization aspects applicable to packet-based networks.

The clocks described in this Recommendation, if embedded into Ethernet network elements, allow transfer of network traceable timing via the Ethernet physical layer. In this context, the Ethernet physical layer is defined by [IEEE 802.3].

The performance requirements in this Recommendation are derived from existing Recommendations. The EEC-Option 1 requirements are based on the [ITU-T G.813] Option 1 clock and the EEC-Option 2 is based on the Type IV clock from [ITU-T G.812], as deployed in an SDH NE.

Both EEC clocks offer similar performance, but are intended for use in networks optimized to either the 2-Mbit/s hierarchy (for Option 1) or to the 1544-kbit/s hierarchy (for Option 2). As the EEC clocks are consistent with existing SDH network element clocks used in the distribution of frequency, synchronization network engineering will not require any change to current network engineering practices.

Synchronization networks in general are based on SDH synchronization distribution as described in [ITU-T G.803]. Synchronization distribution may follow specific regional practices in order to meet the fundamental performance requirements and network interface limits from either [ITU-T G.823] or [ITU-T G.824] for the 2048-kbit/s or 1544-kbit/s hierarchy, respectively. Both [ITU-T G.823] and [ITU-T G.824] are traceable to the fundamental slip rate objectives in [ITU-T G.822].

The EEC clocks are purposely specified to perform in a manner consistent with existing synchronization networks. The Option-1 EEC can be deployed within the synchronization distribution network in exactly the same manner as a [ITU-T G.813] SEC, while the Option-2 EEC can be deployed as per existing [ITU-T G.812] Type IV clocks.

Appendix III

List of Ethernet interfaces applicable to synchronous Ethernet

(This appendix does not form an integral part of this Recommendation)

A list of all Ethernet interfaces listed in [IEEE 802.3] published in 2008 is provided in Table III.1. It specifies the Ethernet interfaces which are valid for synchronous Ethernet operation. Other interfaces may exist; the list of interfaces is not exhaustive and might be updated.

The following considerations have been taken into consideration for the generation of this list.

CSMA/CD

[IEEE 802.3] specifies two operating modes: half-duplex and full-duplex modes.

The original Ethernet interfaces were developed for a single medium that was shared between multiple end stations using the CSMA/CD mechanism. Most interfaces use separate media (or separate carriers) for bidirectional communication between two end stations. The use of half-duplex operation on such bidirectional, point-to-point media serves to mimic the behaviour of legacy shared media operation. In all cases, there is no difference in PHY behaviour between half-duplex and full-duplex modes. The half-duplex functionality is controlled by the media access control sublayer (MAC) and only affects packet transport at layer 2 and above.

Interfaces titled CSMA/CD may be used for the purposes of synchronous Ethernet in all cases where the media is point-to-point.

Constant signal

The interface must permanently transport a signal.

This signal must be coded so that there is a guarantee of transitions so that the clock can be recovered. This is achieved by the 64B/66B encoding in some 10G interfaces; DSQ-128 (2 x 2 pair, PAM-16) signalling for 10G over twisted pair copper; 8B/10B encoding in some 1G interfaces and 10G over 4 channels of fibre or copper; 4D-PAM-5 encoding for 1G over twisted pair copper interfaces; 4B/5B encoding for some 100M interfaces; and MLT-3 for 100M over twisted pair copper interfaces.

All IEEE 802.3 point-to-point PHYs that operate at speed of 100 Mbit/s or greater use constant signalling.

Master/slave

Some bidirectional interfaces are designed to have one side, designated as the clock master, acting as the clock generator, the other side as the slave, which is forced to recover the clock.

Such a configuration will only support unidirectional synchronous Ethernet. Such conditions can be announced under supervision of the Ethernet synchronization message channel (ESMC) process, as defined in [ITU-T G.8264] where synchronous Ethernet reduced interfaces are introduced. For such interfaces, the master/slave resolution should be forced by station management as defined by the appropriate clause in [IEEE 802.3], in accordance with the synchronization network architecture. ESMC reduced interface status should be synchronized with master/slave status.

Two examples of master/slave clock operation are 1000BASE-T and 10GBASE-T.

Auto-negotiation

The auto-negotiation mechanism defined for some sets of PHYs is used to find the highest mutually supported mode of operation for two partners at link start-up time. The algorithm will always favour a higher speed compared to a lower speed and full-duplex to half-duplex. Because the negotiation

happens at link start-up, it should be compatible with synchronous Ethernet but may not be compatible with the synchronization distribution plan. Note that the negotiation is an option for some PHY types and the supported PHY speed and duplex may be forced by management.

Note that there are some cases where auto-negotiation could appear during operation, e.g., during an upgrade. Auto-negotiation must not have any impact on rates and clocks to be compatible with synchronous Ethernet.

Physical loopback

All physical loopback functionalities specified on full-duplex links that interrupt the link for test/check "in-service" are not compatible with synchronous Ethernet. Thus, they should be only allowed during the link set-up.

Point-to-multipoint

Some PHY interfaces are designed for point-to-multipoint operation over passive optical networks. Such links use intermittent signalling for the upstream direction but may be suitable for unidirectional synchronous Ethernet.

Miscellaneous

Some of the older PHY types are rarely used and need not be considered, for example two PHY types are defined for use over DSL.

Implementation issues

Some interfaces transmit signals over parallel cables or fibres. These interfaces use one clock source for all physical lanes, but the recovered clock (and reference point for timestamping) may vary depending on the definition of multi-lane operation. It is not clear at this point whether further definition will be required for the operation of synchronous Ethernet over these interfaces.

Based on the above considerations, Table III.1 lists the PHY interfaces specified by [IEEE 802.3] and designates which ones may be considered for synchronous Ethernet compatibility, which should not be considered, and which may be unidirectional only.

Table III.1 – List of Ethernet interfaces eligible to synchronous Ethernet

PHY	Description	[IEEE 802.3] clause	Coding	Synchronous Ethernet capable
10BASE2	10 Mbit/s coaxial	10	Manchester, intermittent	No
10BASE5	*10 Mbit/s coaxial*	*8*	*Manchester, intermittent*	*No (Note 1)*
10BASE-F	10 Mbit/s fibre	15	NRZ, intermittent	No
10BASE-FP	*10 Mbit/s fibre, star*	*16*	*NRZ, intermittent*	*No (Note 1)*
10BASE-T	10 Mbit/s TP copper	14	Manchester, intermittent	No
100BASE-BX10	100 Mbit/s bidi fibre	58, 66	4B/5B	Yes
100BASE-FX	100 Mbit/s fibre	24, 26	4B/5B	Yes
100BASE-LX10	100 Mbit/s fibre	58, 66	4B/5B	Yes
100BASE-T2	*100 Mbit/s TP copper*	*32*	*PAM-5*	*No (Note 1)*

Table III.1 – List of Ethernet interfaces eligible to synchronous Ethernet

PHY	Description	[IEEE 802.3] clause	Coding	Synchronous Ethernet capable
100BASE-T4	*100 Mbit/s TP copper*	*23*	*8B6T*	*No (Note 1)*
100BASE-TX	100 Mbit/s TP copper	24, 25	MLT-3	Yes
1000BASE-BX10	1 Gbit/s bidi fibre	59, 66	8B/10B	Yes
1000BASE-CX	1 Gbit/s twinax	39	8B/10B	Yes
1000BASE-KX	1 Gbit/s backplane	70	8B/10B	Yes
1000BASE-LX	1 Gbit/s fibre	38	8B/10B	Yes
1000BASE-PX	1 Gbit/s PON	38	8B/10B	Unidirectional
1000BASE-SX	1 Gbit/s fibre	38	8B/10B	Yes
1000BASE-T	1 Gbit/s TP copper	40	4D-PAM5	Unidirectional (Note 2)
10BROAD36	*10 Mbit/s coax*	*11*	*BPSK*	*No (Note 1)*
10GBASE-CX4	10 Gbit/s 4x twinax	54	8B/10B	Yes
10GBASE-ER	10 Gbit/s fibre	49, 52	64B/66B	Yes
10GBASE-EW	10 Gbit/s fibre	50, 52	64B/66B	Yes
10GBASE-KR	10 Gbit/s backplane	72	64B/66B	Yes
10GBASE-KX4	10 Gbit/s 4x backplane	71	8B/10B	Yes
10GBASE-LR	10 Gbit/s fibre	49, 52	64B/66B	Yes
10GBASE-LRM	10 Gbit/s fibre	68	64B/66B	Yes
10GBASE-LW	10 Gbit/s fibre	50, 52	64B/66B	Yes
10GBASE-LX4	10 Gbit/s 4λ fibre	50, 52	8B/10B	Yes
10GBASE-SR	10 Gbit/s fibre	49, 52	64B/66B	Yes
10GBASE-SW	10 Gbit/s fibre	50, 52	64B/66B	Yes
10GBASE-T	10 Gbit/s TP copper	55	DSQ-128	Yes (Note 3)
10PASS-TS	>10 Mbit/s DSL	61, 62	DMT	No
1BASE-5	*1 Mbit/s TP copper*	*12*	*Manchester*	*No (Note 1)*
2BASE-TL	>2 Mbit/s DSL	61, 63	PAM	No
10/1GBASE-PR	10 Gbit/s/1 Gbit/s PON	76	64B/66B/8B/10B	Unidirectional
10GBASE-PR	10 Gbit/s PON	76	64B/66B	Unidirectional
40GBASE-KR4	40 Gbit/s 4x backplane	84	64B/66B	Yes
40GBASE-CR4	40 Gbit/s 4x twinax	85	64B/66B	Yes

Table III.1 – List of Ethernet interfaces eligible to synchronous Ethernet

PHY	Description	[IEEE 802.3] clause	Coding	Synchronous Ethernet capable
40GBASE-SR4	40 Gbit/s 4x fibre	86	64B/66B	Yes
40GBASE-LR4	40 Gbit/s 4λ fibre	87	64B/66B	Yes
100GBASE-CR10	100 Gbit/s 10x twinax	85	64B/66B	Yes
100GBASE-SR10	100 Gbit/s 10x fibre	86	64B/66B	Yes
100GBASE-LR4	100 Gbit/s 4λ fibre	88	64B/66B	Yes
100GBASE-ER4	100 Gbit/s 4λ fibre	88	64B/66B	Yes
NOTE 1 – These rows (in italics) are deprecated. NOTE 2 – Noise transfer is not measured on a loop-timed interface. NOTE 3 – 10GBASE-T may support dual master or master/slave clocking (i.e., unidirectional synchronous Ethernet).				

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Printed in Switzerland
Geneva, 2010