International Telecommunication Union

ITU-T G.8262/Y.1362

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

Amendment 1

(03/2020)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

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SERIES Y: GLOBAL INFORMATION INFRASTRUCTURE, INTERNET PROTOCOL ASPECTS, NEXT-GENERATION NETWORKS, INTERNET OF THINGS AND SMART CITIES

Timing characteristics of synchronous equipment slave clock

Amendment 1

Recommendation ITU-T G.8262/Y.1362 (2018) – Amendment 1

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Recommendation ITU-T G.8262/Y.1362

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Summary

Recommendation ITU-T G.8262/Y.1362 outlines requirements for timing devices used in synchronizing network equipment that uses the physical layer to deliver frequency synchronization. This Recommendation defines the requirements for clocks, e.g., bandwidth, frequency accuracy, holdover and noise generation.

Amendment 1 provides the following updates:

– Updates references in clause 2,

– Adds a note in clause 9.2.1,

– Changes Figure 13 in clause 11.2.1,

– Adds PAM4 interfaces in Appendix III,

– Adds a sentence in Appendix VII.

History

Edition	Recommendation	Approval	Study Group	Unique ID*
1.0	ITU-T G.8262/Y.1362	2007-08-13	15	11.1002/1000/9190
1.1	ITU-T G.8262/Y.1362 (2007) Amd. 1	2008-04-29	15	11.1002/1000/9417
1.2	ITU-T G.8262/Y.1362 (2007) Amd.2	2010-01-13	15	11.1002/1000/10432
2.0	ITU-T G.8262/Y.1362	2010-07-29	15	11.1002/1000/10909
2.1	ITU-T G.8262/Y.1362 (2010) Amd. 1	2012-02-13	15	11.1002/1000/11523
2.2	ITU-T G.8262/Y.1362 (2010) Amd. 2	2012-10-29	15	11.1002/1000/11814
3.0	ITU-T G.8262/Y.1362	2015-01-13	15	11.1002/1000/12389
3.1	ITU-T G.8262/Y.1362 (2015) Cor. 1	2016-11-13	15	11.1002/1000/13105
4.0	ITU-T G.8262/Y.1362	2018-11-29	15	11.1002/1000/13766
4.1	ITU-T G.8262/Y.1362 (2018) Amd. 1	2020-03-15	15	11.1002/1000/14208

Keywords

EEC, jitter, OEC, synchronization, wander.

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* To access the Recommendation, type the URL http://handle.itu.int/ in the address field of your web browser, followed by the Recommendation's unique ID. For example, http://handle.itu.int/11.1002/1000/11830-en.

FOREWORD

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Introduction

The synchronization method implicit in this Recommendation is the master-slave method using a synchronous physical layer (e.g., ETY, STM-N) for distributing a frequency synchronization reference originating from a primary reference clock (PRC) or from a primary reference time clock (PRTC). Such methods are widely implemented to synchronize time division multiplexing (TDM) and mobile backhaul networks.

Recommendation ITU-T G.8262/Y.1362

Timing characteristics of synchronous equipment slave clock

Amendment 1

Editorial note: This is a complete-text publication. Modifications introduced by this amendment are shown in revision marks relative to Recommendation ITU-T G.8262/Y.1362 (2018).

1 Scope

This Recommendation outlines minimum requirements for timing devices used in synchronizing network equipment that support synchronous clocks. It supports clock distribution based on the network-synchronous line-code methods (e.g., synchronous Ethernet, synchronous OTN to deliver frequency synchronization).

This Recommendation focuses on the requirements for the synchronous Ethernet equipment clock (EEC) and the synchronous OTN equipment clock (OEC).

The Recommendation allows for proper network operation when a synchronous equipment clock (Option 1 or 2) is timed from another network equipment clock or a higher-quality clock.

Included in this Recommendation are requirements for clock accuracy, noise transfer, holdover performance, noise tolerance and noise generation. These requirements apply under the normal environmental conditions specified for the equipment.

This Recommendation contains two options for synchronous equipment clocks. The first option, referred to as "Option 1", applies to synchronous equipment designed to interwork with networks optimized for the 2048 kbit/s hierarchy. These networks allow the worst-case synchronization reference chain as specified in Figure 8-5 of [ITU-T G.803]. The second option, referred to as "Option 2", applies to synchronous equipment designed to interwork with networks optimized for the 1544 kbit/s hierarchy. The synchronization reference chain for these networks is defined in clause II.3 of [ITU-T G.813].

A synchronous equipment slave clock should comply with all the requirements specific to one option and should not mix requirements between Options 1 and 2. In the clauses where one requirement is specified, the requirements are common to both options.

The intent of the synchronous Ethernet and synchronous OTN is to interoperate with each other and with existing synchronization networks based on [ITU-T G.813].

Careful consideration should be taken when interworking between networks with synchronous equipment clocks based on Option 1 and networks with synchronous equipment clocks based on Option 2.

Some synchronous network elements (NEs) may have a higher-quality clock. This Recommendation allows for proper network operation when synchronous equipment (Option 1 or 2) is timed from either another synchronous equipment (like option) clock, or a higher-quality clock. Hierarchical timing distribution is recommended for synchronous networks. Timing should not be passed from a synchronous clock in free-run/holdover mode to a higher-quality clock since the higher-quality clock should not follow the free-run/holdover signal during fault conditions.

OTN 3R regenerators, as specified in [ITU-T G.8251], provide through-timing capability and can transmit timing via synchronous OTN.

More information on synchronous Ethernet can be found in [ITU-T G.781], [ITU-T G.8261] and [ITU-T G.8264], and for synchronous OTN can be found in [ITU-T G.709] and [ITU-T G.7041].

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T G.703] Recommendation ITU-T G.703 (2016), *Physical/electrical characteristics of hierarchical digital interfaces*.

[ITU-T G.709] Recommendation ITU-T G.709 (2016), *Interfaces for the optical transport network.*

[ITU-T G.781] Recommendation ITU-T G.781 (2017), *Synchronization layer functions.*

[ITU-T G.7041] Recommendation ITU-T G.7041/Y.1303 (2016), *Generic framing procedure.*

[ITU-T G.803] Recommendation ITU-T G.803 (2000), *Architecture of transport networks based on the synchronous digital hierarchy (SDH).*

[ITU-T G.810] Recommendation ITU-T G.810 (1996), *Definitions and terminology for synchronization networks*.

[ITU-T G.811] Recommendation ITU-T G.811 (1997), *Timing characteristics of primary reference clocks*.

[ITU-T G.812] Recommendation ITU-T G.812 (2004), *Timing requirements of slave clocks suitable for use as node clocks in synchronization networks*.

[ITU-T G.813] Recommendation ITU-T G.813 (2003), *Timing characteristics of SDH equipment slave clocks (SEC).*

[ITU-T G.825] Recommendation ITU-T G.825 (2000), *The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH).*

[ITU-T G.8251] Recommendation ITU-T G.8251 (2018~~0~~), *The control of jitter and wander within the optical transport network (OTN).*

[ITU-T G.8261] Recommendation ITU-T G.8261/Y.1361 (2019~~3~~), *Timing and synchronization aspects in packet networks*.

[ITU-T G.8264] Recommendation ITU-T G.8264/Y.1364 (2017), *Distribution of timing information through packet networks*.

[ITU-T G.8272] Recommendation ITU-T G.8272 (2018~~5~~), *Timing characteristics of primary reference time clocks*.

[IEEE 802.3] IEEE Standard 802.3 (2018), *IEEE Standard for Ethernet*.

3 Definitions

The terms and definitions used in this Recommendation are contained in [ITU-T G.810].

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

BITS	Building Integrated Timing Source
BPSK	Binary Phase Shift Keying
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DSL	Digital Subscriber Line
EC	Equipment Clock
EEC	synchronous Ethernet Equipment Clock
ESMC	Ethernet Synchronization Message Channel
ETH	Ethernet MAC layer network
ETY	Ethernet PHY layer network
GNSS	Global Navigation Satellite System
MAC	Media Access Control
MTIE	Maximum Time Interval Error
NE	Network Element
NRZ	Non-Return to Zero
OAM	Operations, Administration and Maintenance
OEC	OTN Equipment Clock
OTN	Optical Transport Network
PAM	Pulse Amplitude Modulation
PHY	Physical (layer)
ppm	parts per million
PRC	Primary Reference Clock
PRTC	Primary Reference Time Clock
SDH	Synchronous Digital Hierarchy
SEC	Synchronous Equipment Clock (NOTE – see Conventions)
SSM	Synchronization Message Channel
SSU	Synchronization Supply Unit
STM-N	Synchronous Transport Module-N
TDEV	Time Deviation
TDM	Time Division Multiplexing
UI	Unit Interval
UTC	Coordinated Universal Time

5 Conventions

SEC: synchronous equipment clock: A generic term representing the SDH equipment clock ([ITU-T G.813]), the Ethernet equipment clock (EEC) and the OTN equipment clock, which are defined in this Recommendation.

6 Frequency accuracy

6.1 Option 1

Under free-running conditions, the equipment clock output frequency accuracy should not be greater than 4.6 ppm with regard to a reference traceable to a [ITU-T G.811] or [ITU-T G.8272] clock.

NOTE – The time interval for this accuracy is for further study. Values of one month and one year have been proposed.

6.2 Option 2

Under prolonged holdover conditions, the output frequency accuracy of the different types of node clocks should not exceed 4.6 ppm with regard to a reference traceable to a primary reference clock, over a time period T of one year.

NOTE – The time period T applies after 30 days of continuous synchronized operation.

7 Pull-in, hold-in and pull-out ranges

7.1 Pull-in range

7.1.1 Option 1

The minimum pull-in range should be ±4.6 ppm, whatever the internal oscillator frequency offset may be.

7.1.2 Option 2

The minimum pull-in range should be ±4.6 ppm, whatever the internal oscillator frequency offset may be.

7.2 Hold-in range

7.2.1 Option 1

The hold-in range for the Option 1 equipment clock is not required.

7.2.2 Option 2

The hold-in range for the Option 2 equipment clock should be ±4.6 ppm, whatever the internal oscillator frequency offset may be.

7.3 Pull-out range

7.3.1 Option 1

The pull-out range is for further study. A minimum value of ±4.6 ppm has been proposed.

7.3.2 Option 2

The pull-out range is not applicable.

8 Noise generation

The noise generation of an equipment clock represents the amount of phase noise produced at the output when there is an ideal input reference signal or the clock is in holdover state. A suitable reference, for practical testing purposes, implies a performance level of at least ten times more stable than the output requirements. The ability of the clock to limit this noise is described by its frequency stability. The maximum time interval error (MTIE) and time deviation (TDEV) are useful means for characterization of noise generation performance.

MTIE and TDEV are measured through an equivalent 10-Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 seconds. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\tau$).

8.1 Wander in locked mode

8.1.1 Option 1

When the equipment clock is in the locked mode of operation synchronized to a wander-free reference, the MTIE measured using the synchronized clock configuration defined in Figure 1a of [ITU-T G.810] should have the limits in Table 1, if the temperature is constant (within ±1°K):

Table 1 – Wander generation (MTIE) for Option 1 with constant temperature

MTIE limit [ns]	Observation interval τ [s]
40	$0.1 < \tau \leq 1$
$40\ \tau^{0.1}$	$1 < \tau \leq 100$
$25.25\ \tau^{0.2}$	$100 < \tau \leq 1000$

The resultant requirement is shown by the thick solid line in Figure 1.

When temperature effects are included, the allowance for the total MTIE contribution of a single equipment clock increases by the values in Table 2.

Table 2 – Additional wander generation (MTIE) for Option 1 with temperature effects

Additional MTIE allowance [ns]	Observation interval τ [s]
$0.5\ \tau$	$\tau \leq 100$
50	$\tau > 100$

The resultant requirements are shown by the thin solid line in Figure 1.

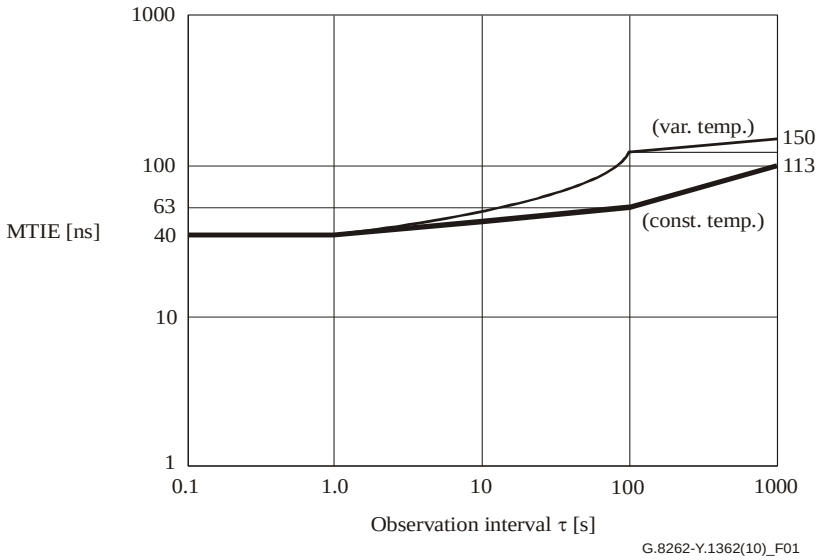

Figure 1 – Wander generation (MTIE) for Option 1

When the equipment clock is in the locked mode of operation, the TDEV measured using the synchronized clock configuration defined in Figure 1a of [ITU-T G.810] should have the limits in Table 3, if the temperature is constant (within ±1°K):

Table 3 – Wander generation (TDEV) for Option 1 with constant temperature

TDEV limit [ns]	Observation interval τ [s]
3.2	$0.1 < \tau \leq 25$
$0.64\ \tau^{0.5}$	$25 < \tau \leq 100$
6.4	$100 < \tau \leq 1000$

The resultant requirements are shown in Figure 2.

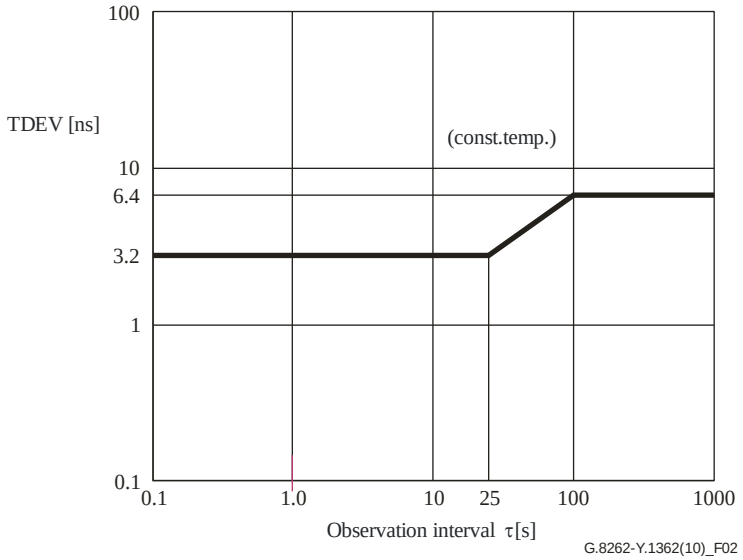

Figure 2 – Wander generation (TDEV) for Option 1 with constant temperature

The allowance for the total TDEV contribution of a single equipment clock when temperature effects are included is for further study.

8.1.2 Option 2

When the equipment clock clock is in the locked mode of operation synchronized to a wander-free reference, the MTIE and TDEV measured at the output under constant temperature (within ±1°K) shall be below the limits in Tables 4 and 5 respectively.

Table 4 – Wander generation (MTIE) for Option 2 with constant temperature

MTIE limit [ns]	Observation interval τ [s]
20	$0.1 < \tau \leq 1$
$20\ \tau^{0.48}$	$1 < \tau \leq 10$
60	$10 < \tau \leq 1000$

Table 5 – Wander generation (TDEV) for Option 2 with constant temperature

TDEV limit [ns]	Observation interval τ [s]
$3.2\ \tau^{-0.5}$	$0.1 < \tau \leq 2.5$
2	$2.5 < \tau \leq 40$
$0.32\ \tau^{0.5}$	$40 < \tau \leq 1000$
10	$1000 < \tau \leq 10\ 000$

The resultant requirements are shown in Figures 3 and 4.

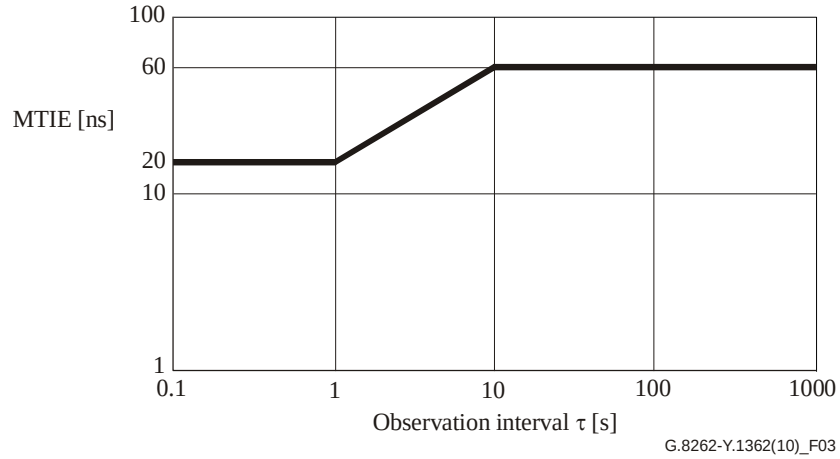

Figure 3 – Wander generation (MTIE) for Option 2 with constant temperature

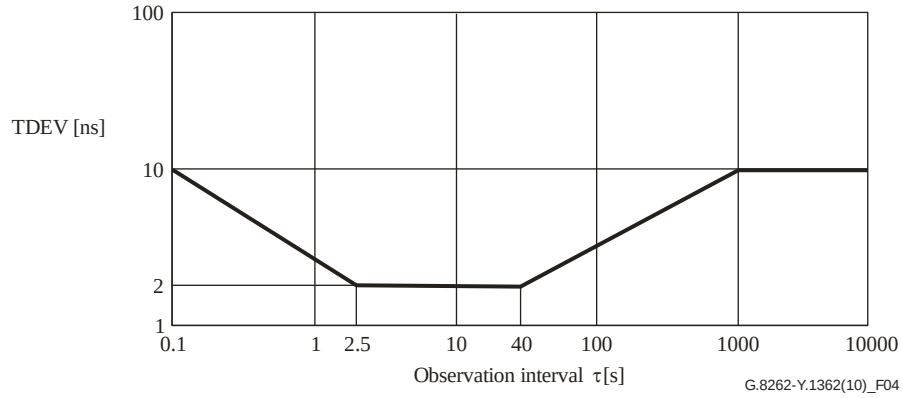

Figure 4 – Wander generation (TDEV) for Option 2 with constant temperature

8.2 Non-locked wander

When a clock is not locked to a synchronization reference, the random noise components are negligible compared to deterministic effects like initial frequency offset. Consequently, the non-locked wander effects are included in clause 11.2.

8.3 Jitter

While most requirements in this Recommendation are independent of the output interface at which they are measured, this is not the case for jitter production; jitter generation requirements utilize existing Recommendations that have different limits for different interface rates. These requirements are stated separately for the interfaces identified in clause 12.

8.3.1 Option 1 EEC and Option 2 EEC jitter generation

Output jitter at a synchronous Ethernet interface:

In the absence of input jitter at the synchronization interface, the intrinsic jitter at the synchronous Ethernet output interfaces, as measured over a 60-second interval, should not exceed the limits given in Table 6.

Table 6 – Synchronous Ethernet jitter generation for Option 1 EEC and Option 2 EEC

Interface	Measuring filter	Peak-to-peak amplitude (UI)
1G (Notes 1, 2, 4, 5)	2.5 kHz to 10 MHz	0.50
10G (Notes 1, 3, 4, 5)	20 kHz to 80 MHz	0.50
25G (Note 1, 4, 5, 6)	20 kHz to 200 MHz	1.2

NOTE 1 – There is no specific high-band jitter requirement for synchronous Ethernet. The relevant IEEE 802.3 jitter requirements shall be met in addition to the specific synchronous Ethernet wideband jitter requirements specified in this table. [IEEE 802.3] defines measurement methodologies. The applicability for those measurement methodologies in a synchronization network environment is for further study.

NOTE 2 – 1G includes 1000BASE-KX, -SX, -LX; multi-lane interfaces are for further study.

NOTE 3 – 10G includes 10GBASE-SR/LR/ER, 10GBASE-LRM, 10GBASE-SW/LW/EW and multi-lane interfaces consisting of 10G lanes including 40GBASE-KR4/CR4/SR4/LR4 and 100GBASE-CR10/SR10.

NOTE 4 – 25G includes 25GBASE-SR, 25GBASE-LR, 25GBASE-ER, and multi-lane interfaces consisting of 25G lanes including 100GBASE-LR4/ER4.

NOTE 5 – 1G: (1000BASE-KX, -SX, -LX) 1 UI = 0.8 ns
10G (10GBASE-SR/LR/ER, -LRM, 40GBASE-KR4/CR4/SR4/LR4, 100GBASE-CR10/SR10): 1 UI = 96.97 ps
10G (10GBASE-SW/LW/EW): 1 UI = 100.47 ps
25G (25GBASE-SR, -LR, -ER, 100GBASE-LR4/ER4): 1 UI = 38.79 ps

NOTE 6 – The peak-to-peak jitter amplitude for 25G lanes is increased from 0.5 UI to 1.2 UI, i.e., by a factor of 2.4. To compensate for this increase, the high-pass corner frequency used for 10G should first be increased by a factor of 2.5 to take account of the increase in line rate from 10G, and then decreased by a factor of 2.4 to take account of the increase in amplitude. This gives a high-pass corner frequency of 20.833 kHz, which has been rounded down to 20 kHz for convenience; this rounding to a lower value is slightly stricter.

8.3.2 Output jitter at 2048 kHz, 2048 kbit/s, 1544 kbit/s and STM-N interfaces

Jitter generation for the 2048 kHz and 2048 kbit/s interface, and for the synchronous transport module-N (STM-N) interface are defined for Option 1 in clause 7.3 of [ITU-T G.813].

Jitter generation for the 1544 kbit/s interface and for the STM-N interfaces are defined for Option 2 in clause 7.3 of [ITU-T G.813].

8.3.3 OTN equipment clock (OEC) jitter generation

Jitter generation for the synchronous OTN interface is defined in clause A.5.1 of [ITU-T G.8251].

9 Noise tolerance

The noise tolerance of an equipment clock indicates the minimum phase noise level at the input of the clock that should be accommodated whilst:

– not causing any alarms;

– not causing the clock to switch reference;

– not causing the clock to go into holdover.

NOTE – There are no output noise requirements in terms of noise tolerance. The relevant specifications are noise generation and noise transfer.

In general, the noise tolerance of the equipment clock is the same as the network limit for the synchronization interface in order to maintain acceptable performance. However, the synchronization interface network limit may be different according to the application. Therefore, in order to determine the equipment clock noise tolerance, the worst-case network limit should be used. An explanation of the different network limits is given in Appendix I of [ITU-T G.813].

The wander and jitter tolerances given in clauses 9.1 and 9.2 represent the worst levels that a synchronization carrying interface should exhibit. The TDEV signal used for a conformance test should be generated by adding white Gaussian noise sources of which each has been filtered to obtain the proper type of noise process with the proper amplitude.

MTIE and TDEV are measured through an equivalent 10-Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 seconds. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\tau$).

9.1 Wander tolerance

9.1.1 Option 1

The input wander tolerance expressed in MTIE and TDEV limits is given in Tables 7 and 8, respectively.

Table 7 – Input wander tolerance (MTIE) for Option 1

MTIE limit [µs]	Observation interval τ [s]
0.25	$0.1 < \tau \leq 2.5$
0.1 τ	$2.5 < \tau \leq 20$
2	$20 < \tau \leq 400$
0.005 τ	$400 < \tau \leq 1000$

Table 8 – Input wander tolerance (TDEV) for Option 1

TDEV limit [ns]	Observation interval τ [s]
12	$0.1 < \tau \leq 7$
1.7 τ	$7 < \tau \leq 100$
170	$100 < \tau \leq 1000$

The resultant requirements are shown in Figures 5 and 6.

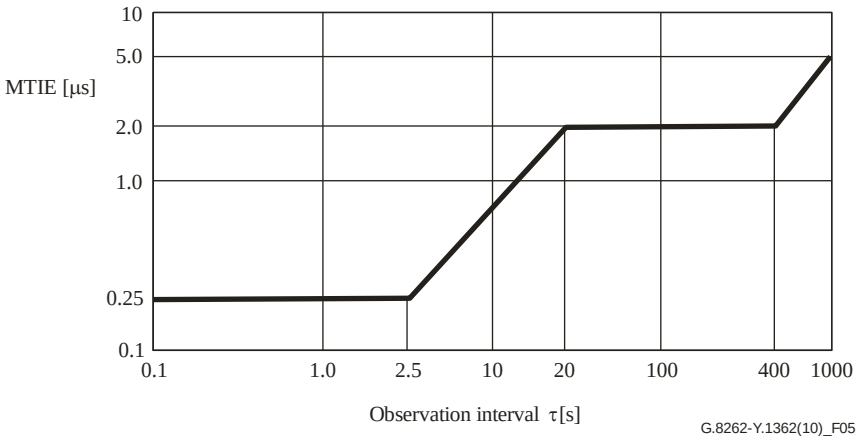

Figure 5 – Input wander tolerance (MTIE) for Option 1

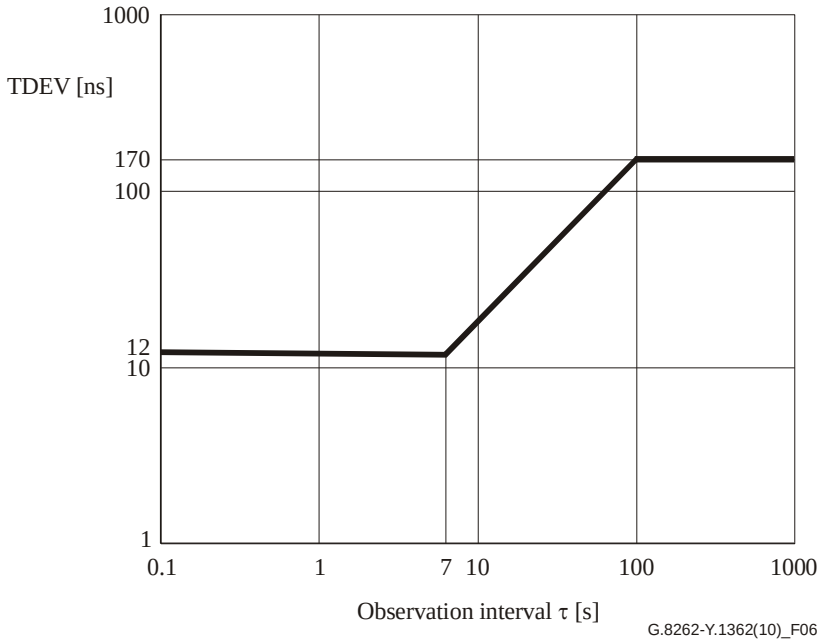

Figure 6 – Input wander tolerance (TDEV) for Option 1

Suitable test signals that check conformance to the mask in Figure 6 are being studied. Test signals with a sinusoidal phase variation can be used, according to the levels in Table 9, to check conformance to the mask in Figure 5.

Table 9 – Lower limit of maximum tolerable sinusoidal input wander for Option 1

Peak-to-peak wander amplitude			**Wander frequency**				
A_1 [µs]	A_2 [µs]	A_3 [µs]	f_4 [mHz]	f_3 [mHz]	f_2 [mHz]	f_1 [Hz]	f_0 [Hz]
0.25	2	5	0.32	0.8	16	0.13	10

The resultant requirements are shown in Figure 7.

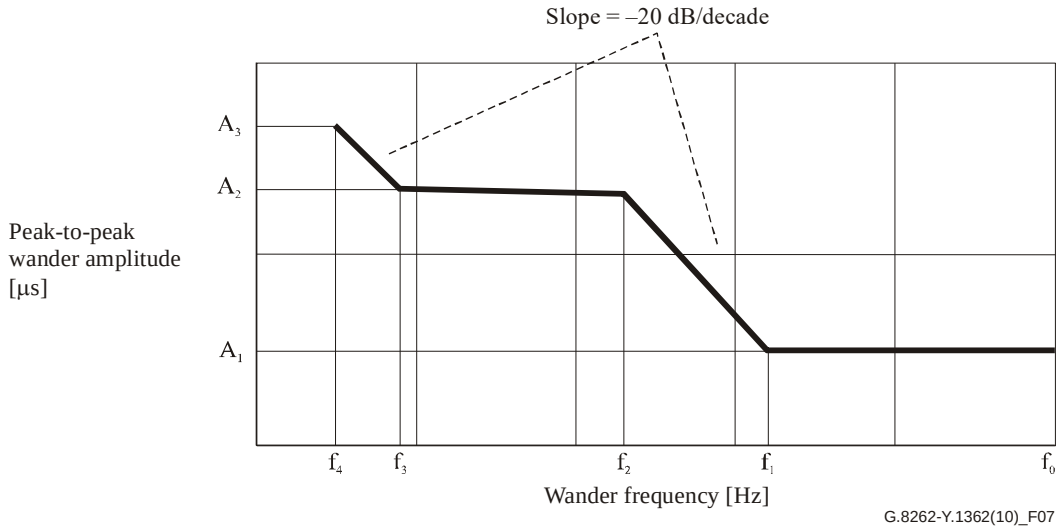

Figure 7 – Lower limit of maximum tolerable sinusoidal input wander for Option 1

9.1.2 Option 2

The input wander tolerance expressed in TDEV is specified in Table 10.

Table 10 – Input wander tolerance (TDEV) for Option 2

TDEV limit [ns]	Observation interval τ [s]
17	$0.1 < \tau \leq 3$
$5.77\ \tau$	$3 < \tau \leq 30$
$31.6325\ \tau^{0.5}$	$30 < \tau \leq 1000$

The resultant requirement is shown in Figure 8. A requirement expressed in MTIE is not defined.

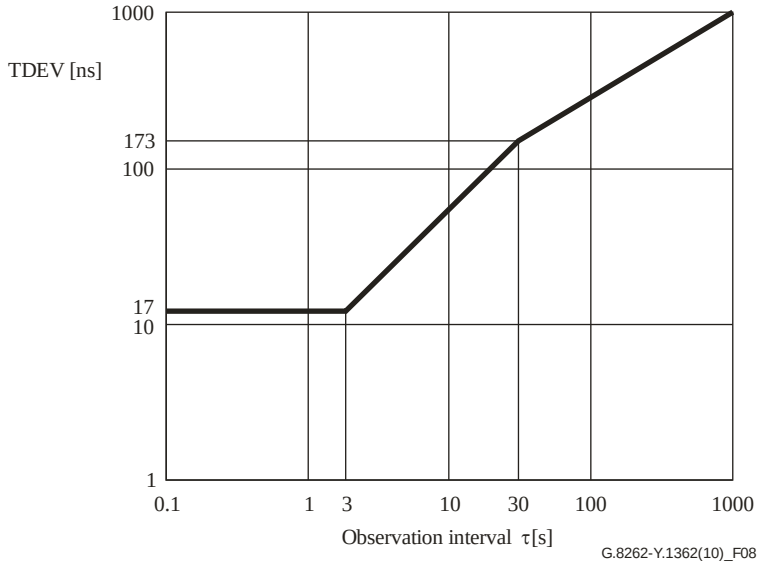

Figure 8 – Input wander tolerance (TDEV) for Option 2

9.2 Jitter tolerance

This clause defines the jitter tolerance for Option 1 EEC, Option 2 EEC and the OEC.

9.2.1 Jitter tolerance for EEC

Jitter tolerance at a synchronous Ethernet interface:

The lower limit of maximum tolerable input jitter for 1G Ethernet interfaces for Option 1 EEC and Option 2 EEC is given in Table 11 and Figure 9.

Table 11 – 1G synchronous Ethernet wideband jitter tolerance for Option 1 EEC and Option 2 EEC

Peak-peak jitter amplitude (UI)	Frequency f (Hz)
312.5	$10 < f \leq 12.1$
$3750\ f^{-1}$	$12.1 < f \leq 2.5$ k
1.5	2.5 k $< f \leq 50$ k
NOTE – 1G includes 1000BASE-KX, -SX, -LX; multi-lane interfaces are for further study.	

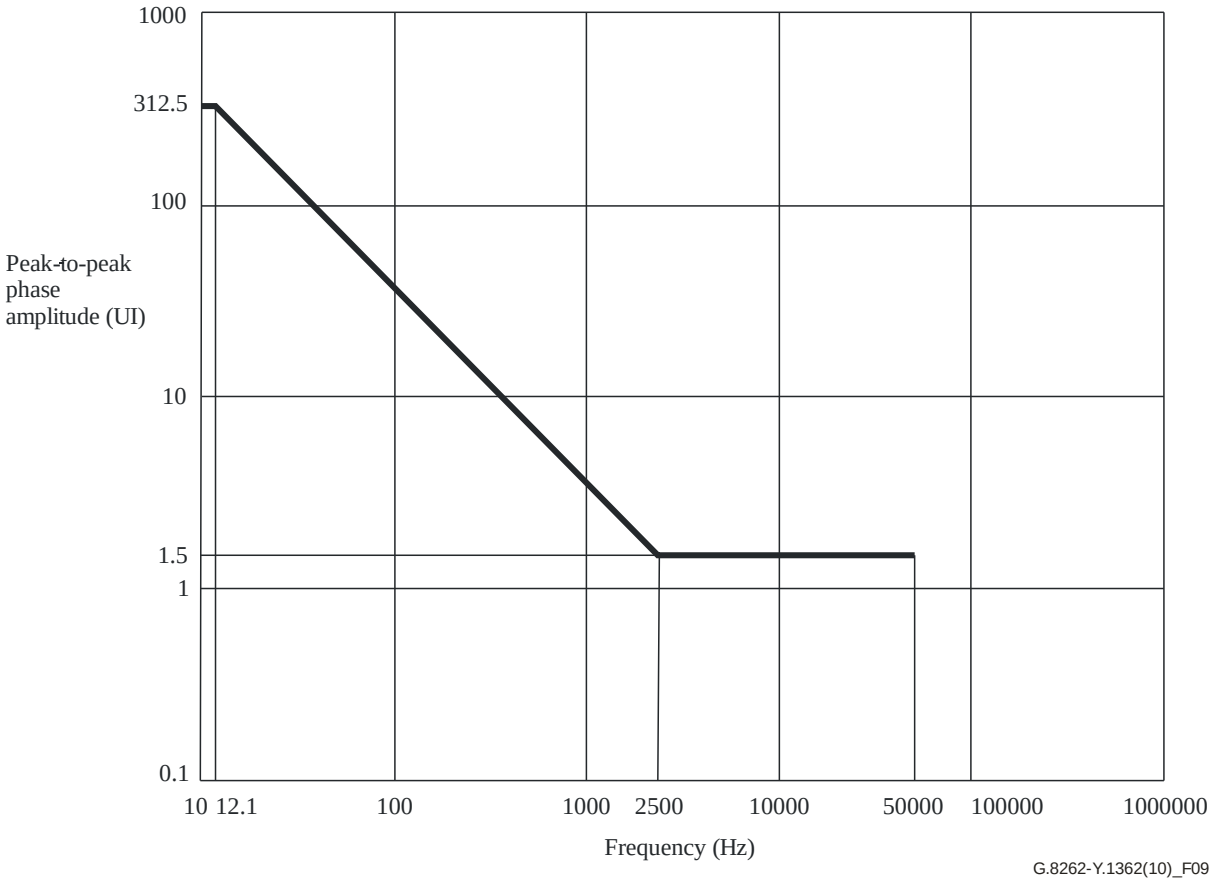

Figure 9 – 1G synchronous Ethernet wideband jitter tolerance for Option 1 EEC and Option 2 EEC

NOTE 1 – The relevant IEEE 802.3 jitter tolerance requirements shall be met in addition to the specific synchronous Ethernet wideband jitter tolerance requirements.

NOTE 2 – For testing purposes, high frequency jitter tolerance and test signal generation for Ethernet traffic interfaces above 637 kHz are specified by [IEEE 802.3].

NOTE 3 – The slope above 50 kHz is 20 dB/decade. The actual values between 50 kHz and 637 kHz are for further study as the measurement methods between [IEEE 802.3] and ITU-T are not fully comparable. Information on the ITU jitter specification can be found in Appendix I of [ITU-T G.825].

The lower limit of maximum tolerable input jitter for 10G Ethernet interfaces for Option 1 EEC and Option 2 EEC is given in Table 12 and Figure 10.

Table 12 – 10G synchronous Ethernet wide-band jitter tolerance for Option 1 EEC and Option 2 EEC

Peak-peak jitter amplitude (UI)	Frequency f (Hz)
2488	$10 < f \leq 12.1$
$30000\ f^{-1}$	$12.1 < f \leq 20$ k
1.5	20 k $< f \leq 40$ k
NOTE – 10G includes 10GBASE-SR/LR/ER, 10GBASE-LRM, 10GBASE-SW/LW/EW and multi-lane interfaces consisting of 10G lanes including 40GBASE-KR4/CR4/SR4/LR4 and 100GBASE-CR10/SR10.	

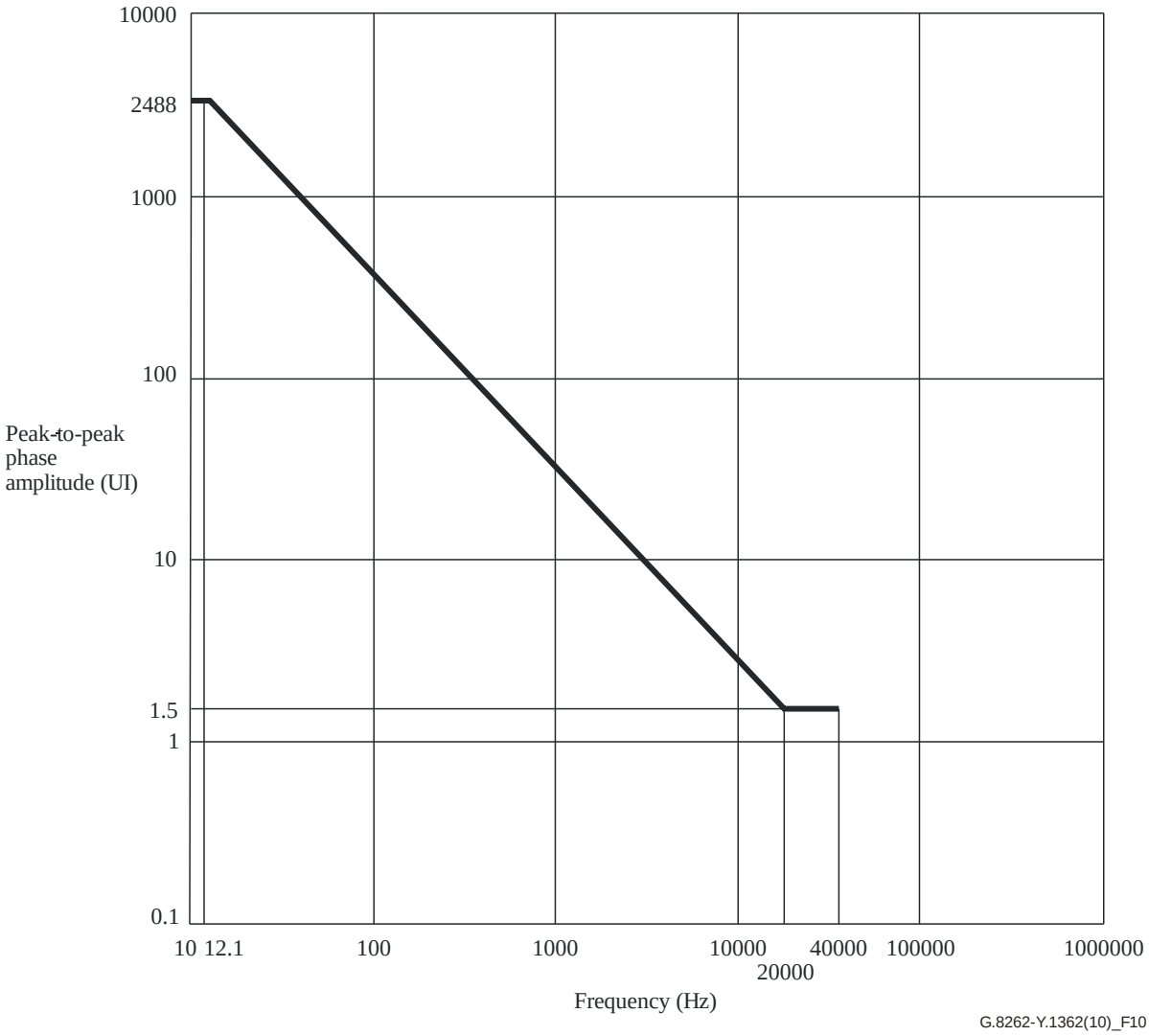

Figure 10 – 10G synchronous Ethernet wide-band jitter tolerance for Option 1 EEC and Option 2 EEC

NOTE 4 – The relevant [IEEE 802.3] jitter tolerance requirements shall be met in addition to the specific synchronous Ethernet wideband and jitter tolerance requirements.

NOTE 5 – The measurements methods between [IEEE 802.3] and ITU-T are not fully comparable. Information on the ITU jitter specification can be found in Appendix I of [ITU-T G.825].

The lower limit of maximum tolerable input jitter for 25G Ethernet interfaces for Option 1 EEC and Option 2 EEC is given in Table 13.

Table 13 – 25G synchronous Ethernet wide-band jitter tolerance for Option 1 EEC and Option 2 EEC

Peak-peak jitter amplitude (UI)	Frequency f (Hz)
6445	$10 < f \leq 11.17$
$72000f^{-1}$	$11.17 < f \leq 20$ k
3.6	20 k < f ≤ 100 k
NOTE – 25G includes 25GBASE-SR, 25GBASE-LR, 25GBASE-ER, and multi-lane interfaces consisting of 25G lanes including 100GBASE-LR4/ER4.	

The jitter specification for 50G, 100G (PAM4), and 200G interfaces is for further study.

9.2.2 Jitter tolerance at 2048 kHz, 2048 kbit/s, 1544 kbit/s and STM-N interfaces

The lower limit of maximum tolerable input jitter for 2048 kHz and 2048 kbit/s signals is defined for Option 1 in clause 8.2 of [ITU-T G.813].

The lower limit of maximum tolerable jitter for external 1544 kbit/s synchronization is defined for Option 2 in clause 8.2 of [ITU-T G.813].

The lower limit of maximum tolerable input jitter for STM-N interfaces is defined in [ITU-T G.825].

9.2.3 Jitter tolerance for OEC

Jitter tolerance for the synchronous OTN interface is defined in clause 6 of [ITU-T G.8251].

10 Noise transfer

The transfer characteristic of the equipment clock determines its properties with regard to the transfer of excursions of the input phase relative to the carrier phase. The equipment clock can be viewed as a low-pass filter for the differences between the actual input phase and the ideal input phase of the reference. The minimum and the maximum allowed bandwidths for this low-pass filter behaviour are based on the considerations described in Appendix II of [ITU-T G.813] and are indicated below.

In the passband, the phase gain of the equipment clock should be smaller than 0.2 dB (2.3%). The above applies to a linear equipment clock model. However, this model should not restrict implementation.

10.1 Option 1

The minimum bandwidth requirement for an Option 1 equipment clock is 1 Hz. The maximum bandwidth requirement for an Option 1 equipment clock is 10 Hz.

10.2 Option 2

Synchronous Ethernet, synchronous OTN, or SDH NEs, when referenced to a synchronous Ethernet, synchronous OTN, or STM-N timing signal that meets the input TDEV mask in Figure 8 and Table 10, shall output signals that meet the output TDEV limits in Table 14.

Table 14 – Wander transfer for Option 2 (maximum output wander when input wander meets Table 10)

TDEV limit [ns]	Observation interval τ [s]
10.2	$0.1 < \tau \leq 1.73$
$5.88\ \tau$	$1.73 < \tau \leq 30$
$32.26\ \tau^{0.5}$	$30 < \tau \leq 1000$

The resultant requirement is shown in the mask of Figure 11. The purpose of these masks is to ensure that the maximum bandwidth of an Option 2 equipment clock is 0.1 Hz. These masks should not be used to verify phase gain peaking. There is no requirement for a minimum bandwidth.

TDEV is measured through an equivalent 10-Hz, first-order, low-pass measurement filter at a maximum sampling time τ_0 of 1/30 seconds. The minimum measurement period for TDEV is twelve times the integration period ($T = 12\tau$).

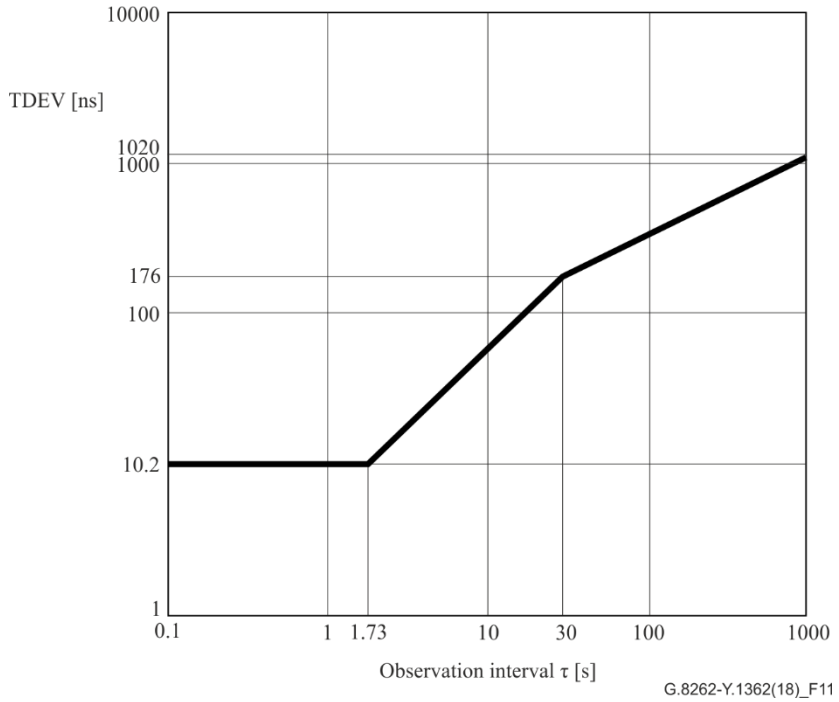

Figure 11 – Wander transfer for Option 2 (maximum output wander when input wander meets Figure 8)

NOTE – The values of this transfer mask are 2% higher than the mask found in Figure 8 in the passband.

The masks in Figures 8 and 11 are used to verify wander tolerance and measure TDEV transfer respectively; they do not represent the network wander limit needed to be met for the payload wander accumulation requirement. In practice, this will not cause loss of synchronization at an equipment clock, as the network wander tolerance limit in Figure 11 is within the pass band of the Option 2 equipment clock. However, it will cause higher wander accumulation.

11 Transient response and holdover performance

The requirements in this clause apply to situations where the input signal is affected by disturbances or transmission failures (e.g., short interruptions, switching between different synchronization signals, loss of reference, etc.) that result in phase transients at the equipment clock output. The ability to withstand disturbances is necessary to avoid transmission defects or failures. Transmission failures and disturbances are common stress conditions in the transmission environment.

It is recommended that all the phase movements at the output of the equipment clock stay within the levels described in the following clauses.

Measurements of MTIE for Option 2 clocks are carried out through an equivalent 100-Hz, first-order, low-pass measurement filter.

11.1 Short-term phase transient response

11.1.1 Option 1

This requirement reflects the performance of the clock in cases when the (selected) input reference is lost due to a failure in the reference path and a second reference input signal, traceable to the same reference clock, is available simultaneously, or shortly after the detection of the failure (e.g., in cases of autonomous restoration). In such cases, the reference is lost for at most 15 seconds. The output phase variation, relative to the input reference before it was lost, is bounded by the following requirements:

The phase error should not exceed $\Delta t + 5 \times 10^{-8} \times S$ seconds over any period S up to 15 seconds. Δt represents two phase jumps that may occur during the transition into and out of the holdover state which both should not exceed 120 ns with a temporary frequency offset of no more than 7.5 ppm.

The resultant overall requirement is summarized in Figure 12. This figure is intended to depict the worst-case phase movement attributable to an equipment clock reference clock switch. Clocks may change state more quickly than is shown here. Background information on the requirements that drove this requirement is provided in Appendix II of [ITU-T G.813].

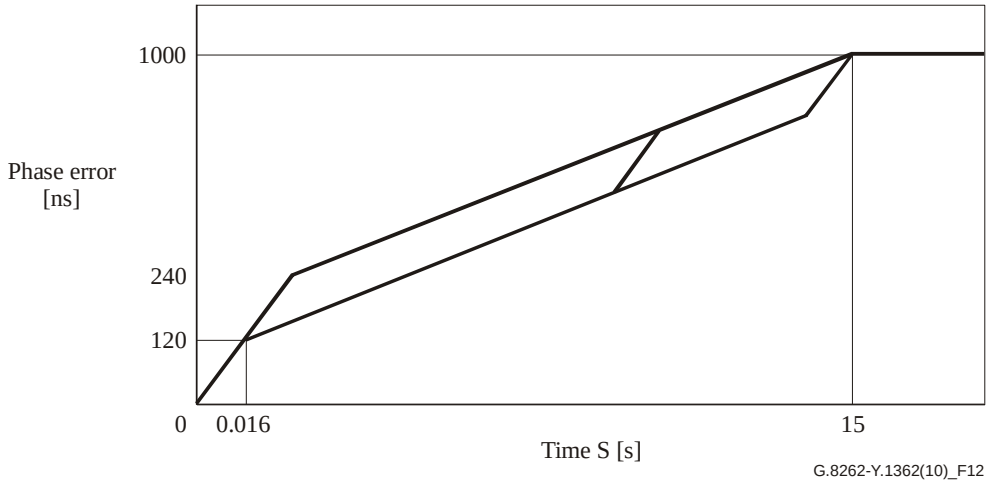

Figure 12 – Maximum phase transient at the output due to reference switching for Option 1

Figure 12 shows two phase jumps in the clock switching transient. The first jump reflects the initial response to a loss of the synchronization reference source and subsequent entry into holdover. The magnitude of this jump corresponds to a frequency offset less than 7.5 ppm for a duration less than 16 ms. After 16 ms, the phase movement is restricted to lie underneath the line with a slope of 5×10^{-8} in order to constrain pointer activity. The second jump, which is to take place within 15 seconds after entering holdover, accounts for the switching to the secondary reference. The same requirements are applicable for this jump. After the second jump, the phase error should remain constant and smaller than 1 µs.

NOTE – The output phase excursion, when switching between references which are not traceable to the same primary reference clock (PRC), is for further study.

In cases where the input synchronization signal is lost for more than 15 seconds, the requirements in clause 11.2 apply.

11.1.2 Option 2

During clock rearrangement operations (e.g., reference switching), the output of the clock should meet the MTIE requirement as defined in clause 11.4.2.

11.2 Long-term phase transient response (holdover)

This requirement bounds the maximum excursions in the output timing signal. Additionally, it restricts the accumulation of the phase movement during input signal impairments or internal disturbances.

11.2.1 Option 1

When an equipment clock loses all its references, it enters the holdover state. The phase error, ΔT, at the output of the equipment clock relative to the input at the moment of loss of reference should, over any period $S > 15$ s, meet the following:

$$\left|\Delta T(S)\right| \le \left\{(a_1 + a_2)S + 0.5bS^2 + c\right\} \quad \text{[ns]}$$

where:

a_1 = 50 ns/s (see Note 1)

a_2 = 2000 ns/s (see Note 2)

b = 1.16×10^{-4} ns/s^2 (see Note 3)

c = 120 ns (see Note 4)

This limit is subject to a maximum frequency offset of ±4.6 ppm. The behaviour for $S < 15$ s is defined in clause 11.1.

NOTE 1 – The frequency offset a_1 represents an initial frequency offset corresponding to 5×10^{-8} (0.05 ppm).

NOTE 2 – The frequency offset a_2 accounts for temperature variations after the clock went into holdover and corresponds to 2×10^{-6} (2 ppm). If there are no temperature variations, the term a_2S should not contribute to the phase error.

NOTE 3 – The drift b is caused by ageing: 1.16×10^{-4} ns/s^2 corresponds to a frequency drift of 1×10^{-8}/day (0.01 ppm/day). This value is derived from typical ageing characteristics after ten days of continuous operation. It is not intended to measure this value on a per day basis, as the temperature effect will dominate.

NOTE 4 – The phase offset c takes care of any additional phase shift that may arise during the transition at the entry of the holdover state.

The resultant overall requirement for constant temperature (i.e., when the temperature effect is negligible) is summarized in Figure 13.

$$\left|\Delta T(S)\right| \le \left(a_1 S + \frac{b}{2}S^2 + c\right) \quad \text{[ns]}$$

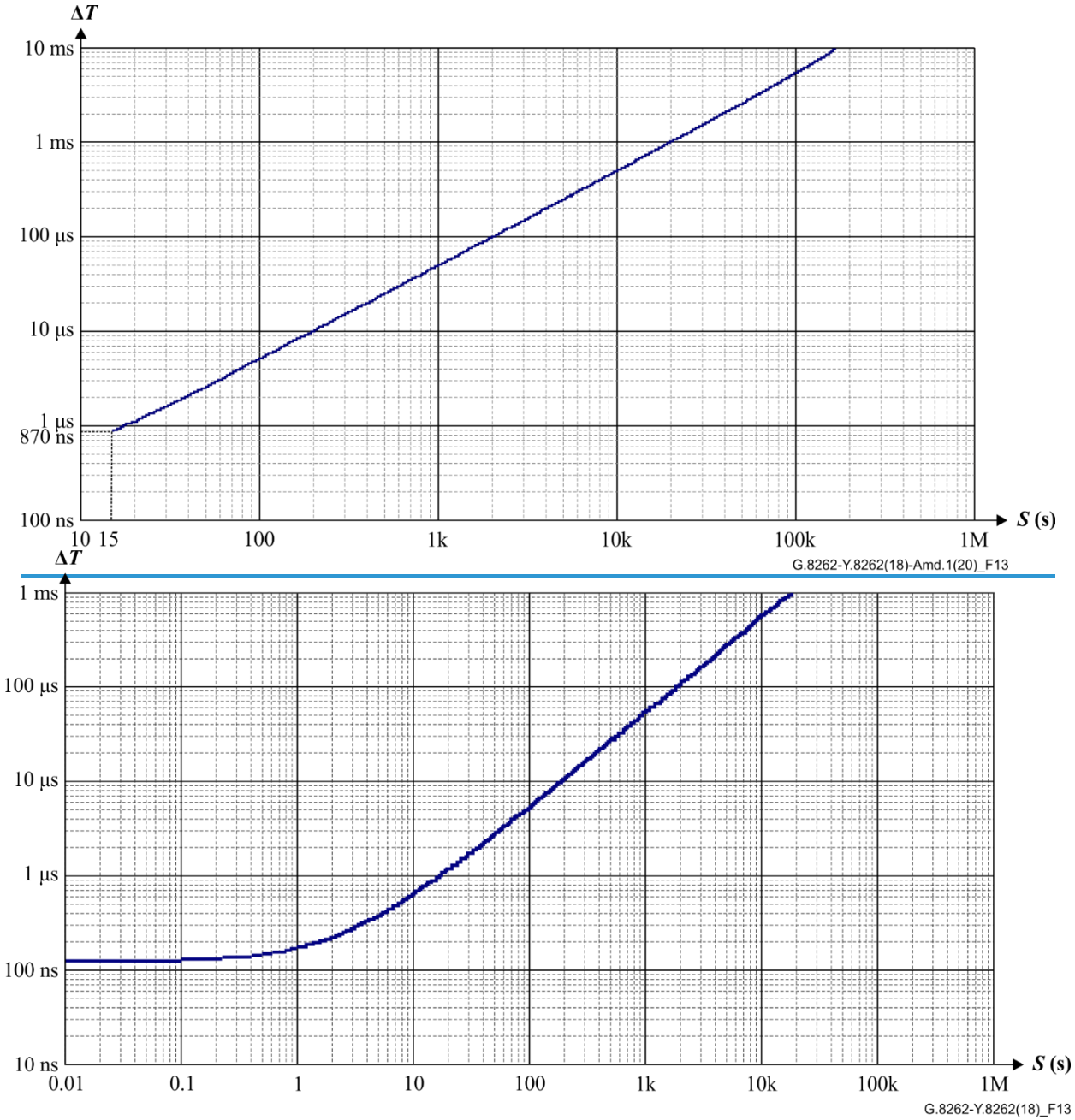

Figure 13 – Permissible phase error for an Option 1 under holdover operation at constant temperature

11.2.2 Option 2

When an equipment clock clock loses all its references, it enters the holdover state. The phase error, ΔT, at the output of the slave clock from the moment of loss of reference, should, over any period of S seconds, meet the following:

$$\left|\Delta T(S)\right| \le \left\{(a_1 + a_2)S + 0.5bS^2 + c\right\} \quad \text{[ns]}$$

The derivative of $\Delta T(S)$, the fractional frequency offset, should, over any period of S seconds, meet the following:

$$\left|d\left(\Delta T(S)\right)/dS\right| \le \left\{a_1 + a_2 + bS\right\} \quad \text{[ns/s]}$$

The second derivative of $\Delta T(S)$, the fractional frequency drift, should, over any period of S seconds, meet the following:

$$\left| d^2\left(\Delta T(S)\right)/dS^2 \right| \le d \quad \left[\text{ns/s}^2\right]$$

In applying the above requirements for the derivative of $\Delta T(S)$ and the second derivative of $\Delta T(S)$, the period S must begin after any transient associated with entry into holdover is over. During this transient period, the transient requirements of clause 11.4.2 apply.

NOTE 1 – a_1 represents an initial frequency offset under constant temperature conditions (±1 K).

NOTE 2 – a_2 accounts for temperature variations after the clock went into holdover. If there are no temperature variations, the term $a_2 S$ should not contribute to the phase error.

NOTE 3 – b represents the average frequency drift caused by aging. This value is derived from typical aging characteristics after 60 days of continuous operation. It is not intended to measure this value on a per day basis, as the temperature effect will dominate.

NOTE 4 – The phase offset c takes care of any additional phase shift that may arise during the transition at the entry of the holdover state.

NOTE 5 – d represents the maximum temporary frequency drift rate at constant temperature allowed during holdover. However, it is not required that d and b be equal. Note that for some time periods, especially for short periods, this parameter may be difficult to test and the measured value may not be meaningful.

The permissible phase error specification for Option 2 equipment clock is shown in Table 15.

Table 15 – Transient response specification during holdover

	Option 2
Applies for	***S* > TBD**
a_1 [ns/s]	50
a_2 [ns/s]	300
b [ns/s^2]	4.63×10^{-4}
c [ns]	1000
d [ns/s^2]	4.63×10^{-4}
TBD: To be defined.	

11.3 Phase response to input signal interruptions

An interruption to the input signal may last for different durations of time. A short-term interruption is a short period of time when the input signal is not available.

NOTE 1 – If the input signal experiences a short-term interruption, the clock may take action such as entering holdover until the input signal is restored, or selecting another input source, or other implementation specific behaviour.

NOTE 2 – The characteristics of a short-term interruption that would cause the equipment clock to take different courses of action, and that are not already covered in this Recommendation, should be considered implementation specific. These characteristics may include length of interruption or magnitude of phase change on the input signal before and after the interruption.

11.3.1 Option 1

For short-term interruptions on synchronization input signals that do not cause reference switching, the output phase variation should not exceed 120 ns, with a maximum frequency offset of 7.5 ppm for a maximum period of 16 ms.

11.3.2 Option 2

This is for further study.

11.4 Phase discontinuity

11.4.1 Option 1

NOTE – Infrequent internal testing or other internal disturbances could refer, for instance, to equipment protection switching between two internal clock cards within the synchronous Ethernet equipment clock (excluding major hardware failures) or maintenance activity.

In cases of infrequent internal testing or other internal disturbances (but excluding major hardware failures, e.g., those that would give rise to clock equipment protection switches) within the equipment clock, the following conditions should be met:

– The phase variation over any period *S* (ms) up to 16 ms should not exceed 7.5*S* ns;

– The phase variation over any period *S* (ms) from 16 ms up to 2.4 s should not exceed 120 ns;

– For periods greater than 2.4 s, the phase variation for each interval of 2.4 s should not exceed 120 ns with a temporary offset of no more than 7.5 ppm up to a total amount of 1 µs.

11.4.2 Option 2

In cases of infrequent internal testing or rearrangement operations within the slave clock, the phase transient at the output of Option 2 should meet the MTIE specifications as specified in Table 16.

Table 16 – MTIE at the output due to reference switching/rearrangement operations for Option 2

MTIE limit [ns]	Observation interval τ [s]
Not specified	$\tau \leq 0.014$
$7.6 + 885\ \tau$	$0.014 < \tau \leq 0.5$
$300 + 300\ \tau$	$0.5 < \tau \leq 2.33$
1000	$2.33 < \tau$

This MTIE requirement is illustrated in Figure 14.

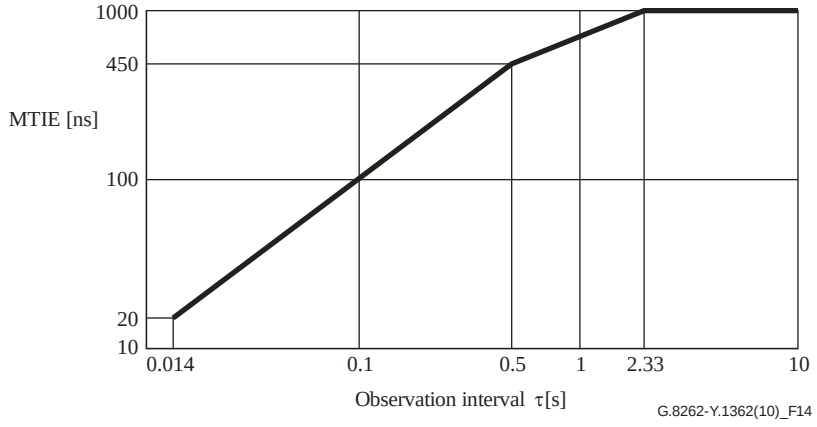

Figure 14 – MTIE at the output due to reference switching/rearrangement operations for Option 2

12 Interfaces

The requirements in this Recommendation are related to reference points internal to the network elements (NEs) in which the clock is embedded and are, therefore, not necessarily available for

measurement or analysis by the user. Therefore, the performance of the equipment clock is not defined at these internal reference points, but rather at the external interfaces of the equipment.

The synchronization input and output interfaces for equipment in which the equipment clock may be contained are:

– 1544 kbit/s interfaces according to [ITU-T G.703];
– 2048 kHz external interfaces according to [ITU-T G.703];
– 2048 kbit/s interfaces according to [ITU-T G.703];
– STM-N traffic interfaces (for hybrid NEs);
– 64 kHz interface according to [ITU-T G.703];
– 6312 kHz external interfaces according to [ITU-T G.703];
– Synchronous Ethernet interfaces;
– Synchronous OTN interfaces.

All of the above interfaces may not be implemented on all equipments. These interfaces should comply with the jitter and wander requirements as defined in this Recommendation.

Ethernet copper interfaces allow half-duplex mode and collisions on a line which could squelch the signals and destroy the timing; therefore synchronous Ethernet interfaces must work only in full-duplex and have a continuous bit stream.

NOTE – To support interoperability with existing network equipments, interfaces to and from external network clocks may optionally support synchronization message channel (SSM).

Appendix I

Hybrid network elements using STM-N and Ethernet (ETY) interfaces

(This appendix does not form an integral part of this Recommendation.)

The EEC clocks may support the use of hybrid network elements (NEs) at any place in a synchronization chain as shown in Appendix XII of [ITU-T G.8261]. Figure I.1 illustrates a hybrid NE and timing relations between the equipment clock (EC) and STM-N and ETY interfaces.

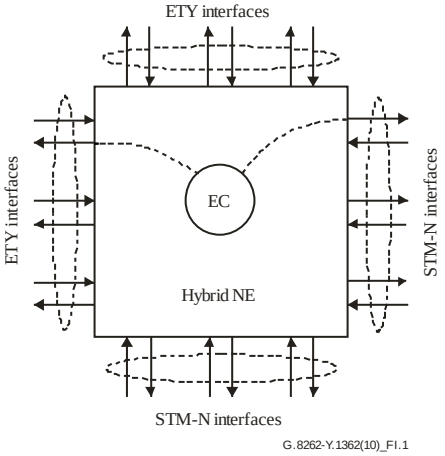

Figure I.1 – Hybrid NE using STM-N and Ethernet (ETY) interfaces

For hybrid NEs, timing transfer may be supported from any type of input interface to any type of output interface as shown in Table I.1.

Table I.1 – Combination of input and output ports for timing distribution

Timing input	Timing output
STM-N	STM-N
STM-N	ETY
STM-N	T4
ETY	STM-N
ETY	ETY
ETY	T4
T3	STM-N
T3	ETY

The use of ETY interfaces for timing distribution and the use of hybrid NEs should not require modifications of deployed SDH NEs or clocks (PRC, SSU), e.g., no new SSM code point for STM-N interfaces. Code point "0000" should also not be used.

Appendix II

Relationship between requirements contained in this Recommendation and other key synchronization-related Recommendations

(This appendix does not form an integral part of this Recommendation.)

This appendix describes the relationship between the clock performance requirements contained within the body of this Recommendation and the key synchronization Recommendations that are under development, or have been developed within Question 13 (Network synchronization and time distribution performance) of ITU-T Study Group 15.

This Recommendation describes performance requirements for synchronous equipment clocks. This Recommendation addresses synchronous Ethernet and synchronous OTN clocks.

The basic concept of synchronous Ethernet is described in [ITU-T G.8261], the first ITU-T Recommendation to detail network synchronization aspects applicable to packet-based networks.

If a clock described in this Recommendation is embedded in an Ethernet network element, it allows transfer of network traceable timing via the Ethernet physical layer. In this context, the Ethernet physical layer is defined by [IEEE 802.3]. If a clock described in this Recommendation is embedded in an OTN network element, it allows transfer of network traceable timing via the OTN physical layer. In this context, the OTN physical layer is defined by [ITU-T G.709].

The performance requirements in this Recommendation are derived from existing Recommendations. Option 1 requirements are based on the [ITU-T G.813] Option 1 clock, and Option 2 requirements are based on the Type IV clock [ITU-T G.812] as deployed in an SDH NE.

Both Option 1 and Option 2 clocks offer similar performance, but are intended for use in the networks optimized for either the 2048 kbit/s hierarchy (for Option 1) or for the 1544 kbit/s hierarchy (for Option 2). As the equipment clocks are consistent with existing SDH network element clocks used in the distribution of frequency, synchronization network engineering will not require any change to current network engineering practices.

Synchronization networks in general are based on SDH synchronization distribution as described in [ITU-T G.803]. Synchronization distribution may follow specific regional practices in order to meet the fundamental performance requirements and network interface limits from either [b-ITU-T G.823] or [b-ITU-T G.824] for the 2048 kbit/s or 1544 kbit/s hierarchy, respectively. Both [b-ITU-T G.823] and [b-ITU-T G.824] are based on the fundamental slip rate objectives in [b-ITU-T G.822].

The equipment clocks are purposely specified to perform in a manner consistent with existing synchronization networks. The Option 1 can be deployed within the synchronization distribution network in exactly the same manner as a [ITU-T G.813] SDH Equipment Clock, while the Option 2 clock can be deployed as per existing [ITU-T G.812] Type IV clocks.

Appendix III

List of Ethernet interfaces applicable to synchronous Ethernet

(This appendix does not form an integral part of this Recommendation.)

A list of all Ethernet interfaces listed in [IEEE 802.3] is provided in Table III.1. It specifies the Ethernet interfaces which are valid for synchronous Ethernet operation. Other interfaces may exist; the list of interfaces is not exhaustive and might be updated.

The following considerations have been taken into consideration for the generation of this list.

CSMA/CD

[IEEE 802.3] specifies two operating modes: half-duplex and full-duplex modes.

The original Ethernet interfaces were developed for a single medium that was shared between multiple end stations using the carrier sense multiple access with collision detection (CSMA/CD) mechanism. Most interfaces use separate media (or separate carriers) for bidirectional communication between two end-stations. The use of half-duplex operation on such bidirectional, point-to-point media serves to mimic the behaviour of legacy shared media operation. In all cases, there is no difference in PHY behaviour between half-duplex and full-duplex modes. The half-duplex functionality is controlled by the media access control (MAC) sublayer and only affects packet transport at layer 2 and above.

Interfaces titled CSMA/CD may be used for the purposes of synchronous Ethernet in all cases where the media is point-to-point.

Constant signal

The interface must permanently transport a signal.

This signal must be coded so that there is a guarantee of transitions so that the clock can be recovered. This is achieved by the 64B/66B encoding in some 10G interfaces; DSQ-128 (2 x 2 pair, PAM-16) signalling for 10G over twisted pair copper; 8B/10B encoding in some 1G interfaces and 10G over 4 channels of fibre or copper; 4D-PAM-5 encoding for 1G over twisted pair copper interfaces; 4B/5B encoding for some 100M interfaces; and MLT-3 for 100M over twisted pair copper interfaces.

All IEEE 802.3 point-to-point physical layers (PHYs) that operate at speed of 100 Mbit/s or greater use constant signalling.

Master/slave

Some bidirectional interfaces are designed to have one side, designated as the clock master, acting as the clock generator, the other side as the slave, which is forced to recover the clock.

Such a configuration will only support unidirectional synchronous Ethernet. Such conditions can be announced under supervision of the Ethernet synchronization message channel (ESMC) process, as defined in [ITU-T G.8264] where synchronous Ethernet reduced interfaces are introduced. For such interfaces, the master/slave resolution should be forced by station management as defined by the appropriate clause in [IEEE 802.3], in accordance with the synchronization network architecture. ESMC reduced interface status should be synchronized with master/slave status.

Two examples of master/slave clock operation are 1000BASE-T and 10GBASE-T.

Auto-negotiation

The auto-negotiation mechanism defined for some sets of physical (layer) (PHY)s is used to find the highest mutually supported mode of operation for two partners at link start-up time. The algorithm will always favour a higher speed compared to a lower speed and full-duplex to half-duplex. Because the negotiation happens at link start-up, it should be compatible with synchronous Ethernet but may not be compatible with the synchronization distribution plan. Note that the negotiation is an option for some PHY types and the supported PHY speed and duplex may be forced by the management.

Note that there are some cases where auto-negotiation could appear during operation, e.g., during an upgrade. Auto-negotiation must not have any impact on the rates and the clocks to be compatible with synchronous Ethernet.

Physical loopback

All physical loopback functionalities specified on full-duplex links that interrupt the link for test/check "in-service" are not compatible with synchronous Ethernet. Thus, they should be only allowed during the link set-up.

Point-to-multipoint

Some PHY interfaces are designed for point-to-multipoint operation over passive optical networks. Such links use intermittent signalling for the upstream direction but may be suitable for unidirectional synchronous Ethernet.

Removable transceivers

Many different physical interfaces are provided using removable Ethernet transceivers such as 1G SFP, 10G SFP+ and 100G CFPs. While the PHY technology of the interface may support synchronous Ethernet as indicated within this appendix, there are specific requirements on the removable transceiver and the equipment host for successful operation.

On the assumption that the removable transceiver does not operate as an EEC (e.g., applicable low-pass filter, ESMC processing, etc.) then the removable transceiver and matching equipment host need to support transfer of timing in both directions across the transceiver.

For example, most removable transceivers providing 1000BASE-T do not support the transfer of timing to the host system. It is necessary to check the capabilities of the specific removable transceiver in use, in combination with the host equipment, to ensure that synchronous Ethernet is supported.

Miscellaneous

Some of the older PHY types are rarely used and need not be considered, for example two PHY types are defined for use over digital subscriber line (DSL).

Implementation issues

Some interfaces transmit signals over parallel cables or fibres. These interfaces use one clock source for all physical lanes, but the recovered clock (and reference point for timestamping) may vary depending on the definition of multi-lane operation. It is not clear at this point whether further definition will be required for the operation of synchronous Ethernet over these interfaces.

Based on the above considerations, Table III.1 lists the PHY interfaces specified by [IEEE 802.3] and designates which ones may be considered for synchronous Ethernet compatibility, which should not be considered, and which may be unidirectional only.

Table III.1 – List of Ethernet interfaces eligible to synchronous Ethernet

PHY	Description	[IEEE 802.3] clause	Coding	Synchronous Ethernet capable
10BASE2	10 Mbit/s coaxial	10	Manchester, intermittent	No
10BASE5	*10 Mbit/s coaxial*	*8*	*Manchester, intermittent*	*No (Note 1)*
10BASE-F	10 Mbit/s fibre	15	NRZ, intermittent	No
10BASE-FP	*10 Mbit/s fibre, star*	*16*	*NRZ, intermittent*	*No (Note 1)*
10BASE-T	10 Mbit/s TP copper	14	Manchester, intermittent	No
100BASE-BX10	100 Mbit/s bidi fibre	58, 66	4B/5B	Yes
100BASE-FX	100 Mbit/s fibre	24, 26	4B/5B	Yes
100BASE-LX10	100 Mbit/s fibre	58, 66	4B/5B	Yes
100BASE-T2	*100 Mbit/s TP copper*	*32*	*PAM-5*	*No (Note 1)*
100BASE-T4	*100 Mbit/s TP copper*	*23*	*8B6T*	*No (Note 1)*
100BASE-TX	100 Mbit/s TP copper	24, 25	MLT-3	Yes
1000BASE-BX10	1 Gbit/s bidi fibre	59, 66	8B/10B	Yes
1000BASE-CX	1 Gbit/s twinax	39	8B/10B	Yes
1000BASE-KX	1 Gbit/s backplane	70	8B/10B	Yes
1000BASE-LX	1 Gbit/s fibre	38	8B/10B	Yes
1000BASE-PX	1 Gbit/s PON	38	8B/10B	Unidirectional
1000BASE-SX	1 Gbit/s fibre	38	8B/10B	Yes
1000BASE-T	1 Gbit/s TP copper	40	4D-PAM5	Unidirectional (Note 2)
10BROAD36	*10 Mbit/s coax*	*11*	*BPSK*	*No (Note 1)*
10GBASE-CX4	10 Gbit/s 4x twinax	54	8B/10B	Yes
10GBASE-ER	10 Gbit/s fibre	49, 52	64B/66B	Yes
10GBASE-EW	10 Gbit/s fibre	50, 52	64B/66B	Yes
10GBASE-KR	10 Gbit/s backplane	72	64B/66B	Yes
10GBASE-KX4	10 Gbit/s 4x backplane	71	8B/10B	Yes
10GBASE-LR	10 Gbit/s fibre	49, 52	64B/66B	Yes
10GBASE-LRM	10 Gbit/s fibre	68	64B/66B	Yes
10GBASE-LW	10 Gbit/s fibre	50, 52	64B/66B	Yes
10GBASE-LX4	10 Gbit/s 4λ fibre	50, 52	8B/10B	Yes
10GBASE-SR	10 Gbit/s fibre	49, 52	64B/66B	Yes
10GBASE-SW	10 Gbit/s fibre	50, 52	64B/66B	Yes
10GBASE-T	10 Gbit/s TP copper	55	DSQ-128	Yes (Note 3)

Table III.1 – List of Ethernet interfaces eligible to synchronous Ethernet

PHY	Description	[IEEE 802.3] clause	Coding	Synchronous Ethernet capable
10PASS-TS	>10 Mbit/s DSL	61, 62	DMT	No
1BASE-5	*1 Mbit/s TP copper*	*12*	*Manchester*	*No (Note 1)*
2BASE-TL	>2 Mbit/s DSL	61, 63	PAM	No
10/1GBASE-PR	10 Gbit/s/1 Gbit/s PON	76	64B/66B/8B/10B	Unidirectional
10GBASE-PR	10 Gbit/s PON	76	64B/66B	Unidirectional
25GBASE-CR	25 Gbit/s one lane of twinaxial copper cable	110	64B/66B	Yes
25GBASE-CR-S	25 Gbit/s one lane of twinaxial copper cable without RS-FEC	110	64B/66B	Yes
25GBASE-KR	25 Gbit/s one lane of an electrical backplane	111	64B/66B	Yes
25GBASE-KR-S	25 Gbit/s one lane of an electrical backplane without RS-FEC	111	64B/66B	Yes
25GBASE-SR	25 Gbit/s multimode fibre	112	64B/66B	Yes
25GBASE-T	25 Gbit/s point-to-point 4-pair balanced twisted-pair medium	113	16-level PAM	Unidirectional
25GBASE-ER	25 Gbit/s single-mode fibre, with reach up to at least 40 km	114	64B/66B	Yes
25GBASE-LR	25 Gbit/s single-mode fibre, with reach up to at least 10 km	114	64B/66B	Yes
40GBASE-KR4	40 Gbit/s 4x backplane	84	64B/66B	Yes
40GBASE-CR4	40 Gbit/s 4x twinax	85	64B/66B	Yes
40GBASE-SR4	40 Gbit/s 4x fibre	86	64B/66B	Yes
40GBASE-LR4	40 Gbit/s 4λ fibre	87	64B/66B	Yes
50GBASE-CR	50 Gbit/s, one twinax	136	PAM4	Yes
50GBASE-KR	50 Gbit/s, an electrical backplane	137	PAM4	Yes
50GBASE-SR	50 Gbit/s one lane, multimode fibre	138	PAM4	Yes
50GBASE-FR	50 Gbits/s, one lane, single mode fibre	139	PAM4	Yes

Table III.1 – List of Ethernet interfaces eligible to synchronous Ethernet

PHY	Description	[IEEE 802.3] clause	Coding	Synchronous Ethernet capable
50GBASE-LR	50 Gbits/s, one lane, single mode fibre up to 10km	139	PAM4	Yes
100GBASE-CR10	100 Gbit/s 10x twinax	85	64B/66B	Yes
100GBASE-SR10	100 Gbit/s 10x fibre	86	64B/66B	Yes
100GBASE-LR4	100 Gbit/s 4λ fibre	88	64B/66B	Yes
100GBASE-ER4	100 Gbit/s 4λ fibre	88	64B/66B	Yes
100GBASE-CR2	100 Gbit/s 2 twinax	136	PAM4	Yes
100GBASE-KR2	100 Gbit/s over two electrical backplanes	137	PAM4	Yes
100GBASE-SR2	100 Gbit/s 2 lane, multimode fibre	138	PAM4	Yes
200GBASE-DR4	200 Gbit/s 4x fibre	121	64B/66B	Yes
200GBASE-FR4	200 Gbit/s 4λ fibre, up to 2km reach	122	64B/66B	Yes
200GBASE-LR4	200 Gbit/s 4λ fibre, up to 10km reach	122	64B/66B	Yes
200GBASE-CR4	200 Gbit/s, 4 twinax	136	PAM4	Yes
200GBASE-KR4	200 Gbit/s, 4 electrical backplanes	137	PAM4	Yes
200GBASE-SR4	200 Gbit/s, 4 lane multimode fibre	138	PAM4	Yes
400GBASE-FR8	400 Gbit/s 8λ fibre, up to 2km reach	122	64B/66B	Yes
400GBASE-LR8	400 Gbit/s 8λ fibre, up to 10km reach	122	64B/66B	Yes

NOTE 1 – These rows (in italics) are deprecated.

NOTE 2 – Noise transfer is not measured on a loop-timed interface.

NOTE 3 – 10GBASE-T may support dual master or master/slave clocking (i.e., unidirectional synchronous Ethernet).

NOTE 4 – 100GBASE-DR interface is for further study.

Appendix IV

Considerations related to synchronous Ethernet over 1000BASE-T and 10GBASE-T

(This appendix does not form an integral part of this Recommendation.)

Synchronous Ethernet requires the relevant synchronization parameters of the network elements (e.g., link selected as candidate synchronization reference, priority) to be configured according to the network synchronization plan.

The following discussion focuses on 1000BASE-T and 10GBASE-T, as for these interfaces the timing direction could become incompatible with the network synchronization plan due to the configuration of the master-slave relationship as defined by [IEEE 802.3].

NOTE – The following applies to unidirectional (from a synchronization viewpoint) interfaces. The application of similar rules to links in a ring where the timing chain might have to be reversed is for further study.

The following convention is used below:

- Clock master/slave: IEEE 802.3 master or slave state.
- Sync master/slave: ITU-T G.8264 sync timing chain master or slave state.

In order to allow the proper setting of SyncE over 1000BASE-T and 10GBASE-T links, the Ethernet PHY could be configured either with a manual configuration or via auto-negotiation.

If manual configuration is used, the operator must take care to correctly configure the clock master/slave setting of the PHY ports according to the network synchronization plan so that candidates for sync slaves are clock slaves and the sync master ports are clock masters. The use of manual configuration, if not properly done, may result in a failure condition and the consequent loss of the traffic connection to the equipment.

As an example, if by mistake both ends are forced to be masters, the result is a configuration fault (see Table 40-5 – 1000BASE-T MASTER-SLAVE configuration resolution table in [IEEE 802.3]).

If auto-negotiation is used, the previous potential issues are prevented by the network element thus avoiding the result of a link not working.

NOTE – In this case, even if the PHY ports are not configured according to the network synchronization plan, the auto-negotiation may fail to get working network synchronization (with no indication of such timing discrepancy) but it will not jeopardize the possibility of getting working Ethernet traffic, and subsequent actions are possible in order to correct the PHY port setting.

A possible sequence of steps to be followed when auto-negotiation is used is described below.

NOTE – It is assumed that these synchronous Ethernet interfaces are configured in synchronous operation mode:

1. All 1000BASE-T and 10GBASE-T ports must allow auto-negotiation.
2. Auto-negotiation is initiated:
    - In the case of 1000BASE-T, all ports shall be configured with Bit 9.12 = 0 (auto-negotiation – not forced). If a port is involved in the network synchronization plan, the port that should act as sync master must be configured with Bit 9.10 = 1 (Table 40-3 in [IEEE 802.3]) and the port that should act as sync slave must be configured with Bit 9.10 = 0. If details on the network synchronization plan are not available, ports should be configured with Bit 9.10 = 1. The configuration is done as per Table 40-5 in [IEEE 802.3] ("The device with the higher SEED value is configured as MASTER, otherwise SLAVE"). When details on the network synchronization plan are made available, having ports with Bit 9.10 = 1 as the preferred default state allows the

modification of Bit 9.10 on the sync slave side only, usually in the downstream data path (see item 4 below).

NOTE – Having ports with bit 9.10 = 0 as the preferred default state requiring the modification of the Bit 9.10 on the sync master side only, would give a similar result. This Recommendation suggests a default configuration for easier interoperability.

- In the case of 10GBASE-T, all ports shall be configured with Bit U11= 0 (see Table 55-11 in [IEEE 802.3]). If a port is involved in the network synchronization plan, the port that should act as sync master must be configured with Bit U13 = 1 (multiport device, see Table 55-11 in [IEEE 802.3]) and the port that should act as sync slave must be configured with Bit U13 = 0 (single port device, see Table 55-11 in [IEEE 802.3]). If details on the network synchronization plan are not available, ports should be configured with Bit U13 = 1.

  When details on the network synchronization plan are made available, having ports with bit U13 = 1 as the preferred default state allows the modification of the Bit U13 on the sync slave side only, usually in the downstream data path (see item 4 below).

  NOTE – Having ports with bit U13 = 0 as the preferred default state requiring the modification of the Bit U13 on the sync master side only, would give a similar result. This Recommendation suggests a default configuration for easier interoperability.

3. The configuration of the network synchronization parameters in the node according to the network synchronization plan should be done and checked after the clock master/slave of the 1000BASE-T or 10GBASE-T ports has been completed. At this point, the links in the nodes that are clock slave can be configured as sync candidate (if the network synchronization plan requires it).

4. If the network synchronization plan is available only after the clock master/slave procedure has been completed, and if a 1000BASE-T or 10GBASE-T port is not the clock slave, but should be the sync slave candidate according to the network synchronization plan ("sync slave"), this port shall initiate a change clock direction (as part of the sync candidate configuration) by means of the tools defined in Table 40-3 (1000BASE-T) and Table 55-11 (10GBASE-T) of [IEEE 802.3]. In particular,

   - In the case of 1000BASE-T, for this port, Bit 9.10 = 0
   - In the case of 10GBASE-T, for this port, Bit U13 = 0

   NOTE 1 – Any change in parameters for IEEE 802.3 auto-negotiation would force a reset of the interface, leading to link failure for a certain amount of time (variable up to a few seconds).

   NOTE 2 – When these steps are not properly followed (e.g., some of the nodes have been manually configured), a specific alarm might be required in order to notify the operator to take necessary actions.

Appendix V

Considerations for measuring noise transfer for Option 2 clocks

(This appendix does not form an integral part of this Recommendation.)

In transferring noise, an equipment clock generally behaves as a second-order system. The main parameters that impact wander accumulation in the network are the transfer bandwidth and the allowable gain peaking.

A common method to measure noise transfer for Option 2 networks involves the use of TDEV measurements. Since clock tolerance is measured using a signal that meets the TDEV network limit, measuring the output TDEV will provide an indication of the filtering provided by the clock. Some consideration is needed to accommodate gain peaking. For Option 2 clocks, the output TDEV is raised by approximately 2% to reflect the appropriate gain.

The output TDEV shall not exceed the mask shown in Figure 11 when the reference signal is at the noise level given by the TDEV tolerance mask specified in Figure 8 of this Recommendation.

The bandwidth of the clock is approximated by the breakpoint observable at 3 seconds observation time. Details for the approximate relationship between clock bandwidth and TDEV can be found in Appendix I of [ITU-T G.812].

Note, as per [b-ITU-T O.174], additional sources of measurement error may need to be considered if using this methodology to verify the transfer characteristics. According to [b-ITU-T O.174], the TDEV noise generation accuracy of the measurement equipment is only required to be 20%; therefore, the noise amplitude must be carefully calibrated before measuring the transfer function of the clock.

In some cases, the use of sinusoidal signals applied to the input and measured at the output may be suitable to determine the transfer characteristics of the clock, as is specified for Option 1 clocks. Given the transfer gain allowed in the equipment under test is only 2%; care should be taken with the test method and measurement equipment accuracy. The specification of this method is for further study.

The output TDEV noise transfer mask for Option 2 clocks is given in Table 13. The resultant TDEV is shown in the mask of Figure 11.

Appendix VI

Considerations for testing of pull-in range

(This appendix does not form an integral part of this Recommendation.)

This Recommendation defines the minimum pull-in range as ±4.6 ppm from nominal regardless of the equipment clock implementation (e.g., internal free-run clock oscillator frequency). Specifically,

a. The clock needs to lock to the reference even when the reference is at the two extremes, namely +4.6 ppm and −4.6 ppm (and everything in between) from nominal. That is, the pull-in range has to be no less than 9.2 ppm peak-to-peak.

b. The clock needs to be able to respond to a switch even when the two input references are at the two extremes (or anything in between).

Typically, the pull-in range requirement can be satisfactorily qualified by adding a frequency offset of +4.6 ppm and/or −4.6 ppm to the nominal reference input and check if equipment is able to achieve locked state.

The pull-in range needs to be satisfied for the lifetime of the equipment. The manufacturer has to include any additional margin to account for the ageing effect on the internal oscillator.

Appendix VII

Performance estimation for cascaded media converters acting as synchronous equipment clocks

(This appendix does not form an integral part of this Recommendation.)

On some specific media interfaces (e.g., OSC in case of OTN), test equipment may not be available to measure all aspects of the equipment clock performance. For such cases, this appendix describes a back-to-back measurement methodology as shown in Figure VII.1. This appendix also describes how to estimate the performance budget to use for back-to-back equipment clock in Figure VII.1, where each media converter equipment clock is allocated the budget equivalent to a single synchronous equipment slave clock in the body of this Recommendation.

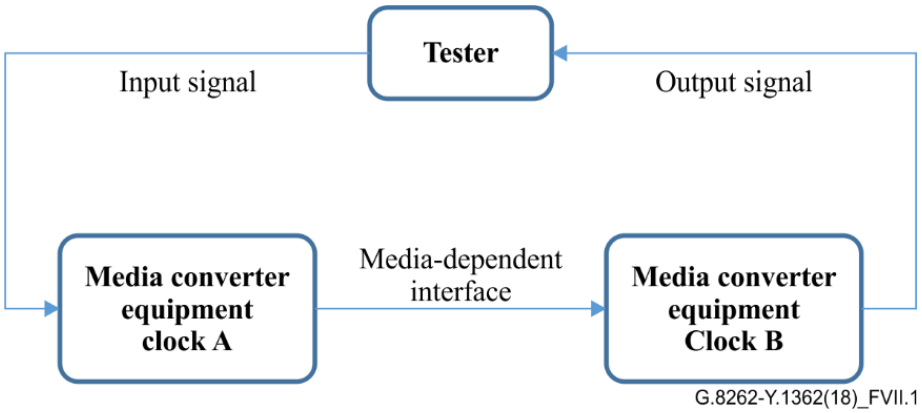

Figure VII.1 – Measurement for testing media converter equipment clocks

NOTE – The performance estimation below can be used for the back-to-back equipment clocks with OTN technology between two media converter equipment clocks, and the performance estimation of back-to-back media converter equipment clocks with other technologies are for further study.

VII.1 Noise generation

The wander generation expected at the output of the media converter equipment clock B can be estimated as the wander generation of a single SEC multiplied by the square root of two. Note that the wander generation of the media converter equipment clock A could be directly verified in isolation via its other interfaces, i.e., 2048 kHz, 2048 kbit/s or Ethernet.

The jitter generation expected at the output of the media converter equipment clock B can be estimated to be same as the jitter generation of a single SEC.

VII.2 Noise tolerance

As the noise tolerance at the input to media converter equipment clock B cannot be tested directly on the interface between the media converter equipment clocks, the test can be done at the input to the media converter equipment clock A using one of its other interfaces, i.e., 2048 kHz, 2048 kbit/s or Ethernet. The noise tolerance at the input of the media converter equipment clock A is estimated to be same as the noise tolerance of a single SEC.

VII.3 Noise transfer

The noise transfer performance estimation for back-to-back option 1 equipment clocks is as follows:

The noise transfer of the output of the cascaded media converter equipment clocks would have:

– A maximum gain of 0.4 dB,

– A maximum bandwidth of 10 Hz,

– A minimum gain of −6 dB for frequencies less than or equal to 1 Hz.

NOTE 1 – The minimum bandwidth specified for one EEC is 1 Hz. If two clocks whose 3 dB bandwidths are 1 Hz are cascaded, the overall gain of the cascaded clocks taken together is −6 dB for frequencies less than or equal to 1 Hz. The 3 dB bandwidth of the cascaded clocks taken together is less than 1 Hz.

NOTE 2 – This clause does not add or modify requirements contained in the normative parts of this Recommendation.

NOTE 3 – The noise transfer test of one single media converter equipment clock could be done in isolation via its other interfaces, i.e., 2048 kHz, 2048 kbit/s or Ethernet.

VII.4 Transient response and holdover performance

The phase transient response and holdover performance of the output of the media converter equipment clock B, including short-term phase transient, long-term phase transient, phase response to input signal interruptions and phase discontinuity, can be estimated to be the same as the transient response and holdover performance of a single SEC. The signal interruption to initiate this test can be done at the link between two media converter equipment clocks A and B, or at the input to the equipment clock A via its other interfaces, i.e., 2048 kHz, 2048 kbit/s or Ethernet. When the signal interruption is introduced on clock A to conduct this test, clock B must be kept locked to the input from clock A in order to measure the resulting transient.

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Printed in Switzerland
Geneva, 2020