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SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Packet over Transport aspects – Synchronization, quality and availability targets

SERIES Y: GLOBAL INFORMATION INFRASTRUCTURE, INTERNET PROTOCOL ASPECTS AND NEXT-GENERATION NETWORKS

Internet protocol aspects – Transport

Network limits for time synchronization in packet networks

Recommendation ITU-T G.8271.1/Y.1366.1

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Recommendation ITU-T G.8271.1/Y.1366.1

Network limits for time synchronization in packet networks

Summary

Recommendation ITU-T G.8271.1/Y.1366.1 specifies the maximum network limits of phase and time error that shall not be exceeded. It specifies the minimum equipment tolerance to phase and time error that shall be provided at the boundary of packet networks at phase and time synchronization interfaces. It also outlines the minimum requirements for the synchronization function of network elements.

This Recommendation addresses the case of time and phase distribution across a network with packet-based method with full timing support to the protocol level from the network.

History

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FOREWORD

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The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

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In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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As of the date of approval of this Recommendation, ITU had not received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementers are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database at http://www.itu.int/ITU-T/ipr/.

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1 Scope

This Recommendation specifies the maximum network limits of phase and time error that shall not be exceeded. It specifies the minimum equipment tolerance to phase and time error that shall be provided at the boundary of packet networks at phase and time synchronization interfaces. It also outlines the minimum requirements for the synchronization function of network elements.

This Recommendation addresses the case of time and phase distribution across a network with packet-based method with full timing support to the protocol level from the network. The packet networks that are in the scope of this Recommendation are currently limited to the following scenarios:

- Ethernet: [IEEE 802.3], [IEEE 802.1D], [IEEE 802.1Q] and [IEEE 802.1Qay]
- MPLS: [IETF RFC 3031] and [ITU-T G.8110]
- IP: [IETF RFC 791] and [IETF RFC 2460]

The physical layer that is relevant to this specification is the Ethernet media type as defined in [IEEE 802.3-2005].

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T G.803] Recommendation ITU-T G.803 (2000), *Architecture of transport networks based on the synchronous digital hierarchy (SDH)*.

[ITU-T G.810] Recommendation ITU-T G.810 (1996), *Definitions and terminology for synchronization networks*.

[ITU-T G.812] Recommendation ITU-T G.812 (2004), *Timing requirements of slave clocks suitable for use as node clocks in synchronization networks*.

[ITU-T G.823] Recommendation ITU-T G.823 (2000), *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy*.

[ITU-T G.8110] Recommendation ITU-T G.8110/Y.1370 (2005), *MPLS layer network architecture*.

[ITU-T G.8260] Recommendation ITU-T G.8260 (2010), *Definitions and terminology for synchronization in packet networks*.

[ITU-T G.8262] Recommendation ITU-T G.8262/Y.1362 (2010), *Timing characteristics of a synchronous Ethernet equipment slave clock.*

[ITU-T G.8271] Recommendation ITU-T G.8271/Y.1366 (2012), *Time and phase synchronization aspects of packet networks*.

[ITU-T G.8272] Recommendation ITU-T G.8272/Y.1367 (2012), *Timing characteristics of primary reference time clocks.*

[ITU-T G.8273] Recommendation ITU-T G.8273/Y.1368 (2013), *Framework of phase and time clocks*.

[ITU-T G.8273.2] Recommendation ITU-T G.8273.2/Y.1368.2 (2014), *Timing characteristics of telecom boundary clocks and telecom time slave clocks*.

[ITU-T G.8275] Recommendation ITU-T G.8275/Y.1369 (2013), *Architecture and requirements for packet-based time and phase distribution*.

[IEEE 802] IEEE 802-2014, *IEEE Standard for Local and Metropolitan Area Networks: Overview and Architecture*.
http://standards.ieee.org/getieee802/802.html

[IEEE 802.1D] IEEE 802.1D-2004, *IEEE Standard for local and metropolitan area networks: Media Access Control (MAC) Bridge*s.
http://standards.ieee.org/findstds/standard/802.1D-2004.html

[IEEE 802.1Q] IEEE 802.1Q-2011, *IEEE Standard for local and metropolitan area networks: Media Access Control (MAC) Bridges and Virtual Bridged Local Area Network*s.
http://standards.ieee.org/findstds/standard/802.1Q-2011.html

[IEEE 802.1Qay] IEEE 802.1Qay-2009, *IEEE Standard for Local and Metropolitan Area Networks: Virtual Bridged Local Area Networks Amendment 10*.
http://standards.ieee.org/findstds/standard/802.1Qay-2009.html

[IEEE 802.3] IEEE 802.3-2008, *Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications.*
http://standards.ieee.org/findstds/standard/802.3-2008.html

[IEEE 1588-2008] IEEE 1588-2008, *Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems*.
http://standards.ieee.org/findstds/standard/1588-2008.html

[IETF RFC 791] IETF RFC 791 (1981), *Internet Protocol (IP)*.
http://www.ietf.org/rfc/rfc0791.txt?number=791

[IETF RFC 2460] IETF RFC 2460 (1998), *Internet Protocol, Version 6 (IPv6) Specification*.
http://www.ietf.org/rfc/rfc2460.txt?number=2460

[IETF RFC 3031] IETF RFC 3031 (2001), *Multiprotocol Label Switching Architecture*.
http://www.ietf.org/rfc/rfc3031.txt?number=3031

3 Definitions

3.1 Terms defined elsewhere

This Recommendation uses the following terms defined elsewhere:

The terms and definitions used in this Recommendation are contained in [ITU-T G.810] and [ITU-T G.8260].

3.2 Terms defined in this Recommendation

None.

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

EEC	Synchronous Ethernet Equipment Clock
GNSS	Global Navigation Satellite System
GPS	Global Positioning System

HRM	Hypothetical Reference Model
PHY	Physical layer
PLL	Phase-Locked Loop
PPS	Pulse Per Second
PRTC	Primary Reference Time Clock
PTP	Precision Time Protocol
SDH	Synchronous Digital Hierarchy
SSM	Synchronization Status Message
SSU	Synchronization Supply Unit
TDD	Time Division Duplex
TE	Time Error
T-BC	Telecom Boundary Clock
T-GM	Telecom Grand Master
T-TC	Telecom Transparent Clock
T-TSC	Telecom Time Slave Clock

5 Conventions

Within this Recommendation, the following conventions are used: the term precision time protocol (PTP) refers to the PTP protocol defined in [IEEE 1588-2008].

The term telecom boundary clock (T-BC) is a device consisting of a boundary clock as defined in [IEEE 1588-2008] and with additional performance characteristics for further study.

The term telecom transparent clock (T-TC) is a device consisting of a transparent clock as defined in [IEEE 1588-2008] and with additional performance characteristics for further study.

The term telecom grand master (T-GM) is a device consisting of a grandmaster clock as defined in [IEEE 1588-2008] and with additional performance characteristics for further study.

The term telecom time slave clock (T-TSC) is a device consisting of a PTP slave only ordinary clock as defined in [IEEE 1588-2008] and with additional performance characteristics for further study.

The terms dynamic time error and time noise are used interchangeably throughout this Recommendation to indicate jitter and wander components of the timing signal.

6 Network reference model

The general network reference model is described in [ITU-T G.8271].

7 Network limits

The following main (i.e., worst case) scenarios have been identified and are considered in the definition of the relevant network limits:

- deployment case 1: time distribution chain with telecom time slave clock (T-TSC) integrated in the end application and end application with a distributed architecture.
- deployment case 2: time distribution chain with a T-TSC external to the end application and end application with a distributed architecture. Note: a specific equipment implementation may also be based on implementing a telecom boundary clock (T-BC) function (instead of a

T-TSC function) and delivering the phase/time reference to the end application via a phase/time synchronization distribution interface.

The deployment cases are shown in Figure 7-1.

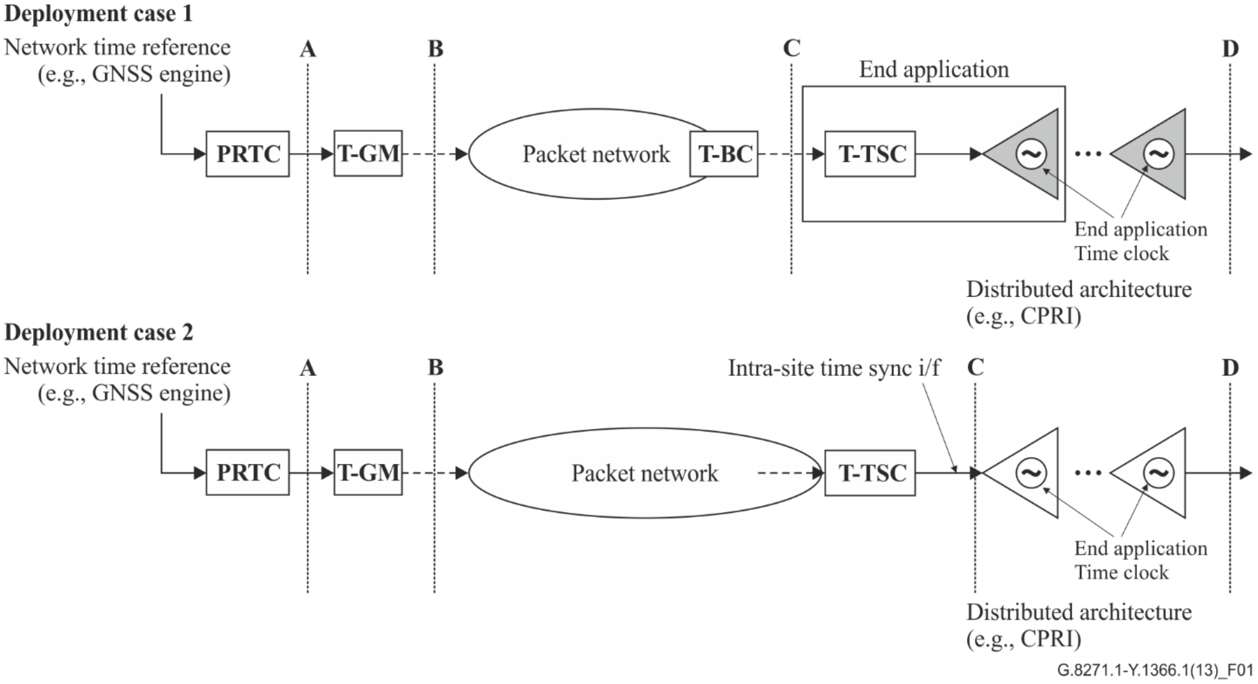


Figure 7-1 – Time synchronization deployment cases

NOTE – An example of distributed architecture is the case of mobile applications where the base stations have the base band unit (also called radio equipment control (REC)) connected remotely to the radio units (also called radio equipment (RE)). In this case a point to point connection (e.g., via fibre) is assumed and chain topologies are possible. The time error (TE) budget applicable to this connection is assumed to be 150 ns; the details on the chain topology are for further study.

7.1 Network limits at reference point A

The network limits applicable at reference point A, i.e., at the output of the primary reference time clock (PRTC), are defined in [ITU-T G.8272]. In particular, according to [ITU-T G.8272] the maximum absolute time error is:

$|TE| \leq 100$ ns

NOTE – This limit is applicable under normal, locked operating conditions. The limit under failure conditions at the PRTC is for further study.

Dynamic time error network limits applicable at the reference point A are also specified in [ITU-T G.8272].

7.2 Network limits at reference point B

In the case of a telecom grand master (T-GM) integrated in the PRTC, the network limits applicable at reference point B are the same as the limits applicable at the reference point A.

In the case of a T-GM external to the PRTC, the network limits applicable at reference point B are for further study.

7.3 Network limits at reference point C

The limits given in this clause represent the maximum permissible levels of phase/time error and noise at interfaces within a packet network in charge of distributing phase/time synchronization according to the applications corresponding to the class 4 listed in Table 1 of [ITU-T G.8271].

The limits applicable to other classes at the reference point C are for further study.

The noise generated by a chain of T-BC is characterized by two main aspects:

1. the constant time error produced by the chain, for instance due to various fixed and uncompensated asymmetries (including the PRTC);
2. the dynamic time error produced by the various components of the chain (including the PRTC). This noise can be classified as low or high frequency noise, with components below or above 0.1 Hz respectively.

The network limits applicable at reference point C are expressed in terms of two quantities:

1. the maximum absolute time error: max |TE|, which includes the constant time error and the low frequency components of the dynamic time error;
2. a suitable metric applied to the dynamic time error component (in particular, MTIE and TDEV are used for measuring noise components with frequency lower than 0.1 Hz, and peak-to-peak TE is used for measuring noise components with frequency higher than 0.1 Hz).

The limits given below shall be met for all operating conditions (except during PTP rearrangements and long holdover conditions in the network and during both PTP and the physical layer frequency rearrangements conditions that are for further study; see also examples in Appendix V), regardless of the amount of equipment preceding the interface. In general, these network limits are compatible with the minimum tolerance to time error and noise that all equipment input ports are required to provide. Further guidance about how to design a phase/time distribution network is provided in Appendix V of this Recommendation. The limits are:

– Maximum absolute time error network limit applicable at the reference point C: max $|TE| \leq$ 1'100 ns.

Dynamic low frequency time error network limit applicable at the reference point C: the specification in terms of MTIE is presented in Table 7-1 and Figure 7-2. The specification in terms of TDEV is for further study.

Table 7-1 – Dynamic time error network limit expressed in MTIE

MTIE limit (ns)	Observation interval, τ (s)
$100 + 75\tau$	$1.3 < \tau \leq 2.4$
$277 + 1.1\tau$	$2.4 < \tau \leq 275$
580	$275 < \tau \leq$ 10'000

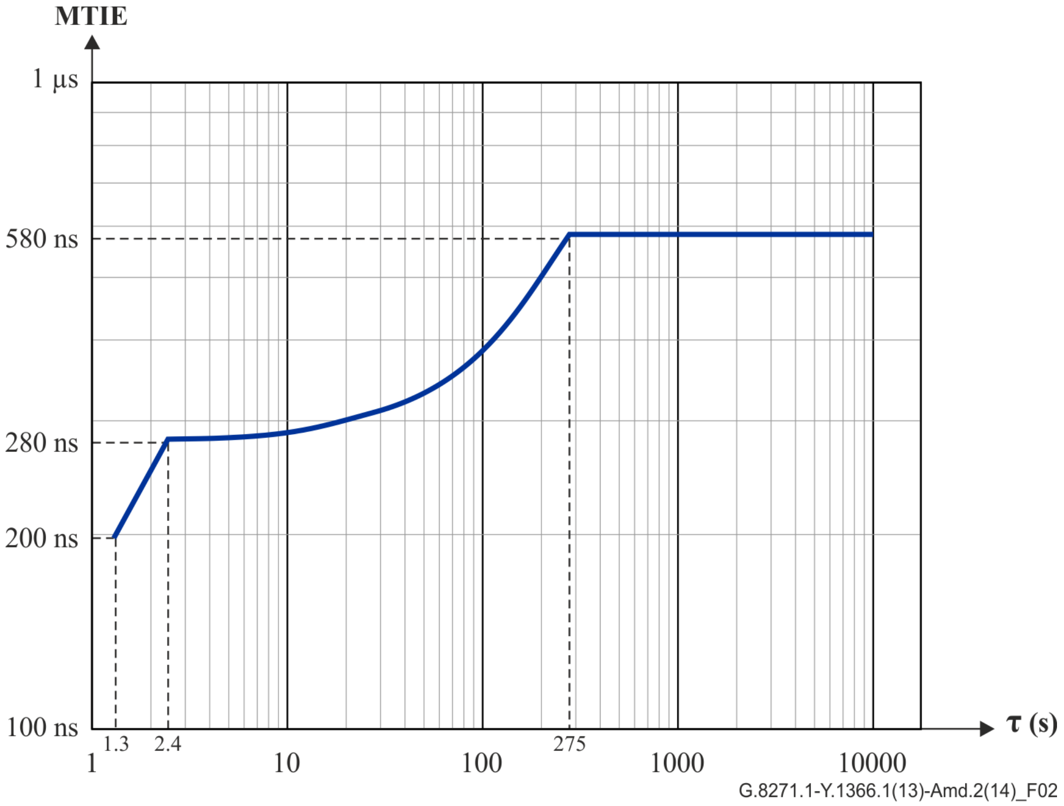


Figure 7-2 – Dynamic time error network limit (MTIE)

A first-order low-pass measurement filter with bandwidth of 0.1 Hz is applied to the TE samples measured at the packet timing interface prior to evaluating the max |TE|, MTIE and TDEV. Network Limits measurements performed on the 1 PPS test output should also perform a similar filtering on the 1 PPS signal.

Additional details on the test equipment characteristics and measurement period are also for further study.

NOTE – The above MTIE specification is the result of a number of conservative assumptions that, in theory, may lead to a dynamic component with max |TE| greater than 300 ns and frequency components less than 0.1 Hz. However, the related dynamic noise component has been demonstrated to have max |TE| that is always less than 300 ns under the assumptions made in this Recommendation and other related recommendations, e.g., [ITU-T G.8273.2].

The following requirement applies for frequency components higher than 0.1 Hz (a first-order high-pass filter with bandwidth of 0.1 Hz should be applied to the TE samples measured at the packet timing interface or to the 1 PPS signal), as measured over a 10'000 second interval:

– peak-to-peak TE amplitude < 200 ns

7.4 Network limit at reference point D

The network limit applicable at reference point D is defined by the specific application as defined in Table 1 of [ITU-T G.8271].

The applications corresponding to the classes 4, 5 and 6 according to Table 1 of [ITU-T G.8271] are currently considered in this Recommendation.

Appendix I

Clock models for noise accumulation simulations

(This appendix does not form an integral part of this Recommendation.)

Simulations are needed to define limits on the various noise types described in [ITU-T G.8271]. To perform these simulations, a simulation model that shows how to simulate each noise type it introduces into the timing signal needs to be defined for each network element participating in the time distribution scheme.

I.1 T-BC models for noise accumulation simulations

This clause describes T-BC models for simulating the transport of time using PTP and frequency using synchronous Ethernet and a T-BC model for simulating the transport of both time and frequency using PTP.

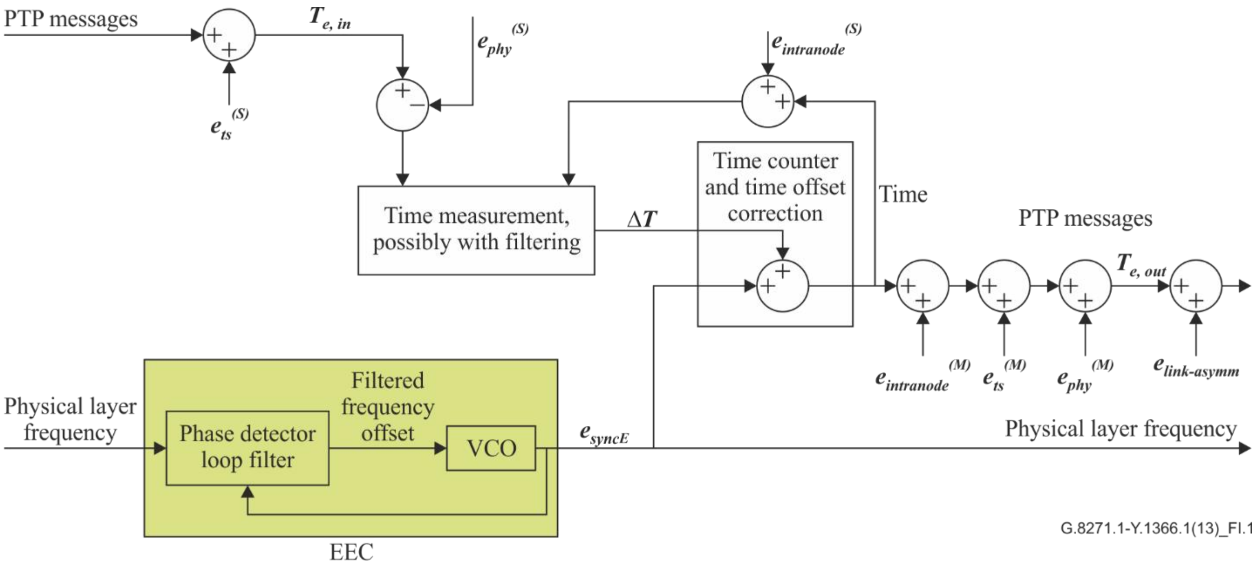


Figure I.1 – Telecom boundary clock model for simulating the transport of time using PTP with synchronous Ethernet assistance

Figure I.1 illustrates a model for simulating the transport of time using PTP with synchronous Ethernet assistance.

NOTE – This model, used for the evaluation of a worst-case noise accumulation when synchronous Ethernet is combined with PTP, may not be representative of all possible implementations.

The synchronous Ethernet equipment clock (EEC) block represents an Ethernet equipment clock, as specified in [ITU-T G.8262]. The EEC input is a physical layer frequency (i.e., a physical layer signal that is used as a frequency reference), and its output is a local frequency (i.e., a physical layer signal that has a frequency and is local to this node) that is optionally propagated to downstream nodes. The noise process, e_{syncE}, represents the synchronous Ethernet phase noise accumulation in the synchronous Ethernet hypothetical reference model (HRM) (see Appendix II).

The time counter (TC) is incremented by the nominal period of the output clock of the EEC block. For example, if the output clock rate is 125 MHz, then the time counter is incremented by 8 ns each rising edge of the synchronous Ethernet output clock. Upon reception and transmission of a PTP event messages, the time counter is sampled. The difference between the actual transmission/reception time and the sampled value of the time counter is modelled as, e_{ts}, since the transmission/reception event can happen between two rising edges of this clock. The effect of e_{ts} on the timestamp for reception of a PTP event message is shown added at the input, and the effect of e_{ts} on the timestamp for transmission of a PTP event message is shown added at the output.

The incoming PTP messages contain information that may be used to obtain an estimate of the grandmaster (i.e., PRTC) time. This estimate is not perfect; it contains errors introduced by the grandmaster, the upstream nodes, and upstream links. The error in the incoming estimate of the grandmaster time is represented by $T_{e,in}$. The noise process, e_{phy}, represents the effect of asymmetry and timestamp sampling uncertainty on the physical layer (PHY) of the input port. The PHY latency asymmetry may be present if timestamping is done at a point other than the reference plane (i.e., the interface between the PHY and the physical medium). Any latency between the point where timestamping actually is done and the reference plane may be compensated for within PTP. However, any uncompensated latencies that result in asymmetry will contribute to e_{phy}. The noise e_{phy} is subtracted from the timing information contained in the incoming PTP messages due to the direction of the time distribution (note, that on the master port of the T-BC it is added). Note that the random process, e_{phy}, may have a static component and a time-varying component.

The timing information contained in the incoming PTP messages, with the noise due to asymmetry on the input port PHY, e_{phy}, and the timestamping error, e_{ts}, is input to the block labelled time measurement, possibly with filtering. This block compares the local time output of the local clock, which is the accumulation of the syncE phase noise, e_{syncE}, and the prior time offset correction, ΔT, with the timing input that represents an estimate of the grandmaster time (with errors as described in the previous paragraph). This block produces the time offset correction, ΔT, between the grandmaster time estimate and the local time. The time measurement block might provide filtering when computing the time offset correction, to reduce the effect of the short-term noise in the observed time error. The filtering characteristics are for further study.

The time counter and time offset correction block produces a local time output (i.e., the output labelled "time"). The input to the time counter and time offset correction block is the output of the EEC and the time offset correction of the time measurement block. The counter and time offset correction block may include a low-pass filtering function. This has the same effect as increasing the output frequency of the EEC block.

The local time is sampled upon transmission and reception of PTP event messages on master ports. The sampled value is the accumulation of the synchronous Ethernet phase noise, e_{syncE}, the timestamp error, e_{ts}, and the offset correction, ΔT. The error due to asymmetry of the PHY on the output port, e_{phy}, is added to the sampled local time to produce the master port output time error, $T_{e,out}$. The quantity, $T_{e,out}$, is input to the next PTP node (T-BC or telecom time slave clock (T-TSC)) downstream via a link model.

Errors due to intranode transmission, $e_{intranode}$, and link asymmetry, $e_{link\text{-}asymm}$, must also be included. The former affects both the time correction and the T-BC output. The latter is shown added to the output of the T-BC.

Figure I.2 describes an equivalent model suitable for analytical studies.

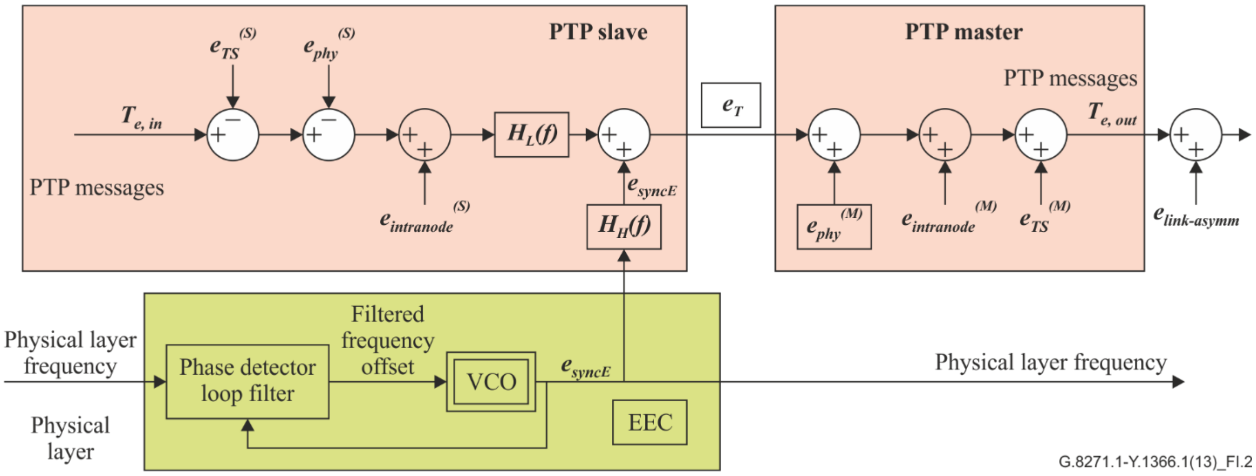
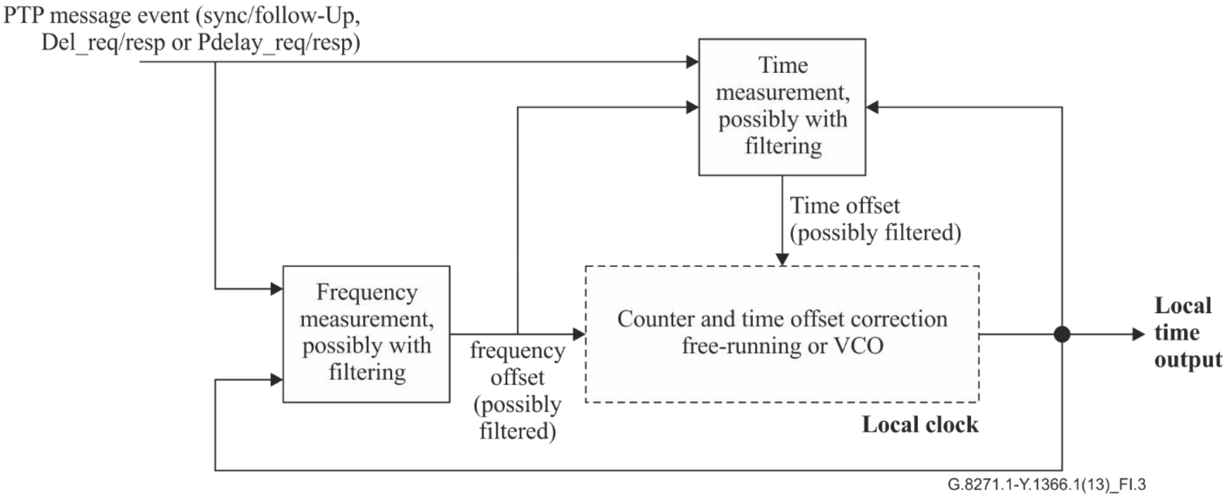


Figure I.2 – Telecom boundary clock model for analytical studies of the transport of time using PTP with synchronous Ethernet assistance

In Figure I.2 the slave clock is assumed to have time error filtering indicated by the low-pass filter $H_L(f)$. The physical layer clock noise experiences a high-pass characteristic, $H_H(f)$. When there is no time error filtering the physical layer clock introduces a time error corresponding to the wander (e_{syncE}) that occurs between successive estimates of the time offset correction.

The following figure describes a model using PTP for time and frequency. The details for this model are for further study.



NOTE – The ingress and egress hardware timestamping needs to be modelled and taken into account.

Figure I.3 – Telecom boundary clock model using PTP for time and frequency

In Figure I.3:

- PTP messages are used for both frequency and time measurements. The PTP messages are timestamps based on the local time output.
- The frequency measurement block uses PTP messages to make frequency measurements. For frequency measurements there are several possibilities (e.g., Sync or Pdelay_req messages) and these are for further study. The frequency measurements could involve filtering and is for further study. The PTP messages are timestamps based on the local time output.
- The time measurement block uses PTP messages for computing a time offset; this block should consider sources of errors such as the effect of timestamping. The PTP messages are timestamps based on the local time output. The time measurement block might provide

filtering, for example, to reduce the effect of the error produced by the timestamping function. The filtering characteristics are for further study.

- The local clock block includes a counter to produce a local timebase output. The input into this block is a frequency measurement from the frequency measurement block and a time correction from the time measurement block. The ways in which these are used is for further study.

For the simulation model using PTP for time and frequency, it can be assumed that filtering is implemented in each boundary clock with a phase-locked loop (PLL)-based clock.

I.2 End-to-end TC models for noise accumulation simulations

This section describes models for simulating the noise added by a PTP transparent clock when using synchronous Ethernet or a free running local oscillator (see [IEEE 1588-2008] for details on the transparent clock functions). The models for the case where PTP is the source for frequency reference are for further study.

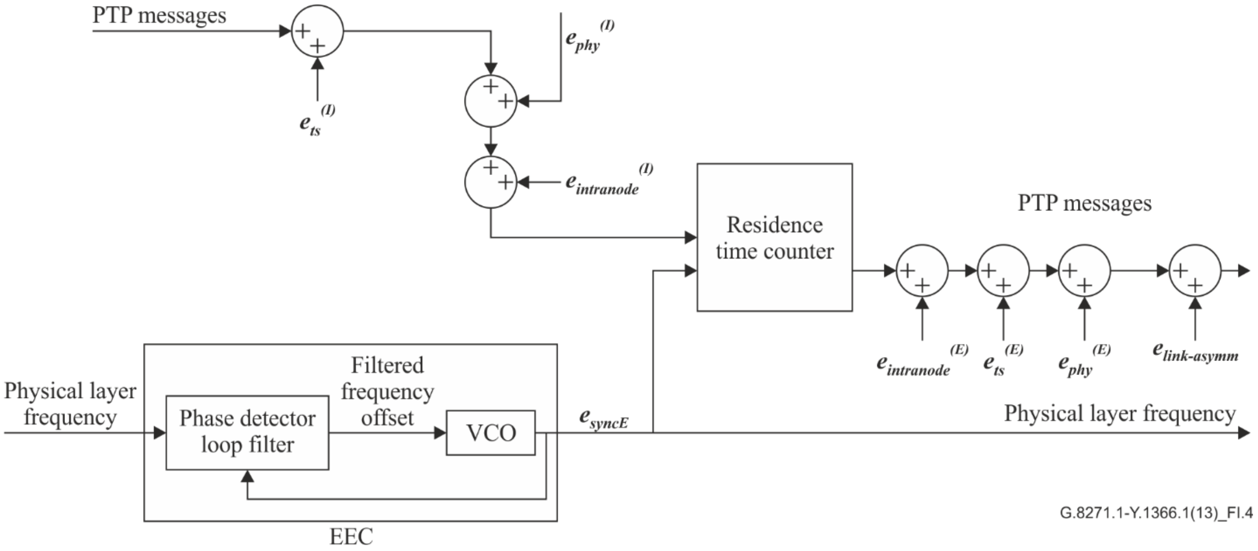


Figure I.4 – Telecom end-to-end transparent clock model for simulating the transport of time using PTP with synchronous Ethernet assistance

Figure I.4 illustrates a model for simulating the transport of time using PTP with optional synchronous Ethernet assistance for the case of an end-to-end transparent clock.

NOTE 1 – This model, used for the evaluation of a worst-case noise accumulation when synchronous Ethernet is combined with PTP, may not be representative of all possible implementations.

NOTE 2 – This model accounts for the noise added by the end-to-end transparent clock to the PTP flow in one direction only. End-to-end transparent clocks operate independently of the PTP traffic flow direction.

The EEC block represents an Ethernet equipment clock, as specified in [ITU-T G.8262]. The EEC input is a physical layer frequency (i.e., a physical layer signal that is used as a frequency reference), and its output is a local frequency (i.e., a physical layer signal that has a frequency and is local to this node) that is optionally propagated to downstream nodes. The noise process, e_{syncE}, represents the synchronous Ethernet phase noise accumulation in the synchronous Ethernet HRM (see Appendix II).

The residence time counter is incremented by the nominal period of the output clock of the EEC block. For example, if the output clock rate is 125 MHz, then the residence time counter is incremented by 8 ns each rising edge of the synchronous Ethernet output clock. Upon reception and transmission of PTP event messages, the residence time counter is sampled. The difference between the actual transmission/reception time and the sampled value of the time counter is modelled as e_{ts}

since the transmission/reception event can happen between two rising edges of this clock. The effect of e_{ts} on the timestamp for reception of a PTP event message is added at the input, and the effect of e_{ts} on the timestamp for transmission of a PTP event message is added at the output. Note that e_{ts} for ingress and egress ports can be uncorrelated and can be of different polarity.

The noise process, e_{phy}, represents the effect of asymmetry and timestamp sampling uncertainty on the PHY. The PHY latency asymmetry may be present if timestamping is done at a point other than the reference plane (i.e., the interface between the PHY and the physical medium). Any latency between the point where timestamping actually is done and the reference plane may be compensated for within PTP. However, any uncompensated latencies that result in asymmetry will contribute to e_{phy}. The noise, e_{phy}, is added to the timing information contained in the incoming PTP messages. Note that the random process, e_{phy}, may have a static component and a time-varying component.

The residence time counter produces a residence time. The input to the residence time counter is the frequency output of the EEC and the ingress and egress time for the PTP event frame.

The residence time counter is sampled upon reception of PTP event messages on ports. The residence time counter will add the accumulation of the synchronous Ethernet phase noise, e_{syncE}, during the residence time.

Errors due to intranode transmission, $e_{intranode}$, and link asymmetry, $e_{link\text{-}asymm}$, must also be included. The latter is shown added to the output of the TC.

Figure I.5 is an equivalent model suitable for analytical studies.

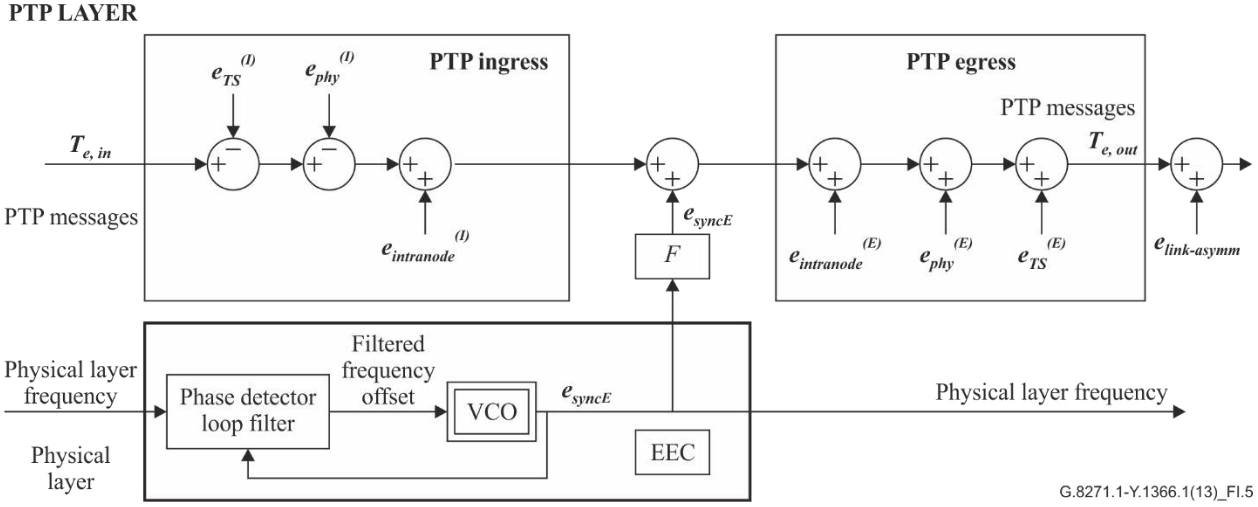


Figure I.5 – Telecom transparent clock model for analytical studies of the transport of time using PTP with synchronous Ethernet assistance.

In Figure I.5, the physical layer clock introduces a time error corresponding to the wander (e_{syncE}) that occurs between the ingress timestamp point and the egress timestamp point. This is equivalent to the time interval error over an observation interval equal to the packet's residence time. As a conservative approximation, this can be modelled as the change of the local clock's time error signal over the maximum allowed residence time R. In the figure above this is indicated by the operator F.

The value of the maximum residence time, R, is for further study. The model for a TC using a free running oscillator to measure the residence time can be modelled using the same model with the EEC replaced with a model for a free running oscillator. This is shown in Figure I.6. For free-running oscillators that have a significant frequency offset, or for relatively large residence times, the error introduced may be dominated by this frequency offset.

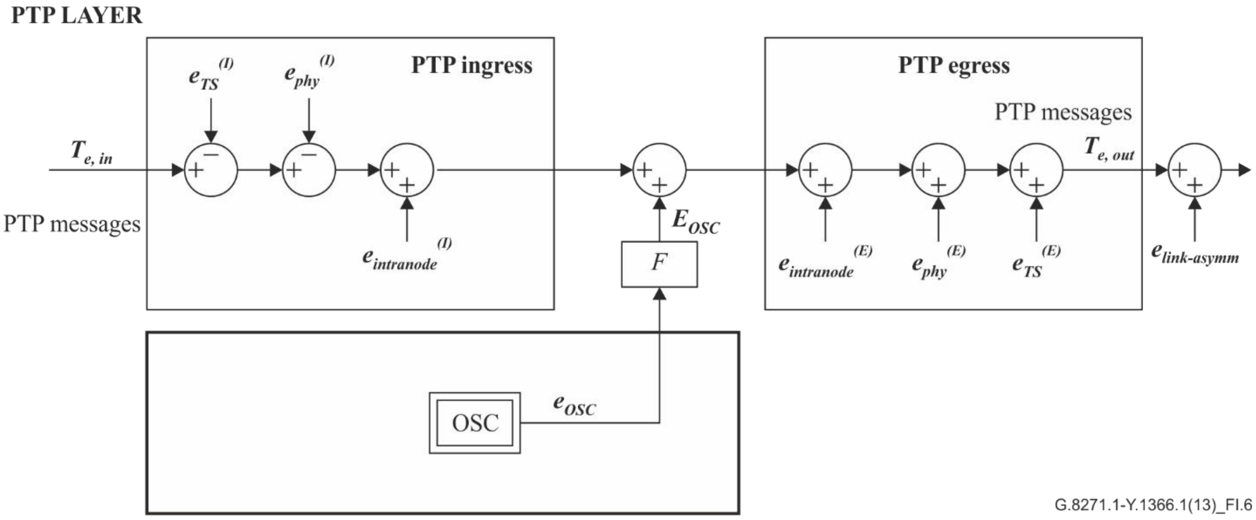


Figure I.6 – Telecom transparent clock model for analytical studies of the transport of time using PTP without synchronous Ethernet assistance

The simulation model for an end-to-end transparent clock using PTP for frequency reference (syntonized transparent clock) is for further study.

Appendix II

HRMs used to derive the network limits

(This appendix does not form an integral part of this Recommendation.)

II.1 HRM composed of T-BCs

The HRM models that are presented in the following caluses are applicable to the network reference models defined in Figure 4 of [ITU-T G.8271] and Figure 7-1 of this Recommendation. This is essential to derive the network limits between point 'B to C' when the packet network consists of network elements with T-BCs.

The purpose of these HRMs is to:

- establish reasonable worst-case network models for phase/time distribution using T-BCs;
- derive network limits and verify that they are consistent with performance requirements. Some of the performance requirements are summarized in Table 1 of [ITU-T G.8271];
- construct end-to-end phase and time error budget.

To determine the network limits, the most important aspects that need to be considered when a reference network is constructed are those that influence the accumulation of phase and time error of a reference "packet time signal" that is transported, and some of these are:

- specification of individual clocks and their noise specifications. In this case [ITU-T G.8273] shall be considered for the characteristics of the clock implemented in the T-BC. The model of the T-BC for noise accumulation simulations is described in Appendix I.
- the composition of a synchronization chain, cascade of clocks and ordering of clocks. This is defined by the related HRM.
- other sources of errors besides the noise generated by clocks. These are described in Appendix I of [ITU-T G.8271].

The following HRMs are based on a shorter chain of 12 clocks and a longer chain of 22 clocks.

II.1.1 HRM without physical layer frequency support from the network

The reference chain below shows a T-GM clock and a T-TSC interconnected by a number of T-BCs.

In this HRM-1 model, both frequency and time are transported via PTP. Both frequency and time follow the same synchronization path. The T-GM acts as both the source of frequency and time (e.g., the T-GM can receive its time and frequency from a global navigation satellite system (GNSS) receiver).

At the end of the chain, the phase/time reference is delivered to an end application (e.g., a mobile base station). Two cases are possible and are represented in the figure below:

1. The T-TSC is embedded in the end application.
2. The T-TSC is external to the end application, and delivers the phase/time reference to the end application via a phase/time synchronization distribution interface (e.g., 1 pulse per second (1 PPS) interface).

NOTE 1 – A specific equipment implementation may also be based on implementing a T-BC function (instead of a T-TSC function) and delivering the phase/time reference to the end application via a phase/time synchronization distribution interface.

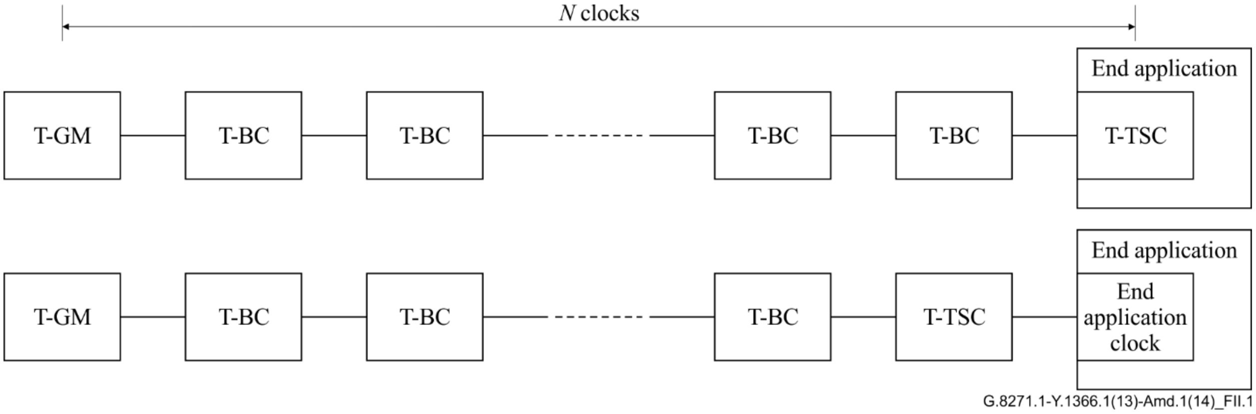


Figure II.1 – HRM-1 without physical layer frequency support

The number of clocks, *N*, cascaded in the HRM-1 for the shorter chain is 12. It corresponds to:

- one T-GM, ten T-BCs and one T-TSC for the case of a T-TSC embedded in the end application;
- one T-GM, nine T-BCs, one T-TSC and the end application clock for the case of a T-TSC external to the end application.

The number of clocks, *N*, cascaded in the HRM-1 for the longer chain is 22. It corresponds to:

- one T-GM, 20 T-BCs and one T-TSC for the case of a T-TSC embedded in the end application;
- one T-GM, 19 T-BCs, one T-TSC and the end application clock for the case of a T-TSC external to the end application.

NOTE 2 − Noise accumulation in networks without physical layer frequency synchronization support is for further study.

II.1.2 HRM with physical layer frequency support from the network

The reference chains below represent the cases where phase/time is transported via PTP and frequency via synchronous digital hierarchy (SDH)/synchronous Ethernet.

NOTE 1 – The analysis has been done with a synchronous Ethernet network based on option 1 EECs (see [ITU-T G.8262]).

Congruent scenario

In this HRM-2 model, both frequency and phase/time follow the same synchronization path.

At the end of the chain, the phase/time reference is delivered to an end application (e.g., a mobile base station). Two cases are possible and are represented in the figure below:

1. The T-TSC is embedded in the end application.
2. The T-TSC is external to the end application, and delivers the phase/time reference to the end application via a phase/time synchronization distribution interface (e.g., 1PPS interface).

NOTE 2 – A specific equipment implementation may also be based on implementing a T-BC function (instead of a T-TSC function) and delivering the phase/time reference to the end application via a phase/time synchronization distribution interface.

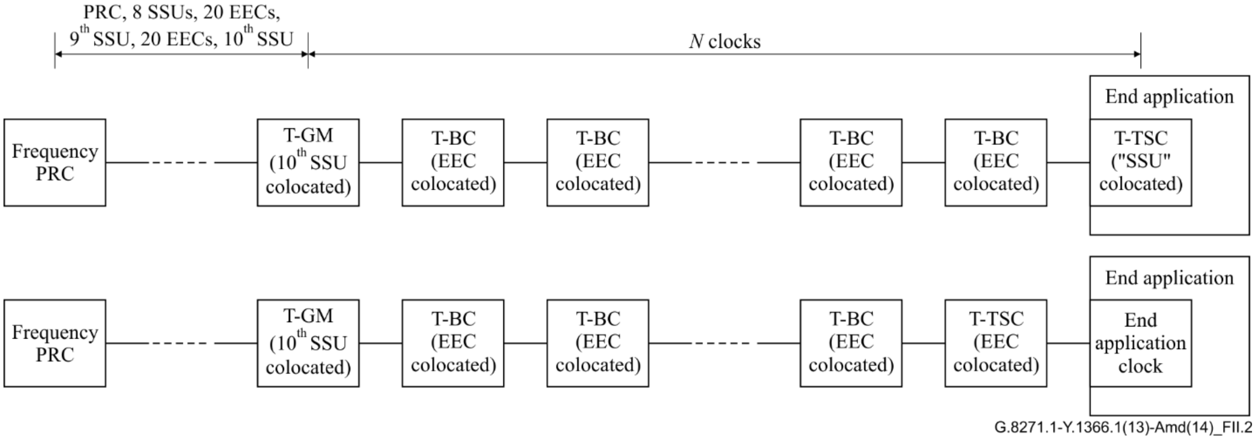


Figure II.2 – HRM-2 with physical layer frequency support – congruent scenario

The number of clocks, *N*, cascaded in the HRM-2 for the shorter chain is 12. It corresponds to:

- one T-GM, ten T-BCs and one T-TSC for the case of a T-TSC embedded in the end application;
- one T-GM, nine T-BCs, one T-TSC and the end application clock for the case of a T-TSC external to the end application.

The number of clocks, *N*, cascaded in the HRM-1 for the longer chain is 22. It corresponds to:

- one T-GM, 20 T-BCs and one T-TSC for the case of a T-TSC embedded in the end application;
- one T-GM, 19 T-BCs, one T-TSC and the end application clock for the case of a T-TSC external to the end application.

The following physical layer frequency clocks are co-located with the PTP clocks:

- for the T-GM: a synchronization supply unit (SSU) supporting phase/time transport;
- for the T-BC: an EEC supporting phase/time transport;
- for the T-TSC external to the end application: an EEC supporting phase/time transport;
- for the T-TSC embedded in the end application: the clock supporting phase/time transport is for further study. The initial assumption is that this clock might be close to the characteristics of an SSU (e.g., equivalent type of oscillator, but some characteristics of the clock may be different, e.g., different bandwidth). For the purpose of the simulations it is assumed that this clock is the only timing function of the end application (no other clock is cascaded after).

The SDH/synchronous Ethernet reference chain is a full [ITU-T G.803] reference chain with the EECs as close to the end of the chain as possible: a PRC, followed by 8 SSUs, followed by 20 EECs, followed by an SSU, followed by 20 EECs, followed by an SSU (co-located with the T-GM), followed by 9 EECs (each co-located with a T-BC) related to the shorter chain or 19 EECs (each co-located with a T-BC) related to the longer chain, followed by a final EEC (co-located with the T-TSC external to the end application or with a last T-BC). A final clock is at the end of the chain: either the "end application clock", or a clock co-located with the T-TSC embedded in the end application.

Non-congruent scenario

In this HRM-3 model, phase/time and frequency synchronization follow different synchronization paths (i.e., phase/time is distributed horizontally and frequency vertically). This model is similar in spirit to Figure A.1 of [ITU-T G.823] and is used to represent a possible worst-case scenario when PTP and SDH/synchronous Ethernet are used.

At the end of the chain, the phase/time reference is delivered to an end application (e.g., a mobile base station). Two cases are possible and are represented in the figures below:

1. The T-TSC is embedded in the end application;
2. The T-TSC is external to the end application, and delivers the phase/time reference to the end application via a phase/time synchronization distribution interface (e.g., 1PPS interface).

NOTE 3 – A specific equipment implementation may also be based on implementing a T-BC function (instead of a T-TSC function) and delivering the phase/time reference to the end application via a phase/time synchronization distribution interface.

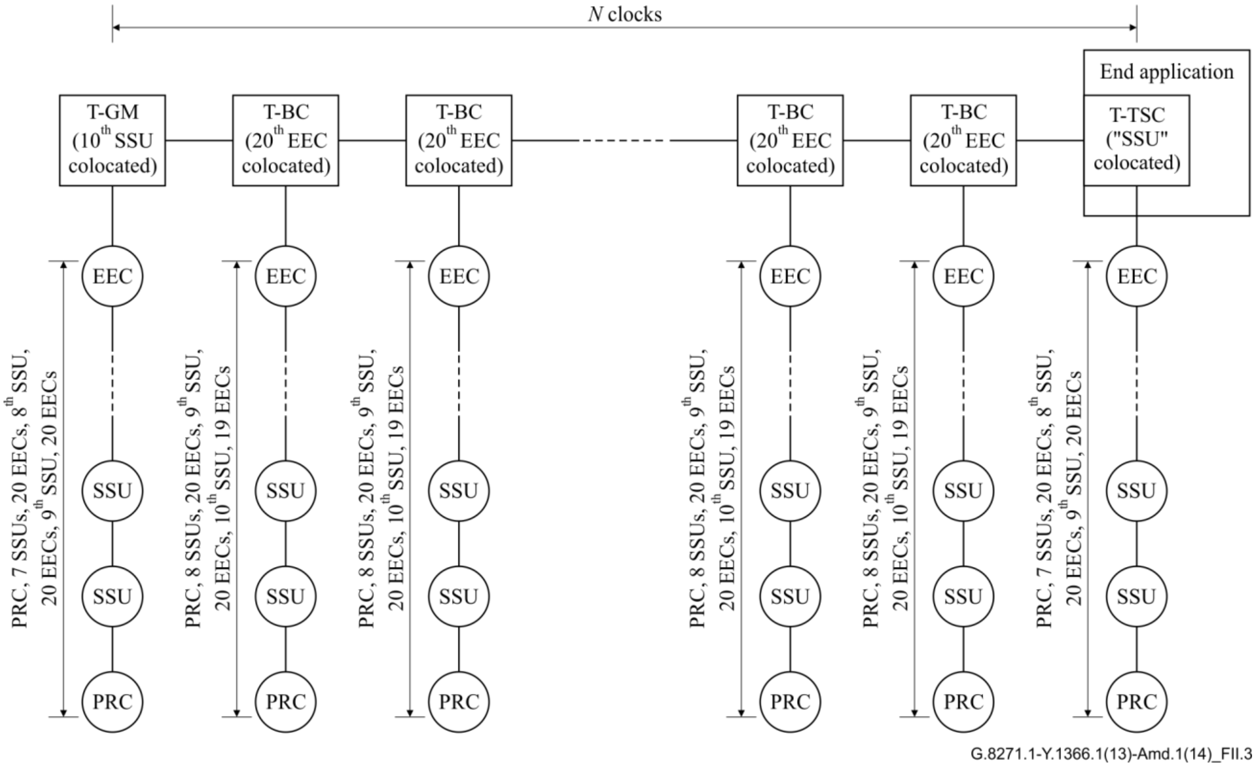


Figure II.3 – HRM-3 with physical layer frequency support – non-congruent scenario, deployment case 1

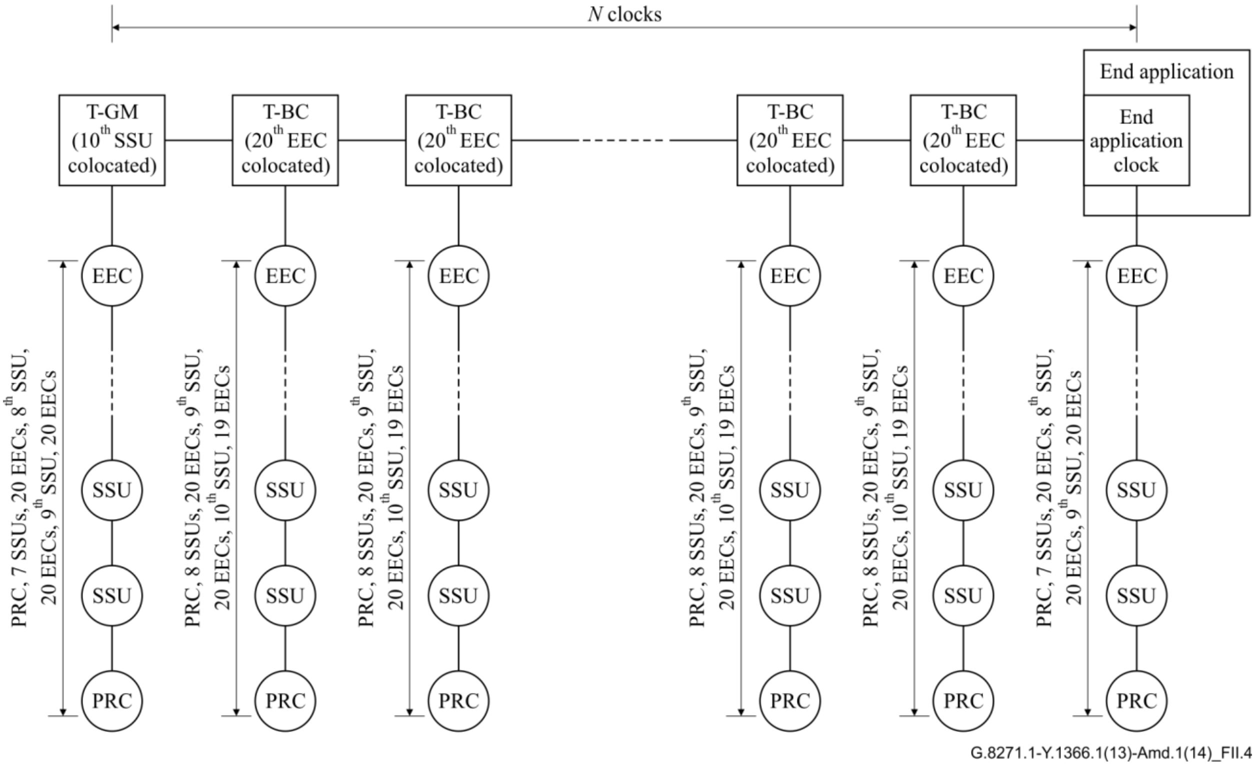


Figure II.4 – HRM-3 with physical layer frequency support – non-congruent scenario, deployment case 2

The number of clocks, *N*, cascaded in the HRM-3 for the shorter chain is 12. It corresponds to:

- one T-GM, ten T-BCs and one T-TSC for the case of a T-TSC embedded in the end application;
- one T-GM, nine T-BCs, one T-TSC and the end application clock for the case of a T-TSC external to the end application.

The number of clocks, *N*, cascaded in the HRM-1 for the longer chain is 22. It corresponds to:

- one T-GM, 20 T-BCs and one T-TSC for the case of a T-TSC embedded in the end application;
- one T-GM, 19 T-BCs, one T-TSC and the end application clock for the case of a T-TSC external to the end application.

The following physical layer frequency clocks are co-located with the PTP clocks:

- for the T-GM: an SSU supporting phase/time transport;
- for the T-BC: an EEC supporting phase/time transport;
- for the T-TSC external to the end application: an EEC supporting phase/time transport;
- for the T-TSC embedded in the end application: the clock supporting phase/time transport is for further study. The initial assumption is that this clock might be close to the characteristics of an SSU (e.g., equivalent type of oscillator, but some characteristics of the clock may be different, e.g., different bandwidth). For the purpose of the simulations it is assumed that this clock is the only timing function of the end application (no other clock is cascaded after).

The SDH/synchronous Ethernet reference chain is a full [ITU-T G.803] reference chain with the EECs as close to the end of the chain as possible (the final SSU may be at the end of the chain):

- for the PTP clocks supported by an EEC: a PRC, followed by 8 SSUs, followed by 20 EECs, followed by an SSU, followed by 20 EECs, followed by an SSU, followed by 19 EECs with the 20th EEC being integrated in the T-BC or T-TSC clock;
- for the PTP clocks supported by an SSU: a PRC, followed by 7 SSUs, followed by 20 EECs, followed by an SSU, followed by 20 EECs, followed by an SSU, followed by 20 EECs with the 10th SSU being integrated in the T-GM or T-TSC clock .

Appendix III

Network limits considerations

(This appendix does not form an integral part of this Recommendation.)

III.1 Measurement of network limits in case of deployment case 1

In the case of a network with full timing support and a T-BC as the last equipment of the chain, the measurement of the network limits for deployment case 1 at reference point C can be performed according to the following main approaches (note, telecom transparent clock (T-TC) may be integrated in the chain; this is for further study):

a) If available, via the output PPS test interface from the last BC of the chain (see Figure III.1). Note that, any additional source of error between the 1PPS measurement point and the actual reference point C has to be taken into account (e.g., link asymmetry).

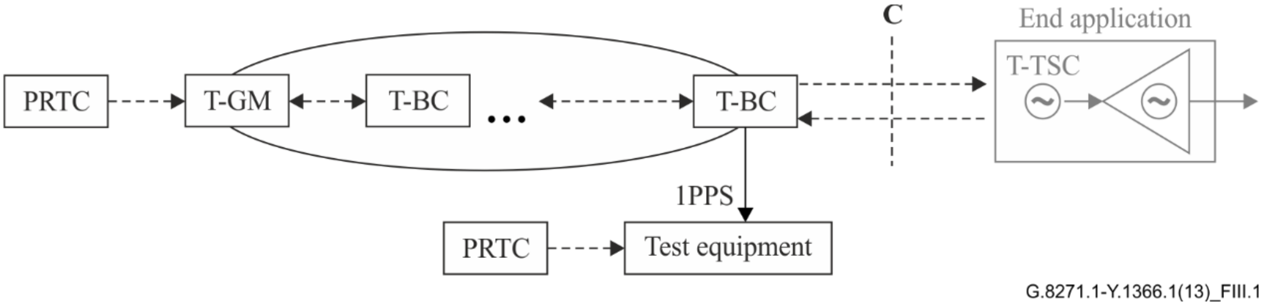


Figure III.1 – Deployment case 1 network limits measurement, option a)

b) Directly from the two-way PTP flow via a passive PTP monitor equipment (see "packet timing monitor" definition in [ITU-T G.8260]) connected to the test equipment. With the passive technique, a packet-based test device monitors packet exchanges over a communication link. In this way, the test device acts as an observer and it does not directly participate in the packet timing protocol, and there may be significant other non-synchronization-related traffic loading the T-BC port in addition to the synchronization packets of interest. This measurement can be performed by monitoring the outgoing Sync messages (and Follow_Up messages in case of two-steps clocks). Compensation for the additional delay between the T-BC output port and the test equipment is required. In particular, if the cable delay from the master port to the tap is known as "X" ns and the monitor establishes the time-of-passage of the Sync message at the tap as TM2 and extracts the time-of-departure from the master port as the time-stamp T1 (it may need to use the Follow_up), the forward time error of the master port is estimated as:

$$T_{fwd\_error} \approx (\mathrm{TM2} - \mathrm{T1} - \mathrm{X})$$

As an alternative, the packets in the reverse direction could also be used. In this case, the Delay Request messages can be timestamped by the PTP monitor with corresponding Delay Response messages providing timestamps from the T-BC. As before, compensation for the additional delay between the T-BC output port and the test equipment is required. For a cable delay of "X" ns, if the PTP Monitor timestamp of the Delay Request message is TM3 and the timestamp from the Delay Response message is T4, the reverse time error of the master port is estimated as the reverse time-stamp error:

$$T_{rev\_error} \approx (\mathrm{TM3} - \mathrm{T4} + \mathrm{X})$$

According to a further alternative approach the measurement can be performed using the full set of PTP messages exchanged between the T-TSC and the T-BC. In particular, the monitor establishes the time-of-passage of the Sync message at the tap as TM2 and reads the time-of-departure of the Sync message from the master port as T1. It also establishes the time-of-passage of the Delay_Request message at the tap as TM3 and reads the time-of-arrival of the Delay_Request message at the master port from the Delay_Response message as T4. Assuming that the packet rates in the two directions are the same and that the Sync message and Delay_Request message are close together in time, combined fwd/reverse time error, or time-transfer error, at the (master) port of the T-BC can be estimated as:

$$T_{combined\_error} \approx (TM2 - T1 - T4 + TM3)/2$$

The case where the forward and reverse packet rates are different, or require interpolation, is for further study.

The effective time error of the T-BC, $T_{err}(t)$ (either the forward time-stamp error, reverse time-stamp error or combined error) may be used to estimate the relevant metrics, such as the constant time error as described in [ITU-T G.8260].

It is noted that because this Recommendation addresses network performance requirements, it is expected that the three aforementioned error formulae provide equally valid estimates of the time error of the T-BC's internal clock.

Additional information regarding measurement of master port time-stamp error and time-transfer error is available in Annex A of [ITU-T G.8273].

This approach is described in Figure III.2.

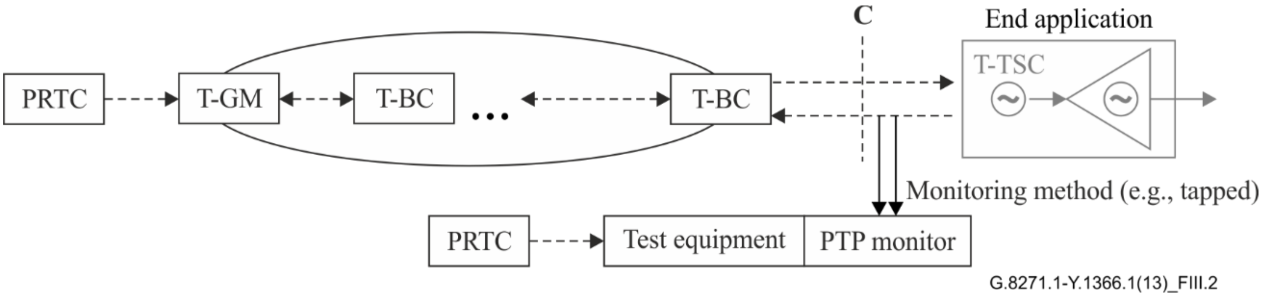


Figure III.2 – Deployment case 1 network limits measurement, option b)

c) From the two-way PTP flow via an active measurement probe (e.g., prior to the start of the service, or connecting the active monitor to a dedicated port of the T-BC). The measurement is performed using the full set of the PTP messages exchanged between the test equipment and the T-BC.

In particular, the monitor establishes the time-of- arrival of the Sync message as T2 and reads the time-of-departure of the Sync message from the master port as T1. It also establishes the time-of- departure of the Delay_Request message from the PTP Monitor as T3 and reads the time-of-arrival of the Delay_Request message at the master port from the Delay_Response message as T4. Assuming that the Sync message and Delay_Request message packet rates are the same and that the Sync message and Delay_request message are close together in time, an estimate of the time error at the port of the T-BC can be computed as:

$$T_{combined\_error} \approx (T2 - T1 - T4 + T3)/2$$

The case where the forward and reverse packet rates are different, or require interpolation, is for further study.

Additional information regarding measurement of the master port time-stamp error and time-transfer error is provided in [ITU-T G.8273] Annex A.

Assuming all ports of the T-BC behave similarly, the effective time error of the T-BC, $T_{err}(t)$ (either the forward time-stamp error, reverse time-stamp error or combined error) may be used to estimate the relevant metrics, such as the constant time error as described in [ITU-T G.8260].

This approach is described in Figure III.3.

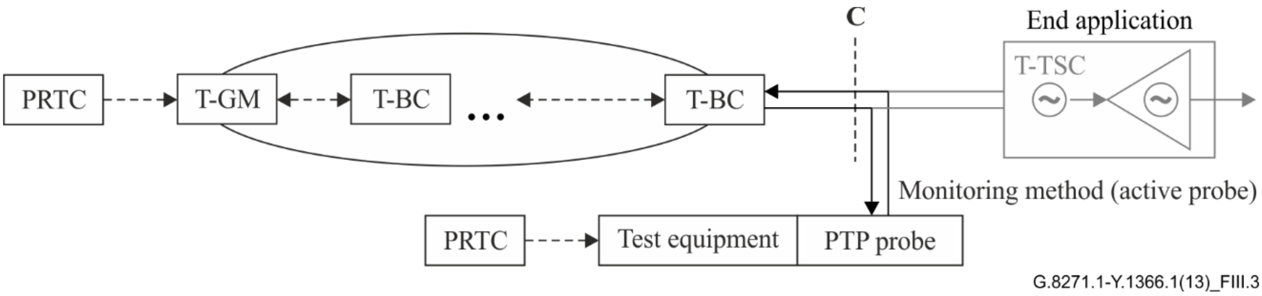


Figure III.3 – Deployment case 1 network limits measurement, option c)

In all cases the measurement is performed with respect to a PRTC.

Appendix IV

Constant and dynamic time error and error accumulation

(This appendix does not form an integral part of this Recommendation.)

IV.1 Introduction

Network limits for time error are expressed in terms of maximum absolute time error. That is, if time error measurement data is the sequence, $\{x(n\tau_0)\}$, the maximum absolute time error is

$$\max|TE| = \max_n |x(n\tau_0)| \tag{IV-1}$$

It may be advantageous to consider the time error in terms of "time-wander" and "time-jitter", representing the lower and higher frequency components of the time error. Denoting by $\{y(n\tau_0)\}$ the low-pass-filtered version of $\{x(n\tau_0)\}$, the maximum absolute time-wander is given by

$$\max|TE_W| = \max_n |y(n\tau_0)| \tag{IV-2}$$

where the subscript indicates that the measurement is related to time-wander. The Fourier frequency separating time-wander (the cut-off frequency of the low-pass filter) is for further study.

The time error measurement data, $\{x(n\tau_0)\}$, is generated either from the packet-based timing signal (e.g., PTP) or from a dedicated time output signal (e.g., 1PPS).

IV.2 Components of time error

The accumulated time error, $TE(t)$, at any reference point may be expressed in terms of a constant and a dynamic time error component, indicated as cTE and $dTE(t)$, respectively.

$$TE(t) = cTE + dTE(t) \tag{IV-3}$$

Constant time error, defined in [ITU-T G.8260], is a useful construct to express time error components that are immune to filtering. Such time error components are the result of, for example, asymmetry in the transmission medium between network elements, asymmetries within network elements, the beating effect in near-synchronous time-stamping, and so on. The power-spectrum of the constant time error is assumed to be equivalent to a delta function at $f = 0$ in the Fourier frequency domain.

The dynamic time error component, $dTE(t)$, is related to random noise accumulation (e.g., due to T-BC time-stamping or wander accumulated in the synchronous Ethernet network and injected into the time synchronization plane when synchronous Ethernet is used in combination with PTP or due to packet-delay variation experienced by the timing signal packets). The power spectrum of the dynamic time error is spread out over the Fourier frequency domain and the power can be reduced, to some extent, by low-pass filtering (e.g., as a result of the bandwidth of a given clock function within a network element).

To facilitate the analysis, it helps to further decompose the dynamic time error signal into two uncorrelated sub-components: $d^H TE(t)$ and $d^L TE(t)$ which represent the high and low frequency sub-bands of the dynamic time error, and where the bands are divided based on the bandwidth of the filter action of network element "i". Such decomposition is useful for analysing the accumulation of noise in a chain of time clocks. (Analysis of transient and hold-over budgets is also important, but is separate from this discussion). To a first approximation, the low-pass filter action of the network element can be modelled as an ideal low-pass filter with cut-off frequency B (Hz),

$$dTE(t) = d^L TE(t) + d^H TE(t) \tag{IV-4}$$

which separates the total time error into three components:

$$TE(t) = cTE + d^L TE(t) + d^H TE(t) \tag{IV-5}$$

The above decomposition of time error into three sub components is illustrated in the following table.

Table IV.1 – Decomposition of time error into sub-components

<table>
<tr><td rowspan="3">$TE(t)$</td><td colspan="2">cTE</td></tr>
<tr><td rowspan="2">$dTE(t)$</td><td>$d^{H}TE(t)$</td></tr>
<tr><td>$d^{L}TE(t)$</td></tr>
</table>

IV.3 Accumulation of time error in a chain of clocks

The accumulation of time error in a chain of clocks can be analysed in terms of the constant time error and dynamic time error components introduced above. It is important to note that the three components of time error described above accumulate differently. Specifically, the inherent low-pass nature of the clock filtering in a network element affects the incoming dynamic time error but passes the incoming constant time error component essentially unchanged. Furthermore, the network element may add both constant and dynamic time error. One approach to illustrating the accumulation of time error is described with reference to Figure IV.1.

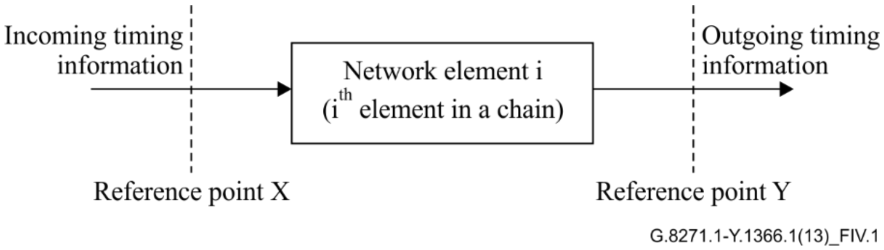


Figure IV.1 – Accumulation of time error

The maximum absolute time error at reference points X and Y are:

$$\max|TE_X(t)| = \max|cTE_X + dTE_X(t)| \tag{IV-6}$$

$$\max|TE_Y(t)| = \max|cTE_Y + dTE_Y(t)| \tag{IV-7}$$

where the subscripts "X" and "Y" indicates the value measured at reference points X and Y, respectively.

The constant time error at Y can be represented as the sum of the constant time error at X (cTE_X) plus the constant time error generated internally by the network element "i" (cTE_i)

$$cTE_Y = cTE_X + cTE_i \tag{IV-8}$$

The dynamic time error, dTE_Y, at Y is more complex, because a simple sum cannot be used. This is because the network element introduces a low-pass filter. As described above, the dynamic time error at X (the input of the network element "i") can be decomposed into high and low band sub-components:

$$dTE_X(t) = d^{L}TE_X(t) + d^{H}TE_X(t) \tag{IV-9}$$

and the dynamic time error introduced by the network element "i" can similarly be expressed in terms of low-frequency and high-frequency components as:

$$dTE_i(t) = d^{L}TE_i(t) + d^{H}TE_i(t) \tag{IV-10}$$

Then, the dynamic time error at Y (the output of the network element "i"), is a combination of the dynamic time error introduced by element "i" and the dynamic time error at X, the input dynamic time error being filtered by the processing of that element. The high band dynamic time error at X will, to a first approximation, be filtered out by the network element, while the low band dynamic time error at X will, to a first approximation, be passed through the network element. Low-band dynamic time error generated by the network element will, to some extent, be compensated by the time tracking action of the network element, but some residual low-band dynamic time error is expected to remain.

Therefore, we can represent the dynamic time error at Y in terms of the low band dynamic time error at X [$d^L TE_X(t)$], and the dynamic time error generated internally by network element "i" [$d^L TE_i(t)$ and $d^H TE_i(t)$]:

$$dTE_Y(t) \cong d^L TE_X(t) + d^L TE_i(t) + d^H TE_i(t) \qquad \text{(IV-11)}$$

Substituting these two decompositions into the equation for maximum absolute time error at Y, we get the following expression:

$$max|TE_Y| = max|(cTE_X + cTE_i) + (d^L TE_X(t) + d^L TE_i(t)) + d^H TE_i(t)| \qquad \text{(IV-12)}$$

Therefore, the maximum absolute time error at point Y depends on:

- the constant time error at X
- the constant time error introduced by network element "i"
- the low-band dynamic time error at X
- the dynamic time error introduced by network element "i" (low-band and high-band).

More generally, in a chain of time clocks, to a first order approximation:

- the constant time error, and link asymmetry, accumulates linearly
- the low-band dynamic time error accumulates incoherently
- the high-band dynamic time error is contributed mainly by the last element in the chain.

In a chain of time clocks, where the N nodes are indexed by the letter i, and the (N–1) links are indexed by the letter j, the maximum absolute time error at the output of the N^{th} node can be upper bounded as

$$\max|TE_N| \le \sum_{i=1}^{N} |cTE_i| + \sum_{j=1}^{N-1} |linkTE_j| + \sqrt{\left\{ \sum_{i=1}^{N} \left[\max\left|d^L TE_i(t)\right|\right]^2 \right\} + \left[\max\left|d^H TE_N(t)\right|\right]^2} \qquad \text{(IV-13)}$$

here $linkTE_j$ denotes the asymmetry of link j, RSS denotes the square root of the sum of the squares of the N low-band dynamic time error contributions from each node, and the high-band dynamic time error of the last (N^{th}) node.

With this construct, constant time error accumulates coherently (simple summation) and dynamic time error accumulates incoherently (square-root of sum of squares) for the low band; the high band dynamic time error is present only as the contribution from the last stage. Stated differently, the mean values of the various sources of time error accumulate linearly and the variances of the various sources of time error accumulate linearly.

Therefore, the performance specification of a network element should include the following:

- maximum allowed constant time error generation;
- maximum allowed low and high band dynamic time error generation;
- dynamic time error bandwidth range (min/max);
- minimum dynamic time error input tolerance.

Appendix V

Example of design options

(This appendix does not form an integral part of this Recommendation.)

As described in Appendix IV the network limits are expressed in terms of the maximum time error, max |TE| and this is the result of two main components:

1. the dynamic time error component, $dTE(t)$;
2. the constant time error component cTE.

In order to take into account:

a) the internal noise sources of the end application (indicated by TE_{EA})

b) the residual noise caused by the dynamic time error component, and

c) short holdover at the end application during rearrangements in the synchronization network (indicated by TE_{REA}),

the network limit applicable at reference point C expressed in terms of maximum absolute time error must satisfy the following relationship:

$$\max |TE| \leq (TE_D - TE_{EA} - TE_{REA}) \qquad \text{(V-1)}$$

with:

$$|(cTE + dTE')| + TE_{HO} \leq \max |TE| \qquad \text{(V-2)}$$

Where TE_D indicates the network limit at reference point D expressed in terms of maximum absolute time error, TE_{HO} represents the budget allocated to holdover and rearrangements in the network and $|dTE'|$ is the maximum absolute value of a filtered version of the dynamic time error component $dTE(t)$. In practice dTE' estimates the dynamic component of the time error at the output of the end application.

NOTE 1 – The end application is not required to handle long time synchronization holdover periods but only short interruptions that could be caused by network rearrangements. Time synchronization and rearrangements that may happen in the network and that are modeled by TE_{HO} are included in the network limits. As a first approximation, TE_{REA} and TE_{HO} shall not be considered at the same time; in fact, TE_{REA} assumes that the end application enters holdover as soon as a failure is detected in the network, while TE_{HO} assumes that the end application continues to be locked to the incoming reference and in this case there is no need to allocate a budget to TE_{REA}.

NOTE 2 – The terms cTE and dTE' in the previous relationship are not measured separately, but indicate the components that build max |TE|. In the worst case, cTE and dTE' are both of the same polarity, but in a specific deployment they may partly compensate each other if the polarity is different.

The simulations performed have shown that it is possible to limit $|dTE'|$ to 200 ns or less (i.e., in the worst case $|dTE'|$ = 200 ns), and this value is considered in the time error budgeting analysis. Refer to Appendices I and II for further information on these simulations.

NOTE 3 – In order to meet the TE_D limits, the End application shall tolerate noise at points C. In case $dTE(t)$ exceeds the target limit of 200 ns, the end application should provide appropriate filtering to reduce the noise at reference point D to the value of dTE', expressed in terms of maximum absolute time error. Further information is provided in Appendix VI.

NOTE 4 – The time to restore (e.g., time to lock to a secondary time-synchronization reference) at the end application depends on the availability of physical frequency synchronization support and on the characteristics of the clock implemented in the end application.

Further information on the protection scenarios and related budget is provided in this Appendix and in [ITU-T G.8275].

Based on (V-1) and (V-2), the following applies:

$$|cTE| \leq \mathrm{TE_D} - (\mathrm{TE_{EA}} + \mathrm{TE_{HO}} + dTE') \qquad \text{(V-3)}$$

or, in case the end application enters holdover during network rearrangements,

$$|cTE| \leq \mathrm{TE_D} - (\mathrm{TE_{EA}} + \mathrm{TE_{REA}} + dTE') \qquad \text{(V-3)'}$$

Assuming the worst case of $|dTE'| = 200$ ns, and $\mathrm{TE_{EA}} = 150$ ns,

$$|cTE| \leq \mathrm{TE_D} - (350\ \mathrm{ns} + \mathrm{TE_{HO}}) \qquad \text{(V-4)}$$

or, in case the End Application enters holdover during network rearrangements,

$$|cTE| \leq \mathrm{TE_D} - (350\ \mathrm{ns} + \mathrm{TE_{REA}}) \qquad \text{(V-4)'}$$

The constant time error component cTE is due to static contributions to the time error, mainly related to link asymmetries and PTP clock (T-BC, T-GM and T-TSC) constant time error accumulation.

NOTE 5 – cTE can be considered approximately constant over time assuming there are no changes in the network (e.g., re-routing).

In particular cTE can be expressed as follows:

$$|cTE| = ce_{ref} + ce_{ptp\_clocks} + ce_{link\_asyms} \qquad \text{(V-5)}$$

where ce_{ref} is the accuracy of the PRTC as specified in [ITU-T G.8272], ce_{ptp_clocks} is the sum of PTP clocks constant time error as planned to be defined as part of the T-BC specification, and ce_{link_asyms} is the overall time error due to link asymmetries. ce_{ptp_clocks} for m number of PTP clocks (T-GM, T-BC or T-TSC) in a chain can be expressed as follows:

$$ce_{ptp\_clocks} = \sum_{n=1}^{m} ce_{ptp\_clock,n} \qquad \text{(V-6)}$$

where $ce_{ptp\_clock,n}$ is the constant time error for each PTP clock.

ce_{link_asyms} for m+1 number of links can be expressed as follows:

$$ce_{link\_asyms} = \sum_{n=1}^{m+1} ce_{link\_asym,n} \qquad \text{(V-7)}$$

where $ce_{link\_asym,n}$ is the time error due to link asymmetry for each link.

Assuming Level of accuracy 4 as per Table 1 of [ITU-T G.8271] (i.e., $\mathrm{TE_D} = 1.5$ us) and that $ce_{ref} = 100$ ns, this leads to:

$$cTE = ce_{ref} + ce_{ptp\_clocks} + ce_{link\_asyms} \leq 1'500\ \mathrm{ns} - 350\ \mathrm{ns} - \mathrm{TE_{HO}} = 1'150\ \mathrm{ns} - \mathrm{TE_{HO}} \qquad \text{(V-8)}$$

and therefore

$$ce_{ptp\_clocks} + ce_{link\_asyms} + \mathrm{TE_{HO}} \leq 1'150\ \mathrm{ns} - 100\ \mathrm{ns} = 1'050\ \mathrm{ns} \qquad \text{(V-9)}$$

or, in case the End Application enters holdover during network rearrangements:

$$|cTE| = ce_{ref} + ce_{ptp\_clocks} + ce_{link\_asyms} \leq 1'500\ \mathrm{ns} - 350\ \mathrm{ns} - \mathrm{TE_{REA}} = 1'150\ \mathrm{ns} - \mathrm{TE_{REA}} \qquad \text{(V-10)}$$

and therefore

$$ce_{ptp\_clocks} + ce_{link\_asyms} + \mathrm{TE_{REA}} \leq 1'150\ \mathrm{ns} - 100\ \mathrm{ns} = 1'050\ \mathrm{ns} \qquad \text{(V-11)}$$

For the case of an HRM of 10 T-BCs, of constant TE of 50 ns (T-BC with constant time error class A, see [ITU-T G.8273.2]) and assuming that the constant time error for the T-GM also is 50 ns, this leads to

$$ce_{ptp\_clocks} = 50\ \mathrm{ns} + (10 \times 50\ \mathrm{ns}) = 550\ \mathrm{ns} \qquad \text{(V-12)}$$

and, therefore, in the worst case

$$\mathrm{TE}_{\mathrm{HO}} + e_{link\_asyms}\ 1'050\ \mathrm{ns} - 550\ \mathrm{ns} = 500\ \mathrm{ns} \qquad \text{(V-13)}$$

or, in case the end application enters holdover during network rearrangements:

$$\mathrm{TE}_{\mathrm{REA}} + e_{link\_asyms} = 1'050\ \mathrm{ns} - 550\ \mathrm{ns} = 500\ \mathrm{ns} \qquad \text{(V-14)}$$

For the case of an HRM of 20 T-BCs, of constant TE of 20 ns (T-BC with constant time error class B, see [ITU-T G.8273.2]), and assuming that the constant time error for the T-GM also is 20 ns, this leads to

$$ce_{ptp\_clocks} = 20\ \mathrm{ns} + (20 \times 20\ \mathrm{ns}) = 420\ \mathrm{ns} \qquad \text{(V-15)}$$

and, therefore, in the worst case

$$\mathrm{TE}_{\mathrm{HO}} + e_{link\_asyms} = 1'050\ \mathrm{ns} - 420\ \mathrm{ns} = 630\ \mathrm{ns} \qquad \text{(V-16)}$$

or, in case the end application enters holdover during network rearrangements:

$$\mathrm{TE}_{\mathrm{REA}} + e_{link\_asyms} = 1'050\ \mathrm{ns} - 420\ \mathrm{ns} = 630\ \mathrm{ns} \qquad \text{(V-17)}$$

NOTE 6 – The deployment of a long chain of clocks requires particular attention in the network planning (e.g., in the control of link asymmetries, also after network rearrangements), for which the design of networks with shorter chain of clocks might be often considered more appropriate.

In order to provide an example on how time error can be allocated in a typical network deployment, some consideration can be made on potential network failure conditions in order to evaluate possible values for $\mathrm{TE}_{\mathrm{HO}}$ while meeting the overall requirement:

$$|cTE + dTE'| + \mathrm{TE}_{\mathrm{HO}} \leq \max |\mathrm{TE}| = 1'100\ \mathrm{ns}, \text{ as per clause 7.2.}$$

The long-term holdover condition is handled as a special case where the 1.5 μs limit is exceeded, assuming this is a particularly rare event. The time error due to the holdover in this case is assumed to be, in the worst case, 2'400 ns. Short-term failure conditions should instead be handled within the 1.5 μs requirement. In particular, there are two main short-term failure conditions that can be considered relevant:

a) T-GM change (e.g., due to loss of PRTC traceability of one of the redundant GMs in the network). A typical case is when the End Application enters holdover for a short period (e.g., 1 minute);

b) Short interruption of the GNSS signal (e.g., 5 minutes), As an example this might be relevant for a case of synchronous Ethernet (or internal oscillator) used as back up to the PRTC and the end application continues to be locked to the PTP reference.

As an example, it could be assumed that failure scenario a) can be handled within $\mathrm{TE}_{\mathrm{REA}} = 250$ ns (in the case where the rearrangement is handed within 60 s).

Depending on a specific deployment, only failure scenario a) or b) might be of interest.

The following table presents an example related to failure scenario a) (NOTE – The terms building the network limit of 1'100 ns are indicated by a shaded area in the table), an example of failure condition b where the network limit of 1'100 ns at point C would be exceeded (this is for further study) and an example of a long-time synchronization holdover that would lead to exceeding the target requirement TE_{D} at reference point D.

Table V.1 – Example of time error allocation

Budget Component	Failure scenario a)	Failure scenario b)	Long Holdover periods (e.g., 1 day)
PRTC (ce_{ref})	100 ns	100 ns	100 ns
Holdover and Rearrangements in the network (TE_{HO})	**NA**	**400 ns**	**2'400 ns**
Random and error due to synchronous Ethernet rearrangements (dTE')	200 ns	200 ns	200 ns
Node Constant including intrasite (ce_{ptp_clock})	550 ns (Note 1)	550 ns (Note 1)	550 ns (Note 1)
	420 ns (Note 2)	420 ns (Note 2)	420 ns (Note 2)
Link Asymmetries (ce_{link_asym}) (Note 3)	250 ns	100 ns	100 ns
	380 ns	230 ns	230 ns
Rearrangements and short Holdover in the End Application (TE_{REA})	250 ns	**NA**	NA
End application (TE_{EA})	150 ns	150 ns	**150 ns**
Total (TE_D)	**1'500 ns**	**1'500 ns**	**3'500 ns (Note 4)**

NOTE 1 – It is assumed in these examples that the T-GM and all T-BCs contribute constant TE of 50 ns as per type A T-BC (see [ITU-T G.8273.2]).

In deployment case 1 the HRM is composed of: 10 T-BCs, 1 T-GM and 11 links.

In deployment case 2 the HRM is composed of: 1 T-GM, 1 T-TSC, 9 T-BCs, 1 intra-site link, and 10 links. The time error budget allocated to the time synchronization distribution in the intra-site connection between the packet clock and the end application in the worst case is 50 ns. In order to get the same constant time error limit as per deployment case 1, it should be assumed that, for example, the T-GM, the T-TSC, and the intra-site connection contribute with 100 ns in total.

NOTE 2 – It is assumed in these examples that the T-GM and all T-BCs contribute constant TE of 20 ns as per type B T-BC clock (see [ITU-T G.8273.2]).

In deployment case 1 the HRM is composed of: 20 T-BCs, 1 T-GM and 21 links.

In deployment case 2 the HRM is composed of: 1 T-GM, 1 T-TSC, 19 T-BCs, 1 intra-site link, and 20 links. The time error budget allocated to the time synchronization distribution in the intra-site connection between the packet clock and the end application in the worst case is 20 ns. In order to get the same constant time error limit as per deployment case 1, it should be assumed that, for example, the T-GM, the T-TSC, and the intra-site connection contribute with 40 ns in total.

NOTE 3 – In order to simplify the comparison between deployment cases 1 and 2, the same number of links should be assumed in both deployment cases. In order to do that, the additional link of the deployment case 1 model, could be combined with the T-GM budget.

NOTE 4 – Exceeding the TE_D limit of 1’500 ns is related to the operator requirements in terms of service degradation.

2.6) Appendix VI, Mitigation of time error due to synchronous Ethernet transients

Replace Appendix VI with the following text:

Appendix II, clause II.1.2 illustrates HRMs for the transport of phase/time via PTP with physical layer frequency support. Figure II.2 illustrates the congruent scenario, where the frequency and phase/time transports follow the same synchronization path. Figure III.3 illustrates the non-congruent scenario, where the frequency and phase/time transports follow different synchronization paths. A rearrangement of the physical layer frequency, e.g., synchronous Ethernet, transport results in phase/time error at each T-BC, the T-TSC, and the end application. The time error is generally larger in the congruent scenario than in the non-congruent scenario, because in the congruent scenario each T-BC has errors due to the rearrangement transient in both the time and frequency planes. The latter occurs in the physical layer frequency input to a T-BC, and the former occurs in PTP Sync messages input to a T-BC from the upstream T-BC. In the non-congruent scenario, a T-BC has an error due only to the physical layer frequency input (assuming that only one synchronous Ethernet reference chain at a time undergoes a rearrangement).

Details on requirements and solutions to address this issue are provided in [ITU-T G.8273.2].

NOTE 1 – In the case where in the congruent scenario the T-BC does not comply with [ITU-T G.8273.2] Annex B, the time error due to the synchronous Ethernet rearrangement can be reduced to an acceptable level by using an end application clock with sufficiently narrow bandwidth and sufficiently small gain peaking, and by collocating a suitable clock with the end application in the frequency plane. For the HRM of Appendix II, a maximum end application clock bandwidth of 5 MHz, with a maximum gain peaking of 0.1 dB, will reduce the time error due to the synchronous Ethernet rearrangement to an acceptable level. The analysis was done assuming an [ITU-T G.812] type I clock is collocated with the end application clock in the frequency plane; however, a different type of clock might still result in an acceptable time error. This has not been verified.

In the non-congruent scenario, the time error will be acceptable if the T-BCs, T-TSC, and end application have minimum bandwidth of 0.05 Hz, maximum bandwidth of 0.1 Hz and maximum gain peaking of 0.1 dB, and if the frequency plane clocks collocated with the T-BCs, T-TSC, and end application are EECs. This is true whether or not the synchronous Ethernet transient is rejected at each T-BC.

NOTE 2 – The case of a network where synchronization status message (SSM) is not used is for further study.

Appendix VI

Mitigation of time error due to synchronous Ethernet transients

(This appendix does not form an integral part of this Recommendation.)

Appendix II, clause II.1.2 illustrates HRMs for the transport of phase/time via PTP with physical layer frequency support. Figure II.2 illustrates the congruent scenario, where the frequency and phase/time transports follow the same synchronization path. Figure III.3 illustrates the non-congruent scenario, where the frequency and phase/time transports follow different synchronization paths. A rearrangement of the physical layer frequency, e.g., synchronous Ethernet, transport results in phase/time error at each T-BC, the T-TSC, and the end application. The time error is generally larger in the congruent scenario than in the non-congruent scenario, because in the congruent scenario each T-BC has errors due to the rearrangement transient in both the time and frequency planes. The latter occurs in the physical layer frequency input to a T-BC, and the former occurs in PTP Sync messages input to a T-BC from the upstream T-BC. In the non-congruent scenario, a T-BC has an error due only to the physical layer frequency input (assuming that only one synchronous Ethernet reference chain at a time undergoes a rearrangement).

Details on requirements and solutions to address this issue are planned to be defined in the relevant recommendation (e.g., requirements on the T-BC). As an example, in the congruent scenario, the time error due to the synchronous Ethernet rearrangement can be reduced to an acceptable level if the physical layer signal is rejected after the physical layer transient is detected. Note that the rejection of the physical layer signal is an implementation method. This method permits switching temporarily, for a short period, upon detection of a synchronous Ethernet failure (e.g., using the synchronization status message (SSM) information), from a mode where synchronous Ethernet support is used for frequency transport to a mode where only the PTP messages are used to recover frequency; after the synchronous Ethernet reconfiguration is completed, the mode of operation is still expected to become again based on synchronous Ethernet for frequency transport. Specifically, the synchronous Ethernet signal is rejected when the SSM indicating the synchronous Ethernet signal is no longer PRC-traceable is received by the EEC collocated with that T-BC, and the synchronous Ethernet signal is again used at a time, $T_{reacq,}$ after receipt of the SSM indicating the synchronous Ethernet signal is again PRC-traceable is received by the EEC collocated with that T-BC. Any phase jump when the synchronous Ethernet signal is rejected must not exceed X, and any phase jump when the synchronous Ethernet signal is reacquired must not exceed Y.

The values T_{reacq}, X and Y are being defined as part of the T-BC specification.

NOTE 1 – Alternative solutions might be considered, e.g., acting on the PLL bandwidth filtering in the time synchronization plane.

NOTE 2 – In the case where in the congruent scenario the T-BC does not meet these additional requirements, the time error due to the synchronous Ethernet rearrangement can be reduced to an acceptable level by using an end application clock with sufficiently narrow bandwidth and sufficiently small gain peaking, and by collocating a suitable clock with the end application in the frequency plane. For the HRM of Appendix II, a maximum end application clock bandwidth of 5 MHz, with a maximum gain peaking of 0.1 dB, will reduce the time error due to the synchronous Ethernet rearrangement to an acceptable level. The analysis was done assuming an [ITU-T G.812] type I clock is collocated with the end application clock in the frequency plane; however, a different type of clock might still result in an acceptable time error. This has not been verified.

In the non-congruent scenario, the time error will be acceptable if the T-BCs, T-TSC, and end application have maximum bandwidth of 0.1 Hz and maximum gain peaking of 0.1 dB, and if the frequency plane clocks collocated with the T-BCs, T-TSC, and end application are EECs. This is true whether or not the synchronous Ethernet transient is rejected at each T-BC.

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