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ITU-T G.8272.1 (01/2024)

SERIES G: Transmission systems and media, digital systems and networks

Packet over Transport aspects – Synchronization, quality and availability targets

Timing characteristics of enhanced primary reference time clocks

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Recommendation ITU-T G.8272.1

Timing characteristics of enhanced primary reference time clocks

Summary

Recommendation ITU-T G.8272.1 specifies the requirements for enhanced primary reference time clocks (ePRTCs) suitable for time and phase synchronization in packet networks. It defines the error allowed at the time output of the ePRTC. These requirements apply under the normal environmental conditions specified for the equipment.

History *

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Enhanced primary reference time clock, ePRTC, primary reference time clock, PRTC, synchronization, time error, wander.

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Recommendation ITU-T G.8272.1

Timing characteristics of enhanced primary reference time clocks

1 Scope

This Recommendation specifies the requirements for enhanced primary reference time clocks (ePRTCs) suitable for time, phase and frequency synchronization in packet networks. These requirements apply under the normal environmental conditions specified for the equipment.

The ePRTC provides a reference time signal traceable to a recognized time standard (e.g., coordinated universal time (UTC)) and also a frequency reference. Compared with the primary reference time clock (PRTC) as defined in [ITU-T G.8272], the ePRTC is subject to more stringent output performance requirements and includes a frequency input directly from an autonomous primary reference clock. The performance of the autonomous primary reference clock for this particular application is specified in Annex A.

An ePRTC provides the reference signal for time, phase and frequency synchronization for clocks within a network or section of a network. In particular, the ePRTC can also provide the reference signal to the telecom grand master (T-GM) within the network node where the ePRTC is located.

This Recommendation defines the ePRTC output requirements, including for an ePRTC integrated with a T-GM clock.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T G.703] Recommendation ITU-T G.703 (2016), *Physical/electrical characteristics of hierarchical digital interfaces*.

[ITU-T G.810] Recommendation ITU-T G.810 (1996), *Definitions and terminology for synchronization networks*.

[ITU-T G.811] Recommendation ITU-T G.811 (1997), *Timing characteristics of primary reference clocks*.

[ITU-T G.811.1] Recommendation ITU-T G.811.1 (2017), *Timing characteristics of enhanced primary reference clocks*.

[ITU-T G.8260] Recommendation ITU-T G.8260 (2022), *Definitions and terminology for synchronization in packet networks*.

[ITU-T G.8271] Recommendation ITU-T G.8271/Y.1366 (2020), *Time and phase synchronization aspects of packet networks*.

[ITU-T G.8272] Recommendation ITU-T G.8272/Y.1367 (2018), *Timing characteristics of primary reference time clocks*.

3 Definitions

Definitions related to synchronization are contained in [ITU-T G.810] and [ITU-T G.8260].

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

ePRTC enhanced Primary Reference Time Clock

FM Frequency Modulation

GNSS Global Navigation Satellite System

MTIE Maximum Time Interval Error

NE Network Equipment

PPS Pulse Per Second

PRC Primary Reference Clock

PRTC Primary Reference Time Clock

PTP Precision Time Protocol

TDEV Time Deviation

T-GM Telecom Grand Master

UTC Coordinated Universal Time

5 Conventions

None.

6 Time error, wander and jitter in locked mode

The time error noise generation of an ePRTC is characterized by two main aspects:

1) the constant time error (time offset) at its output compared with the applicable primary time standard (e.g., UTC);

2) the amount of phase error (wander and jitter) produced at its output.

For the characterization of the second aspect described above (phase error), the calculation of the maximum time interval error (MTIE) and the time deviation (TDEV) is useful.

Clause 6.1 defines the time error requirements applicable at the output of the ePRTC, which correspond to the combination of the two aspects described above (constant time error and phase error). No requirement is defined for the constant time error component taken alone, only when it is combined with the phase error.

Clauses 6.2 and 6.3 define the wander and jitter requirements applicable at the output of the ePRTC, which correspond to the second aspect described above (phase error).

The performance specified in clauses 6.1 and 6.2 also applies to the output of the combined ePRTC and T-GM function when integrated into a single piece of equipment. Therefore, there is no additional allowance for the inclusion of the T-GM function.

NOTE – Optimization of the noise inside the equipment is possible by combining the two functions. Therefore, the total noise of equipment that integrates the ePRTC and T-GM can be the same as equipment that only contains the ePRTC.

6.1 Time error in locked mode

Under normal, locked operating conditions, the time output of the ePRTC, or the combined ePRTC and T-GM function, should be accurate to within 30 ns or better when verified against the applicable primary time standard (e.g., UTC). For the ePRTC this value includes all the noise components, i.e., the constant time error (time offset) and the phase error (wander and jitter) of the ePRTC.

For the combined ePRTC and T-GM function, the time error samples are measured through a moving-average low-pass filter of at least 100 consecutive time error samples. This filter is applied by the test equipment to remove errors caused by timestamp quantization, or any quantization of packet position in the test equipment, before calculating the maximum time error. Normal, locked operating conditions mean that:

– The ePRTC is fully locked to the incoming reference time signal, and is not operating in warm-up;
– There are no failures or facility errors in the reference path, including but not limited to antenna failures;
– The environmental conditions are within the operating limits specified for the equipment;
– The equipment is properly commissioned and calibrated for fixed offsets such as antenna cable length, cable amplifiers and receiver delays;
– The reference time signal (e.g., global navigation satellite system (GNSS) signal) is operating within limits, as determined by the relevant operating authorities;
– If the reference time signal is operated over a radio system such as GNSS, multipath reflections and interference from other local transmissions, such as jamming, must be minimized to an acceptable level;
– There are no extreme propagation anomalies, such as severe thunderstorms or solar flares.

6.2 Wander in locked mode

The wander requirements apply to all the interfaces listed in clause 9.2.2.

When the ePRTC is in the normal, locked mode of operation, the wander, expressed in MTIE, measured using a similar configuration as the synchronized clock configuration defined in Figure 1a of [ITU-T G.810] (with the use of a time standard instead of a frequency standard), should have the limits shown in Table 1.

Table 1 – Wander generation (MTIE)

MTIE limit (ns)	Observation interval τ (s)
4	$0.1 < \tau \leq 1$
$0.11114 \times \tau + 3.89$	$1 < \tau \leq 100$
$0.0375 \times 10^{-3}\ \tau + 15$	$100 < \tau \leq 400\,000$
30	$\tau > 400\,000$

The resultant requirements are shown in Figure 1.

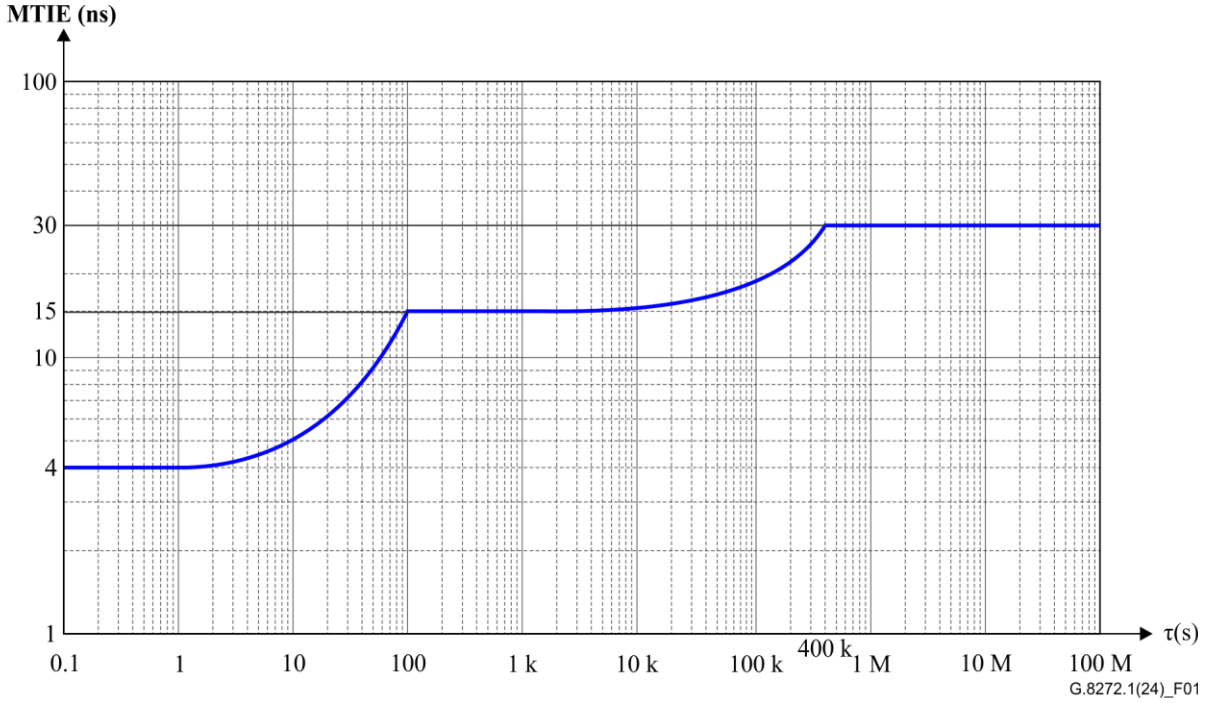


Figure 1 – MTIE as a function of an observation (integration) interval τ

NOTE 1 – For the 1 pulse per second (PPS) output interface, the MTIE mask is applicable for observation intervals greater than or equal to 1 second.

When the ePRTC is in the normal, locked mode of operation, the wander, expressed in TDEV, measured using a similar configuration as the synchronized clock configuration defined in Figure 1a of [ITU-T G.810] (with the use of a time standard instead of a frequency standard), should have the limits shown in Table 2.

Table 2 – Wander generation (TDEV)

TDEV limit (ns)	Observation interval τ (s)
1	$0.1 < \tau \leq 30\ 000$
$3.33333 \times 10^{-5}\tau$	$30\ 000 < \tau \leq 300\ 000$
10	$300\ 000 < \tau < 1\ 000\ 000$

The resultant requirements are shown in Figure 2.

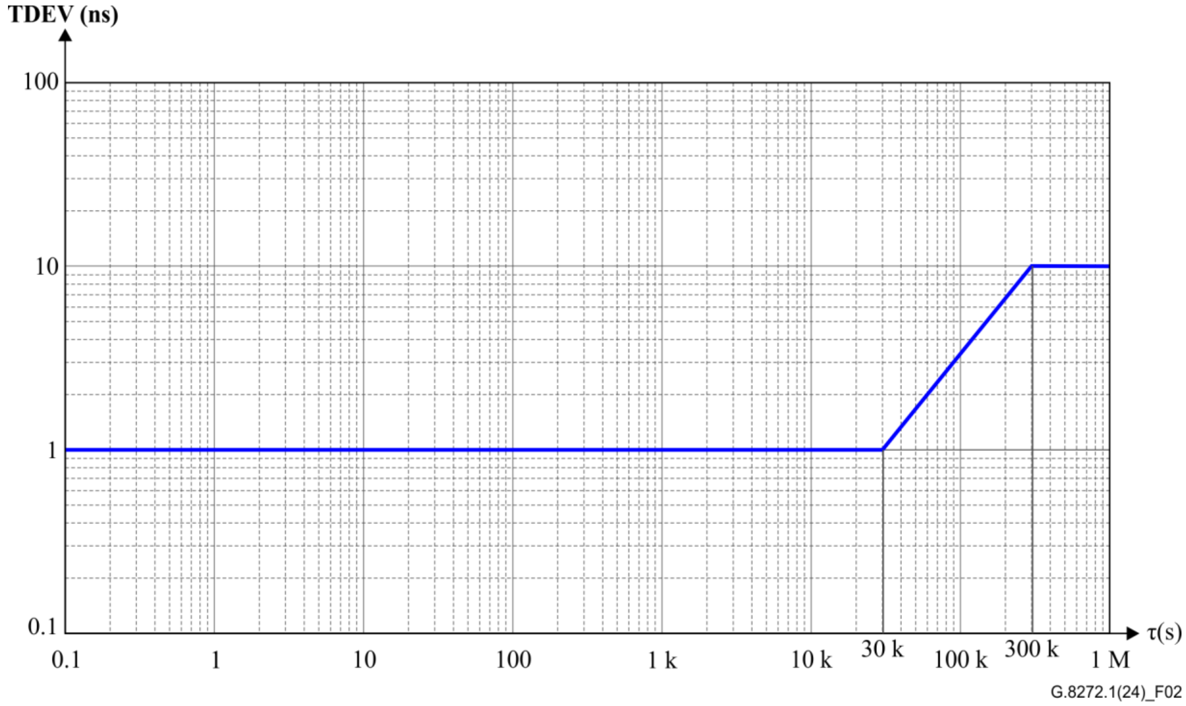


Figure 2 – TDEV as a function of an observation (integration) interval τ

NOTE 2 – For the 1 PPS output interface, the TDEV mask is applicable for observation intervals greater than or equal to 1 second.

The applicable MTIE and TDEV requirements for the 1 PPS output interfaces are based on the time interval error of the 1 PPS signal taken at one sample per second and without any low-pass filtering.

The applicable MTIE and TDEV requirements for synchronous Ethernet, 2048 kHz, 2048 kbit/s and 1544 kbit/s output interfaces are measured through an equivalent 10 Hz, first-order, low-pass measurement filter, at a maximum sampling time τ_0 of 1/30 seconds.

The applicable MTIE and TDEV requirements for an Ethernet interface carrying PTP messages are measured through a moving-average low-pass filter of at least 100 consecutive time error samples. This filter is applied by the test equipment to remove errors caused by timestamp quantization, or any quantization of packet position in the test equipment, before calculating the MTIE and TDEV.

The minimum measurement period for TDEV is 12 times the integration period ($T = 12\tau$).

NOTE 3 – In the case of PTP, a sample is a single estimate of 2-way time error, calculated by combining the packets in forward and reverse directions. It is calculated by the test equipment measuring the difference between the time from the PRTC and the reference time. As an example, according to [b-ITU-T G.8275.1], the PTP message rate is 16 packets/second in each direction; therefore, there are 16 samples per second, calculated by combining a pair of packets in each direction.

6.3 Jitter

6.3.1 Output port jitter

While most specifications in this Recommendation are independent of the output interface at which they are measured, this is not the case for jitter generation. Jitter generation specifications must utilize existing specifications that are currently specified differently for different interfaces. These requirements are stated separately for some of the interfaces identified in clause 9.

The applicable jitter requirements for 2048 kHz, 2048 kbit/s, 1544 kbit/s and 10 MHz output interfaces are defined in [ITU-T G.811].

The intrinsic jitter for the other interfaces identified in clause 9 is for further study.

6.3.2 Input port jitter tolerance

The 10 MHz input interface should tolerate jitter as defined by [ITU-T G.811] for the 10 MHz output interface.

The jitter tolerance for the other interfaces identified in clause 9 is for further study.

7 Phase discontinuity

The phase discontinuity for an ePRTC is for further study.

8 Transient response and holdover performance

8.1 Transient between time locked and frequency reference locked

For the transition from time locked to frequency reference locked, the MTIE mask in clause 6.2 applies for a period up to 900 seconds.

The transition from frequency reference locked to time locked is for further study.

8.2 Phase/time holdover based on frequency reference during loss of phase/time input

When an ePRTC loses all its input phase and time references, it enters the phase/time holdover state. Under these circumstances, the ePRTC will rely on an autonomous primary reference clock (PRC) frequency reference input compliant with [ITU-T G.811.1] (ePRC).

The phase/time holdover requirement bounds the maximum excursions in the output timing signal. Additionally, it restricts the accumulation of the phase movement during input signal impairments or internal disturbances.

8.2.1 Time error in holdover mode

For the ePRTC-A, the holdover requirements for time error are as follows:

– From the start of phase/time holdover, after a period of continuous normal (locked mode) operation of *L* days, the time output of the ePRTC should be accurate, when verified against the applicable primary time standard (e.g., UTC), to within a value increasing linearly from 30 ns to 100 ns over a holdover period of *H* days, as defined in Table 3. These are the three cases from Table 3:
  - For $L < 6$ days, the holdover period *H* is 70 000 seconds or 0.81 days.
  - For values of *L* between 6 days and 40 days, the holdover period increases linearly, with *H* set equal to *L*.
  - For $L > 40$ days, the holdover period *H* is 40 days.

Figure 3 shows the general case (see Appendix V for specific examples).

For the ePRTC-B, a higher-performance ePRTC, the holdover requirements are for further study.

NOTE 1 – The ePRC for phase/time holdover can be placed at the local site with the ePRTC or at a remote site connected by a synchronization network, provided that the frequency input to the ePRTC satisfies the requirements in [ITU-T G.811.1].

Table 3 – ePRTC-A phase/time holdover requirements

Locked mode duration L (days)	Holdover Time t (s)	Time error $\Delta x(t)$ (ns)
L < 6 days	$0 < t \leq 70\ 000$	$\lvert\Delta x(t)\rvert \leq 30 + 1.000{\times}10^{-3}t$
6 days ≤ L ≤ 40 days	$0 < t \leq L \cdot 86\ 400$ (L days)	$\lvert\Delta x(t)\rvert \leq 30 + 70\ t\ /\ (L \cdot 86\ 400)$
L > 40 days	$0 < t \leq 3\ 456\ 000$ (40 days)	$\lvert\Delta x(t)\rvert \leq 30 + 2.025463{\times}10^{-5}t$
NOTE – t=0 represents the start of holdover.		

NOTE 2 – In Figure 3, *H* refers to the maximum applicable holdover time from the table. This is 70 000 for the first case, *L* 86 400 for the second case, and 3 456 000 for the third case. For further information, including a graphical representation of Table 3, see Appendix V.

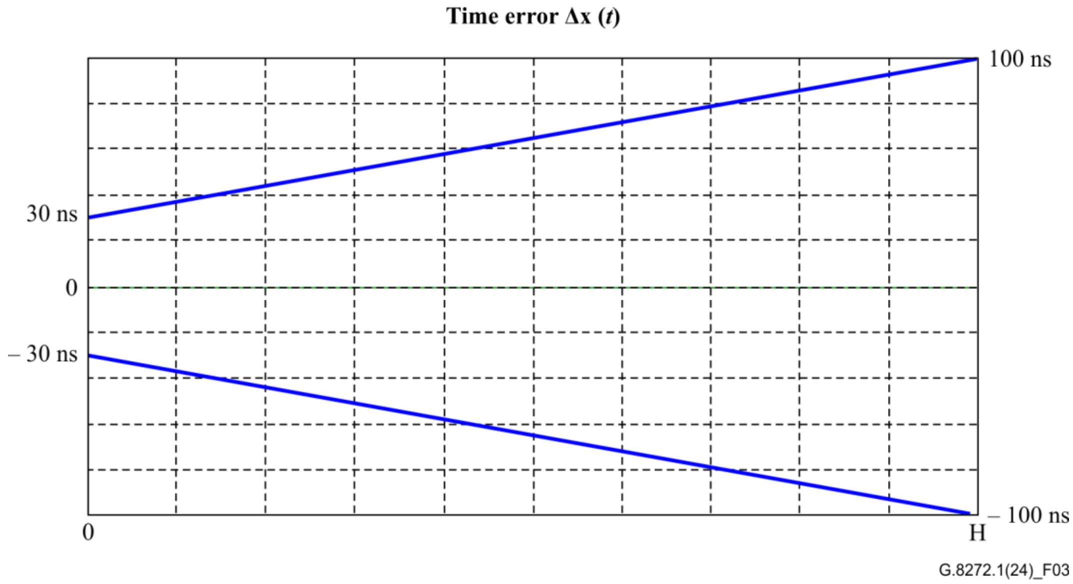


Figure 3 – ePRTC-A phase/time holdover requirements

NOTE 3 – Additional background information on these ePRTC holdover requirements is included in Appendix II.

8.2.1 Wander in holdover mode

For the ePRTC-A, holdover is based on the frequency reference during loss of phase/time input requirements, and the following requirements apply for TDEV and MTIE.

This wander in holdover mode specification is valid for holdover mode including transition into holdover mode. Synchronizing back after holdover is ffs.

For ePRTC-A holdover, the following MTIE limits apply.

Table 4 – Wander generation (MTIE)

MTIE limit (ns)	Observation interval τ (s)
4	$0.1 < \tau \leq 1$
$0.11114 \times \tau + 3.89$	$1 < \tau \leq 100$
$0.0375 \times 10^{-3}\tau + 15$	$100 < \tau \leq 10\ 000$

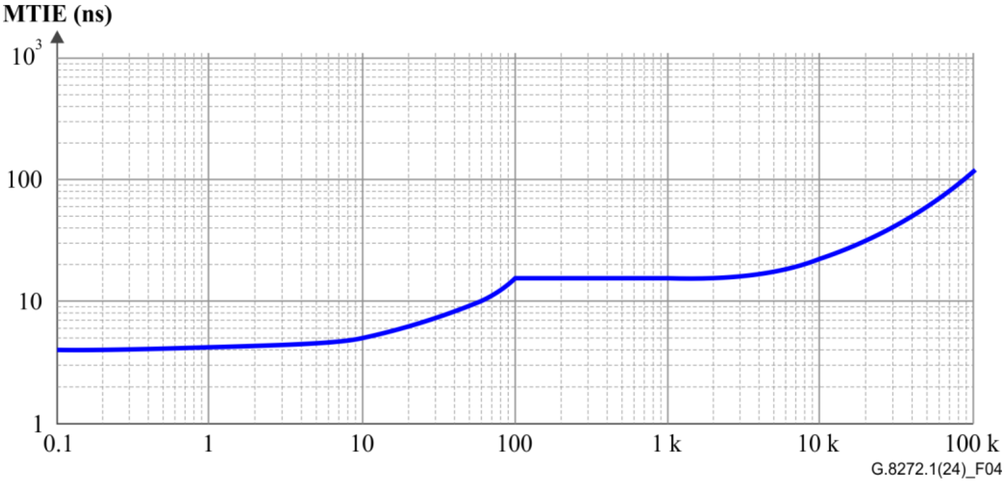


Figure 4 – MTIE as a function of an observation (integration) period τ

NOTE 1 – Longer observation time and corresponding MTIE mask is for further study.

For ePRTC-A holdover, the following TDEV limits apply.

Table 5 – Wander generation (TDEV)

TDEV limit [ns]	Observation interval τ [s]
1	$0.1 < \tau \leq 10\,000$

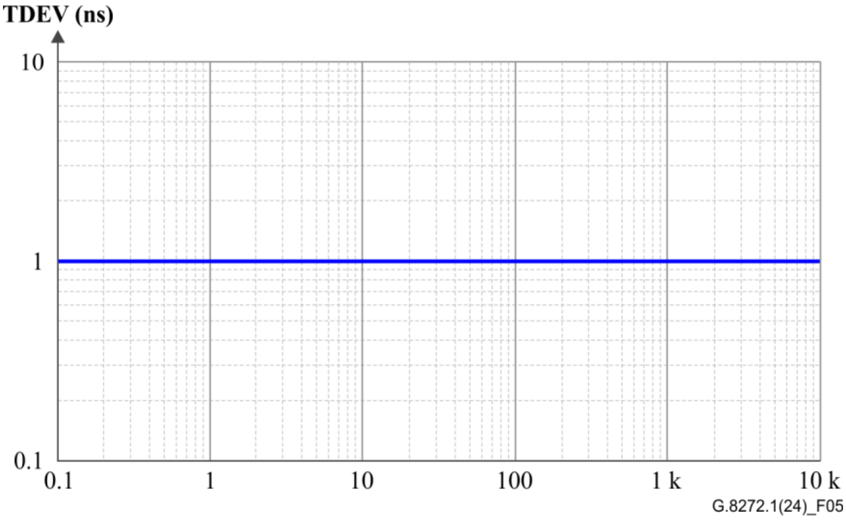


Figure 5 – TDEV as a function of an observation (integration) period τ

NOTE 2 – Longer observation time and corresponding TDEV mask is for further study.

9 Interfaces

The requirements in this Recommendation are related to reference points that may be internal to the equipment or network equipment (NE) in which the ePRTC is embedded and are, therefore, not necessarily available for measurement or analysis by the user. Consequently, the performance of the ePRTC is not specified at these internal reference points, but rather at the external interfaces of the equipment.

Note that not all of the interfaces below need to be implemented on all equipment.

9.1 Phase and time interfaces

The output phase and time interfaces specified for the equipment in which the ePRTC may be contained are:

– ITU-T V.11-based time/phase distribution interface, as defined in [ITU-T G.703] and [ITU-T G.8271];

  For the ePRTC ITU-T V.11-based time/phase distribution interface, it is necessary to limit cable length to 5 m or less and a high-quality cable should be used. The following requirements apply:

  - The 1 PPS signal generation accuracy tolerance is ±4 ns;
  - The cable delay compensation accuracy tolerance is ±2 ns;
  - The 1 PPS signal detection accuracy tolerance is ±4 ns.

– 1 PPS 50 Ω phase-synchronization measurement interface, as defined in [ITU-T G.703] and [ITU-T G.8271];

– Ethernet interface carrying PTP messages;

  NOTE – Ethernet interfaces can combine synchronous Ethernet for frequency and PTP messages.

– Other interfaces are for further study.

9.2 Frequency interfaces

In addition to phase and time interfaces, frequency interfaces are used.

9.2.1 Inputs

At least one input frequency interface must be provided from an autonomous PRC. The input frequency interfaces specified for the equipment in which the ePRTC may be contained are:

– 2048 kHz interfaces according to [ITU-T G.703] with additional jitter and wander requirements as specified herein (see Note);

– 2048 kbit/s interfaces according to [ITU-T G.703] with additional jitter and wander requirements as specified herein (see Note);

– 10 MHz interfaces according to [ITU-T G.703] with additional jitter and wander requirements as specified herein;

– Other interfaces are for further study.

Performance requirements of the autonomous PRC are given in Annex A.

NOTE – The requirements for jitter for the 2 048 kHz and 2 048 kbit/s interfaces need to be tighter than what is defined in [ITU-T G.703] and [ITU-T G.811] to meet the ePRTC requirements. The exact values are for further study.

9.2.2 Outputs

At least one output frequency interface must be provided. The output frequency interfaces specified for the equipment in which the ePRTC may be contained are:

– 2048 kHz interfaces according to [ITU-T G.703] with additional jitter and wander requirements as specified herein;

– 1544 kbit/s interfaces according to [ITU-T G.703] with additional jitter and wander requirements as specified herein;

– 2048 kbit/s interfaces according to [ITU-T G.703] with additional jitter and wander requirements as specified herein;

– Synchronous Ethernet interfaces;

– ITU-T V.11-based time/phase distribution interface, as defined in [ITU-T G.703] and [ITU-T G.8271];
– 1 PPS 50 Ω phase-synchronization measurement interface, as defined in [ITU-T G.703] and [ITU-T G.8271];
– 10 MHz interfaces according to [ITU-T G.703]; with additional jitter and wander requirements as specified herein;
– Other interfaces are for further study.

Annex A

ePRTC autonomous primary reference clock requirements

(This annex forms an integral part of this Recommendation.)

Performance requirements for the ePRTC autonomous primary reference clock are described in [ITU-T G.811.1], the Recommendation defining the enhanced PRC (ePRC).

NOTE – Clarifying the term "autonomous" in the context of this document, a caesium atomic clock is an example of an autonomous PRC. A GNSS timing receiver, on the other hand, is not an example of an autonomous PRC, as it relies on external signals for establishing precise time and frequency.

Appendix I

ePRTC functional model

(This appendix does not form an integral part of this Recommendation.)

A simplified model of the ePRTC is provided in this appendix to describe its functionality and to define the various interfaces and functions that collectively define an ePRTC.

Figure I.1 represents a functional model and it is not intended to specify any specific implementation.

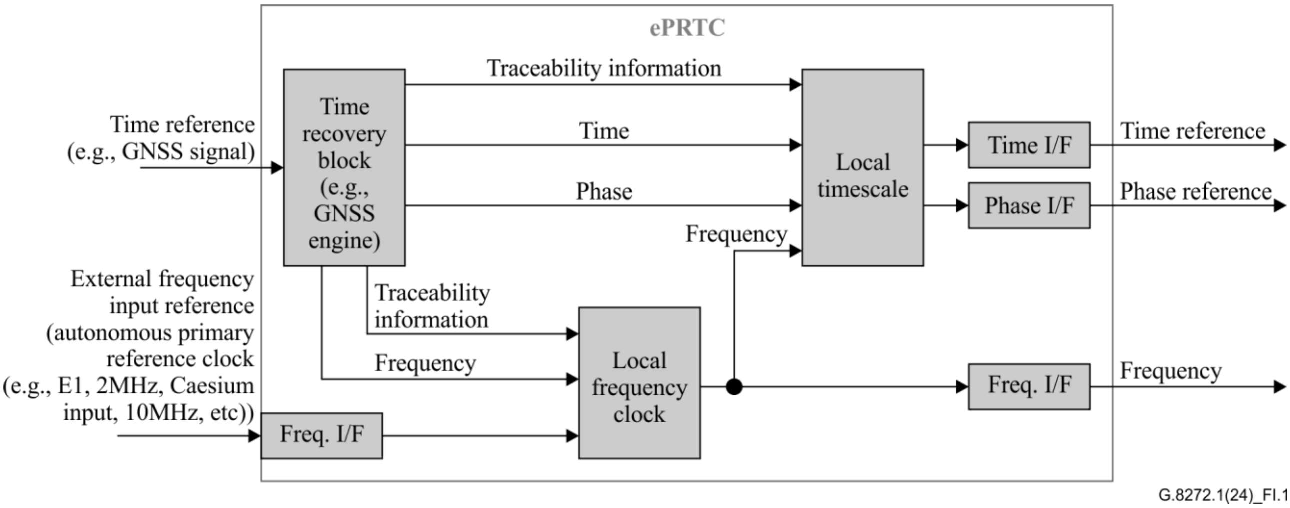


Figure I.1 – ePRTC functional model

NOTE – The output interfaces shown in Figure I.1 correspond to logical interfaces; in some ePRTC implementations, the time logical interface and the phase logical interface may be merged into the same phase/time physical interface. In addition to the time reference, the time logical interface may carry associated information on the traceability of the reference.

The main function of an ePRTC is to deliver a primary time reference to be used in the time and/or phase synchronization of other clocks of the network.

An ePRTC receives a time reference from a system with access to a recognized primary time standard (e.g., from a global navigation satellite system or from a national laboratory participating in time standards generation) and delivers this reference signal to other clocks within a network or section of a network.

The main difference between the PRTC and the ePRTC is the input from an external autonomous primary reference clock (PRC) (e.g., caesium clock). Therefore, an ePRTC includes an external input frequency interface and it must also implement at least one output frequency interface. The ePRTC can also include multiple input frequency references used to ensemble a very stable frequency reference. A possible use of the output frequency interface may be to measure the phase error of the ePRTC, using traditional telecom signals.

Finally, the ePRTC may also deliver traceability information, reflecting the status of the clock (i.e., locked on its input reference signal, in holdover). The details of this traceability information are for further study.

The functionality of the ePRTC is defined based on the individual blocks in Figure I.1. A description of the functions is provided in Table I.1. Note that the specific grouping of the functions is for description only and is not intended to specify how the ePRTC may be implemented.

Table I.1 – ePRTC functions

Time recovery	Receives and processes the external time interface (e.g., from GNSS antenna). Provides output signals to generate frequency, phase and time. Provides traceability information.
Local frequency clock	The local frequency clock generates the internally-used frequency timing signals. It synchronizes to an autonomous PRC input (e.g., E1, 2048 kHz, 10 MHz). The output of the local frequency clock provides a reference to the local timescale generation block.
Local timescale	Maintains the local representation of the primary timescale, based on the frequency generated by the local frequency clock. This block also generates the time and phase reference output signals.
I/F	Interface function necessary to generate a physical signal.

Appendix II

ePRTC holdover model

(This appendix does not form an integral part of this Recommendation.)

II.1 General clock model

The methodology to evaluate the holdover performance is based on the well-established clock model [b-Sullivan], [b-Bregni]. The clock model provides a well-defined relationship between the fundamental attributes of a clock and the time-error performance capabilities of the clock.

When both the deterministic and stochastic components are included, the general time-error accumulation governing equation is:

$$x(n\tau_0) = \sum_{j=0}^{2} c_j (n\tau_0)^j + \varphi_x(n\tau_0) \qquad \text{(II.1)}$$

where $c_0=a_0$, $c_1=y_0$, $c_2=½d$, and the TDEV of the stochastic components is:

$$\sigma_\varphi(\tau) = \left[\sum_{i=1}^{3} e_i(\tau)^i \right]^{1/2} \qquad \text{(II.2)}$$

Summarizing each term based on the index *i* (the index *j* corresponds to the index *i* divided by 2 when *i* is even):

$i = 0$: Initial time offset at start of holdover (limited by initial time error during normal tracking; not applicable to stability);

$i = 1$: Contribution from the white frequency modulation (FM) noise component ($\tau^{1/2}$ TDEV dependence for the time accumulation process);

$i = 2$: Linear time-error accumulation associated with the initial frequency offset and the flicker noise FM component;

$i = 3$: Contribution from the random walk FM noise component ($\tau^{3/2}$ TDEV dependence for the time accumulation process), note this is usually insignificant for atomic clocks used in ePRTC applications;

$i = 4$: Contribution associated with drift in the clock and flicker walk FM (τ^2 component of TDEV, which is not relevant for atomic clocks used in ePRTC applications; because of this, it is not included in equation (II.2)).

II.2 Ideal holdover model

In applying the general clock model to the ePRTC, the first observation is that in an ideal case, the deterministic clock state components (clock phase, clock frequency and clock drift) could be known perfectly. It is useful to see how well an atomic clock can maintain timekeeping in two steps, the first described here in clause II.2 and the second described in clause II.3.

The ideal holdover performance is considered, as this is the performance limitation of the clocks themselves. The results in this section show the ideal timekeeping capability, as examples, of three types of atomic clocks:

1) ePRC-A;

2) ePRC-B;

3) ePRC-C.

The term ePRC is an acronym for enhanced PRC, which performs at least at the level of the PRC defined in Annex A. The ideal holdover performance of such clocks is limited by the intrinsic noise performance. For example, the flicker FM noise floor (i.e., the minimum value of MDEV) for a standard caesium tube clock (ePRC-A example) is typically 1.5×10^{-14}, while a high-performance caesium tube clock (ePRC-B example) flicker FM noise floor is typically 3 times better (5×10^{-15}). An atomic clock based on Ytterbium cold ion microwave technology (ePRC-C example), represents a significant improvement over high-performance caesium, with a tenfold improvement in intrinsic noise performance (flicker noise typically better than 5×10^{-16}).

The two graphs (one at a 30-day scale and another at a 300-day scale) contained in Figure II.1 show the accumulated time-error performance, i.e., TDEV, for six example cases: (1) one ePRC-A (blue), (2) dual ensemble of ePRC-A (red), (3) one ePRC-B (green), (4) dual ensemble of ePRC-B (purple), (5) one ePRC-C (light blue) and (6) dual ensemble of e-PRC-C (orange). In each case, ensembling shows performance improvement.

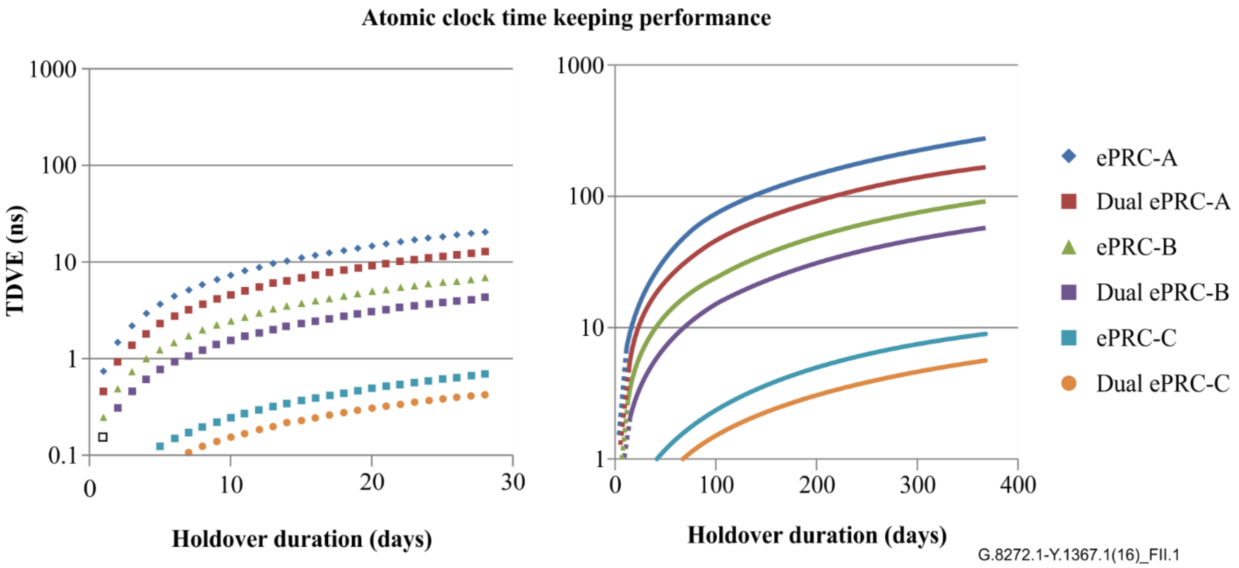


Figure II.1 – Atomic clock time keeping (30-day and 300-day scales)

II.3 ePRTC holdover performance characterization

A key capability of an ePRTC is the capability to maintain normal timing performance during extended GNSS outage events. Such events can be the results of maintenance, equipment failure or intentional or unintentional jamming.

The results summarized below are based on a complete simulation of an ePRTC based on these three components:

1) Intrinsic noise of the clock – The deterministic and stochastic components of the clock model described above;

2) GNSS reference noise – The simulation model includes the receiver noise as well as a diurnal model of ionospheric delay;

3) Measurement noise – A small component associated with the performance of a well-designed ePRTC system.

The simulation models one particular ePRTC clock algorithm. At the core of all clock algorithms is the behaviour that the short-term noise is dominated by the clock performance and the long-term noise is dominated by the reference performance. A well-designed filter algorithm will mitigate noise peaking in the response.

For an ePRTC with multiple atomic clock inputs, an ensembling function is also required. Also, dynamic filtering performance is required to address non-steady conditions such as start-up and clock outages. The internal characteristics of the filtering algorithm are beyond the scope of the ePRTC standard. This example is provided to show the holdover performance obtainable with ePRTC technology.

The graph in Figure II.2 shows the performance of ePRTC systems for a 14-day GNSS outage when operating with different alternative local atomic clocks. The graph includes six examples as before: single/dual standard performance caesium, single/dual high-performance caesium and single/dual next-generation atomic clock.

This illustrates the key capability of an ePRTC to support outages beyond several days without serious time keeping degradation. This time error is constrained to be better than a PRTC for a minimum outage period of two weeks. Such events can be the results of maintenance, equipment failure or intentional or unintentional jamming. All example clocks meet the ePRTC holdover requirement from clause 8.2, which is shown with the solid red lines, by a comfortable margin.

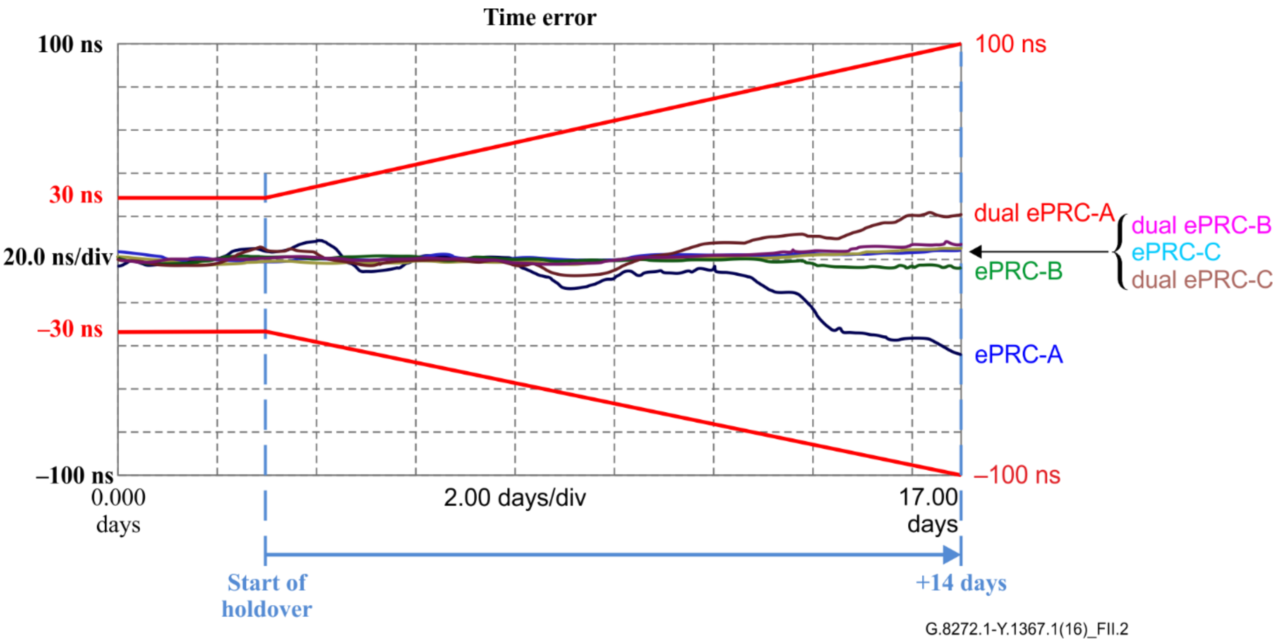


Figure II.2 – Atomic clock 14-day holdover (starts after three days)

Appendix III

Testing ePRTC holdover

(This appendix does not form an integral part of this Recommendation.)

This appendix provides a methodology for testing ePRTC holdover. Testing ePRTC holdover involves establishing ePRTC locked mode for the required period of time prior to invoking and measuring ePRTC holdover.

This Recommendation places requirements on ePRTC locked mode, which are stated in clause 6.1:

Normal, locked operating conditions mean that:

– The ePRTC is fully locked to the incoming reference time signal, and is not operating in warm-up;
– There are no failures or facility errors in the reference path, including but not limited to antenna failures;
– The environmental conditions are within the operating limits specified for the equipment;
– The equipment is properly commissioned and calibrated for fixed offsets such as antenna cable length, cable amplifiers and receiver delays;
– The reference time signal (e.g., global navigation satellite system (GNSS) signal) is operating within limits, as determined by the relevant operating authorities;
– If the reference time signal is operated over a radio system such as GNSS, multipath reflections and interference from other local transmissions, such as jamming, must be minimized to an acceptable level;
– There are no extreme propagation anomalies, such as severe thunderstorms or solar flares.

One effective way of controlling the conditions related to GNSS, which are the majority of the outlined conditions, is the use of a GNSS simulator. GNSS simulators generate a radio frequency (RF) signal, mimicking the signal that would be obtained from a satellite constellation, including the apparent "motion" of the satellites, the appearance and disappearance as they come up over the horizon and subsequently set. The simulator can be programmed with the "position" and "time" of the device under test at a given time and date, producing the correct satellite signals that would be observed from a receiver at that location and time.

It should also be noted that the requirement that "the environmental conditions are within the operating limits specified for the equipment" apply to both locked mode and holdover mode.

A GNSS simulator generates a 1PPS output which can be used as the reference signal measured against the ePRTC under test. Any difference between the two is the time or phase error produced by the device under test. A time interval counter is used to compare the time difference of a 1 PPS output signal from the ePRTC against that of the reference receiver. The experimental set-up is shown in Figure III.1. The frequency reference to the GNSS simulator should be separate from that used by the ePRTC.

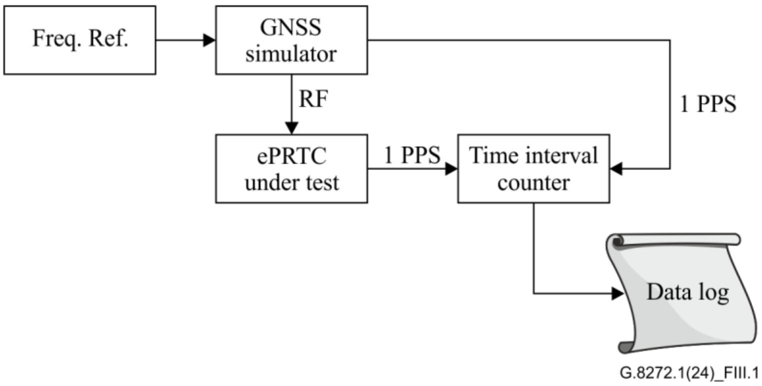


Figure III.1 – Comparing time accuracy of an ePRTC against a GNSS simulator

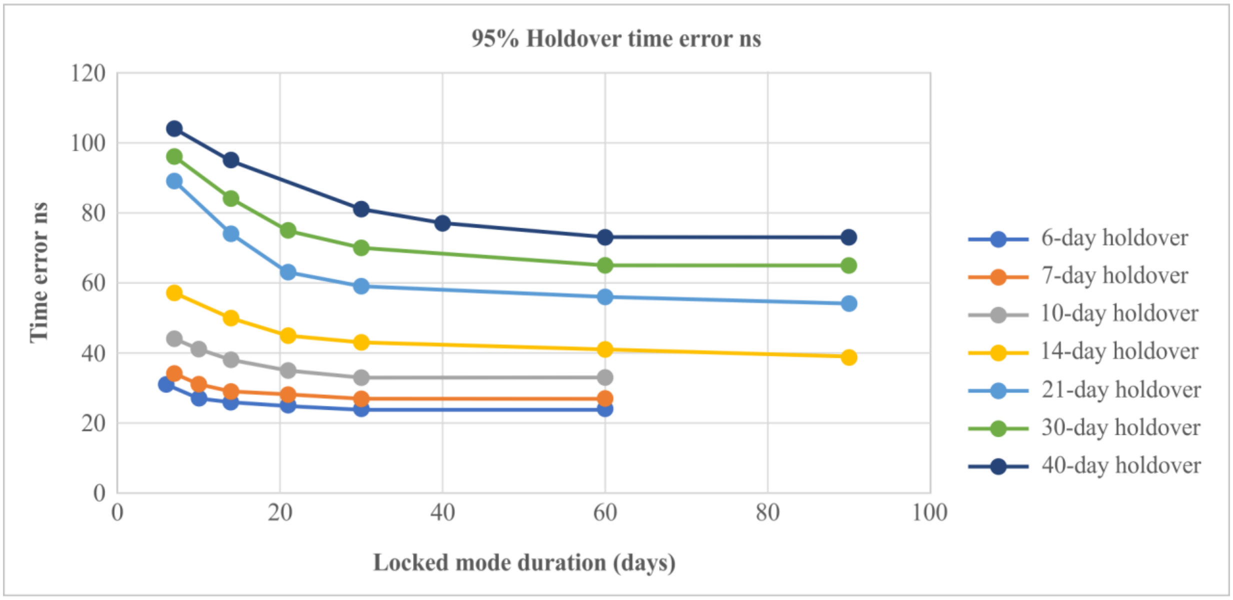
Appendix IV

ePRTC locked mode duration and holdover period

(This appendix does not form an integral part of this Recommendation.)

This appendix provides analysis for studying the ePRTC holdover period and requisite period of normal operation (locked mode duration). To gain strong statistical confidence, a simulated caesium time-error signal with a duration of 60 years was generated. The intensity of the noise processes was set to reflect a caesium operating at the specification limits. Figure IV.1 represents the following analysis:

1. The holdover analysis is performed for both a locked mode period (locked mode duration) and holdover period as specified. For the analysis, holdover periods of 6, 7, 10, 14, 21, 30 and 40 were studied.
2. Six locked mode periods, chosen from these eight locked mode periods – 6, 7, 10, 14, 21, 30, 60 and 90 days, – were investigated for each of the seven holdover periods mentioned in item 1 above.
3. For each locked mode period, the holdover time uncertainty is calculated for 360 experiments consisting of locked mode and holdover periods uniformly distributed over the 60-year simulated caesium noise process. The case of a single caesium clock was considered. Holdover time uncertainty is the magnitude of the difference between predicted time (based on studying the caesium clock during locked mode) and actual time at the end of the holdover period (based on actual caesium clock performance during holdover).
4. The 360 holdover experiments generate 360 time-error data samples. The magnitude of the samples is next processed into first a histogram representing the probability distribution function and the finally a cumulative distribution function. The value of 95% is defined as a statistically significant upper limit and is plotted for each of the six locked mode periods in Figure IV.1.
5. The 95% points for various locked mode periods are found by arranging the result sample distribution for a particular locked mode period into a cumulative distribution function and then determining the holdover value from that cumulative distribution function, where the magnitude of 95% of the sample points are at or below that value.
6. One key finding is that the holdover performance does improve with locked mode duration. It is observed that the improvement levels off with locked mode duration as the flicker noise dominates the frequency estimation, which results in an uncertainty floor that does not improve with more observation time.
7. To achieve 100 ns, a reserve for the time error during normal tracking must be allocated. For this analysis a value of 80 ns is allocated to incremental time error during holdover. From Figure IV.1 for 40-day holdover, it can be seen that 80 ns (95%) is achieved with margin after 40 days of locked mode operation.



G.8272.1(24)_FIV.1

Figure IV.1 – Holdover time error vs locked-mode duration for various holdover periods ranging from 6-day holdover to 40-day holdover

It is instructive to mark the points where locked mode duration L is set equal to holdover period H, as this is applicable to the holdover requirements in the second row of Table 3. For these cases, marked with large black dots in Figure IV.2, the analysis shows that there is a larger margin for shorter holdover periods even though there is a shorter locked mode duration. As an example, for L = H = 6 days, the 95% point time-error point is 31 ns, while for L = H = 14 days, the 95% time-error point is 50 ns. In all cases, the value of the 95% time-error point increases as the value of H increases where H is itself set to L. Again, these points are marked with the large black dots in Figure IV.2.

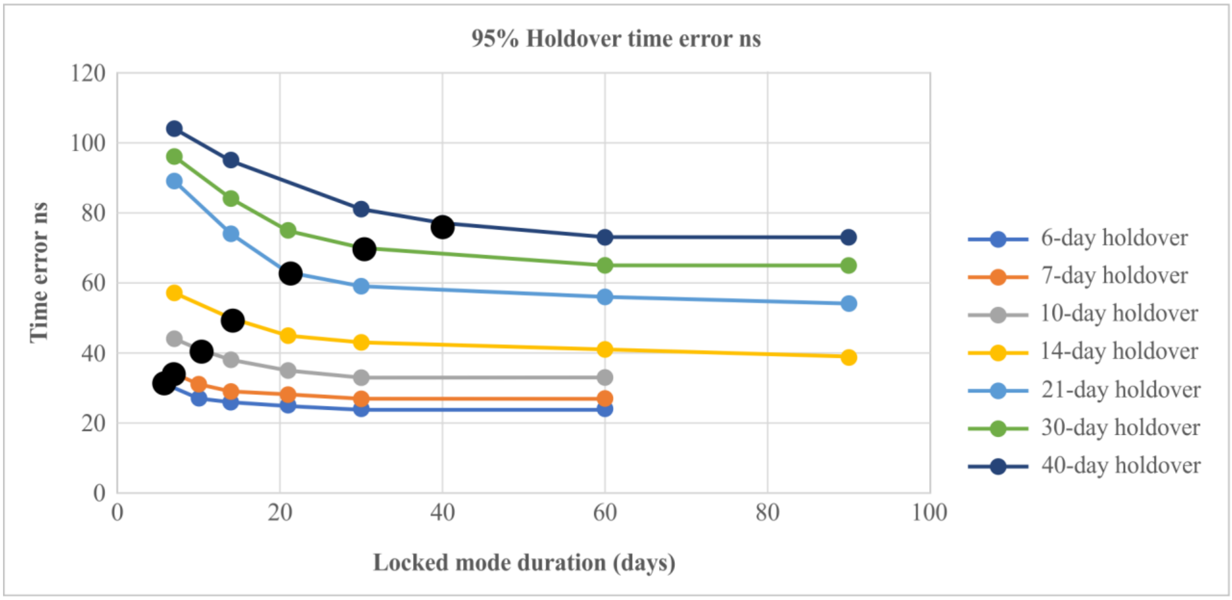


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Figure IV.2 – Holdover time error vs locked-mode duration with H = L points marked

Appendix V

ePRTC parametric holdover

(This appendix does not form an integral part of this Recommendation.)

The ePRTC holdover requirement covers a range of values depending on duration of locked mode L prior to entering holdover. There are three ranges specified in Table 3: (1) < 6 days of locked mode, (2) 6 to 40 days of locked mode, and (3) > 40 days of locked mode. In all cases, the holdover requirement ranges linearly from the locked mode requirement of 30 ns to 100 ns over the prescribed holdover period. For the first range and the third range there is a single holdover requirement while for the second range the holdover requirement varies based on locked mode duration.

In clause 8.2 there is a generalized graph in Figure 3 with holdover time *t* ranging from 0 to H, where H refers to maximum applicable holdover time from Table 3. H is 70 000 for the first case, L iz 86 400 for the second case, and 3 456 000 for the third case. Again, H is a constant for the first and third cases representing a single holdover requirement for those cases.

It is instructive to show H graphically over the entire range covered in Table 3. A constant H applicable to a range of L values maps to a horizontal line, so there are two horizontal lines, one at the beginning and one at the end. In between these two horizontal lines is a sloped line depicting the second case with holdover time as a linear function of locked mode duration as it ranges from 6 days to 40 days.

Note that there is a discontinuity at L = 6 days between the first flat line and the sloped line to the right. The requirement to the left applies to L < 6 days and the sloped line to right applies to L ≥ 6 days. Thus for L = 6 days, the requirement is 6 days of holdover. There is no discontinuity at L = 40 days.

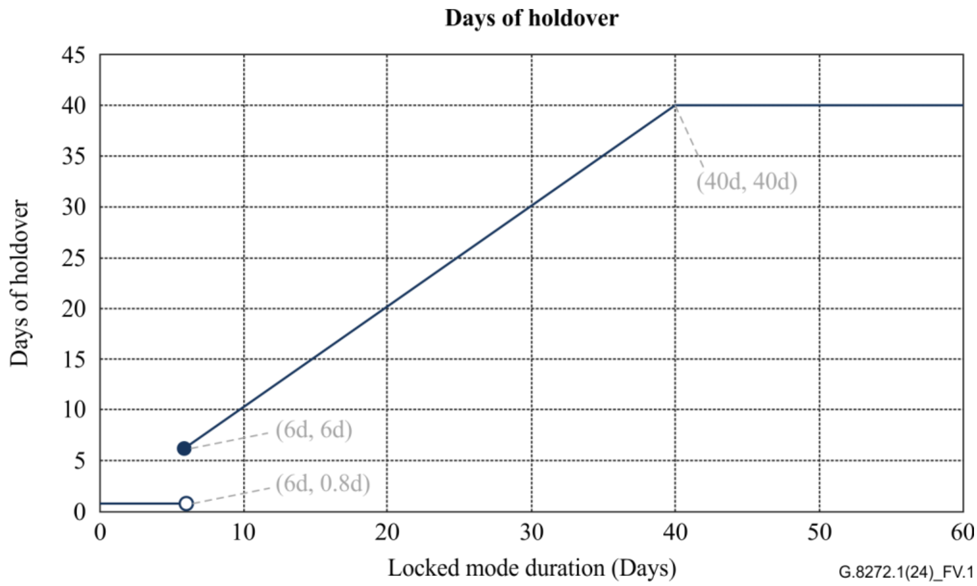

Figure V.1 – Days of holdover as a function of locked mode duration (graphical representation of Table 3)

NOTE 1 – For the case where L < 6 days, the holdover is based on the 1 part in 10^{12} frequency accuracy of the ePRC according to [ITU-T G.811.1].

NOTE 2 – For the case where L > 40 days, a point is reached where further ePRTC locked-time does not improve holdover.

If a specific value of locked mode duration L is chosen, the generalized graph in Figure 3 from clause 8.2 shows numbers on the x-axis. It is useful to show a couple of examples. Figure V.2 shows the holdover requirement for a locked mode duration of 6 days and Figure V.3 shows the holdover requirement for a locked mode duration greater than or equal to 40 days.

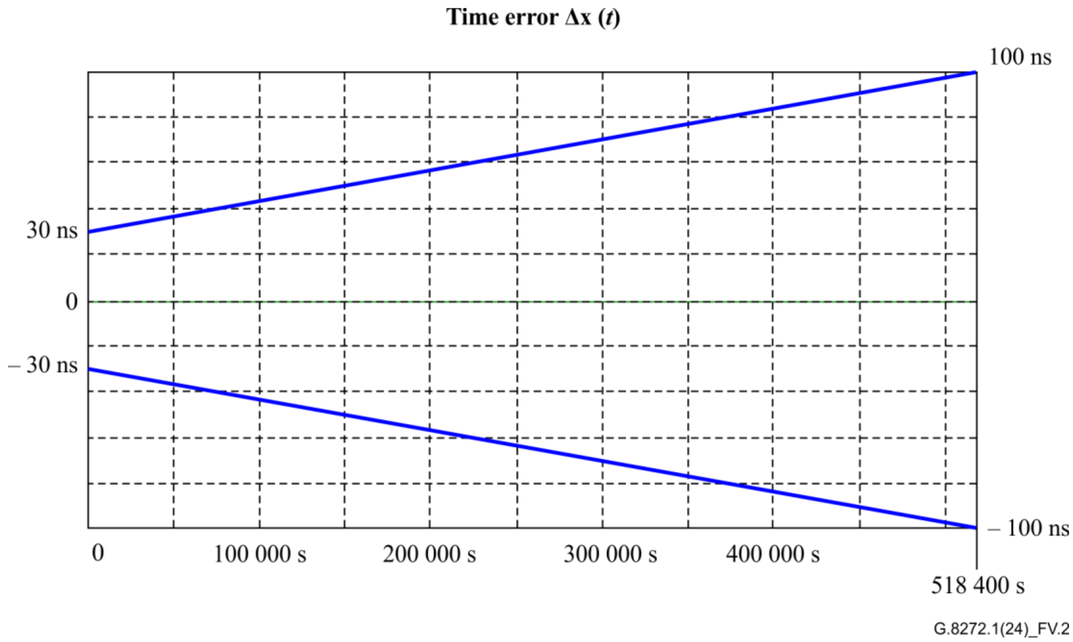

Figure V.2 – ePRTC-A phase/time holdover requirements for L = 6 days

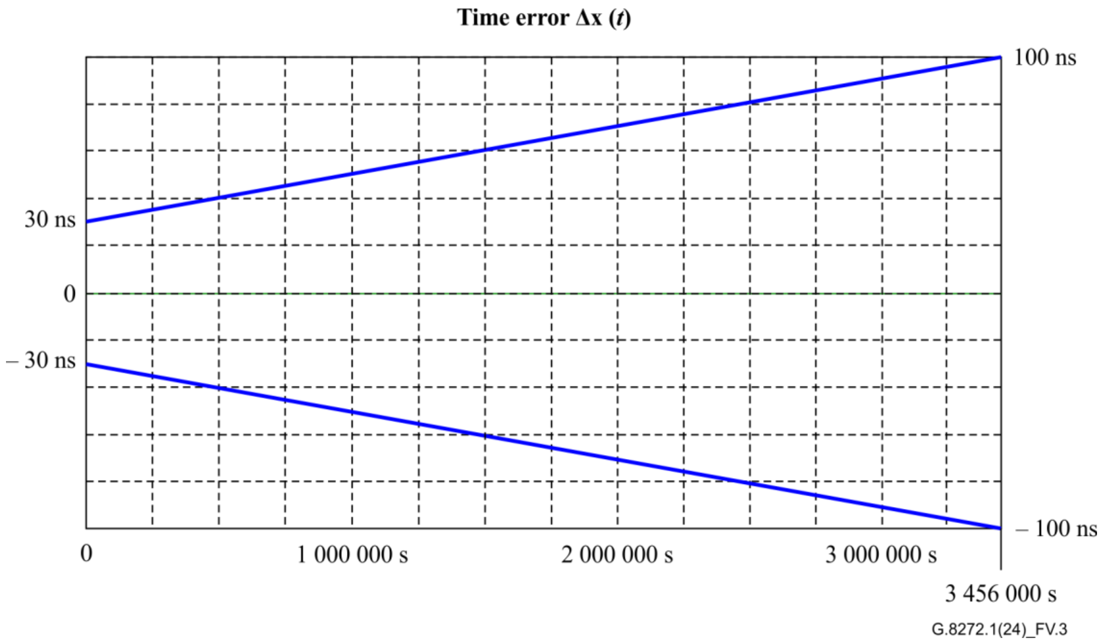

Figure V.3 – ePRTC-A phase/time holdover requirements for L ≥ 40 days

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