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DIGITAL SYSTEMS AND NETWORKS

**Transport of IEEE 10GBASE-R in optical
transport networks (OTN)**

ITU-T G-series Recommendations – Supplement 43



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Supplement 43 to ITU-T G-series Recommendations

Transport of IEEE 10GBASE-R in optical transport networks (OTN)

Summary

Supplement 43 to ITU-T G-series Recommendations describes several approaches for transport of 10G LAN PHY over SDH and OTN transport networks. As some of these approaches use rates, formats and mappings that are not defined in ITU-T Recommendations, this supplement analyses various attributes of the different approaches to provide guidance regarding their applicability to different network contexts.

This supplement relates to Recommendations ITU-T G.872, G.709/Y.1331, G.798, G.707/Y.1322, G.8010/Y.1306, G.8012/Y.1308, G.959.1 and G.696.1

Source

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Supplement 43 to ITU-T G-series Recommendations

Transport of IEEE 10GBASE-R in optical transport networks (OTN)

1 Scope

This supplement describes different approaches for transport of 10GBASE-R signals in optical transport networks via an ODU2 or non-standard ODU2-like frame format (i.e., rates, formats and mappings that are not defined in ITU-T Recommendations). This supplement includes descriptions related to multiplexing the non-standard ODU2-like structures into ODU3-like signals. Different attributes of the varying solutions are described to help provide guidance on which approaches are appropriate to which network contexts.

Including a currently non-standard mapping in this supplement does not preclude considering that mapping for standardization at a future date.

2 References

- [ITU-T G.694.1] Recommendation ITU-T G.694.1 (2002), *Spectral grids for WDM applications: DWDM frequency grid*.
- [ITU-T G.696.1] Recommendation ITU-T G.696.1 (2005), *Longitudinally compatible intra-domain DWDM applications*.
- [ITU-T G.707] Recommendation ITU-T G.707/Y.1322 (2007), *Network node interface for the synchronous digital hierarchy (SDH)*.
- [ITU-T G.709] Recommendation ITU-T G.709/Y.1331 (2003), *Interfaces for the Optical Transport Network (OTN)*.
- [ITU-T G.798] Recommendation ITU-T G.798 (2006), *Characteristics of optical transport network hierarchy equipment functional blocks*.
- [ITU-T G.870] Recommendation ITU-T G.870/Y.1352 (2004), *Terms and definitions for optical transport networks (OTN)*.
- [ITU-T G.872] Recommendation ITU-T G.872 (2001), *Architecture of optical transport networks*.
- [ITU-T G.959.1] Recommendation ITU-T G.959.1 (2006), *Optical transport network physical layer interfaces*.
- [ITU-T G.7041] Recommendation ITU-T G.7041/Y.1303 (2008), *Generic framing procedure (GFP)*.
- [ITU-T G.8001] Recommendation ITU-T G.8001/Y.1354 (2006), *Terms and definitions for Ethernet frames over Transport (EoT)*.
- [ITU-T G.8010] Recommendation ITU-T G.8010/Y.1306 (2004), *Architecture of Ethernet layer networks*.
- [ITU-T G.8012] Recommendation ITU-T G.8012/Y.1308 (2004), *Ethernet UNI and Ethernet NNI*.
- [ITU-T G.8251] Recommendation ITU-T G.8251 (2001), *The control of jitter and wander within the optical transport network (OTN)*.

[IEEE 802.3] IEEE 802.3-2005, *Information Technology – Telecommunications and Information Exchange Between Systems – LAN/MAN – Specific Requirements – Part 3: Carrier sense multiple access with collision detection (CSMA/CD) access method and physical layer specifications.*
<http://ieeexplore.ieee.org/servlet/opac?punumber=10531>

3 Definitions

None.

4 Abbreviations and acronyms

This supplement uses the following abbreviations and acronyms:

| | |
|--------|---|
| CBR10G | Constant Bit Rate signal of 9 953 280 kbit/s \pm 20 ppm (see [ITU-T G.870]) |
| CBR2G5 | Constant Bit Rate signal of 2 488 320 kbit/s \pm 20 ppm (see [ITU-T G.870]) |
| FCS | Frame Check Sequence |
| FEC | Forward Error Correction |
| GFP | Generic Framing Procedure |
| GMP | Generic Mapping Procedure |
| IaDI | Intra-Domain Interface (see [ITU-T G.870]) |
| IPG | Inter-Packet Gap |
| IrDI | Inter-Domain Interface (see [ITU-T G.870]) |
| JC | Justification Control |
| JOH | Justification Overhead |
| MAC | Media Access Control |
| MFAS | MultiFrame Alignment Signal |
| MSI | Multiplex Structure Identifier |
| NJO | Negative Justification Opportunity |
| OCC | Optical Channel Carrier with full functionality (see [ITU-T G.870]) |
| OCCr | Optical Channel Carrier with reduced functionality (see [ITU-T G.870]) |
| ODU | Optical Data Unit |
| OH | Overhead |
| OPU | Optical Payload Unit |
| OTU | Optical Transmission Unit |
| PHY | Physical layer |
| PJO | Positive Justification Opportunity |
| PT | Payload Type |
| SDH | Synchronous Digital Hierarchy |
| SFD | Start-of-Frame Delimiter |
| SONET | Synchronous Optical Network |
| TS | Tributary Slot |

| | |
|------|--------------------|
| TSOH | Time Slot Overhead |
| WAN | Wide Area Network |

5 Conventions

Transmission order: The order of transmission of information in all the figures in this supplement is first from left to right and then from top to bottom. Within each byte, the most significant bit is transmitted first. The most significant bit (bit 1) is illustrated at the left in all the figures.

6 Standard mappings

6.1 10GBASE-W (WAN PHY) via STM-64

[IEEE 802.3] has defined a WAN interface for compatibility with SDH/SONET transport. In the Ethernet domain, this interface is supported via a WAN interface sub-layer (clause 50 of [IEEE 802.3]) that limits the effective data rate of the XGMII from 10 Gbit/s to 9.95328 Gbit/s prior to 64B/66B coding and insertion in an SDH/SONET format frame. The mapping of this data into the frame of an SDH STM-64 (VC-4-64c) is illustrated in Annex F of [ITU-T G.707].

Even if the interface provides only the ± 20 ppm clock accuracy required by clause 50 of [IEEE 802.3], rather than SDH clock tolerances (± 4.6 ppm), this can be transported via ODU2 according to the mapping specified in clause 17.1.2 of [ITU-T G.709].

6.2 GFP-F mapping of 10GBASE-R (LAN PHY) payload only into OPU2

A payload information transparent mapping can be performed according to clause 7.3 of [ITU-T G.709] using the following process:

- Terminate (sink) the 64B/66B line code, preamble, SFD and IPG as per [IEEE 802.3].
- Apply GFP-F framing.
- Encode into an OPU2 according to clause 7.3 of [ITU-T G.709].

On the assumption that MAC frames do not on average exceed the maximum size specified by [IEEE 802.3] (1518 octets excluding the preamble, SFD and IPG), the bit rate required is for a signal that is +100 ppm from the nominal bit rate, approximately 9'922'968.791 kbit/s.

If maximum size jumbo frames are used, the bit rate required for a signal that is +100 ppm from the nominal bit rate is approximately 9'995'002.399 kbit/s.

Note that in the mapping of GFP frames into OPU_k specified in clause 7.3 of [ITU-T G.709], the entire OPU2 payload area of 9'995'277 kbit/s is available (i.e., the fixed stuff bytes of the CBR10G mapping are not present). For an OPU2 that is running at the minimum rate of -20 ppm from the nominal value, this is reduced to 9'995'077.058 kbit/s.

With standard IEEE 802.3 termination, this mapping can fully transport every ETH_CI traffic unit from a 10GBASE-R signal over an OPU2. Refer to Table V.4 of [ITU-T G.7041], where a characterization is given of the MAC rate throughput (not counting overhead) of 10GBASE-R signals versus GFP mappings. The MAC rate throughput of a 10GBASE-R interface, assuming a worst case situation of 9618-byte jumbo-frames is 9'986'502 bit/s. The MAC rate throughput of GFP mapping of the same MAC frames into ODU2 is 9'986'970 bit/s, which is greater than what is required to carry the entire MAC payload from a 10GBASE-R signal.

7 Non-standard mappings

This means rates, formats and mappings that are not fully defined in ITU-T Recommendations.

7.1 Bit transparent mapping of 10GBASE-R signal into OPU2e

This mapping has been moved to clause 17.1 of [ITU-T G.709].

With this mapping, the resulting OTU-like OTU2e signal must be clocked at a nominal bit rate of 11.0957 Gbit/s, as opposed to the standard OTU2 nominal bit rate of 10.709225316 Gbit/s.

7.2 Bit transparent mapping of 10GBASE-R signal into OPU1e

This mapping uses the mapping of CBR2G5 signal into OPU1, defined in clause 17.1.1 of [ITU-T G.709]. It has the same attributes as the clause 7.1 mapping above, but since the fixed stuff bytes of the CBR10G mapping are not left free, the overall data rate is somewhat less (11.0491 Gbit/s rather than 11.0957 Gbit/s). As with the clause 7.1 option, the clock tolerance of the underlying Ethernet signal (± 100 ppm) rather than that of a standard OTU2 signal (± 20 ppm), standard methods for control of jitter and wander according to [ITU-T G.8251] do not apply.

A unique payload type (PT) shall be specified in payload structure identifier (PSI). For example, code "0x80" (reserved code for proprietary use per Table 15-8 of [ITU-T G.709] – Payload type code points) is to be used.

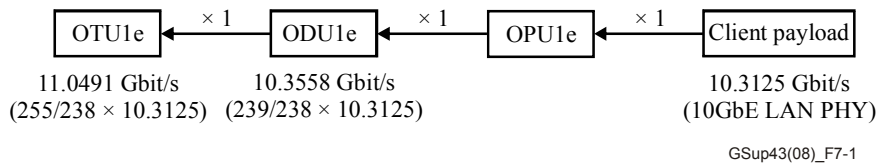


Figure 7-1 – Mapping structure without fixed stuffing

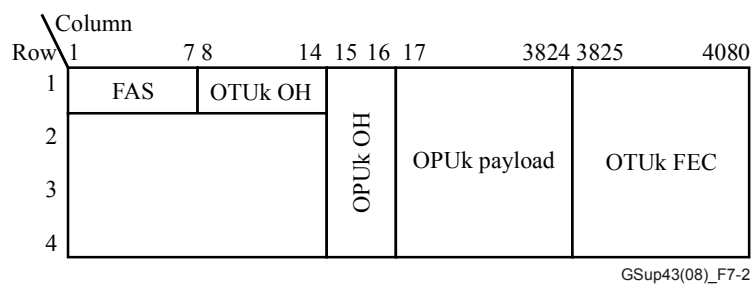


Figure 7-2 – Mapping frame without fixed stuff bytes

7.3 ITU-T G.709 bit-rate compliant information transparent transport of payload and preamble

This mapping has been moved to clauses 17.3.1 and 7.3 of [ITU-T G.709] and clause 7.9 of [ITU-T G.7041].

8 Characteristics of alternative mappings

Table 8-1 provides a summary of the characteristics and applicability of each of the different mappings. Further discussion of each of these characteristics is provided in the indicated clauses.

Table 8-1 – Characteristics of alternative mappings

| Mapping | Clause 6.1 | Clause 6.2 | Clause 7.1 | Clause 7.2 | Clause 7.3 |
|---|-------------------|-------------------|-------------------|-------------------|-------------------|
| ITU-T G.709 bit-rate compliant (clause 8.1) | Yes | Yes | No | No | Yes |
| IrDI/IaDI (clause 8.2) | Both | Both | IaDI only | IaDI only | Both |
| Clock tolerance of client Ethernet signal (clause 8.3) | ±20 ppm (Note 1) | ±100 ppm | ±100 ppm | ±100 ppm | ±100 ppm |
| Clock tolerance of ODUxx signal (clause 8.3) | ±20 ppm | ±20 ppm | ±100 ppm | ±100 ppm | ±20 ppm |
| Jitter/wander according to [ITU-T G.8251] (clause 8.3) | Yes | Yes | No | No | Yes |
| ITU-T G.959.1 optical tributary class (clause 8.4) | NRZ/RZ 10G | NRZ/RZ 10G | NRZ/RZ 40G | NRZ/RZ 40G | NRZ/RZ 10G |
| ITU-T G.696.1 client class (clause 8.4) | 10G | 10G | 40G | 40G | 10G |
| Multiplex to 40G according to [ITU-T G.709] (clause 8.5) | Yes | Yes | No | No | Yes |
| Transport full rate payload (clause 8.6) | No | Yes | Yes | Yes | Yes |
| Transport ordered sets (clause 8.6) | Yes | No | Yes | Yes | Yes (Note 3) |
| Transport full rate preamble and payload (clause 8.6) | Yes | No | Yes | Yes | Yes |
| Transport IPG (clause 8.6) | Yes | No | Yes | Yes | No |
| Full bit transparency (clause 8.6) | Yes | No | Yes | Yes | No |
| Support undisclosed proprietary usage of MAC or PCS sublayer (clause 8.6) | Yes | No | Yes | Yes | Yes (Note 2) |
| BER monitoring based on PCS (clause 8.7) | Yes | No | Yes | Yes | No |

Table 8-1 – Characteristics of alternative mappings

NOTE 1 – [IEEE 802.3] specifies ± 20 ppm for the clock tolerance for a 10GBASE-W interface. [ITU-T G.707] indicates that 10GBASE-W signals that meet the stricter clock tolerance of ± 4.6 ppm may be transported as STM64 in an SDH network. However, the mapping into ODU2 supports any CBR10G signal including STM64 and 10GBASE-W that has a clock tolerance of ± 20 ppm.

NOTE 2 – Proprietary usage of the preamble is supported. Proprietary usage of the IPG is not.

NOTE 3 – While ordered sets are transported, if the ordered sets are close together there is no guarantee that all will be transported or that their original transmitted sequence will be preserved. See [ITU-T G.709] and [ITU-T G.7041].

8.1 ITU-T G.709 bit-rate compliant

ITU-T G.709 bit rate that is generally used to transport signals of approximately 10 Gbit/s is OPU2. The nominal bit rate for an OPU2 payload is 9'995'276.962 kbit/s. This may transport signals directly via mappings such as GFP-F or via STM-64 using the CBR10G mapping specified in clause 17.1.2 of [ITU-T G.709]. Mappings that comply with the [ITU-T G.709] bit rate are networkable signals according to the OTN architecture specified in [ITU-T G.872].

8.2 Inter-domain/intra-domain interfaces

[ITU-T G.872] specifies two different types of interfaces to be used in the optical transport network. inter-domain interfaces (IrDI) are standardized interfaces that may be used at handoff points between operators or between equipment from different vendors within an operator's environment. Intra-domain interfaces (IaDI) are generally applicable only within a single-vendor island within an operator's network to enable the use of unique optical technology, dispersion management, etc., in the context of long-haul optical line systems.

The mappings of 10GBASE-R signals via OPU2e and OPU1e according to clauses 7.1 and 7.2 are inherently intra-domain interfaces. They are not standard ITU-T G.709 bit-rate signals. They do not interwork with standard mappings of Ethernet, e.g., using GFP-F. The two over-clocked mechanisms do not interwork with each other. As a result, such signals are generally only deployed in a point-to-point configuration between equipment that implements the same mapping.

8.3 Timing and synchronization

The timing tolerance for ITU-T G.709 signals is ± 20 ppm. The timing tolerance for 10GBASE-R Ethernet signals is ± 100 ppm. Mappings that simply wrap the Ethernet signal in an ITU-T G.709-like frame (e.g., those described in clauses 7.1 and 7.2) derive their timing from the Ethernet signal, and hence have a timing accuracy of ± 100 ppm.

The control of jitter and wander for ITU-T G.709 signals having a timing accuracy of ± 20 ppm has been extensively analysed in [ITU-T G.8251]. No such analysis has been done for Ethernet-based signals with a timing accuracy of ± 100 ppm. Signals with a timing accuracy of ± 100 ppm should generally only be deployed in point-to-point situations where jitter and wander accumulation is not an issue.

8.4 Optical characteristics

[ITU-T G.959.1] specifies optical tributary classes for 10G operation that are applicable to signals from 2.4 Gbit/s to 10.71 Gbit/s. Signals above 10.71 Gbit/s, including the two over-clocked mappings, only fall within the 40G range of 9.9 Gbit/s to 43.02 Gbit/s. [ITU-T G.696.1] specifies a similar set of ranges for client classes of 10G and 40G. Since the signals according to clauses 7.1 and 7.2 exceed the 10G ranges, the spectral characteristics are beyond that of a standard 10G

channel, which should be taken into account in selecting the appropriate frequency grid for transport of these signals.

8.5 Multiplexing, multi-service

[ITU-T G.709] provides for multiplexing of 10-Gbit/s signals via ODU2 into ODU3. This multiplexing hierarchy allows for optimizing fibre capacity by carrying the largest number of bits per wavelength.

As long as standard bit-rate signals are used in the network, multiplexing to 40 Gbit/s as specified in clause 19 of [ITU-T G.709] is straightforward. Multi-service networking is possible: it is not necessary that all 10 Gbit/s ODU2s be transporting the same type of signal. ODU2 signals carrying diverse payloads including STM-64, GFP-F mapped Ethernet or in turn multiplexing four 2.5-Gbit/s ODU1 signals can be combined in the same 40-Gbit/s wavelength.

But this multiplexing mechanism relies on ODU2 signals of a standard bit rate (10'037'273.924 kbit/s) and timing tolerance (± 20 ppm). This multiplexing mechanism is not specified for non-standard bit rates (e.g., the ODU2e (10.3995 Gbit/s) and ODU1e (10.3558 Gbit/s) signals described in clauses 7.1 and 7.2, respectively). These two non-standard bit rates cannot be multiplexed with any standard bit-rate signals or with each other. The stuff opportunities of the multiplexing mechanism of [ITU-T G.709] are also designed based on an assumption of ± 20 ppm timing tolerance.

8.6 Transparency

Ethernet is a packet technology. Clause 6 of [ITU-T G.8010] defines the characteristic information of an Ethernet layer network as being a non-contiguous flow of ETH_CI traffic units, each consisting of a destination address, a source address and a MAC service data unit, delimited by headers and trailers that are link specific.

8.6.1 Information transparency

All of the mappings discussed in this supplement carry the flow of ETH_CI traffic units, and hence are transparent to the Ethernet layer network characteristic information.

8.6.2 MAC frame transparency

The link-specific headers and trailers used for ETH_CI traffic units carried using the mappings described in this supplement are summarized in Table 8-2.

Table 8-2 – ETH_CI header and trailer used in different mappings

| Mapping (clause) | Header format | Trailer format | Inter-frame filler |
|--------------------------------------|-----------------------------|----------------|--------------------|
| 6.1 | Preamble + SFD | MAC FCS | IPG |
| 6.2 | GFP header | MAC FCS | GFP idle |
| 7.1 | Preamble + SFD | MAC FCS | IPG |
| 7.2 | Preamble + SFD | MAC FCS | IPG |
| See [ITU-T G.709] and [ITU-T G.7041] | GFP header + preamble + SFD | MAC FCS | GFP idle |

In [IEEE 802.3] preambles, SFD, ordered sets and IPG are considered to be overhead, not payload. They do not transit a bridge or a repeater in any standardized full duplex Ethernet technology. They were originally put into the frame format to support collision detection for half duplex Ethernet interfaces at 100 Mbit/s and lower rates. As this is effectively "free space" for full duplex interfaces,

there have been cases where the preamble and IPG have been used to transmit data for undisclosed proprietary purposes.

There are cases where a requirement has been expressed that the preamble and IPG should be carried intact over a transport network. To satisfy this requirement for transport of non-standard Ethernet, it is occasionally necessary to use non-standard mappings in the transport network.

8.6.3 Full rate transparency

As described above, Ethernet is a packet technology. Ethernet interfaces exist at a variety of rates. Multiple different rates of interfaces can be utilized in the same Ethernet network, with packet flows being routed at bridges in the network to their destinations.

Since Ethernet is a packet technology rather than a circuit technology, there is no guarantee that there is enough bandwidth to transport all of the packets routed over any specific link. This may occur because a variety of link speeds are used in the network, or simply because packets may arrive at a bridge over many different links that are routed to the same link, exceeding the capacity of that link. Congestion of this sort can result in delays and discarded packets when the buffer capacity at the bridge is exceeded. This is all part of normal Ethernet operation.

Nevertheless, there are cases where it is deemed important to transport every packet from a 10GBASE-R Ethernet interface over a transport network.

The mapping described in clause 6.1 is accomplished via a 10GBASE-W (10G WAN PHY) interface on an Ethernet bridge. Normal Ethernet bridge operation will result in a maximum packet flow over that link that is approximately 3% less than the maximum possible using a 10GBASE-R (10G LAN PHY) interface.

The mapping described in clause 6.2 is capable of transporting the full packet rate of a 10GBASE-R interface even though the serial bit rate available in the OPU2 is lower. The reasons why the same packet flow can be supported over a lower bit rate include:

- The use of the OTN scrambler (clause 11.2 of [ITU-T G.709]) rather than 64B/66B coding to ensure the transitions required for framing the received signal.
- The use of GFP to delimit packets rather than MAC framing. The GFP header uses the same number of octets as the preamble and SFD but, for MAC framing, an IPG is required (minimum 12 octets) following the MAC FCS.

The use of non-standard mappings (clauses 7.1 and 7.2) is only necessary to achieve both the full 10GBASE-R packet rate and the MAC frame transparency (see clause 8.6.2) that would permit non-standard use of the preamble and IPG or PCS sublayer.

8.7 BER monitoring

[ITU-T G.709] provides, in the ODUk frame structure, for BER monitoring independent of the transmitted client signal using a BIP-8 parity check. This is available at the path (ODUk) and section (OTUk) layer, plus up to six layers of tandem connection monitoring.

In addition, mappings that transport the 64B/66B coding of the PCS sublayer can perform BER monitoring from MAC termination to MAC termination within the client layer itself through the detection of invalid 66B codewords.

Mappings that decode 64B/66B before transmitting the packets (e.g., clause 6.2 using GFP-F framing) can still utilize this coding for BER monitoring across the segments of the path using a 10GBASE-R physical interface, but would use the BIP-8 within the ODU2 overhead to monitor BER for OTN segments of the path.

9 Multiplexing four ODU2e signals into ODU3e

This clause introduces a multiplexing method of 4 x ODU2e that are defined in clause 7.1, now moved to clause 17.1 of [ITU-T G.709]. The resulting ODU3e signals defined in clauses 9.1 and 9.2 are referred to as ODU3e1 and ODU3e2, respectively.

9.1 Asynchronous bit-transparent mapping of 4 x ODU2e signal into OPU3e1

9.1.1 Bit rates and capacity of OPU3e1/ODU3e1/OTU3e1

The bit rates and capacity of the OTU3e1 signals are defined in Table 9-1.

The bit rates and capacity of the ODU3e1 signals are defined in Table 9-2.

The bit rates and capacity of the OPU3e1 payload are defined in Table 9-3.

The OTU3e1/ODU3e1/OPU3e1 frame periods are defined in Table 9-4.

Table 9-1 – OTU3e1 types and capacity

| OTU type | OTU nominal bit rate | OTU bit-rate tolerance |
|----------|-----------------------|------------------------|
| OTU3e1 | 44'570'974.576 kbit/s | ±20 ppm |

Table 9-2 – ODU3e1 types and capacity

| ODU type | ODU nominal bit rate | ODU bit-rate tolerance |
|----------|-----------------------|------------------------|
| ODU3e1 | 41'774'364.407 kbit/s | ±20 ppm |

Table 9-3 – OPU3e1 types and capacity

| OPU type | OPU payload nominal bit rate | OPU payload bit-rate tolerance |
|----------|------------------------------|--------------------------------|
| OPU3e1 | 41'599'576.271 kbit/s | ±20 ppm |

Table 9-4 – OTUk/ODUk/OPUk frame periods

| OTU/ODU/OPU type | Period |
|----------------------|--------------|
| OTU3e1/ODU3e1/OPU3e1 | 2.9292606 μs |

9.1.2 ODU2e multiplexing

Figure 9-1 shows the relationship between various time-division multiplexing elements that are defined below and illustrates possible multiplexing structures. Up to four ODU2e signals are multiplexed into an ODTUG3e1 using time-division multiplexing. The ODTUG3e1 is mapped into the OPU3e1.

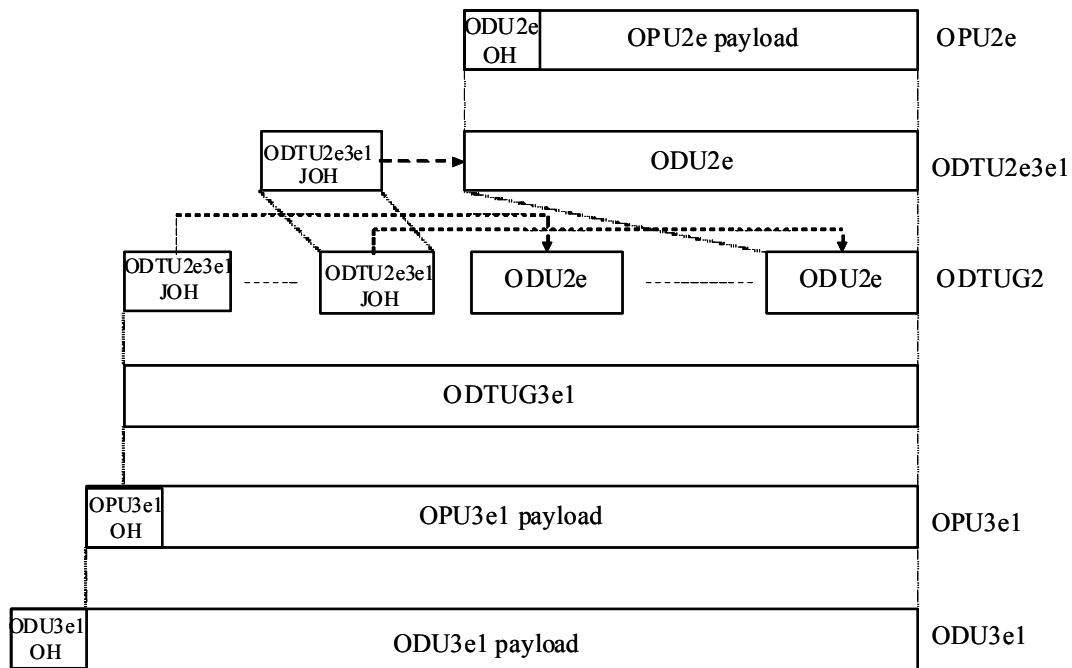


Figure 9-1 – ODU2e into ODU3e1 multiplexing method

9.1.3 Definition of ODU3e1

9.1.3.1 OPU3e1 tributary slot definition

The OPU3e1 is divided into a number of tributary slots (TSs) and these tributary slots are interleaved within the OPU3e1. A tributary slot includes a part of the OPU3e1 OH area and a part of the OPU3e1 payload area. The bytes of the ODU2e frame are mapped into the OPU3e1 payload area of the tributary slot. The bytes of the ODTU2e3e1 justification overhead (JOH) are mapped into the OPU3e1 OH area.

9.1.3.2 OPU3e1 tributary slot allocation

Figure 9-2 presents the OPU3e1 tributary slot allocation. An OPU3e1 tributary slot occupies 6.25% of the OPU3y payload area. It is a structure with 238 columns by 4 rows (see Figure 9-3). The sixteen OPU3e1 TSs are byte interleaved in the OPU3y payload area.

| MFAS Bits | 5678 | Column | 1 | | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | | 3821 | 3822 | 3823 | 3824 |
|-----------|-------|--------|---|-------|----|-----|----------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|------------------|------------------|---------------------------------|------|------|
| 1111 | Row 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 4 | | | | | PSI | JOH TS16 | OPU3e1 TribSlot1 | OPU3e1 TribSlot2 | OPU3e1 TribSlot3 | OPU3e1 TribSlot4 | OPU3e1 TribSlot5 | OPU3e1 TribSlot6 | OPU3e1 TribSlot7 | OPU3e1 TribSlot8 | OPU3e1 TribSlot9 | OPU3e1 TribSlot10 | OPU3e1 TribSlot11 | OPU3e1 TribSlot12 | OPU3e1 TribSlot13 | OPU3e1 TribSlot14 | OPU3e1 TribSlot15 | OPU3e1 TribSlot16 | OPU3e1 TribSlot1 | OPU3e1 TribSlot2 | OPU3e1 payload (4 x 3808 bytes) | | |
| 0000 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 4 | | | | | PSI | JOH TS1 | OPU3e1 TribSlot1 | OPU3e1 TribSlot2 | OPU3e1 TribSlot3 | OPU3e1 TribSlot4 | OPU3e1 TribSlot5 | OPU3e1 TribSlot6 | OPU3e1 TribSlot7 | OPU3e1 TribSlot8 | OPU3e1 TribSlot9 | OPU3e1 TribSlot10 | OPU3e1 TribSlot11 | OPU3e1 TribSlot12 | OPU3e1 TribSlot13 | OPU3e1 TribSlot14 | OPU3e1 TribSlot15 | OPU3e1 TribSlot16 | OPU3e1 TribSlot1 | OPU3e1 TribSlot2 | OPU3e1 payload (4 x 3808 bytes) | | |
| 0001 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 4 | | | | | PSI | JOH TS2 | OPU3e1 TribSlot1 | OPU3e1 TribSlot2 | OPU3e1 TribSlot3 | OPU3e1 TribSlot4 | OPU3e1 TribSlot5 | OPU3e1 TribSlot6 | OPU3e1 TribSlot7 | OPU3e1 TribSlot8 | OPU3e1 TribSlot9 | OPU3e1 TribSlot10 | OPU3e1 TribSlot11 | OPU3e1 TribSlot12 | OPU3e1 TribSlot13 | OPU3e1 TribSlot14 | OPU3e1 TribSlot15 | OPU3e1 TribSlot16 | OPU3e1 TribSlot1 | OPU3e1 TribSlot2 | OPU3e1 payload (4 x 3808 bytes) | | |
| 1111 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0000 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0001 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 3 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Figure 9-2 – OPU3e1 tributary slot allocation

In addition, the justification overhead consisting of justification control (JC) and negative justification opportunity (NJO) signals of the 16 OPU3e1 TSs are located in the overhead area, column 16 of rows 1 to 4. The JOH is assigned to the related tributary slots on a per-frame basis.

The JOH for a tributary slot is available once every 16 frames. A 16-frame multiframe structure is used for this assignment. This multiframe structure is locked to bits 5, 6, 7 and 8 of the MFAS byte as shown in Table 9-5.

Table 9-5 – OPU3e1 justification overhead tributary slots

| MFAS | | | | JOH TS | MFAS | | | | JOH TS | |
|------|---|---|---|--------|------|------|---|---|--------|----|
| Bits | 5 | 6 | 7 | | 8 | Bits | 5 | 6 | | 7 |
| | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 9 |
| | 0 | 0 | 0 | 1 | 2 | 1 | 0 | 0 | 1 | 10 |
| | 0 | 0 | 1 | 0 | 3 | 1 | 0 | 1 | 0 | 11 |
| | 0 | 0 | 1 | 1 | 4 | 1 | 0 | 1 | 1 | 12 |
| | 0 | 1 | 0 | 0 | 5 | 1 | 1 | 0 | 0 | 13 |
| | 0 | 1 | 0 | 1 | 6 | 1 | 1 | 0 | 1 | 14 |
| | 0 | 1 | 1 | 0 | 7 | 1 | 1 | 1 | 0 | 15 |
| | 0 | 1 | 1 | 1 | 8 | 1 | 1 | 1 | 1 | 16 |

9.1.4 ODTU2e3e1 definition

The optical channel data tributary unit 2e3e1 (ODTU2e3e1) is a structure with 952 columns by 64 (16 × 4) rows plus 4 × 1 column of justification overhead. It carries a justified ODU2e signal. The ODTU2e3e1 structure is illustrated in Figure 9-6. The location of the JOH column depends on the OPU3e1 tributary slot used when multiplexing the ODTU2e3e1 into the OPU3e1. They might not be equally distributed.

9.1.5 Mapping ODTU2e3e1 into one OPU3e1 tributary slot

A byte of the ODTU2e3e1 signal is mapped into a byte of one of four OPU3e1 TS #A,B,C,D (A,B,C,D = 1,2,...,16), as indicated in Figure 9-3 for a group of 4 rows out of the ODTU2e3e1.

A byte of the ODTU2e3e1 JOH is mapped into a JOH byte within the OPU3e1 OH allocated to OPU3e1 TS #A,B,C,D.

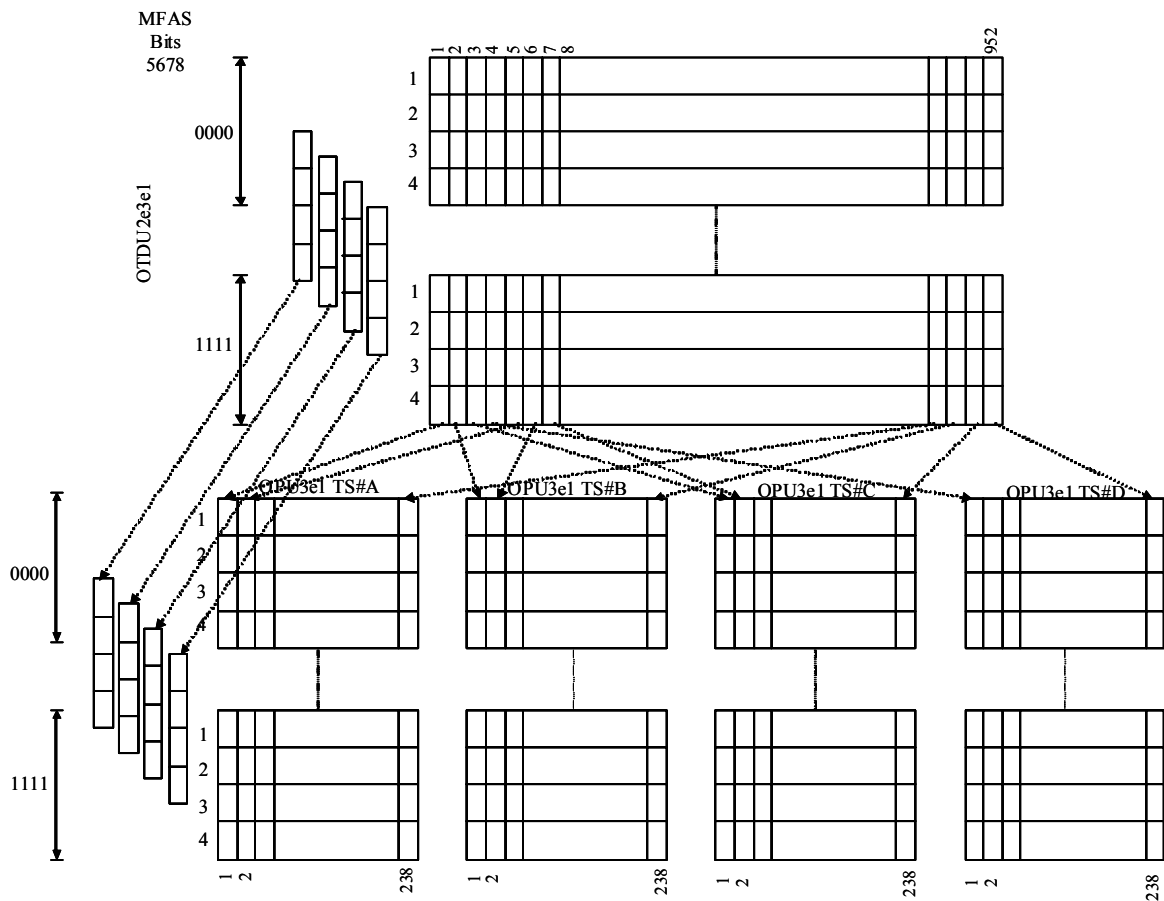


Figure 9-3 – Mapping of ODTU2e3e1 (excluding JOH) into four OPU3e1 TribSlots (#A, #B, #C, #D with A<B<C<D)

9.1.6 OPU3e1 multiplexing overhead

The OPU3e1 multiplex overhead consists of multiplex structure identifier (MSI), justification control A (JCA), justification control B (JCB), negative justification opportunity 1 (NJO1) and negative justification opportunity 2 (NJO2) overhead. The OPU3e1 MSI, JC1, JC2, NJO1 and NJO2 overhead locations are shown in Figure 9-4. In addition, positive justification overhead bytes are located in the OPU3e1 payload. Note that the PJO_x (x=1,2,3) locations are multiframe, ODU2e and OPU3e1 tributary slot dependent.

9.1.6.1 OPU3e1 multiplex structure identifier (MSI)

For the 16 OPU3e1 tributary slots, 16 bytes of the PSI are used as shown in Figure 9-5.

- Bits 1 and 2 indicate the ODU2e type transported in the TS.
- The tributary port # indicates the port number of the ODU2e that is being transported in this TS; in the case of ODU2e, the assignment of tributary ports to tributary slots is flexible.

ODU2e tributary ports are numbered 1 to 4.

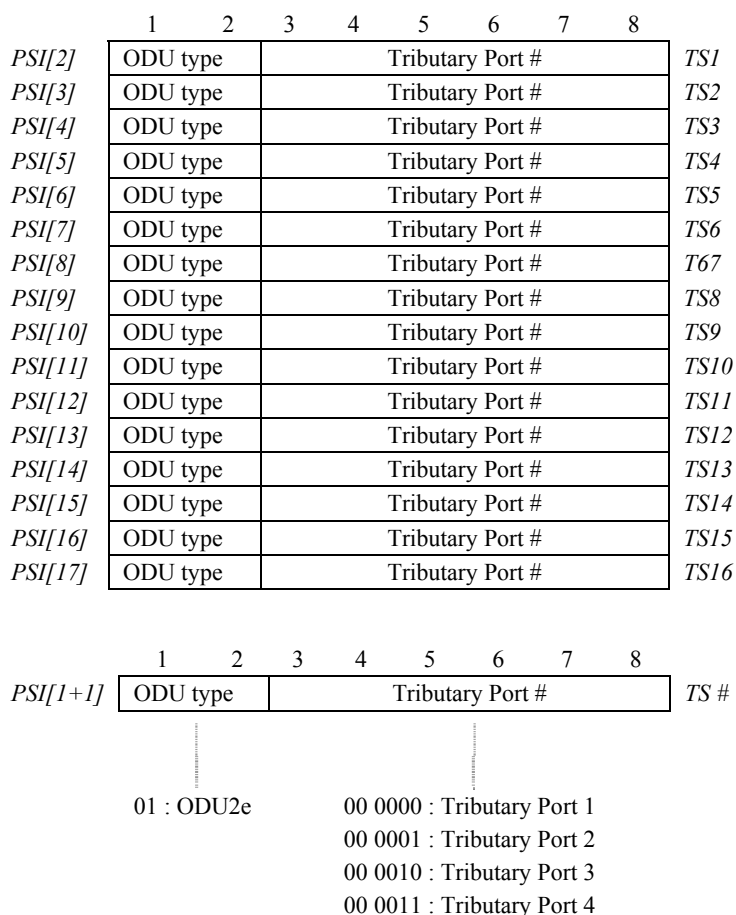


Figure 9-5 – MSI coding for ODU3e1

9.1.6.2 OPU3e1 multiplex justification overhead

The justification overhead for the asynchronous mapping procedure located in column 16 of OPU3e, see Figure 9-4, consists of two justification control bytes (JCA and JCB) and two negative justification opportunity bytes (NJO1 and NJO2). For conventional justification, bits 7 and 8 of JCA, JCB and NJO2 bytes can be used. The three JC1 bits are located in rows 1 (bits 7 and 8), 2 (bits 7 and 8) and 3 (bits 7 and 8). To enhance the frequency tolerance of the accommodated client signal, new justification control bits are defined as JC2 bits which are located in row 1 (bits 3 and 4), row 1 (bits 5 and 6) and row 2 (bits 5 and 6). The NJO1 and NJO2 bytes are located in row 4 and row 3. Bits 7 and 8 of NJO2 bytes are used as justification control bits for conventional justification control, and these bits are also used as negative justification opportunity bits for extended justification. Undefined bits are reserved for future international standardization.

9.1.7 Mapping ODU2e into ODTU2e3e1

A byte of the ODU2e signal is mapped into an information byte of the ODTU2e3e1. Four times per sixteen OPU3e1 frames, it is possible to perform either a positive or a negative justification action.

The four frames in which justification can be performed are related to the JOH of the OPU3e1 TSs in which the ODTU2e3e1 is mapped. Figure 9-6 shows the case with mapping in OPU3e1 TS1, TS5, TS9 and TS10. JC1, JC2, NJO2, NJO1, PJO1, PJO2 and PJO3 generation and interpretation are shown in Table 9-6

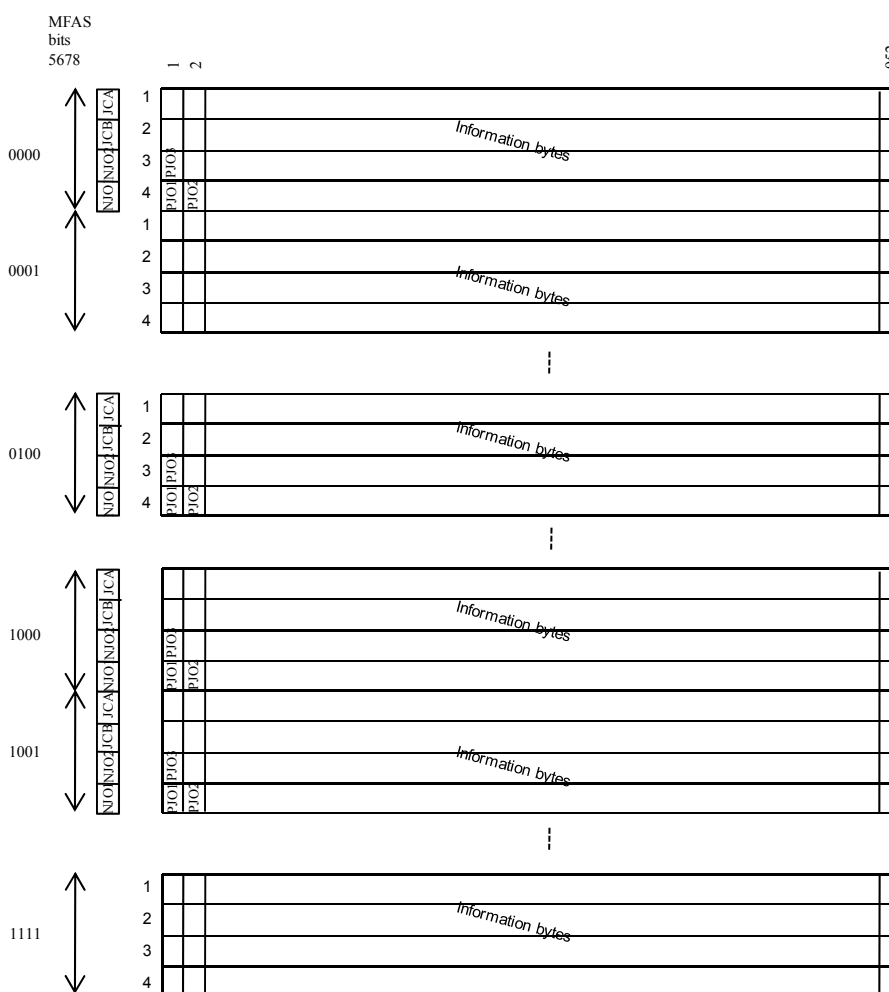


Figure 9-6 – ODTU2e3e1 frame format and mapping of ODU2e

Table 9-6 – JC2, JC1, NJO2, NJO1, PJO1, PJO2 and PJO3 generation and interpretation

| JC2 | JC1 | NJO2 | NJO1 | PJO1 | PJO2 | PJO3 | Interpretation |
|-----|-----|--------------------|--------------------|--------------------|--------------------|--------------------|------------------------------------|
| 00 | 00 | Justification byte | Justification byte | Data byte | Data byte | Data byte | No justification (0) |
| 00 | 01 | Justification byte | Data byte | Data byte | Data byte | Data byte | Negative justification (-1) |
| 00 | 10 | Justification byte | Justification byte | Justification byte | Justification byte | Data byte | Double positive justification (+2) |
| 00 | 11 | Justification byte | Justification byte | Justification byte | Data byte | Data byte | Positive justification (+1) |
| 01 | - | Data byte | Data byte | Data byte | Data byte | Data byte | Double negative justification (-2) |
| 11 | - | Justification byte | Justification byte | Justification byte | Justification byte | Justification byte | Triple positive justification (+3) |

9.2 Asynchronous generic mapping of four ODU2e signals into OPU3e2

9.2.1 Bit rates and capacity of OPU3e2/ODU3e2/OTU3e2

The rates and capacities of OTU3e2/ODU3e2/OPU3e2 are summarized in Table 9-7.

The OTU3e2/ODU3e2/OPU3e2 frame periods are 2.928 μ s.

Table 9-7 – OTU3e2/ODU3e2/OPU3e2 rates and capacities

| Signal type | Nominal bit rate | Tolerance |
|-------------|---|--------------|
| OTU3e2 | $243/217 \times 16 \times 2.488320$ Gbit/s | ± 20 ppm |
| ODU3e2 | $239/255 \times 243/217 \times 16 \times 2.488320$ Gbit/s | ± 20 ppm |
| OPU3e2 | $238/255 \times 243/217 \times 16 \times 2.488320$ Gbit/s | ± 20 ppm |

NOTE – The nominal OTU3e2, ODU3e2 and OPU3e2 payload bit rates are approximately: 44 583 355.576 kbit/s (OTU3e2), 41 785 968.560 kbit/s (ODU3e2) and 41 611 131.871 kbit/s (OPU3e2 payload).

9.2.2 Definition of OTU3e2, ODU3e2 and OPU3e2

The frame structure of the OTU3e2, ODU3e2 and OPU3e2 are the same frame structures as the frame structures of the OTUk, ODUk and OPUk specified in [ITU-T G.709]. The OPU3e2 carries one or more ODUj (j=2e) signals.

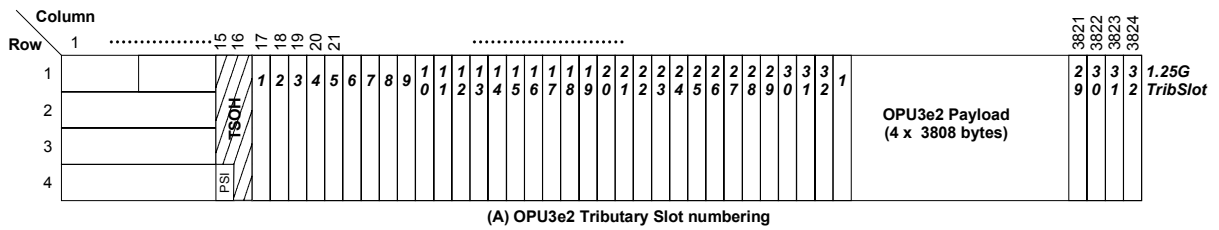
The OTU3e2 FEC is the same as the OTUk (k=1,2,3) FEC specified in [ITU-T G.709].

9.2.2.1 OPU3e2 tributary slot definition

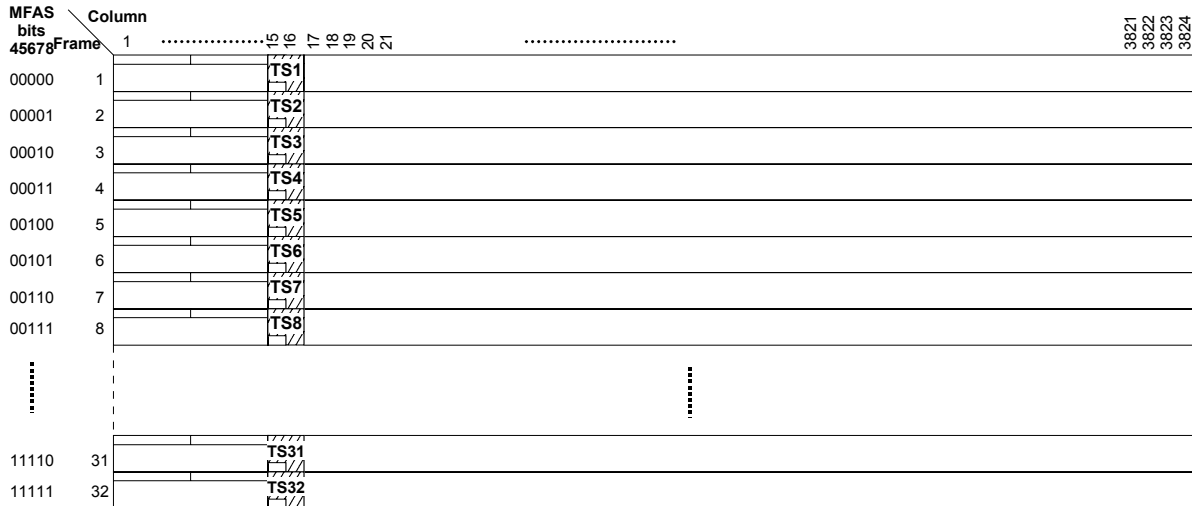
The OPU3e2 is divided into 32 tributary slots (TS) of approximately 1.25 Gbit/s and these tributary slots are interleaved within the OPU3e2. A tributary slot includes a part of the OPU3e2 OH area and a part of the OPU3e2 payload area. The bytes of the ODUj frame are mapped into the ODTUj3e2 payload area and the ODTUj3e2 bytes are mapped into the OPU3e2 tributary slot or slots.

9.2.2.2 OPU3e2 tributary slot allocation

Figure 9-7 presents the OPU3e2 1.25G tributary slot allocation. An OPU3e2 1.25G tributary slot occupies 3.125% of the OPU3e2 payload area. It is a structure with 119 columns by 4 rows. The thirty-two OPU3e2 tributary slots are byte-interleaved into the OPU3e2 payload area.



(A) OPU3e2 Tributary Slot numbering



(B) OPU3e2 Tributary Slot Overhead allocation

Figure 9-7 – OPU3e2 tributary slot allocation

In addition, the tributary slot overhead (TSOH) of the OPU3e2 tributary slots is located in the OPU3e2 overhead area, column 15 of rows 1 to 3 and column 16 of rows 1 to 4. The TSOH is assigned to the related tributary slots on a per-frame basis.

The TSOH for a 1.25G tributary slot is available once every 32 frames. A 32-frame multiframe structure is used for this assignment. This multiframe structure is locked to bits 4,5,6,7,8 of the MFAS byte as shown in Table 9-8.

Table 9-8 – Allocation of OPU3e2 tributary slot overhead to OPU3e2 tributary slots

| MFAS bits 4 5 6 7 8 | Tributary slot |
|------------------------|----------------|
| 0 0 0 0 0 | 1 |
| 0 0 0 0 1 | 2 |
| 0 0 0 1 0 | 3 |
| 0 0 0 1 1 | 4 |
| 0 0 1 0 0 | 5 |
| 0 0 1 0 1 | 6 |
| 0 0 1 1 0 | 7 |
| 0 0 1 1 1 | 8 |
| 0 1 0 0 0 | 9 |
| 0 1 0 0 1 | 10 |
| 0 1 0 1 0 | 11 |
| 0 1 0 1 1 | 12 |
| 0 1 1 0 0 | 13 |
| 0 1 1 0 1 | 14 |
| 0 1 1 1 0 | 15 |
| 0 1 1 1 1 | 16 |

| MFAS bits 4 5 6 7 8 | Tributary slot |
|------------------------|----------------|
| 1 0 0 0 0 | 17 |
| 1 0 0 0 1 | 18 |
| 1 0 0 1 0 | 19 |
| 1 0 0 1 1 | 20 |
| 1 0 1 0 0 | 21 |
| 1 0 1 0 1 | 22 |
| 1 0 1 1 0 | 23 |
| 1 0 1 1 1 | 24 |
| 1 1 0 0 0 | 25 |
| 1 1 0 0 1 | 26 |
| 1 1 0 1 0 | 27 |
| 1 1 0 1 1 | 28 |
| 1 1 1 0 0 | 29 |
| 1 1 1 0 1 | 30 |
| 1 1 1 1 0 | 31 |
| 1 1 1 1 1 | 32 |

9.2.3 ODTUjk definition

9.2.3.1 ODTU2e3e2 definition

The optical channel data tributary unit 2e3e2 (ODTU2e3e2) is a structure with 952 columns by 128 (32×4) rows plus 8×7 bytes of OPU3e2 tributary slot overhead (TSOH). It carries a justified ODU2e signal. The location of the TSOH depends on the OPU3e2 tributary slot used when multiplexing the ODTU2e3e2 into the OPU3e2. They might not be equally distributed.

9.2.4 Multiplexing ODTUjk signals into the OPUk

9.2.4.1 ODTU2e3e2 mapping into eight OPU3e2 tributary slots

A byte of the ODTU2e3e2 signal is mapped into a byte of one of eight OPU3e2 TS #A,B,C,D (A,B,C,D,E,F,G,H = 1,2,...,32), as indicated in Figure 9-8 for a group of 4 rows out of the ODTU2e3e2.

A byte of the ODTU2e3e2 TSOH is mapped into a TSOH byte within the OPU3e2 OH allocated to OPU3e2 TS #A,B,C,D,E,F,G,H.

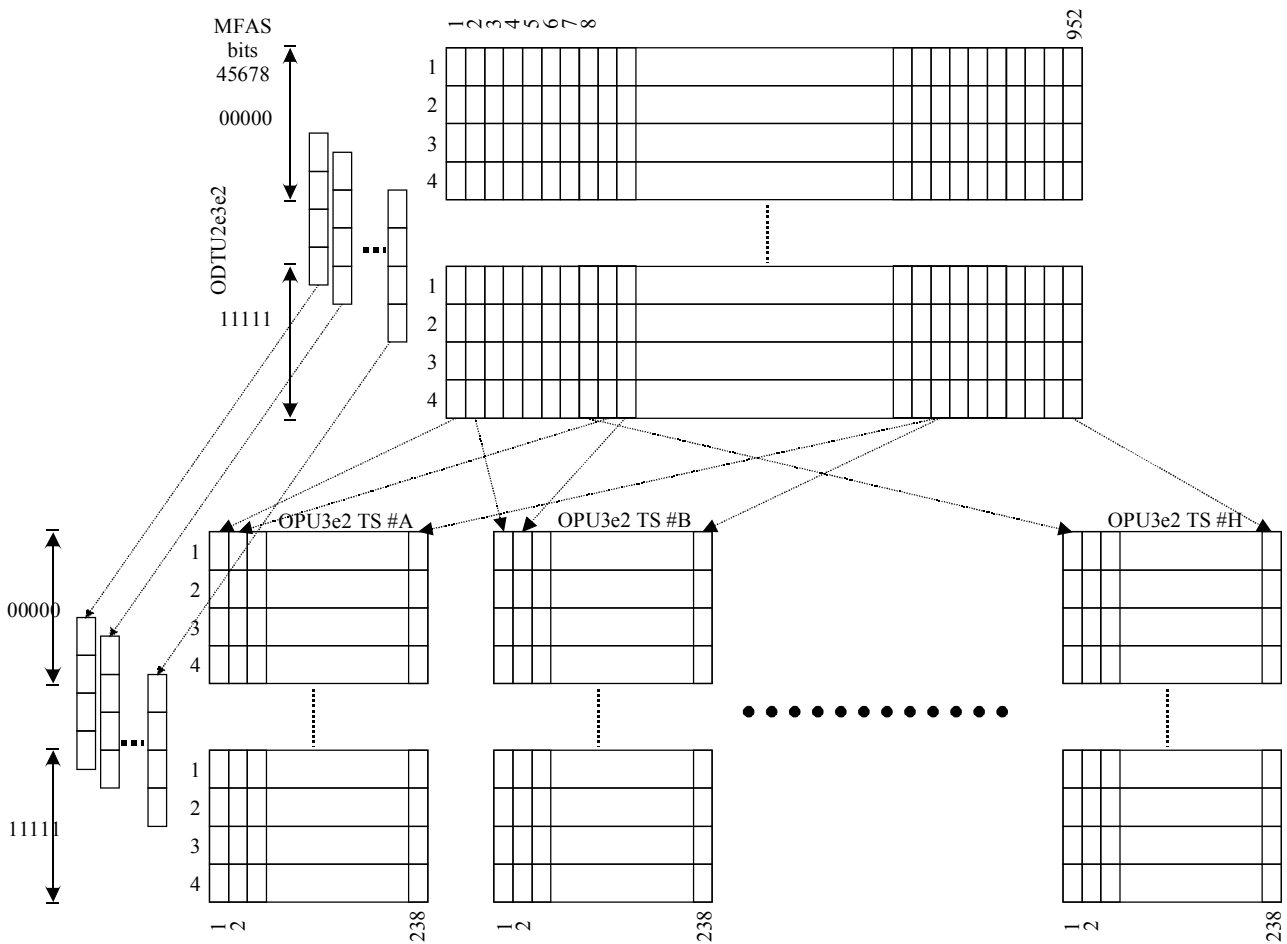


Figure 9-8 – Mapping of ODTU2e3e2 (excluding TSOH) into eight OPU3e2 TribSlots (#A, #B, #C, #D, #E, #F, #G, #H with A<B<C<D<E<F<G<H)

9.2.5 OPU3e2 multiplex overhead

The OPU3e2 multiplex overhead consists of a payload type (PT), a multiplex structure identifier (MSI) and justification overhead. The PT and MSI overhead are located in the PSI multiframe.

ODUj signals mapped into the ODTUj3e2 use the justification overhead for the generic mapping procedure (GMP) that will be specified for the mapping of ODUj into an ODTUj4.

A one-byte payload type is defined in the PSI[0] byte of the payload structure identifier to indicate the composition of the OPU3 signal. The code point for the ODUj multiplexing into OPU3e2 is the same as the one for the ODUj multiplexing into OPU4.

9.2.6 Mapping ODUj into ODTUj3e2

9.2.6.1 Mapping ODU2e into ODTU2e3e2

The mapping of an ODU2e signal into the ODTUj3e2 is performed by means of the asynchronous generic mapping procedure specified for the mapping of ODUj signals into an ODTUj4.

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| Series J | Cable networks and transmission of television, sound programme and other multimedia signals |
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| Series L | Construction, installation and protection of cables and other elements of outside plant |
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