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SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

10-Gigabit-capable passive optical networks: Interface between media access control with serializer/deserializer and physical medium dependent sublayers

ITU-T G-series Recommendations – Supplement 48

ITU-T G-SERIES RECOMMENDATIONS

TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

INTERNATIONAL TELEPHONE CONNECTIONS AND CIRCUITS	G.100–G.199
GENERAL CHARACTERISTICS COMMON TO ALL ANALOGUE CARRIER-TRANSMISSION SYSTEMS	G.200–G.299
INDIVIDUAL CHARACTERISTICS OF INTERNATIONAL CARRIER TELEPHONE SYSTEMS ON METALLIC LINES	G.300–G.399
GENERAL CHARACTERISTICS OF INTERNATIONAL CARRIER TELEPHONE SYSTEMS ON RADIO-RELAY OR SATELLITE LINKS AND INTERCONNECTION WITH METALLIC LINES	G.400–G.449
COORDINATION OF RADIOTELEPHONY AND LINE TELEPHONY	G.450–G.499
TRANSMISSION MEDIA AND OPTICAL SYSTEMS CHARACTERISTICS	G.600–G.699
DIGITAL TERMINAL EQUIPMENTS	G.700–G.799
DIGITAL NETWORKS	G.800–G.899
DIGITAL SECTIONS AND DIGITAL LINE SYSTEM	G.900–G.999
MULTIMEDIA QUALITY OF SERVICE AND PERFORMANCE – GENERIC AND USER-RELATED ASPECTS	G.1000–G.1999
TRANSMISSION MEDIA CHARACTERISTICS	G.6000–G.6999
DATA OVER TRANSPORT – GENERIC ASPECTS	G.7000–G.7999
PACKET OVER TRANSPORT ASPECTS	G.8000–G.8999
ACCESS NETWORKS	G.9000–G.9999

For further details, please refer to the list of ITU-T Recommendations.

Supplement 48 to ITU-T G-series Recommendations

10-Gigabit-capable passive optical networks: Interface between media access control with serializer/deserializer and physical medium dependent sublayers

Summary

Supplement 48 to ITU-T G-series Recommendations provides information on the electrical interface between media access control (MAC) with serializer/deserializer (SERDES) and physical media dependent (PMD) for a 10-Gigabit-capable passive optical network (XG-PON) system with asymmetric nominal data rate of 9.95328 Gbit/s in the downstream direction and 2.48832 Gbit/s in the upstream direction, hereinafter referred to as XG-PON1.

Information is provided in order to facilitate the interoperability level and mass market use of the equipment based on the ITU-T G.987 series of Recommendations. The information provided in this Supplement is complementary to the physical layer requirements and specifications for the XG-PON physical media dependent (PMD) layer for XG-PON described in Recommendation ITU-T G.987.2. This scope of the information provided in this Supplement is focused on the elements in the interface which are important to the XG-PON1 specific interface, and does not intend to cover full specification for the mechanical and physical aspects of the optical PMD, which can be found in various industry multi-source agreement (MSA) PMD specifications for 10G optics.

History

Edition	Recommendation	Approval	Study Group
1.0	ITU-T G Suppl. 48	2010-06-11	15

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The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSA Resolution 1.

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CONTENTS

Supplement 48 to ITU-T G-series Recommendations

10-Gigabit-capable passive optical networks: Interface between media access control with serializer/deserializer and physical medium dependent sublayers

1 Scope

This Supplement describes the electrical interface between the media access control with serializer/deserializer (MAC/SERDES) and the physical medium dependant (PMD) sublayer for a 10-Gigabit-capable passive optical network asymmetric (XG-PON1) system. This Supplement provides the signalling between the MAC/SERDES and PMD, timing requirements and diagrams and electrical characteristics for the interface.

2 References

[ITU-T G.783] Recommendation ITU-T G.783 (2006), *Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks*.

[ITU-T G.825] Recommendation ITU-T G.825 (2000), *The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH)*.

[ITU-T G.957] Recommendation ITU-T G.957 (2006), *Optical interfaces for equipments and systems relating to the synchronous digital hierarchy*.

[ITU-T G.959.1] Recommendation ITU-T G.959.1 (2008), *Optical transport network physical layer interfaces*.

[ITU-T G.984.1] Recommendation ITU-T G.984.1 (2008), *Gigabit-capable passive optical networks (GPON): General characteristics*.

[ITU-T G.984.2] Recommendation ITU-T G.984.2 (2003), *Gigabit-capable Passive Optical Networks (G-PON): Physical Media Dependent (PMD) layer specification; Amendment 2 (2008)*.

[ITU-T G.984.5] Recommendation ITU-T G.984.5 (2007), *Gigabit-capable Passive Optical Networks (G-PON): Enhancement band; Amendment 1 (2009)*.

[ITU-T G.987] Recommendation ITU-T G.987 (2010), *10-Gigabit-capable passive optical network (XG-PON): Definitions, abbreviations, and acronyms*.

[ITU-T G.987.1] Recommendation ITU-T G.987.1 (2010), *10-Gigabit-capable passive optical networks: General requirements*.

[ITU-T G.987.2] Recommendation ITU-T G.987.2 (2010), *10-Gigabit-capable passive optical networks: Physical media dependent layer specification*.

[ITU-T G.987.3] Recommendation ITU-T G.987.3 (2010), *10-Gigabit-capable passive optical networks: Transmission convergence specifications*.

[ITU-T G.988] Recommendation ITU-T G.988 (2010), *Optical network unit management and control interface specification*.

[ITU-T G-Sup.39] ITU-T G-series Recommendations – Supplement 39 (2008), *Optical system design and engineering considerations*.

[SFP+] SFF Committee, SFF-8431 (2009), *Specifications for Enhanced Small Form Factor Pluggable Module SFP+,* Revision 4.1.

[XFP] SFF Committee, INF-8077i (2005), *10 Gigabit Small Form Factor Pluggable Module*, Revision 4.5.

[SFF-8472] SFF Committee, SFF-8472 (2009), *Specification for Diagnostic Monitoring Interface for Optical Transceivers,* Rev 10.4.

3 Definitions

See clause 3 of [ITU-T G.987].

In addition, this Supplement defines the following terms:

3.1 received signal strength indication (RSSI): A measurement of the optical power present in a received signal. It is specifically used in PON to indicate both continuous mode optical receive power at the ONU and burst mode optical receive power measured and averaged for each ONU separately, at the OLT.

3.2 MAC/SERDES: MAC is media access control and SERDES is serializer/deserializer. It refers to the device implementing the media access control meaning the XGTC and above layers and optionally SERDES device connected to the PMD sublayer.

4 Abbreviations and acronyms

See clause 4 of [ITU-T G.987].

5 Conventions

See clause 5 of [ITU-T G.987].

6 Architecture of the optical access network

See [ITU-T G.984.1]. For convenience, Figure 1 of [ITU-T G.984.2] is reproduced below, presented in Figure 6-1:

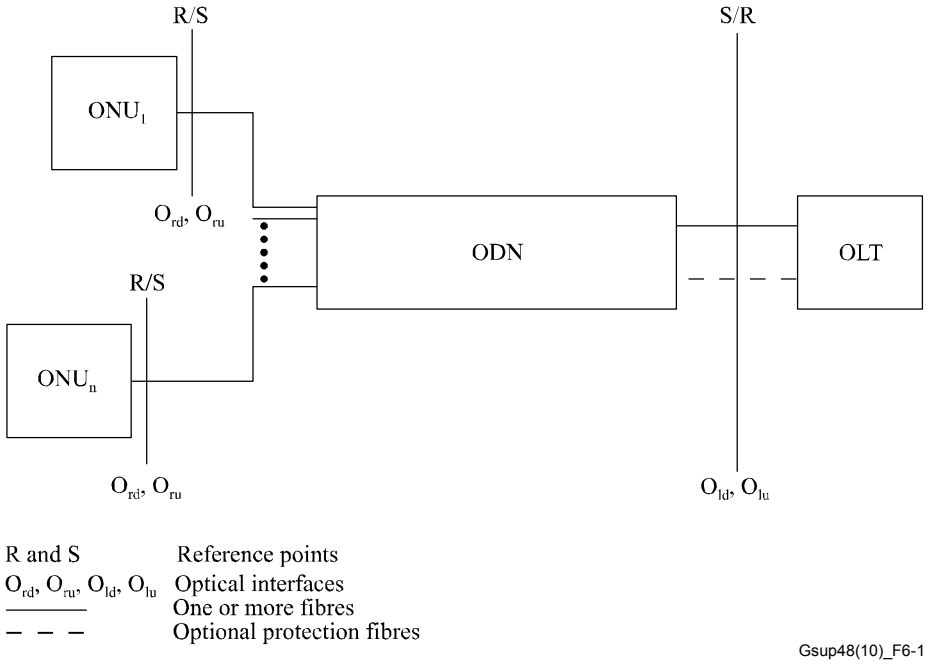


Figure 6-1 – Generic physical configuration of the optical distribution network (reproduced from Figure 1 of [ITU-T G.984.2])

The two directions for optical transmission in the ODN are identified as follows:

– downstream direction for signals travelling from the OLT to the ONU(s); and

– upstream direction for signals travelling from the ONU(s) to the OLT.

Transmission in downstream and upstream directions can take place on the same fibre and components (duplex/diplex configuration).

Figure 6-2 presents reference points between the MAC/SERDES and PMD at the ONU and OLT.

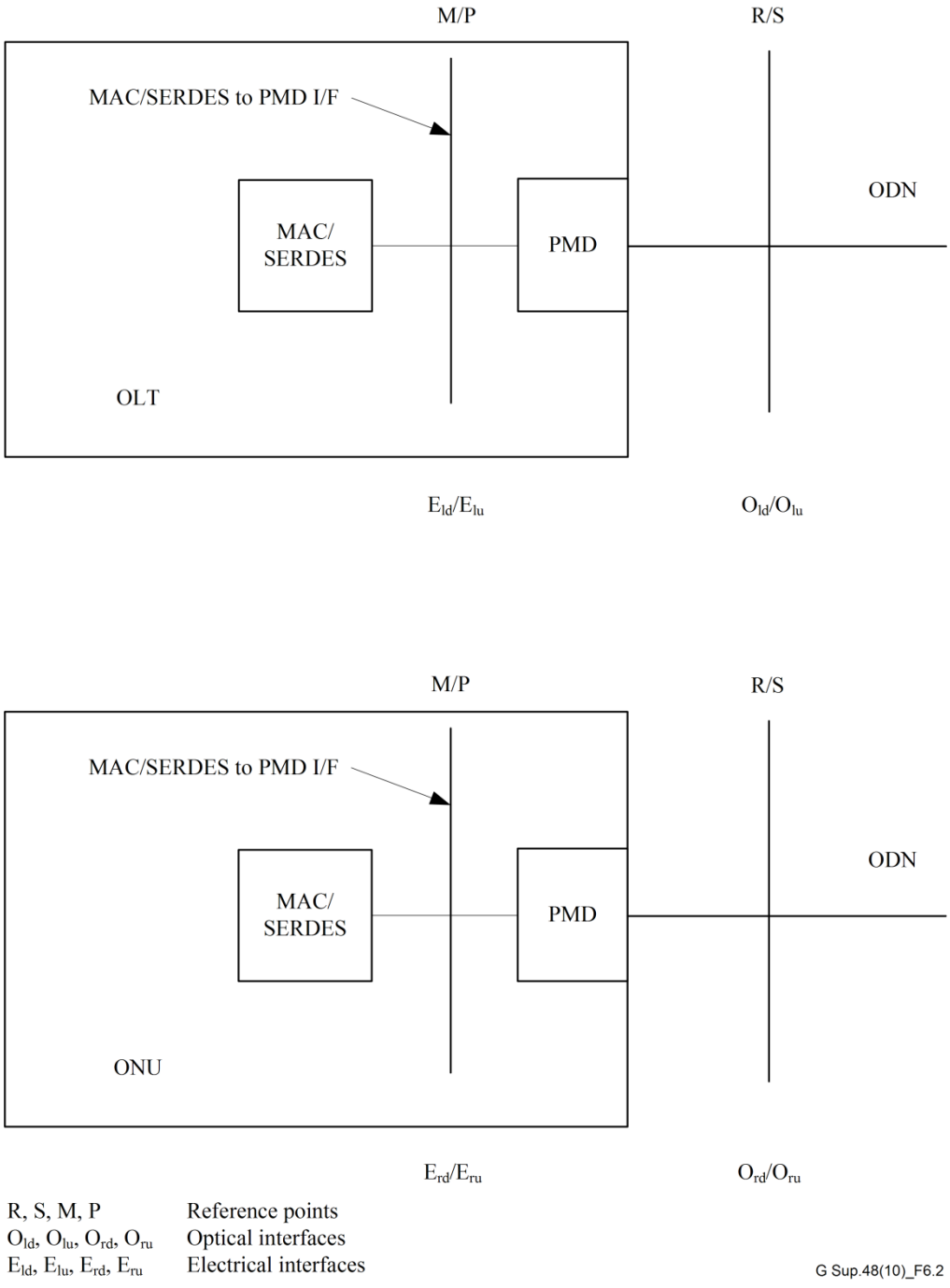


Figure 6-2 – Reference points between the MAC/SERDES and PMD at the architecture of the ONU and OLT

7 MAC/SERDES TO PMD interface requirements

This Supplement defines the electrical interfaces between the PMD optical component and the MAC/SERDES device for XG-PON1, which are operating in asymmetric nominal data rate of 9.95328 Gbit/s in the downstream direction and 2.48832 Gbit/s in the upstream direction. The high speed electrical interface between the MAC/SERDES and the PMD module is an extended specification for the XG-PON1 of electrical interfaces specified in different PMD MSAs, such as the SFI and XFI. The SFI interface is defined for the [SFP+] and XFI for the [XFP]. These electrical interfaces also include transmit pre-emphasis and receive equalization to overcome printed circuit board (PCB) and external media impairments.

At the ONU, the electrical interface for the high speed data transmitter and receiver is based on high speed, low voltage AC coupled logic with a nominal differential impedance of 100 Ω.

At the OLT, the electrical interface for the high speed data transmitter is based on high speed, low voltage AC coupled logic with a nominal differential impedance of 100 Ω.

At the OLT, the electrical interface for the high speed data receiver is based on high speed, low voltage DC coupled logic or AC coupled logic, with a nominal differential impedance of 100 Ω.

The electrical specifications include also lower speed control signals for burst mode transmission and burst mode receiving operation. Control lines operate every burst transmission (every tens hundreds of μs) and can be switched in few ns.

The optical characteristic and specification of the PMD module are defined in [ITU-T G.987.2]. The MAC specification and operation are defined in [ITU-T G.987.3].

It is assumed that the PMD modules complying with this Supplement will be either including clock and data recovery (CDR) function or not including CDR function. It is assumed that the PMD modules and MAC/SERDES devices complying with this Supplement will be allowed to do pre-emphasis function in transmission of the data and equalization in the reception of the data in order to keep the signal integrity of the electrical path. In case the CDR/Retimer is inside the PMD, there might be a need to add at the interface Ref_clk signals to provide it a reference clock for its operation.

7.1 BER performance

BER for XG-PON1 is defined in [ITU-T G.987.2] and [ITU-T G.987.3]. Forward error correction (FEC) is mandatory in downstream operation, and it is mandatory to implement but optional to use in upstream operation. FEC in downstream is RS(248, 216, 32), and FEC in upstream is RS(248, 232, 16) family for the asymmetric rate. Therefore, BER for DS operation is expected to be 10^{-3}, and BER for US operation is expected to be $10^{-12}/10^{-4}$, depending on the disable/enable of the operation of the FEC.

7.2 Line code

The downstream and upstream line coding for XG-PON1 is NRZ.

7.3 Transmission methodology

Bidirectional transmission is accomplished by the use of wavelength division multiplexing (WDM) technique on a single fibre. The upstream signal is time division multiplexed (TDMed) between the different ONUs.

It is therefore assumed that there is a single separate RX interface and a single separate TX interface at the electrical interface, both at the ONU and at the OLT. As the upstream path is time division multiplexed (TDMed) between the different ONUs, the TX at the ONU is switched according to the burst allocation and the RX at the OLT is switched between the different allocation of the ONUs. This operation is marked as "burst mode". Switching time affects the performance of the network.

Timing requirements for switching are defined in [ITU-T G.987.3]. The electrical interface should consider burst mode.

7.4 Coexistence

The operation of an XG-PON1 network should coexist on the same PON with a G-PON network. G-PON and XG-PON1 are WDM multiplexed both in downstream and in upstream channels.

7.5 Diagnostics

It is expected that the PMD will gather diagnostics data of the optical link characteristics, including among the others the received signal strength indicator (RSSI). The electrical interface should define a data path to transfer this diagnostic to the MAC/SERDES.

At the ONU, the gathering of the diagnostic data from the PMD to the MAC/SERDES is expected to be in a digital manner, meaning that the PMD collects the diagnostics data and transfers it to the MAC/SERDES through the host management interface through the memory map, which is not specified in this Supplement and can be found in different MSAs as in [SFF-8472]. No special pins are allocated at the ONU for the RSSI as the optical receive power is continuous.

At the OLT, the gathering of the diagnostic data from the PMD to the MAC/SERDES is expected to be in a digital manner, meaning that the PMD collects the diagnostics data and transfers it to the MAC/SERDES through the host management interface, through the memory map, which is not specified in this Supplement and can be found in different MSAs, as in [SFF-8472]. As the RSSI is measured in burst mode for each ONU, there is a need for a strobe signal that will mark for the PMD the right point to measure the RSSI for the specific ONU desired by the MAC/SERDES. Once the PMD identifies the trigger, it performs the measurement, and then presents the result in a register which can be read through the host management interface. Averaging the RSSI for each ONU and storing the information for each ONU is in the responsibility of the management entity. Timing requirements or the process are described in clause 8.3.2.

Rogue ONU indication

At the ONU, it is expected that indication for rogue ONU would be provided by the host management channel and be polled by the MAC/SERDES for alarm. Indication can be coming through indication of transmission when grant is not enabled or a similar element like checking the average rate of transmission.

7.6 Management

It is expected that the PMD will have a 2-wire management interface. Special PON management attributes should be added in this Supplement.

The following list of parameters is discussed in this Supplement:

ONU:

RSSI power

Rogue ONU indication

Powersave capability – None, TX only, RX+TX

All timing parameters are from clause 8.3.1:

- laser on time of the optics;
- laser off time of the optics;
- time that the optics need before going out of powersave;
- time until optics can go to powersave mode

OLT:

RSSI power

All timing parameters are from clause 8.3.2:

- time from start of the grant to the RX_RESET;
- RX_RESET pulse width;
- RSSI strobe pulse width;
- time until RSSI data is valid in the register;
- strobe delay time for stable monitoring.

8 MAC/SERDES to PMD interface – Electrical interface specifications

This clause provides specification of the electrical interface between the MAC/SERDES and PMD for XG-PON1. In this clause, signal definitions and their timing requirements, together with electrical and AC specifications of the specified interface, will be provided.

8.1 MAC/SERDES to PMD interface pin definitions

8.1.1 MAC/SERDES to PMD interface definition at the ONU

8.1.1.1 Pin definition table

Table 8-1 provides the PON specific pin definition of the ONU MAC/SERDES to PMD interface. The interface is defined from the PMD side. PMD is connected to a SERDES device. Integration between the SERDES and CDR block and MAC chipset is optional.

Table 8-1 – Pin definition of the MAC/SERDES to PMD interface for the ONU

Symbol	Logic		Name/Description
TXD+	LVCML	I	Transmit non inverted data line. AC coupling.
TXD-	LVCML	I	Transmit inverted data line. AC coupling.
RXD+	LVCML	O	Receive non inverted data line AC coupling.
RXD–	LVCML	O	Receive inverted data line. AC coupling.
TX_FAULT	LVTTL	O	Transmit fault.
TX_DIS	LVTTL	I	Transmitter Disable. Turns off the transmitter laser output. (Note 1)
M_DIS	LVTTL	I	Module Disable. Puts the module in sleep. (Note 2)
RX_LOS	LVTTL	O	Receiver loss signal indication.
Ref_clk+	LVCML	I	CDR Reference clock non inverted data line. AC coupling. Optional pin.
Ref_clk–	LVCML	I	CDR Reference clock inverted data line. AC coupling. Optional pin.
Man_D	LVTTL	I/O	Management serial data signal. (Note 3)
Man_C	LVTTL	I	Management clock signal. (Note 3)
NOTE 1 – Signal has burst mode characteristics and switching time is derived from the switching time in [ITU-T G.987.2]. For the timing diagram, see clause 8.3. NOTE 2 – This signal is used for power saving operation as defined in [ITU-T G.987.3]. Signal has burst mode characteristics. Switching time is derived from the powersaving specifications defined in [ITU-T G.987.3]. For the timing diagram, see clause 8.3. NOTE 3 – Serial management signals are referred to PMD specifications like [SFP+] and [XFP] and should operate accordingly.			

8.1.1.2 Interface diagram

Figure 8-1 illustrates the ONU MAC/SERDES to PMD interface. PMD is connected to a SERDES device. Integration between the SERDES and CDR block and MAC chipset is optional.

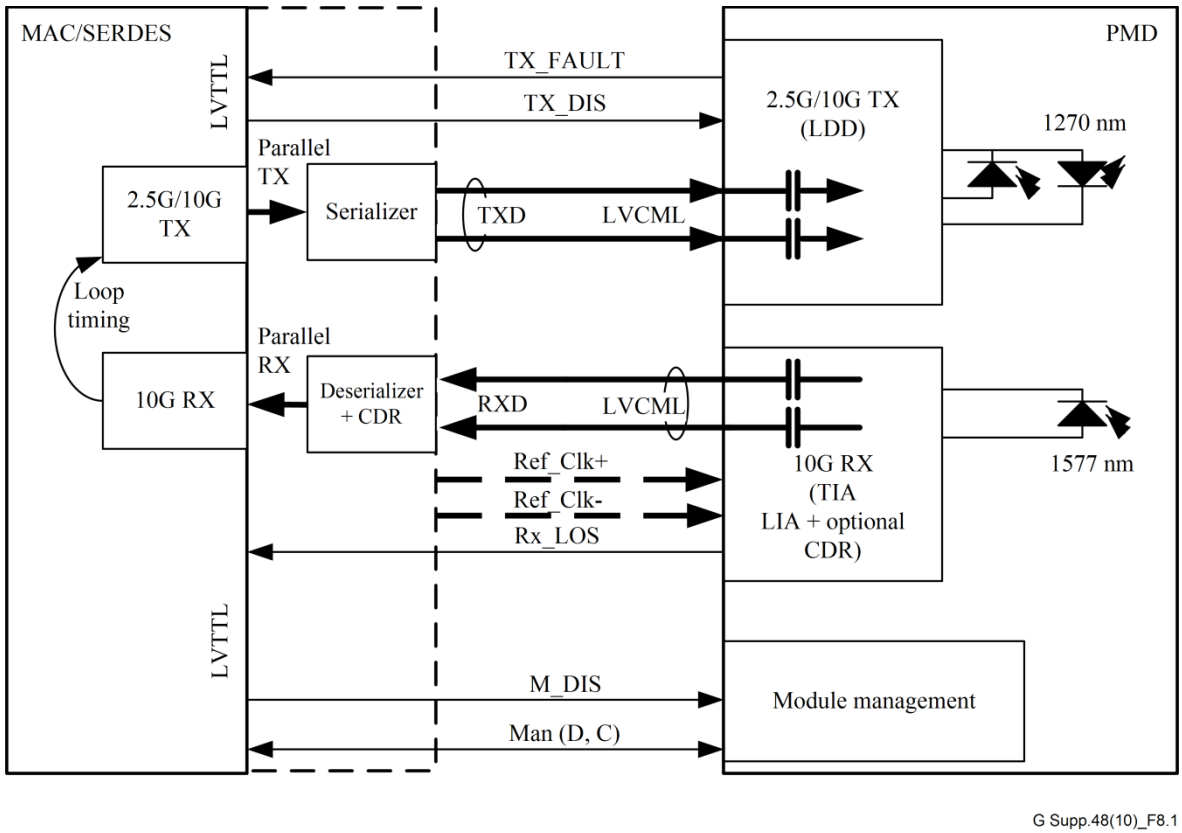


Figure 8-1 – MAC/SERDES to PMD electrical connection at the ONU

8.1.1.3 Interface details

This clause provides the details of the signals. Yet for full specifications, there is a need to refer to the specific PMD specifications, such as [SFP+] or [XFP].

TXD+

TXD+ is the positive non inverted line of the LVCML data input line. It is an input to the PMD module. At the PMD, the input has a DC blocking for AC coupling of the signal.

TXD–

TXD– is the negative, inverted line of the LVCML data input line. It is an input to the PMD module. At the PMD, the input has a DC blocking for AC coupling of the signal.

RXD+

RXD+ is the positive non inverted line of the LVCML data output line. It is an output to the PMD module. At the PMD, the output has a DC blocking for AC coupling of the signal.

RXD–

RXD– is the negative, inverted line of the LVCML data output line. It is an output to the PMD module. At the PMD, the output has a DC blocking for AC coupling of the signal.

TX_FAULT

TX_FAULT is an output of the PMD module and it indicates a fault condition in the transmitter laser or a safety problem. TX_FAULT is an LVTTL signal. If the TX_FAULT is not functional at the PMD, it should be held low by the PMD (not indicating a fault). When TX_FAULT is high, it indicates that the PMD module transmitter has detected a fault condition.

TX_FAULT shall be pulled up by the MAC/SERDES with a resistor or an active termination.

TX_DIS

TX_DIS is an input to the PMD module and it controls the laser transmission. When TX_DIS has a low value, the laser starts to transmit after laser_on time. When TX_DIS is high or is left open, the laser stops transmitting after laser_off time. TX_DIS is an LVTTL signal. TX_DIS shall be pulled up by the PMD with a resistor or an active termination.

M_DIS

M_DIS is an input to the PMD module and it controls the powersave mode of the PMD. When the M_DIS has a low value, the PMD goes to powersave mode after power_down time. When the M_DIS is high or left open, the PMD goes to normal after power_up time. TX_DIS can be activated only after the PMD is back to normal mode. M_DIS is an LVTTL signal. The M_DIS shall be pulled up by the PMD with a resistor or an active termination. Powersave mode can turn off the transmitter or both the receiver and transmitter. This control may also not exist at the PMD at all. The powersave status and capabilities are indicated through the serial management interface.

RX_LOS

RX_LOS is an output of the PMD module and it indicates that the optical power level at the input of the receiver is below the LOS threshold. RX_LOS is an LVTTL signal. When RX_LOS is high, it indicates that the optical power level at the input of the receiver is below the LOS threshold.

If the RX_LOS is not functional at the PMD, it should be held low by the PMD.

RX_LOS shall be pulled up by the MAC/SERDES with a resistor or an active termination.

Ref_clk+

Ref_clk+ is the positive non inverted line of the LVCML CDR reference clock input line, in case a CDR/Retimer is integrated inside the PMD module and it needs a reference clock. It is an optional pin. It is an input to the PMD module. At the PMD, the input has a DC blocking for AC coupling of the signal.

Ref_clk–

Ref_clk– is the negative, inverted line of the LVCML CDR reference clock input line, in case a CDR/Retimer is integrated inside the PMD module and it needs a reference clock. It is an optional pin. It is an input to the PMD module. At the PMD, the input has a DC blocking for AC coupling of the signal.

Man_D

A 2-wire electrical interface used for management. Man_D is the data pin and it is an input/output signal. Man_D is an LVTTL signal.

Man_D shall be pulled up by the MAC/SERDES with a resistor or an active termination.

Man_C

A 2-wire electrical interface used for management. Man_C is the clock pin and it is an input signal to the PMD. Man_C is an LVTTL signal.

Man_C shall be pulled up by the MAC/SERDES with a resistor or an active termination.

8.1.2 MAC/SERDES to PMD interface definition at the OLT

8.1.2.1 Pin definition table

Table 8-2 provides the PON specific pin definition of the OLT MAC/SERDES to PMD interface. The interface is defined from the PMD side. PMD is connected to a SERDES device. Integration between the SERDES and CDR block and MAC chipset is optional.

Table 8-2 – Pin definition of the MAC/SERDES to PMD interface for the OLT

Symbol	Logic		Name/Description
TXD+	LVCML	I	Transmit non inverted data line. AC coupling.
TXD-	LVCML	I	Transmit inverted data line. AC coupling.
RXD+	LVCML	O	Receive non inverted data line. DC coupling or AC coupling.
RXD-	LVCML	O	Receive inverted data line. DC coupling or AC coupling.
TX_FAULT	LVTTL	O	Transmit fault.
TX_DIS	LVTTL	I	Transmitter Disable. Turns off the transmitter laser output.
RX_RESET	LVTTL	I	Resets the receive engine of the optical module. Signals the beginning of the burst from the MAC/SERDES. (Note 1)
RX_LOS	LVTTL	O	Receiver loss signal indication.
RSSI_strobe	LVTTL	I	RSSI strobe signal. Provides a strobe for the power measurement of the optical received signal. It is optional in case a digital sampling is done in the PMD. (Note 2)
Ref_clk+	LVCML	I	CDR Reference clock non inverted data line. AC coupling. Optional pin.
Ref_clk-	LVCML	I	CDR Reference clock inverted data line. AC coupling. Optional pin.
Man_D	LVTTL	I/O	Management serial data signal. (Note 3)
Man_C	LVTTL	I	Management clock signal. (Note 3)
NOTE 1 – Signal has burst mode characteristics, and switching time is derived from the switching time in [ITU-T G.987.2]. For the timing diagram, see clause 8.3. NOTE 2 – Signal has burst mode characteristics, and switching time is derived from the switching time in [ITU-T G.987.2]. For the timing diagram, see clause 8.3. NOTE 3 – Serial management signals are referred to PMD specifications like [SFP+] and [XFP] and should operate accordingly.			

8.1.2.2 Interface diagram

Figure 8-2 illustrates the OLT MAC/SERDES to PMD interface. PMD is connected to a SERDES device. Integration between the SERDES and CDR block and MAC chipset is optional.

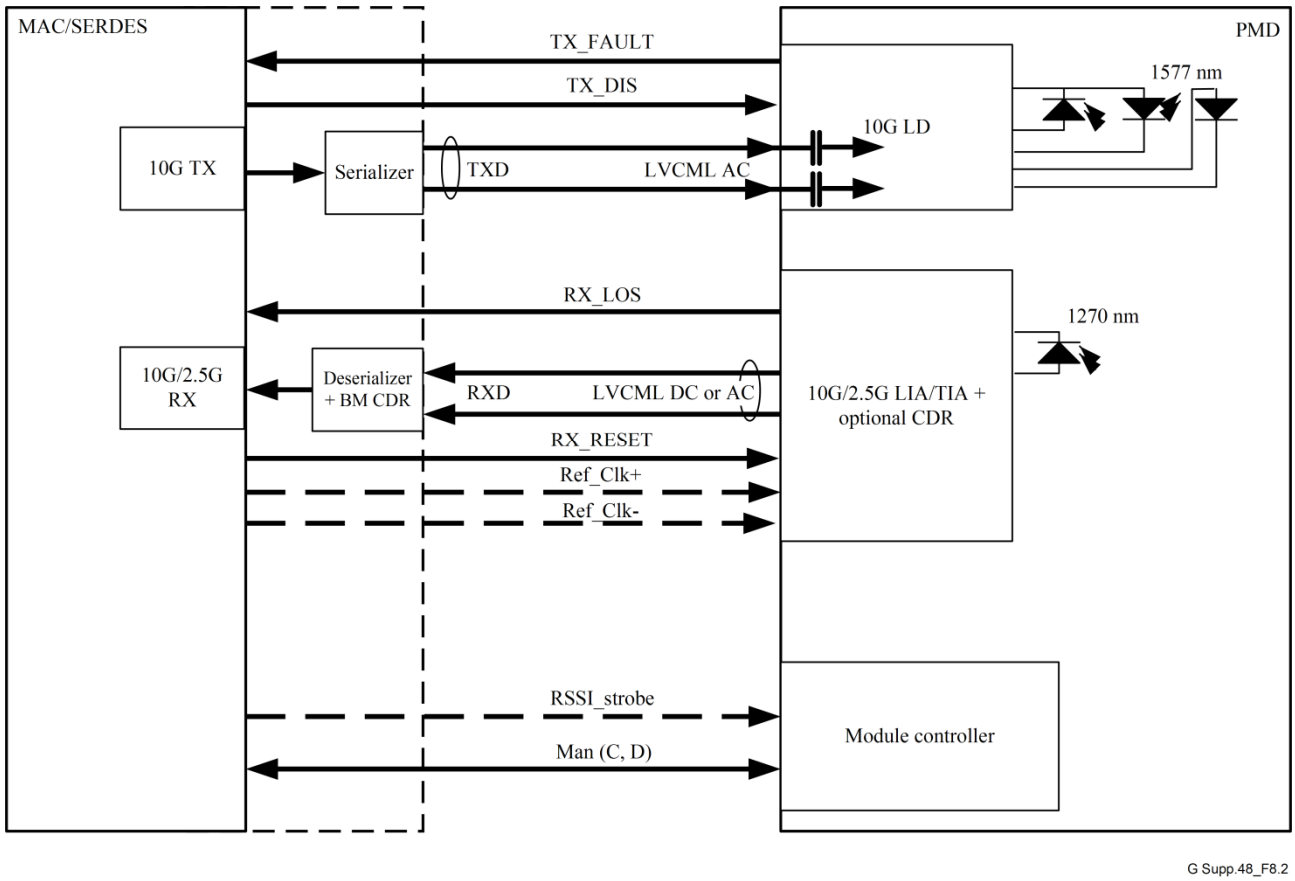


Figure 8-2 – MAC/SERDES to PMD electrical connection at the OLT

8.1.2.3 Interface details

This clause provides the details of the signals. Yet for full specifications, there is a need to refer to the specific PMD specifications, such as [SFP+] or [XFP].

TXD+

TXD+ is the positive non inverted line of the LVCML data input line. It is an input to the PMD module. At the PMD, the input has a DC blocking for AC coupling of the signal.

TXD–

TXD– is the negative, inverted line of the LVCML data input line. It is an input to the PMD module. At the PMD, the input has a DC blocking for AC coupling of the signal.

RXD+

RXD+ is the positive non inverted line of the LVCML data output line. It is an output to the PMD module. There are two options, AC coupled and DC coupled. In AC coupled at the PMD, the output has a DC blocking for AC coupling of the signal. In DC coupled, there is no DC blocking.

RXD–

RXD– is the negative, inverted line of the LVCML data output line. It is an output to the PMD module. There are two options, AC coupled and DC coupled. In AC coupled at the PMD, the output has a DC blocking for AC coupling of the signal. In DC coupled, there is no DC blocking.

TX_FAULT

TX_FAULT is an output of the PMD module and it indicates a fault condition in the transmitter laser or safety problem. TX_FAULT is an LVTTL signal. If the TX_FAULT is not functional at the PMD, it should be held low by the PMD (not indicating a fault). When TX_FAULT is high, it indicates that the PMD module transmitter has detected a fault condition.

TX_FAULT shall be pulled up by the MAC/SERDES with a resistor or an active termination.

TX_DIS

TX_DIS is an input to the PMD module and it controls the laser transmission. When TX_DIS has a low value, the laser starts to transmit after laser_on time. When TX_DIS is high or is left open, the laser stops transmitting after laser_off time. TX_DIS is an LVTTL signal. TX_DIS shall be pulled up by the PMD with a resistor or an active termination.

RX_RESET

RX_RESET is an input to the PMD module and it provides an indication for the burst start to the receiver. When RX_RESET has a high pulse value with a determined width, the receiver gets ready for the burst data after sync_time. RX_RESET is an LVTTL signal. RX_RESET shall be pulled down by the PMD with a resistor or an active termination.

RSSI strobe

RSSI strobe is an input to the PMD module and it provides an indication for the digital RSSI measurement to the receiver (providing the answer through the management interface). When the RSSI strobe has a high pulse value with a determined width, the receiver gets ready for the RSSI measurement after stable_time. RSSI strobe is an LVTTL signal. RSSI strobe is an optional signal. RSSI strobe shall be pulled down by the PMD with a resistor or an active termination.

RX_LOS

RX_LOS is an output of the PMD module and it indicates that the optical power level at the input of the receiver is below the LOS threshold. RX_LOS is an LVTTL signal. When RX_LOS is high, it indicates that the optical power level at the input of the receiver is below the LOS threshold.

If the RX_LOS is not functional at the PMD, it should be held low by the PMD.

RX_LOS shall be pulled up by the MAC/SERDES with a resistor or an active termination.

Ref_clk+

Ref_clk+ is the positive non inverted line of the LVCML CDR reference clock input line, in case a CDR/Retimer is integrated inside the PMD module and it needs a reference clock. It is an optional pin. It is an input to the PMD module. At the PMD, the input has a DC blocking for AC coupling of the signal.

Ref_clk–

Ref_clk– is the negative, inverted line of the LVCML CDR reference clock input line, in case a CDR/Retimer is integrated inside the PMD module and it needs a reference clock. It is an optional pin. It is an input to the PMD module. At the PMD, the input has a DC blocking for AC coupling of the signal.

Man_D

A 2-wire electrical interface used for management. Man_D is the data pin and it is an input/output signal. Man_D is an LVTTL signal.

Man_D shall be pulled up by the MAC/SERDES with a resistor or an active termination.

Man_C

A 2-wire electrical interface used for management. Man_C is the clock pin and it is an input signal to the PMD. Man_C is an LVTTL signal.

Man_C shall be pulled up by the MAC/SERDES with a resistor or an active termination.

8.2 Compliance points

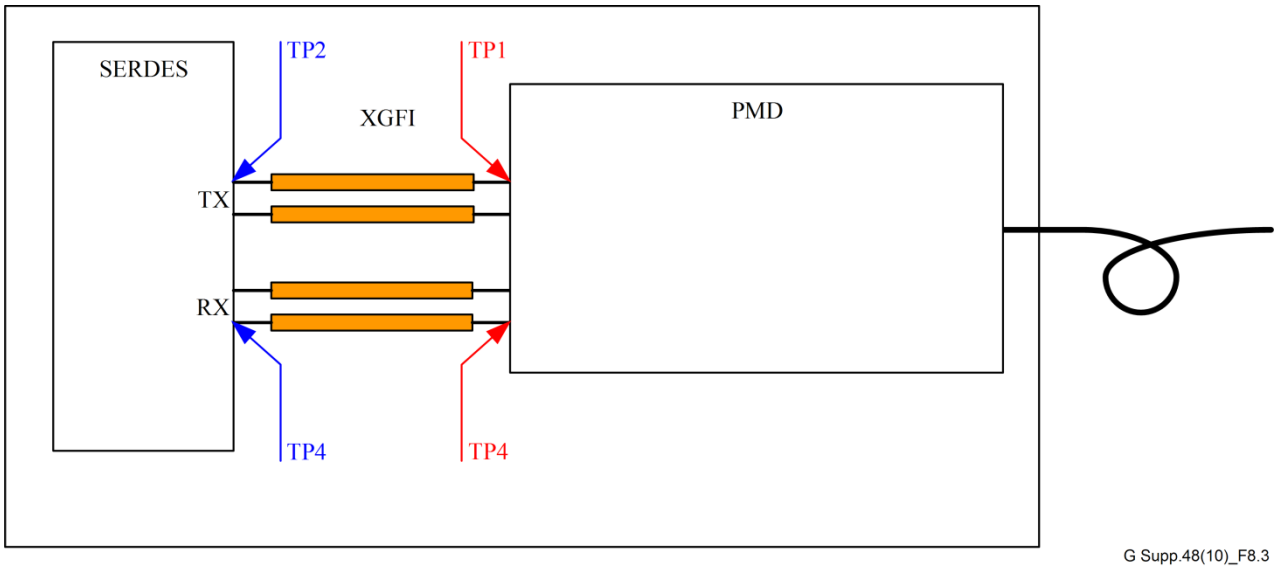


Figure 8-3 – Compliance points between the MAC/SERDES and PMD

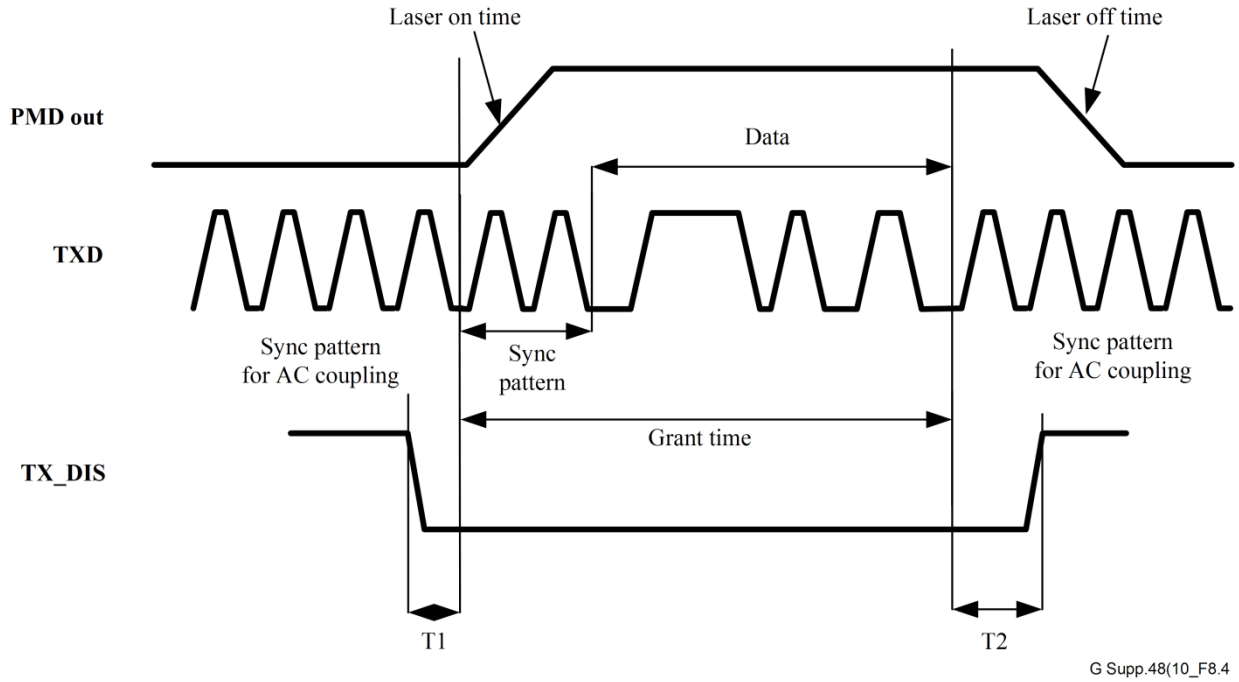
8.3 MAC/SERDES to PMD interface timing diagrams

This clause provides a few timing diagrams which are special for the interfaces provided in this Supplement, such as burst mode operation at the ONU and OLT, RSSI signalling and powersave. These diagrams should come in addition to the timing diagrams provided in the different PMDs specifications used (e.g., [SFP+] and [XFP]).

In this Supplement, there will be no setting for the timing values as it is expected to be achieved by the real PMD component specifications. Values can be stored in the PMD memory map and transferred to the MAC/SERDES through the 2-wire host management channel.

8.3.1 ONU

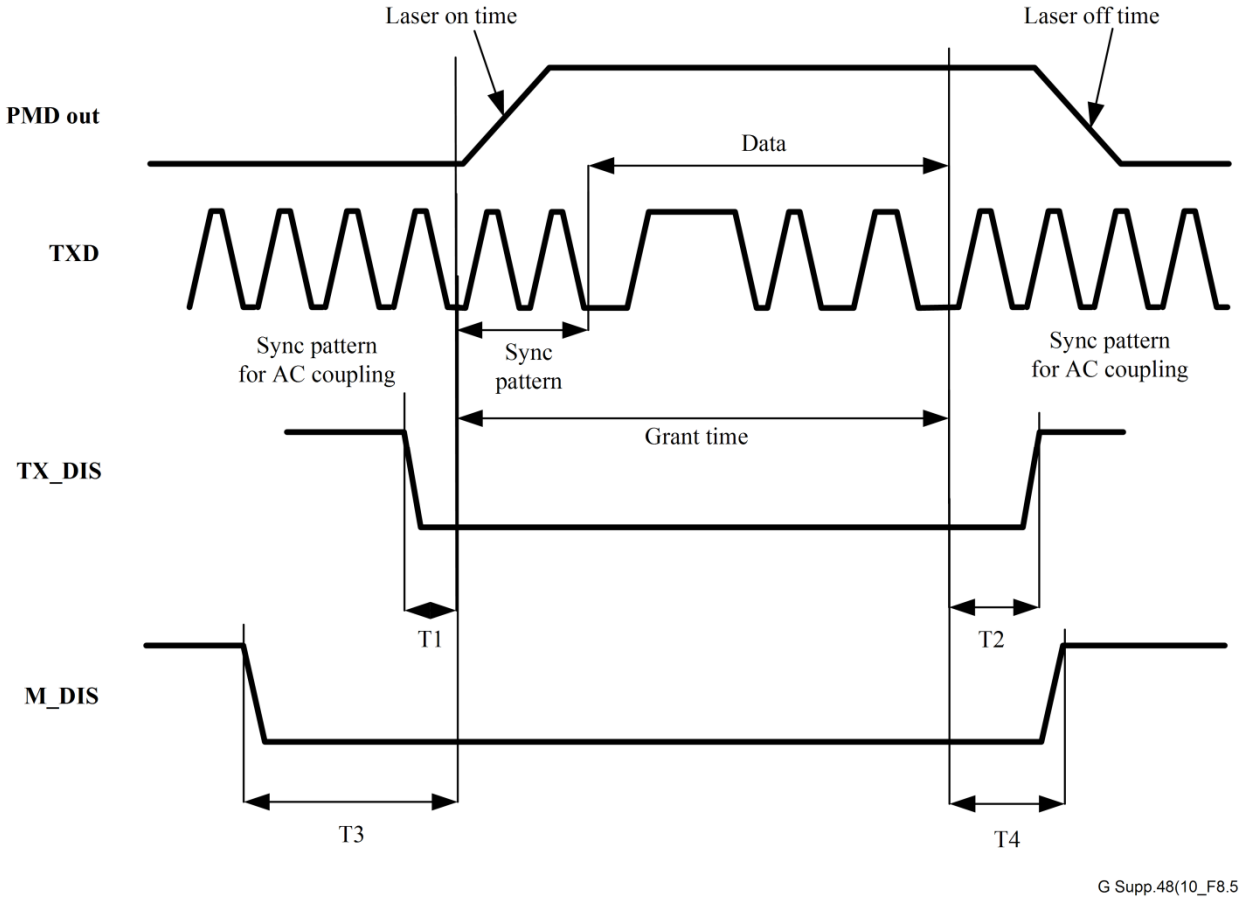
8.3.1.1 TX_DIS control



T1 – TX_DIS falling edge offset from start of grant time
T2 – TX_DIS rising edge offset from start of grant time

Figure 8-4 – TX_DIS timing for the ONU burst mode transmitter

8.3.1.2 M_DIS control

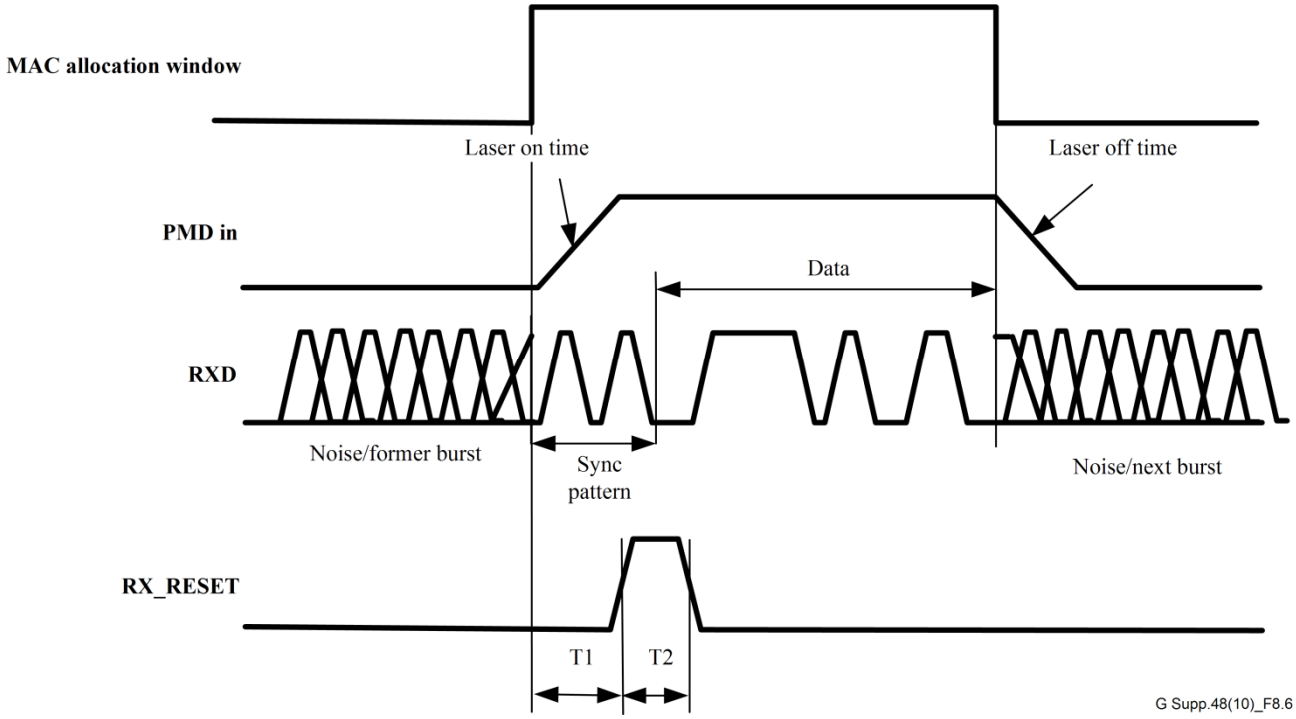


T1 – TX_DIS falling edge offset from start of grant time
T2 – TX_DIS rising edge offset from start of grant time
T3 – Time that the optics need before going out of powersave
T4 – Time until optics can go to powersave mode

Figure 8-5 – M_DIS timing for the ONU transmitter

8.3.2 OLT

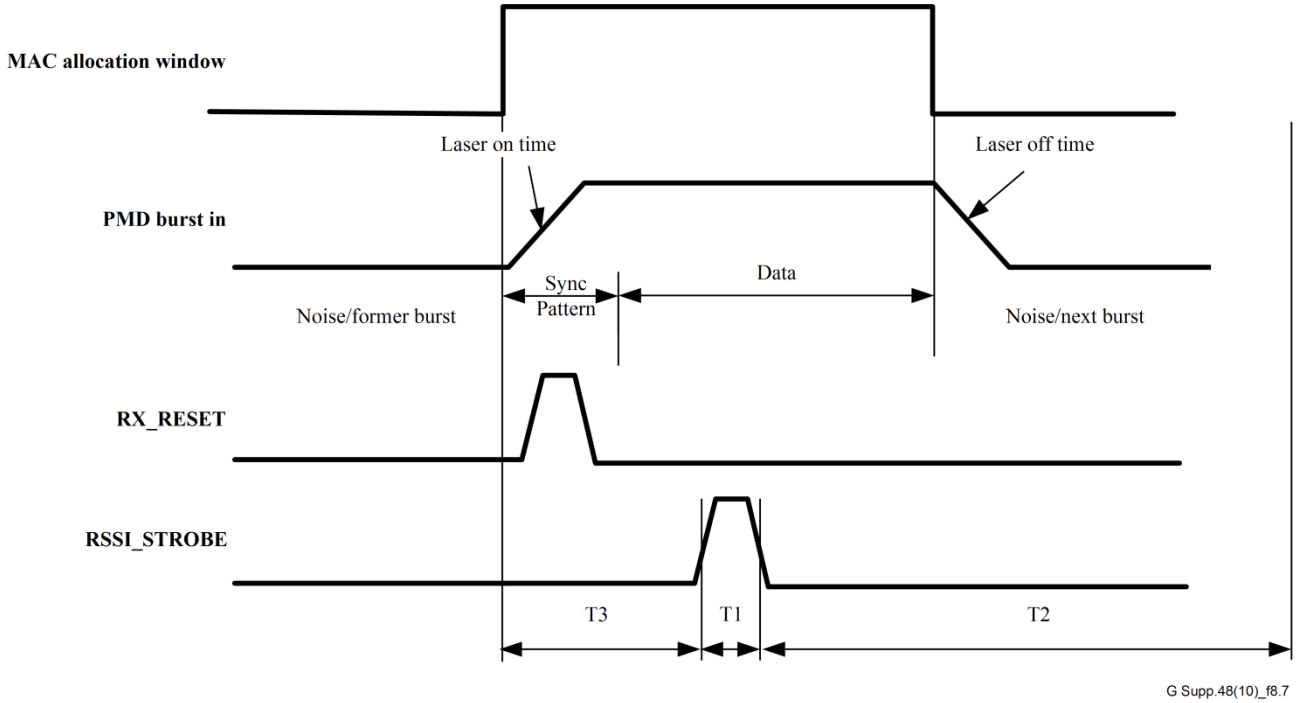
8.3.2.1 RESET signal timing



T1 – Time from start of the grant to the rising edge of RX_RESET
T2 – RX_RESET pulse width

Figure 8-6 – RX_RESET timing for the OLT burst mode receiver

8.3.2.2 Digital RSSI strobe timing



T1 – RSSI strobe pulse width
T2 – Time until RSSI data is valid in the register
T3 – Strobe delay time for stable monitoring. Referred to start of window but really starts after sync time

Figure 8-7 – Digital RSSI strobe timing for the OLT

8.3.3 Mask of transmitter eye diagram

The mask of transmitter eye diagram is defined in the PMD specifications, e.g., [SFP+] and [XFP].

8.3.4 Jitter tolerance

The jitter tolerance of the electrical interface is defined in Jitter Appendix IV of [ITU-T G.987.2], with informative values.

8.3.5 Jitter generation

The jitter generation of the electrical interface is defined in Jitter Appendix IV of [ITU-T G.987.2], with informative values.

8.4 MAC/SERDES to PMD interface electrical and AC specifications

The MAC/SERDES to PMD interface electrical and AC specifications are defined in PMD specifications, e.g., [SFP+] and [XFP].

Added specifications to DC coupled signal:

Parameter	Min	Max	Unit	Conditions
Common mode voltage	Implementation specific	Implementation specific	V	Needed for DC coupled interface

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