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INTERNATIONAL TELECOMMUNICATION UNION

ITU-T

I.432.1

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TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

SERIES I: INTEGRATED SERVICES DIGITAL NETWORK

ISDN user-network interfaces – Layer 1 Recommendations

B-ISDN user-network interface – Physical layer specification: General characteristics

ITU-T Recommendation I.432.1

Superseded by a more recent version

(Previously CCITT Recommendation)

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For further details, please refer to ITU-T List of Recommendations.

Superseded by a more recent version

ITU-T RECOMMENDATION I.432.1

B-ISDN USER-NETWORK INTERFACE – PHYSICAL LAYER SPECIFICTION: GENERAL CHARACTERISTICS

Summary

This Recommendation covers Physical Layer general characteristics for transporting ATM cells at various bit rates, at the T_B and S_B reference points of the B-ISDN User-Network Interface (UNI).

The I.432-Series Recommendations are published as several Recommendations for different bit rates and applications, some of which may be used to take advantage of existing building wiring and equipment. This Recommendation should be used with each of the other Recommendations.

In each Recommendation, functionality is presented in terms of Physical Media Dependent and Transmission Convergence sublayers, and both SDH-based and cell-based formats are included.

Source

ITU-T Recommendation I.432.1 was prepared by ITU-T Study Group 13 (1993-1996) and was approved under the WTSC Resolution No. 1 procedure on the 27th of August 1996.

FOREWORD

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The World Telecommunication Standardization Conference (WTSC), which meets every four years, establishes the topics for study by the ITU-T Study Groups which, in their turn, produce Recommendations on these topics.

The approval of Recommendations by the Members of the ITU-T is covered by the procedure laid down in WTSC Resolution No. 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

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As of the date of approval of this Recommendation, the ITU had/had not received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementors are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database.

CONTENTS

Recommendation I.432.1

B-ISDN USER-NETWORK INTERFACE – PHYSICAL LAYER SPECIFICATION: GENERAL CHARACTERISTICS

(Geneva, 1996)

1 Introduction

1.1 Scope

This Recommendation covers Physical Layer general characteristics for transporting ATM cells at various bit rates, at the T_B and S_B reference points of the B-ISDN User-Network Interface (UNI).

The I.432-Series Recommendations are published as several Recommendations for different bit rates and applications, some of which may be used to take advantage of existing building wiring and equipment. This Recommendation should be used with each of the other Recommendations.

In each Recommendation, functionality is presented in terms of physical media dependent and transmission convergence sublayers, and both SDH-based and cell-based formats are included.

1.2 Background

This Recommendation was previously contained in Recommendation I.432 (as published in March 1993) along with characteristics specific to 155 520 kbit/s and 622 080 kbit/s.

This Recommendation contains those characteristics that are general to all B-ISDN systems at the UNI. Other Recommendations of the I.432-Series Recommendations give relevant characteristics for the specific bit rates.

2 Reference configuration

2.1 Interface location with respect to reference configuration

An interface point I_a is adjacent to the B-TE or the B-NT2 on their network side; interface point I_b is adjacent to the B-NT2 and to the B-NT1 on their user side (see Figure 1).

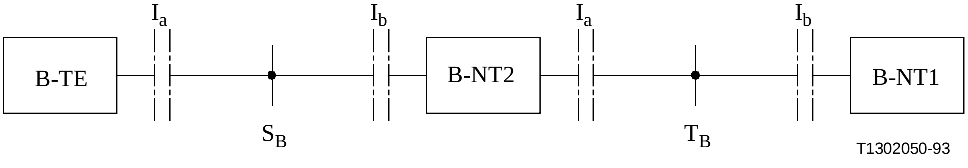
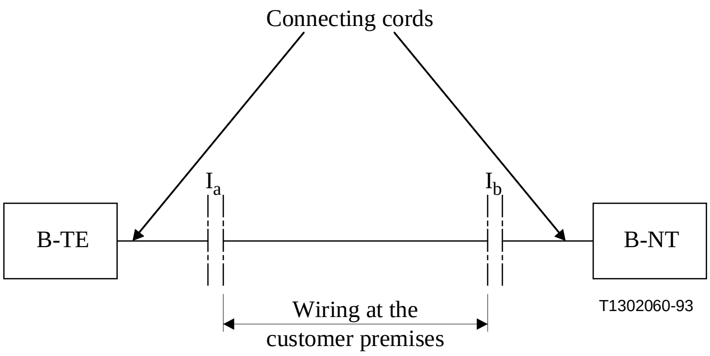


Figure 1/I.432.1 – Reference configuration at reference point S_B/T_B

2.2 Interface location with respect to the customer installation

The interface points are located between the socket and the plug of the connector attached to the B-TE, B-NT2 or B-NT1. The location of the interface point is shown in Figure 2.

In this Recommendation, the term "B-NT" is used to indicate network terminating layer 1 aspects of B-NT1 and B-NT2 functional groups, and the term "TE" is used to indicate terminal terminating layer 1 aspects of B-TE1, B-TA and B-NT2 functional groups, unless otherwise indicated.



NOTE – The length of the connecting cord can be zero.

Figure 2/I.432.1 – Wiring configuration

3 Characteristics of the Physical Media Dependent (PMD) sublayer

Refer to the appropriate bit rate specific Recommendation of the I.432-Series Recommendations.

4 Functions provided by the Transmission Convergence (TC) sublayer

4.1 Transfer capability

4.1.1 SDH-based

The transfer capability for ATM cells includes user information cells, signalling cells, OAM cells, unassigned cells and cells used for cell rate decoupling. It excludes physical layer overhead cells.

4.1.2 Cell-based

For cell-based systems, Physical Layer overhead cells include Physical Layer OAM cells and idle cells.

4.2 Transport-specific TC functions

Refer to the appropriate bit rate specific Recommendation of the I.432-Series Recommendations for both SDH-based and cell-based systems.

4.3 ATM-specific TC functions

4.3.1 ATM cell format

The ATM cell is defined in Recommendation I.361. ATM cells may be carried in one of two formats; as cells carried into an SDH-based frame structure, or as a continuous stream of cells in a cell-based format.

4.3.2 Header Error Control (HEC)

4.3.2.1 Header error control functions

The Header Error Control (HEC) covers the entire cell header. The code used for this function is capable of either:

– single bit error correction; or

– multiple bit error detection.

The detailed description of the HEC procedure is given in 4.3.2.2. Briefly, the transmitting side computes the HEC field value. The receiver has two modes of operation as shown in Figure 3. The default mode provides for single-bit error correction. Each cell header is examined and, if an error is detected, one of two actions takes place. The action taken depends on the state of the receiver. In "correction mode" only single bit errors can be corrected and the receiver switches to "detection mode". In "detection mode", all cells with detected header errors are discarded. When a header is examined and found not to be in error, the receiver switches to "correction mode". The term "no action" in Figure 3 means no correction is performed and no cell is discarded.

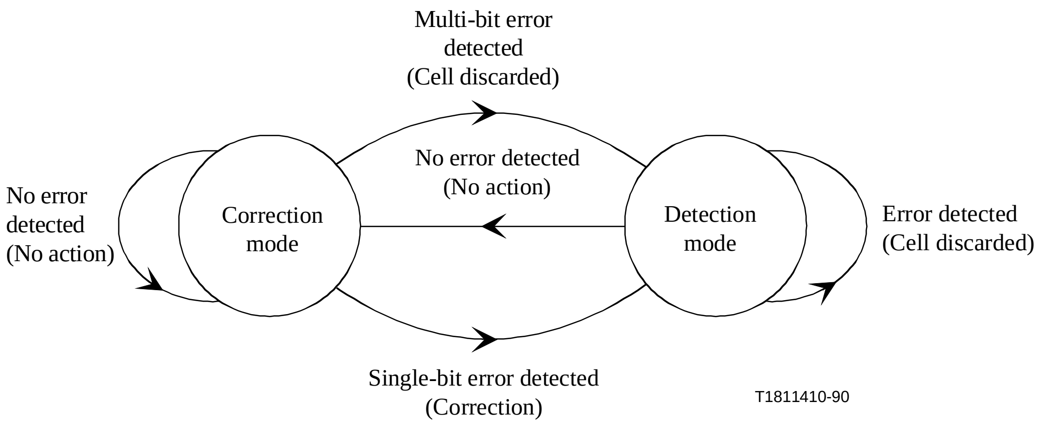
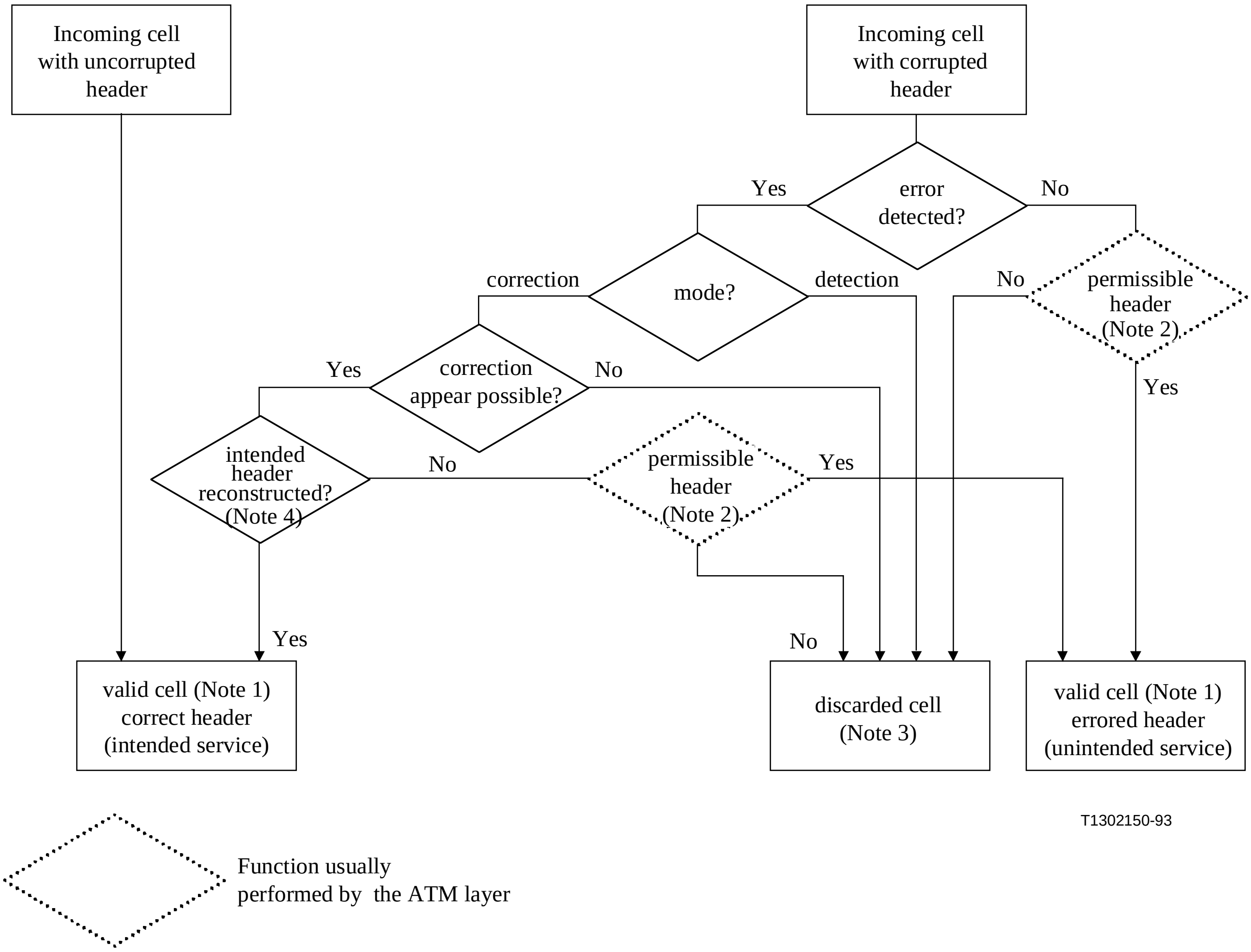


Figure 3/I.432.1 – HEC: Receiver mode of operation

The flow chart in Figure 4 shows the consequence of errors in the ATM cell header. The error protection function provided by HEC provides both recovery from single-bit header errors, and a low probability of the delivery of cells with errored headers under bursty error conditions. The error characteristics of fibre-based transmission systems appear to be a mix of single-bit errors and relatively large burst errors. For some transmission systems the error correction capability might not be invoked.



NOTE 1 – Definition of "valid cell": a cell where the header is declared by the header error control process to be free of errors (Recommendation I.113 [1]).

NOTE 2 – An example of an impermissible header is a header whose VPI/VCI is neither allocated to a connection nor pre-assigned to a particular function (idle cell, OAM cell, etc.) in many instances, the ATM layer will decide if the cell header is permissible.

NOTE 3 – A cell is discarded if its header is declared to be invalid; or if the header is declared to be valid and the resulting header is impermissible.

NOTE 4 – Definition of "intended" header: the header generated by the transmitting device, as it was before being corrupted by one or more errors.

Figure 4/I.432.1 – Consequence of errors in ATM cell header

Appendix I gives information on how random bit errors impact the probability of occurrence of discarded cells and valid cells with errored headers.

4.3.2.2 Header error control sequence generation

The transmitter calculates the HEC value across the entire ATM cell header and inserts the result in the appropriate header field.

The notation used to describe the header error control is based on the property of cyclic codes. (For example code vectors such as 1000000100001 can be represented by a polynomial $P(x) = x^{12} + x^5 + 1$). The elements of an n-element code word are thus the coefficients of a polynomial of order n–1.

In this application, these coefficients can have the value 0 or 1 and the polynomial operations are performed using modulo 2 operations. The polynomial representing the content of a header excluding the HEC field is generated using the first bit of a header as the coefficient of the highest order term.

The HEC field shall be an 8-bit sequence. It shall be the remainder of the division (modulo 2) by the generator polynomial $x^8 + x^2 + x + 1$ of the product x^8 multiplied by the content of the header excluding the HEC field.

At the transmitter, the initial content of the register of the device computing the remainder of the division is preset to all 0s and is then modified by division of the header excluding the HEC field by the generator polynomial (as described above); the resulting remainder is transmitted as the 8-bit HEC.

To significantly improve the cell delineation performance in the case of bit-slips, the following is recommended:

– the check bits calculated by the use of the check polynomial are added (modulo 2) to an 8-bit pattern before being inserted in the last octet of the header;

– the recommended pattern is "01010101" (the left bit is the most significant bit);

– the receiver must subtract (equal to add modulo 2) the same pattern from the 8 HEC bits before calculating the syndrome of the header.

This operation in no way affects the error detection/correction capabilities of the HEC.

As an example, if the first 4 octets of the header were all zeros the generated header before scrambling would be "00000000 00000000 00000000 00000000 01010101". The starting value for the polynomial check is 0s (binary).

4.3.3 Cell delineation

4.3.3.1 Cell delineation and scrambling objectives

Cell delineation is the process which allows identification of the cell boundaries.

The ATM cell header contains a HEC field which is used to achieve cell delineation.

The ATM signal is required to be self-supporting in the sense that it has to be transparently transported on every network interface without any constraints from the transmission systems used.

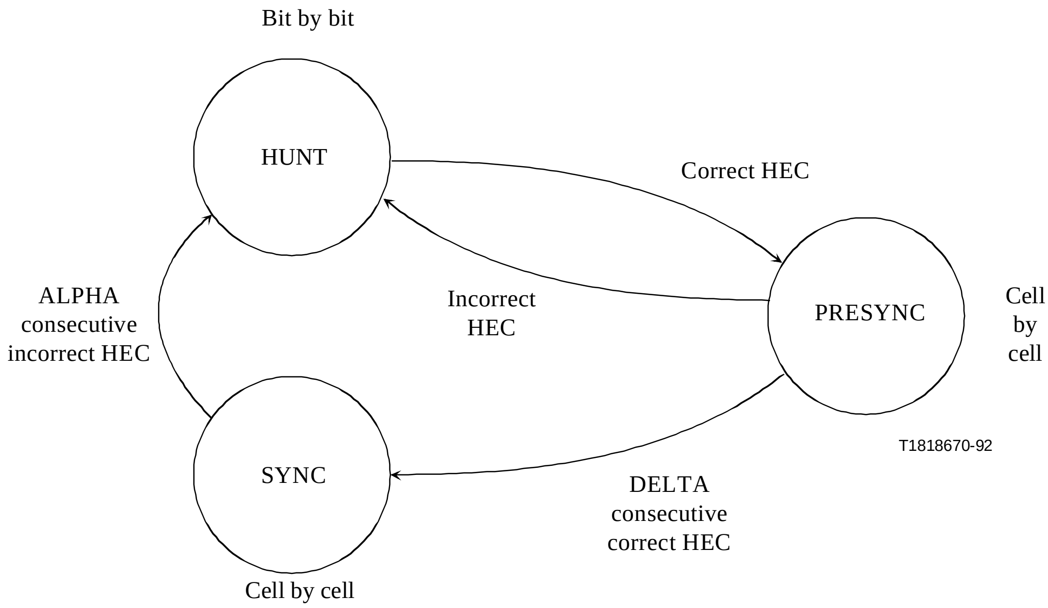
Scrambling will be used to improve the security and robustness of the HEC cell delineation mechanism as described in 4.3.4. In addition it helps randomizing the data in the information field for possible improvement of the transmission performance.

Any scrambler specification must not alter the ATM header structure (as described in Recommendation I.361), HEC (as described in 4.3.2), and cell delineation algorithm (as described in 4.3.3.2).

4.3.3.2 Cell delineation algorithm

Cell delineation is performed by using the correlation between the header bits to be protected (32 bits) and the relevant control bits (8 bits) introduced in the header by the HEC using a shortened cyclic code with generating polynomial $x^8 + x^2 + x + 1$.

Figure 5 shows the state diagram of the HEC cell delineation method.



NOTE – The "correct HEC" means the header has no bit error (syndrome is zero) and has not been corrected.

Figure 5/I.432.1 – Cell delineation state diagram

The details of the state diagram are described below:

1) In the HUNT state, the delineation process is performed by checking bit by bit for the correct HEC (i.e. syndrome equals zero) for the assumed header field. For the cell-based Physical Layer, prior to scrambler synchronization, only the last six bits of the HEC are to be used for cell delineation checking. For the SDH-based interface, all 8 bits are used for acquiring cell delineation. Once such an agreement is found, it is assumed that one header has been found, and the process enters the PRESYNC state. When octet boundaries are available within the receiving Physical Layer prior to cell delineation as with the SDH-based interface, the cell delineation process may be performed octet by octet.

2) In the PRESYNC state, the delineation process is performed by checking cell by cell for the correct HEC. The process repeats until the correct HEC has been confirmed DELTA times consecutively, at which point the process moves to the SYNC state. If an incorrect HEC is found, the process returns to the HUNT state. The total number of consecutive correct HEC required to move from the HUNT state to the SYNC state is therefore DELTA + 1.

3) In the SYNC state the cell delineation will be assumed to be lost if an incorrect HEC is obtained ALPHA times consecutively.

4) Cells with correct HECs (or cell headers with single bit errors which are corrected) that are processed while in the SYNC state shall be passed to the ATM layer. Cells with correct HECs that are checked while in the PRESYNC state may optionally be passed to the ATM layer, but only when they are part of the DELTA consecutive correct HECs necessary for transition to the SYNC state. The cell associated with the first correct HEC (in the HUNT state) may also optionally be passed to the ATM layer in conjunction with the DELTA cells just mentioned. In any case, idle cells and Physical Layer OAM cells are not passed to the ATM layer.

The parameters ALPHA and DELTA are to be chosen to make the cell delineation process as robust and secure as possible and while satisfying the performance specified in 4.3.3.3.

Robustness against false misalignments due to bit errors depends on ALPHA.

Robustness against false delineation in the resynchronisation process depends on the value of DELTA.

For the SDH-based Physical Layer, ALPHA = 7 and DELTA = 6.

For the cell-based Physical Layer, ALPHA = 7 and DELTA = 8.

For other systems, values for ALPHA and DELTA are for further study.

4.3.3.3 Cell delineation performance

This subclause is further study. Figures I.1 and I.2 give provisional information on the performance of the cell delineation algorithm described in 4.3.3.2 in the presence of random bit errors, for various values of ALPHA and DELTA.

4.3.4 Scrambler operation

4.3.4.1 ATM cell level scrambler for the SDH-based systems

The following polynomial has been identified for the SDH-based Physical Layer self-synchronising scrambler $x^{43} + 1$.

This self-synchronising scrambler polynomial has been selected to minimize the error multiplication (two) introduced by the self-synchronising scrambling process.

The operation of this scrambler in relation to the HEC cell delineation state diagram is as follows:

– the scrambler randomizes the bits of the information field only;
– during the five octets header the scrambler operation is suspended and the scrambler state retained;
– in the HUNT state the descrambler is disabled;
– in the PRESYNC and SYNC states the descrambler is enabled for a number of bits equal to the length of the information field, and again disabled for the following assumed header;
– at start up (e.g. at the power up or on re-synchronisation following loss of signal), the first 43 bits of the payload of the first cell transmitted will be used to synchronise the scrambler and descrambler, and as a result the first cell will be corrupted.

4.3.4.2 Scrambler for the cell-based systems

The Distributed Sample Scrambler is recommended for the cell-based UNI.

4.3.4.2.1 Distributed Sample Scrambler (31st Order)

The Distributed Sample Scrambler is an example of a class of scrambler in which randomisation of the transmitted data stream is achieved by modulo addition of a pseudo-random sequence. De-scrambling at the receiver is achieved by modulo addition of an identical locally generated pseudo-random sequence having phase synchronization with the first in respect of the transmitted cells. The scrambler does not affect the performance of the 8-bit HEC mechanism during steady state operation.

Phase synchronisation of a receiver PRBS with polynomial generator order r is achieved by sending r linearly independent source PRBS samples through the transmission channel as conveyed data samples. When received without error, these r samples are sufficient to synchronise the phase of the PRBS generator at the receiver to that of the transmitter PRBS generator.

A simple timing skew between the source PRBS samples and the conveyed PRBS samples serves as a means of decoupling the sample times of the source PRBS samples from the conveyed PRBS samples. This enables linear independence of PRBS samples to be simply achieved by taking samples at equal intervals of half an ATM cell from the source PRBS generator.

4.3.4.2.2 Transmitter operation

The transmitter pseudo random binary sequence is added (modulo 2) to the complete cell bit by bit excepting the HEC field. The pseudo-random sequence polynomial is:

$$x^{31} + x^{28} + 1$$

The CRC octet for each cell is then modified by modulo 2 addition of the CRC calculated on the 32 bits of the scrambler sequence coincident with the first 32 header bits. This is equivalent to calculation of the CRC on the first 32 bits of the scrambled header. The first two bits of the HEC field are then modified as follows by two bits from the PRBS generator. The two bits from the PRBS generator will be referred to as the PRBS source bits and the two bits of the CRC onto which they are mapped will be referred to as the PRBS transport bits.

To the first HEC bit (HEC_8) is added (modulo 2) the value of PRBS generator that was added (modulo 2) 211 bits earlier to the previous cell payload. To the second bit of the HEC field is added (modulo 2) the current value of the PRBS generator. These samples are exactly half a cell apart and the first (U_{t-211}) is delayed by 211 bits before conveyance (requiring one D-type latch for storage) (211 bits is 1 bit less than half a cell). See Tables 1 and 2.

Table 1/I.432.1 – PRBS phase (as added to payload and all header except HEC)

U_{t-1}	U_t	U_{t+1}	U_{t+2}	U_{t+3}	U_{t+4}	U_{t+5}	U_{t+6}	U_{t+7}	U_{t+8}	U_{t+9}

Table 2/I.432.1 – Resultant transmitted data element

CLP + U_{t-1}	HEC_8 + U_{t-211}	HEC_7 + U_{t-1}	HEC_6	HEC_5	HEC_4	HEC_3	HEC_2	HEC_1	1st payload bit + U_{t+8}	2nd payload bit + U_{t+9}

4.3.4.2.3 Receiver Operation

Three basic states of receiver operation are defined:

(1) Acquisition of scrambler synchronisation (following cell delineation).

(2) Verification of scrambler synchronisation.

(3) Steady state operation.

Receiver state (1): Acquisition of scrambler synchronisation (following cell delineation)

The principle of operation is as follows:

Cell delineation

The cell delineation mechanism is independent from the scrambler synchronisation acquisition mechanism. Cell delineation is determined using the last six bits of the HEC field (only). The first two bits have been modified by the modulo addition of the conveyed data samples and cannot therefore be used for delineation or CRC evaluation until the scrambler is synchronised.

Acquisition of scrambler synchronisation

The conveyed bits are extracted by modulo addition of the predicted values for HEC_8 and HEC_7 from the received values. Scrambler synchronisation may for example be achieved by applying the conveyed samples at half cell intervals to a recursive descrambler (Figure II.1). In order to ensure the samples are added into the recursive descrambler at the same interval they were extracted from the source PRBS, the second sample U_{t+1} (derived from HEC_7) is stored for 211 bits before it is used.

Additionally, because both samples are applied to the recursive descrambler 211 bits behind their point of modulo addition to the transmitted data sequence, the recursive descrambler feedforward taps are chosen to generate a sequence that is advanced by 211 samples. Similarly, the verification comparison made in the recursive descrambler between the conveyed bits and their prediction is delay equalised using one bit stores as illustrated in Figure II.1.

Time to achieve scrambler synchronisation

Two bits of information are conveyed per cell which are linearly independent. The number of consecutive error free conveyed samples needed to synchronise the descrambler will be equal to the length of the scrambler, therefore 16 cells provide the 31 samples necessary to synchronise the scrambler.

The scrambler synchronisation process is not disabled during cell delineation; however, the descrambler will not begin to converge until the cell delineation mechanism has located the true position of the HEC sequence in the header and is no longer in its hunt state. Therefore the start of scrambler synchronisation acquisition convergence will be coincident with the final transition from the hunt state to the presync state of the cell delineation mechanism.

Receiver state (2): Verification of scrambler synchronisation

The verification state differs from the acquisition state in that the recursive descrambler is no longer modified with synchronising samples. Verification is needed because undetectable errors in the conveyed bits may have occurred during the acquisition phase. Verification tests the predicted PRBS in the receiver against the remote reference sequence given by the conveyed samples. To verify scrambler acquisition phase overall such that the probability of false synchronisation is less than 10^{-6} requires 16 verifications where the transmission error ratio is better than 10^{-3}.

Receiver State (3): Steady state operation (synchronised scrambler)

In this state the HEC_8 and HEC_7 bits can both be returned to normal use following their descrambling. Properties of error detection and correction are not affected by this process.

Both cell delineation and scrambler synchronisation are in this state reliably monitored by the existing cell delineation state machine.

HEC regeneration and header scrambling

The HEC bits in the transmitted cell were modified prior to transmission to correspond to the HEC for the scrambled header. To reverse this process where required and regenerate an HEC that corresponds to the unscrambled header, the HEC bits may be modified by modulo 2 addition of the CRC calculated on the 32 bits of the descrambler sequence coincident with the first 32 header bits.

Automatic scrambling detection

If scrambling is not used, then the conveyed PRBS samples derived from the corresponding HEC_7 and HEC_8 bits will have value zero. Thus these bits used to derive the phase of the descrambler will seed the descrambler with zeroes inhibiting the PRBS of the descrambler automatically. Therefore, the absence of scrambling by the transmitter can be detected automatically by the receiver and correctly handled.

4.3.4.2.4 State transition diagram and mechanism

The three states of the scrambler are Acquisition, Verification and Steady State.

The transition between these states may be determined by reference to the value of a single confidence counter (C) as follows:

Initial state = Acquisition, Confidence counter initial value = 0

State 1: Acquisition: Confidence counter range 0 to X–1

For every cell received correctly with no errors detected in HEC bits 1 to 6 the confidence counter is incremented by one and the two conveyed bits used to drive the recursive descrambler into synchronisation.

Any error detected in the cell header results in a return to the initial state (the confidence counter being reset to zero).

Transition to the verification state occurs when the counter reaches X (Proposed value of X = 16).

State 2: Verification: Confidence counter range X to Y–1

For every cell received without detected errors, the two conveyed bits are compared to their predicted values. For each cell with two correct predictions received, the confidence counter is incremented. If one or two incorrect predictions are made then the counter is decremented. If the counter falls below V (proposed value 8) the system returns to the acquisition initial state 1 and the confidence counter is reset.

Transition to the steady state occurs when the counter reaches Y (Proposed value of Y = 24).

State 3: Steady state: Confidence counter range Y to Z

The rules for incrementing and decrementing the confidence counter are as for state 2. The acquisition state is returned to automatically should the counter drop below W(= 16). The confidence counter has an upper limit of Z (proposed value 24). See Figure 6.

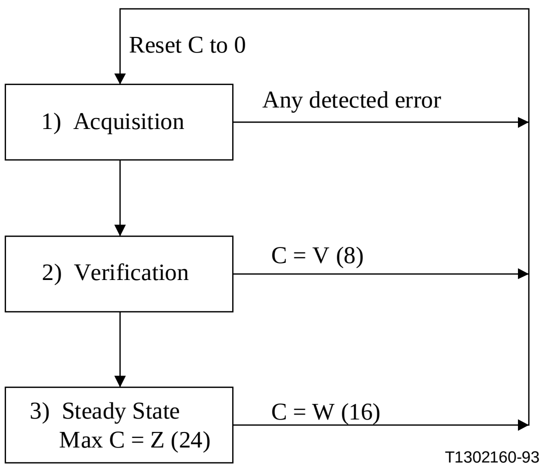


Figure 6/I.432.1 – State transition diagram

4.3.4.3 Scrambler for other systems

For other systems, refer to the relevant clause in the appropriate Recommendation of the I.432-Series Recommendations.

4.3.5 Idle cells

Idle cells cause no action at a receiving node except for cell delineation including HEC verification. They are inserted and discarded for cell rate decoupling. Idle cells are identified by the standardised pattern for the cell header shown in Table 3.

Table 3/I.432.1 – Header pattern for Idle Cell identification

	Octet 1	Octet 2	Octet 3	Octet 4	Octet 5
Header pattern	00000000	00000000	00000000	00000001	HEC = Valid code 01010010
NOTE 1 – The content of the information field is "01101010" repeated 48 times. NOTE 2 – There is no significance to any of these individual header fields from the point of view of the ATM layer, as idle cells are not passed to the ATM layer.					

4.4 OAM Implementation

Refer to the appropriate bit rate specific Recommendation of the I.432-Series Recommendations for both SDH-based and cell-based systems.

5 Operational functions

Refer to the appropriate bit rate specific Recommendation of the I.432-Series Recommendations for both SDH-based and cell-based systems.

6 Power feeding

Refer to the appropriate bit rate specific Recommendation of the I.432-Series Recommendations for both SDH-based and cell-based systems.

7 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; all users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published.

[1] ITU-T Recommendation I.113 (1993), *Vocabulary of terms for broadband aspects of ISDN*.

[2] ITU-T Recommendation I.361 (1995), *B-ISDN ATM layer specification*.

8 Abbreviations

This Recommendation uses the following abbreviations.

ATM	Asynchronous Transfer Mode
B-ISDN	Broadband Integrated Services Digital Network
B-NT	Broadband Network Termination
B-NT1	Broadband Network Termination 1
B-NT2	Broadband Network Termination 2
B-TE	Broadband Terminal Equipment
CRC	Cyclic Redundancy Check
HEC	Header Error Control
IEC	International Electrotechnical Commission
OAM	Operations Administration and Maintenance
PMD	Physical Medium Dependent
PRBS	Pseudo-Random Binary Sequence
SDH	Synchronous Digital Hierarchy
TC	Transmission Convergence
UNI	User-Network Interface
VCI	Virtual Channel Identifier
VPI	Virtual Path Identifier

9 Definitions

None.

10 Keywords

ATM, B-ISDN, UNI, User Network Interface.

APPENDIX I

Impact of random bit errors on cell delineation performance

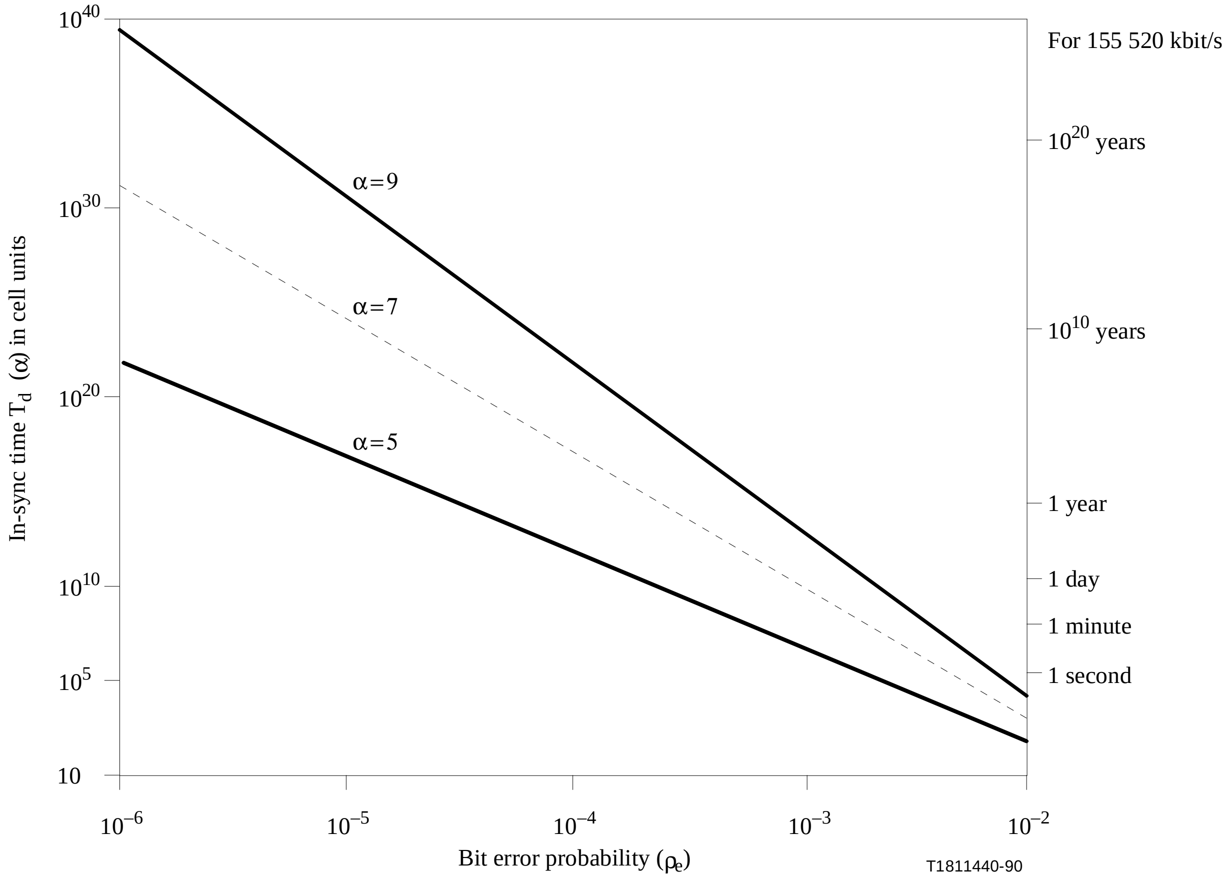


Figure I.1/I.432.1 – In-sync time vs. bit error probability [$T_d(\alpha)$ vs. ρ_e]

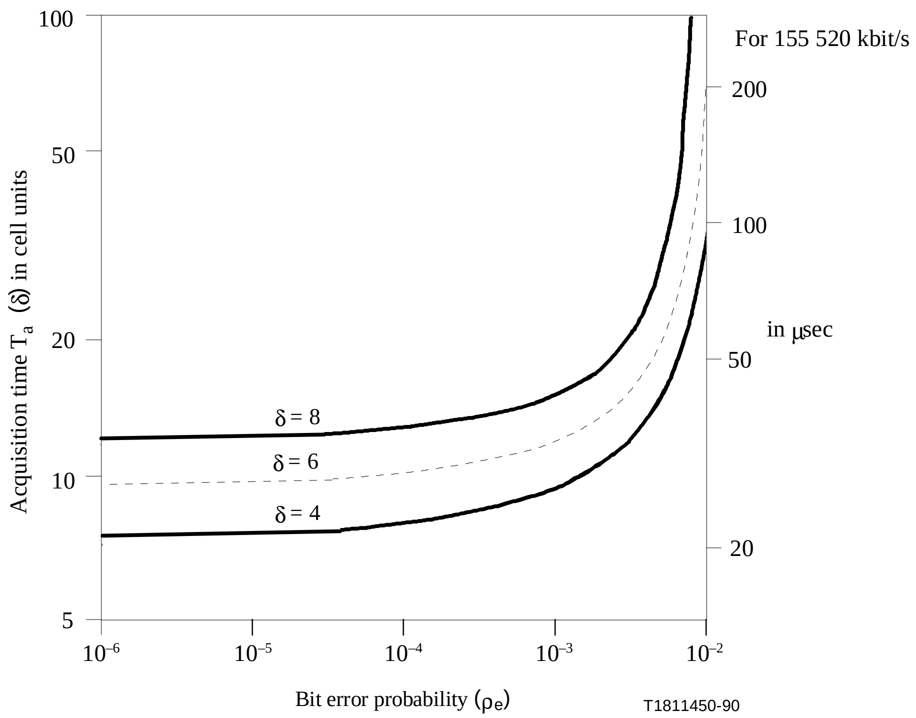


Figure I.2/I.432.1 – Acquisition time vs. bit error probability [$T_a(\delta)$ vs. ρ_e]

APPENDIX II

Distributed sample scrambler descrambler implementation example

Acquisition of scrambler synchronisation

The conveyed bits are extracted by modulo addition of the predicted values for HEC_8 and HEC_7 from the received values. Scrambler synchronisation may for example be achieved by applying the conveyed samples at half cell intervals to a recursive descrambler (Figure II.1). In order to ensure the samples are added into the recursive descrambler at the same interval they were extracted from the source PRBS, the second sample $U_{(t+1)}$ (derived from HEC_7) is stored for 211 bits before it is used.

Additionally, because both samples are applied to the recursive descrambler 211 bits behind their point of modulo addition to the transmitted data sequence, the recursive descrambler feedforward taps are chosen to generate a sequence that is advanced by 211 samples. Similarly, the verification comparison made in the recursive descrambler between the conveyed bits and their prediction is delay equalised using one bit stores as illustrated in Figure II.1.

Example: Implementation: The recursive descrambler

Figure II.1 illustrates the recursive descrambler implementation. Notation of sample values indicates the important sample values in each cell, time being referenced to the conveyed PRBS sample being received with HEC_8.

At time t:

– the receiver PRBS generator sample V_t is at the input to the lower D-type D_2;

– the source PRBS sample $S_t = U_{t-211}$ conveyed via HEC_8 is at input D_1;

– the sample previously stored at the output of the lower D-type is $D_2 = V_{t-211}$

$$EXOR_2 = S_t + D_2 = U_{t-211} + V_{t-211}.$$

The multiplexer selects this output and it is applied to the feedforward taps of the recursive descrambler.

At time t+1:

– the receiver sample V_{t+1} is at the input to D_2;

– the sample $S_{t+1} = U_{t+1}$ is at the input to D_1.

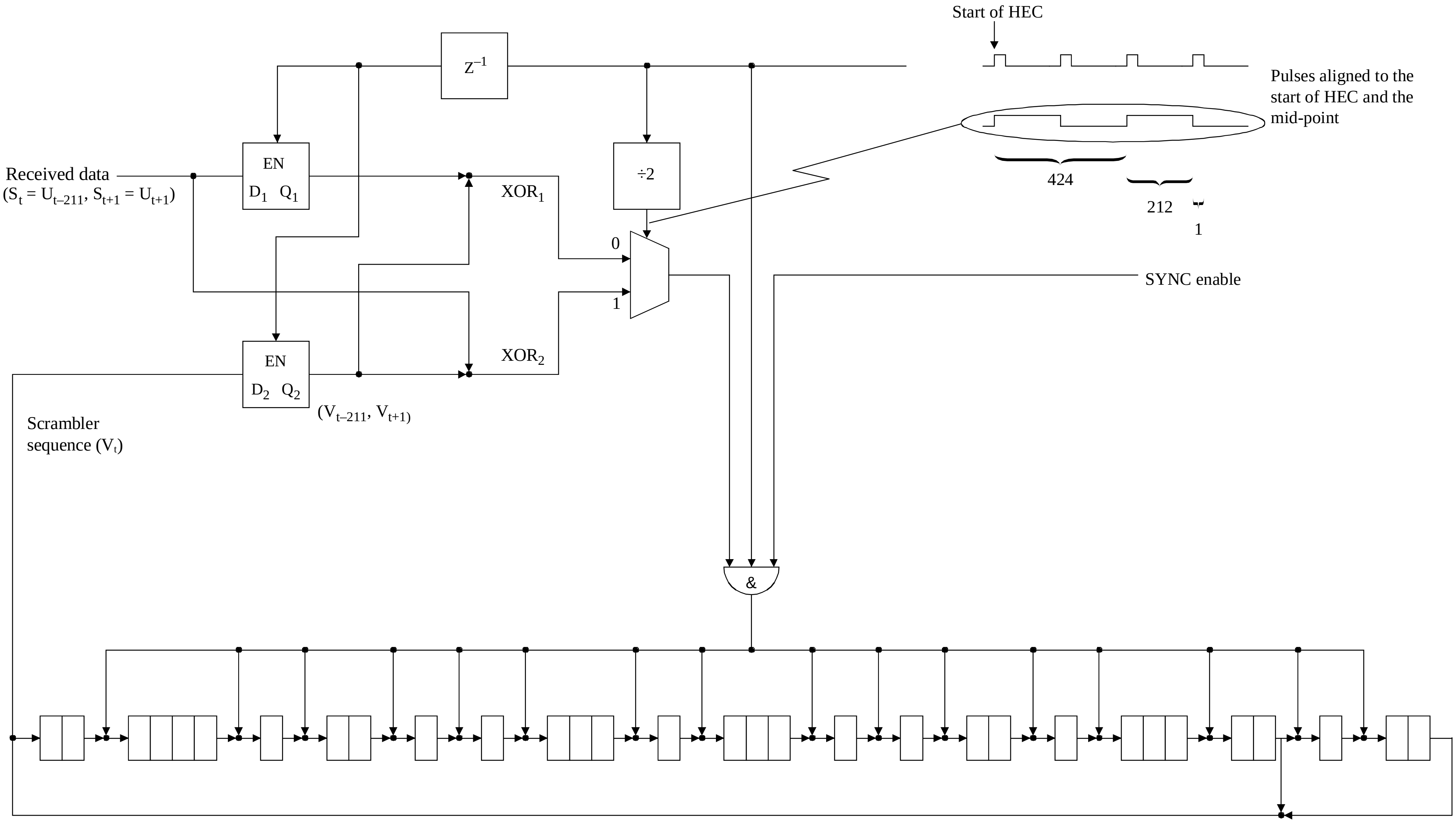
These values are latched on the following clock edge such that:

At time t+2 through until t+212:

– $EXOR_1 = V_{t+1} + U_{t+1}$ which is applied via MUX at time t+212 to the feedforward taps.

At time t+213 = L + t–211 (L being the duration of a cell):

– $D_2 = V_{t+213} = V_{t-211+L}$ (held until the next cell cycle).



All D-types clocked at the data bit rate

$X^{31} + X^{28} + 1$ Polynomial recursive descrambler

Figure II.1/I.432.1 – Example of receiver descrambler

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