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SERIES I: INTEGRATED SERVICES DIGITAL NETWORK

ISDN user-network interfaces – Layer 1 Recommendations

B-ISDN user-network interface – Physical layer specification: General characteristics

ITU-T Recommendation I.432.1

(Previously CCITT Recommendation)

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ITU-T RECOMMENDATION I.432.1

B-ISDN USER-NETWORK INTERFACE – PHYSICAL LAYER SPECIFICATION: GENERAL CHARACTERISTICS

Summary

This Recommendation covers Physical Layer general characteristics for transporting ATM cells at various bit rates, at the T_B and S_B reference points of the B-ISDN User-Network Interface (UNI).

The I.432 series Recommendations are published as several Recommendations for different bit rates and applications, some of which may be used to take advantage of existing building wiring and equipment. This Recommendation should be used with each of the other Recommendations.

In each Recommendation, functionality is presented in terms of Physical Media Dependent and Transmission Convergence sublayers, and both SDH-based and cell-based formats are included.

Source

ITU-T Recommendation I.432.1 was prepared by ITU-T Study Group 13 (1997-2000) and was approved under the WTSC Resolution No. 1 procedure on the 15th of February 1999.

Keywords

ATM, B-ISDN, UNI, User Network Interface.

FOREWORD

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As of the date of approval of this Recommendation, the ITU had received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementors are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database.

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Recommendation I.432.1

B-ISDN USER-NETWORK INTERFACE – PHYSICAL LAYER SPECIFICATION: GENERAL CHARACTERISTICS

(Geneva, 1999)

1 Scope

This Recommendation covers Physical Layer general characteristics for transporting ATM cells at various bit rates, at the T_B and S_B reference points of the B-ISDN User-Network Interface (UNI).

The I.432 series Recommendations are published as several Recommendations for different bit rates and applications, some of which may be used to take advantage of existing building wiring and equipment. This Recommendation should be used with each of the other Recommendations.

In each Recommendation, functionality is presented in terms of physical media dependent and transmission convergence sublayers, and both SDH-based and cell-based formats are included.

2 Background

This Recommendation was previously contained in Recommendation I.432 (as published in March 1993) along with characteristics specific to 155 520 kbit/s and 622 080 kbit/s.

This Recommendation contains those characteristics that are general to all B-ISDN systems at the UNI. Other Recommendations of the I.432 series give relevant characteristics for the specific bit rates.

3 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; all users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published.

[1] ITU-T Recommendation I.113 (1997), *Vocabulary of terms for broadband aspects of ISDN*.

[2] ITU-T Recommendation I.361 (1995), *B-ISDN ATM layer specification*.

[3] ITU-T Recommendation I.432.2 (1996), *B-ISDN User-network interface – Physical layer specification: 155 520 kbit/s and 622 080 kbit/s operation.*

4 Definitions and abbreviations

4.1 Definitions

None.

4.2 Abbreviations

This Recommendation uses the following abbreviations.

ATM	Asynchronous Transfer Mode
B-ISDN	Broadband Integrated Services Digital Network
B-NT	Broadband Network Termination
B-NT1	Broadband Network Termination 1
B-NT2	Broadband Network Termination 2
B-TA	Broadband Terminal Adaptor
B-TE	Broadband Terminal Equipment
CLP	Cell Loss Priority
CRC	Cyclic Redundancy Check
HEC	Header Error Control
IEC	International Electrotechnical Commission
OAM	Operations Administration and Maintenance
PMD	Physical Medium Dependent
PRBS	Pseudo-Random Binary Sequence
SDH	Synchronous Digital Hierarchy
TC	Transmission Convergence
TE	Terminal Equipment
UNI	User-Network Interface
VCI	Virtual Channel Identifier
VPI	Virtual Path Identifier

5 Reference configuration

5.1 Interface location with respect to reference configuration

An interface point I_a is adjacent to the B-TE or the B-NT2 on their network side; interface point I_b is adjacent to the B-NT2 and to the B-NT1 on their user side (see Figure 1).

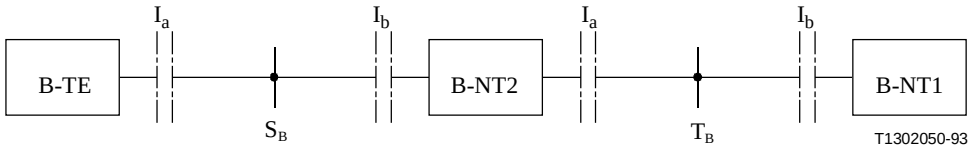
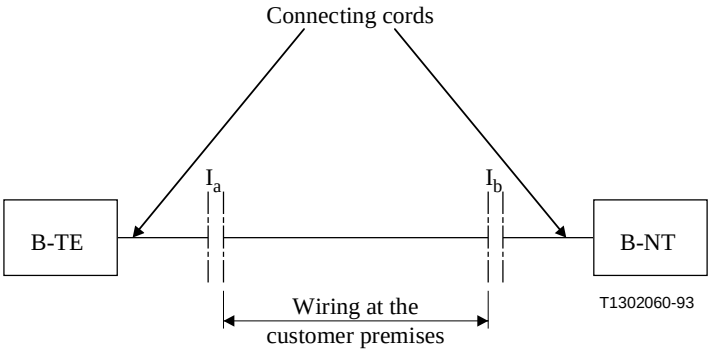


Figure 1/I.432.1 – Reference configuration at reference point S_B/T_B

5.2 Interface location with respect to the customer installation

The interface points are located between the socket and the plug of the connector attached to the B-TE, B-NT2 or B-NT1. The location of the interface point is shown in Figure 2.

In this Recommendation, the term "B-NT" is used to indicate network terminating layer 1 aspects of B-NT1 and B-NT2 functional groups, and the term "TE" is used to indicate terminal terminating layer 1 aspects of B-TE1, B-TA and B-NT2 functional groups, unless otherwise indicated.



NOTE – The length of the connecting cord can be zero.

Figure 2/I.432.1 – Wiring configuration

6 Characteristics of the Physical Media Dependent (PMD) sublayer

Refer to the appropriate bit rate specific Recommendation of the I.432 series.

7 Functions provided by the Transmission Convergence (TC) sublayer

7.1 Transfer capability

7.1.1 SDH-based

The transfer capability for ATM cells includes user information cells, signalling cells, OAM cells, unassigned cells and cells used for cell rate decoupling. It excludes physical layer overhead cells.

7.1.2 Cell-based

For cell-based systems, Physical Layer overhead cells include Physical Layer OAM cells and idle cells.

7.2 Transport-specific TC functions

Refer to the appropriate bit rate specific Recommendation of the I.432 series for both SDH-based and cell-based systems.

7.3 ATM-specific TC functions

7.3.1 ATM cell format

The ATM cell is defined in Recommendation I.361 [2]. ATM cells may be carried in one of two formats; as cells carried into an SDH-based frame structure, or as a continuous stream of cells in a cell-based format.

7.3.2 Header Error Control (HEC)

7.3.2.1 Header Error Control functions

The Header Error Control (HEC) covers the entire cell header. The code used for this function is capable of either:

– single bit error correction; or

– multiple bit error detection.

The detailed description of the HEC procedure is given in 7.3.2.2. Briefly, the transmitting side computes the HEC field value. The receiver has two modes of operation as shown in Figure 3. The default mode provides for single-bit error correction but should only be applied while the cell delineation mechanism is in the SYNC state, and for a cell-based Physical Layer while the descrambler is in the steady state. Each cell header is examined and, if an error is detected, one of two actions takes place. The action taken depends on the state of the receiver. In "correction mode" only single bit errors can be corrected and the receiver switches to "detection mode". In "detection mode", all cells with detected header errors are discarded. When a header is examined and found not to be in error, the receiver switches to "correction mode". The term "no action" in Figure 3 means no correction is performed and no cell is discarded.

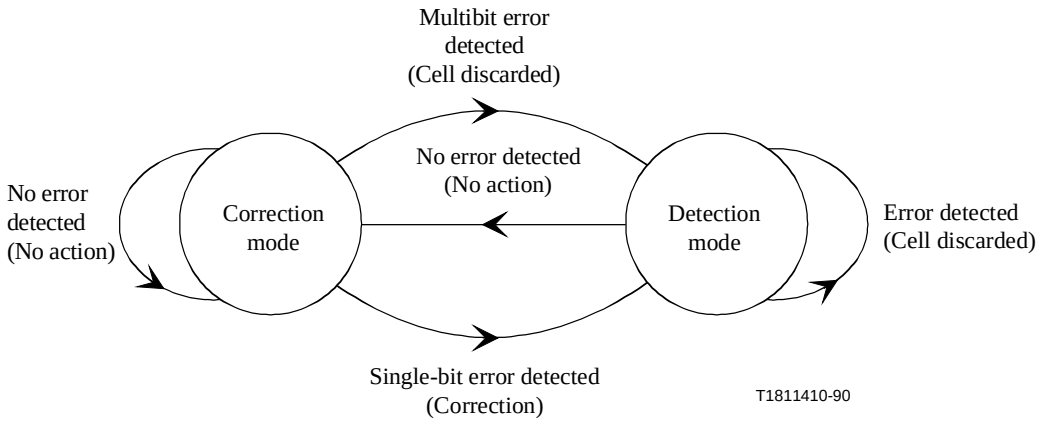
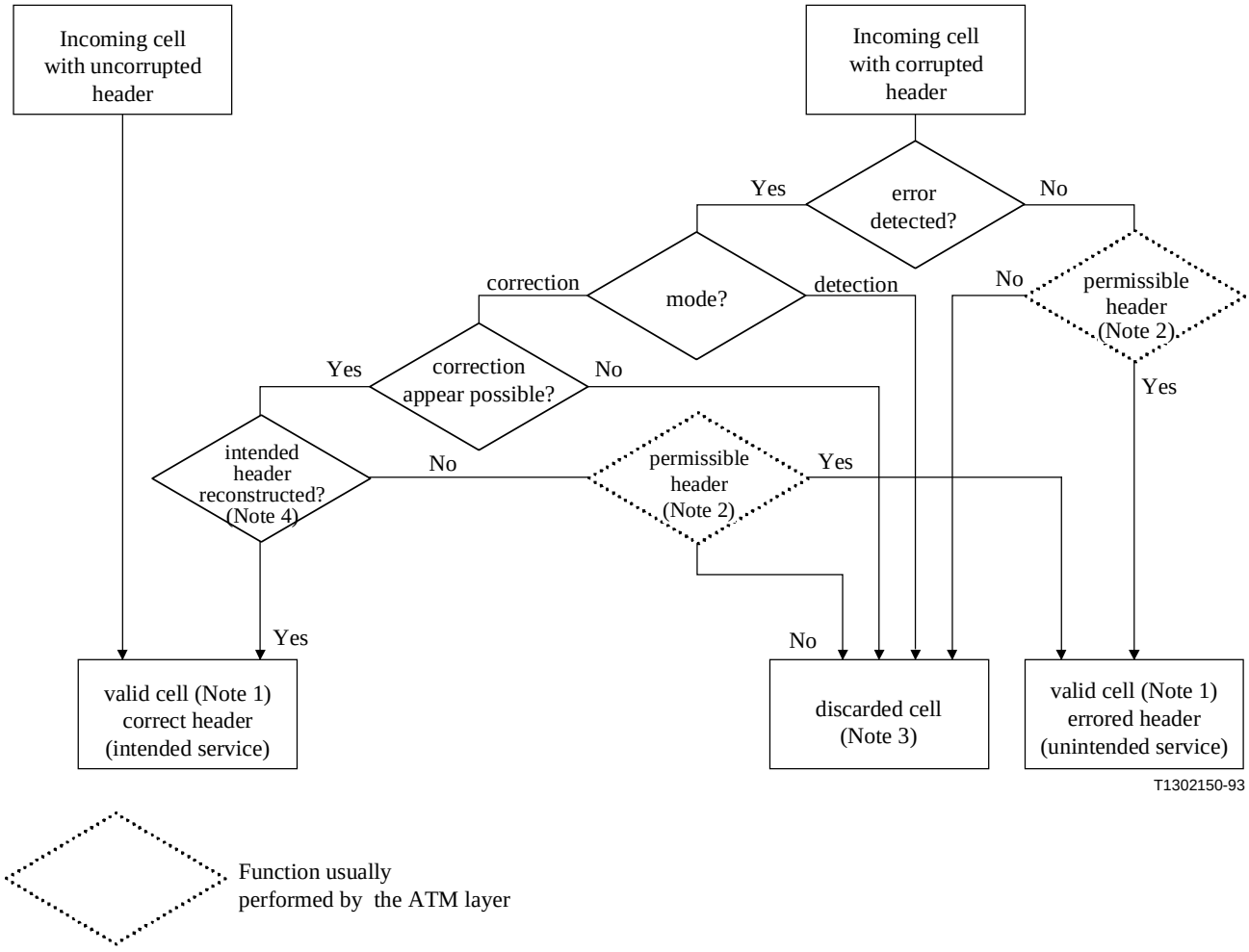


Figure 3/I.432.1 – HEC: Receiver mode of operation

The flow chart in Figure 4 shows the consequence of errors in the ATM cell header. The error protection function provided by HEC provides both recovery from single-bit header errors, and a low probability of the delivery of cells with errored headers under bursty error conditions. The error characteristics of fibre-based transmission systems appear to be a mix of single-bit errors and relatively large burst errors. For some transmission systems the error correction capability might not be invoked.



NOTE 1 – Definition of "valid cell": a cell where the header is declared by the Header Error Control process to be free of errors (see Recommendation I.113 [1]).

NOTE 2 – An example of an impermissible header is a header whose VPI/VCI is neither allocated to a connection nor pre-assigned to a particular function (idle cell, OAM cell, etc.) in many instances, the ATM layer will decide if the cell header is permissible.

NOTE 3 – A cell is discarded if its header is declared to be invalid; or if the header is declared to be valid and the resulting header is impermissible.

NOTE 4 – Definition of "intended" header: the header generated by the transmitting device, as it was before being corrupted by one or more errors.

Figure 4/I.432.1 – Consequence of errors in ATM cell header

Appendix I gives information on how random bit errors impact the probability of occurrence of discarded cells and valid cells with errored headers.

7.3.2.2 Header error control sequence generation

The transmitter calculates the HEC value across the entire ATM cell header and inserts the result in the appropriate header field.

The notation used to describe the header error control is based on the property of cyclic codes. (For example code vectors such as 1000000100001 can be represented by a polynomial $P(x) = x^{12} + x^5 + 1$). The elements of an n-element code word are thus the coefficients of a polynomial of order n–1. In this application, these coefficients can have the value 0 or 1 and the

polynomial operations are performed using modulo 2 operations. The polynomial representing the content of a header excluding the HEC field is generated using the first bit of a header as the coefficient of the highest order term.

The HEC field shall be an 8-bit sequence. It shall be the remainder of the division (modulo 2) by the generator polynomial $x^8 + x^2 + x + 1$ of the product x^8 multiplied by the content of the header excluding the HEC field.

At the transmitter, the initial content of the register of the device computing the remainder of the division is preset to all 0s and is then modified by division of the header excluding the HEC field by the generator polynomial (as described above); the resulting remainder is transmitted as the 8-bit HEC.

To significantly improve the cell delineation performance in the case of bit-slips, the following is recommended:

– the check bits calculated by the use of the check polynomial are added (modulo 2) to an 8-bit pattern before being inserted in the last octet of the header;

– the recommended pattern is "0101 0101" (the left bit is the most significant bit);

– the receiver must subtract (equal to add modulo 2) the same pattern from the 8 HEC bits before calculating the syndrome of the header.

This operation in no way affects the error detection/correction capabilities of the HEC.

As an example, if the first 4 octets of the header were all zeros the generated header before scrambling would be "0000 0000 0000 0000 0000 0000 0000 0000 0101 0101". The starting value for the polynomial check is 0 (binary).

7.3.3 Cell delineation

7.3.3.1 Cell delineation and scrambling objectives

Cell delineation is the process which allows identification of the cell boundaries.

The ATM cell header contains a HEC field which is used to achieve cell delineation.

The ATM signal is required to be self-supporting in the sense that it has to be transparently transported on every network interface without any constraints from the transmission systems used.

Scrambling will be used to improve the security and robustness of the HEC cell delineation mechanism as described in 7.3.5. In addition it helps randomizing the data in the information field for possible improvement of the transmission performance.

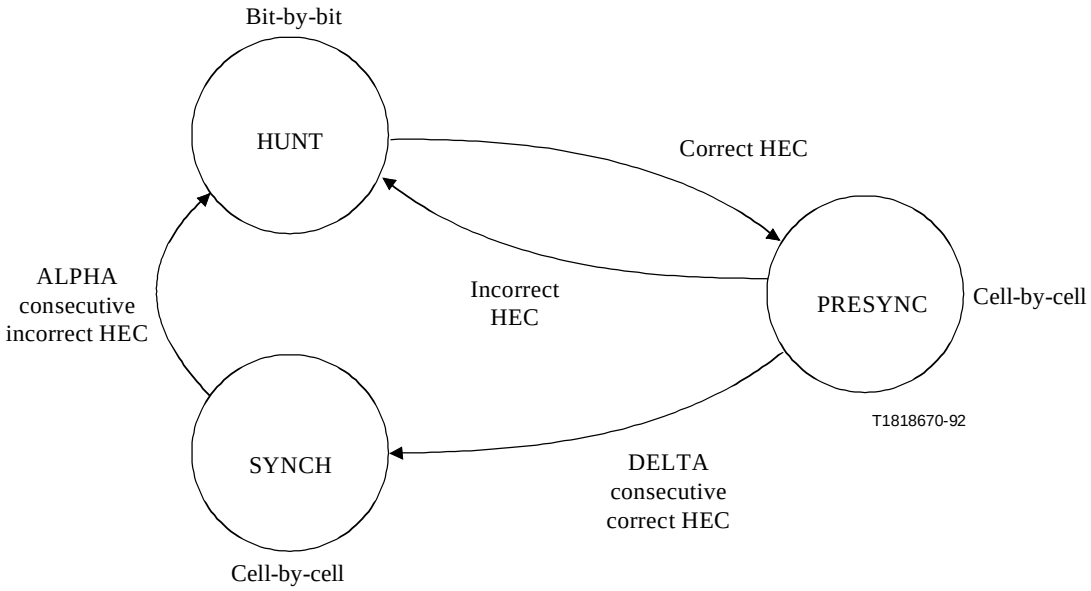
Any scrambler specification must not alter the ATM header structure (as described in Recommendation I.361 [2]), HEC (as described in 7.3.2), and cell delineation algorithm (as described in 7.3.3.2).

7.3.3.2 Cell delineation algorithm

Cell delineation is performed by using the correlation between the header bits to be protected (32 bits) and the relevant control bits (8 bits) introduced in the header by the HEC using a shortened cyclic code with generating polynomial $x^8 + x^2 + x + 1$.

Figure 5 shows the state diagram of the HEC cell delineation method.

NOTE – For a cell-based Physical Layer, during descrambler acquisition and verification states, only the last six bits of the HEC field are to be used for cell delineation checking, and all eight thereafter. For an SDH-based interface, all 8 bits of the HEC are used for acquiring cell delineation.



NOTE – The "correct HEC" means the header has no bit error (syndrome is zero) and has not been corrected.

Figure 5/I.432.1 – Cell delineation state diagram

The details of the state diagram are described below:

1) In the HUNT state, the delineation process is performed by checking bit by bit for the correct HEC (i.e. syndrome equals zero) for the assumed header field. For the cell-based Physical Layer, prior to descrambler synchronization, only the last six bits of the HEC are to be used for cell delineation checking. For the SDH-based interface, all 8 bits are used for acquiring cell delineation. Once such an agreement is found, it is assumed that one header has been found, and the process enters the PRESYNC state. When octet boundaries are available within the receiving Physical Layer prior to cell delineation as with the SDH-based interface, the cell delineation process may be performed octet-by-octet.

2) In the PRESYNC state, the delineation process is performed by checking cell by cell for the correct HEC. For the cell-based Physical Layer, prior to descrambler synchronization, only the last six bits of the HEC field are to be used for cell delineation checking. The process repeats until the correct HEC has been confirmed DELTA times consecutively, at which point the process moves to the SYNC state. If an incorrect HEC is found, the process returns to the HUNT state. The total number of consecutive correct HECs required to move from the HUNT state to the SYNC state is therefore DELTA + 1.

3) In the SYNC state the cell delineation will be assumed to be lost if an incorrect HEC is obtained ALPHA times consecutively.

4) For SDH-based Physical Layer, cells with correct HECs (or cell headers with single bit errors which are corrected) that are processed while in the SYNC state shall be passed to the ATM layer. For cell-based Physical Layer, cells with correct HECs (or cell headers with single bit errors which are corrected) that are processed while in the SYNC state shall be passed to the ATM layer provided the descrambler is in steady state. Idle cells and Physical Layer OAM cells are not passed to the ATM layer.

The parameters ALPHA and DELTA are to be chosen to make the cell delineation process as robust and secure as possible and while satisfying the performance specified in 7.3.3.3.

Robustness against false indication of misalignments due to bit errors in the channel depends on ALPHA.

Robustness against false delineation in the resynchronization process depends on the value of DELTA.

For an SDH-based Physical Layer, ALPHA = 7 and DELTA = 6.

For a cell-based Physical Layer, ALPHA = 7 and DELTA = 8.

DELTA is derived from the ATM cell length and number of HEC bits used for checking. The values of DELTA given achieve a probability of false delineation of better than 10^{-14}, independent of bit errors in the channel. The value of ALPHA ensures good in-synchronization performance where the transmission bit error ratio is better than 10^{-3}.

7.3.3.3 Cell delineation performance

Figures I.1 and I.2 give provisional information on the performance of the cell delineation algorithm described in 7.3.3.2 in the presence of random bit errors, for various values of ALPHA and DELTA. These results represent mean values for SDH-based system and assume that all 8 bits of the HEC are being used.

7.3.4 Scrambler operation

7.3.4.1 ATM cell level scrambler for SDH-based systems

In order to insure cell delineation performance, SDH-based Physical Layers are recommended to use a self-synchronizing scrambler with polynomial $x^{43} + 1$.

This self-synchronizing scrambler polynomial has been selected to minimize the error multiplication introduced by the self-synchronizing scrambling process to two.

The operation of the $x^{43} + 1$ self-synchronizing scrambler in relation to the HEC cell delineation state diagram is as follows:

– the scrambler randomizes the bits of the information field only;

– during the five octets header the scrambler operation is suspended and the scrambler state retained;

– in the HUNT state the descrambler is disabled;

– in the PRESYNC and SYNC states the descrambler is enabled for a number of bits equal to the length of the information field, and again disabled for the following assumed header;

– at start up (e.g. at the power up or on re-synchronization following loss of signal), the first 43 bits of the payload of the first cell transmitted will be used to synchronize the scrambler and descrambler, and as a result the first cell will be corrupted.

7.3.4.2 Scrambler for cell-based systems

In order to insure cell delineation performance, a 31^{st} order Distributed Sample Scrambler is recommended for a cell-based UNI.

The Distributed Sample Scrambler (DSS) is an additive scrambler that does not introduce error multiplication, and is of sufficiently high performance that an underlying PMD sub-layer can rely on it to provide a high degree of randomization.

7.3.4.2.1 Distributed Sample Scrambler (31^{st} order) operation

The Distributed Sample Scrambler is an example of a class of scrambler in which randomization of the transmitted data stream is achieved by modulo addition of a pseudo-random sequence.

Descrambling at the receiver is achieved by modulo addition of an identical locally generated pseudo-random sequence having phase synchronization with the first in respect of the transmitted cells. The descrambler does not affect the performance of the 8-bit HEC mechanism during steady state operation.

Phase synchronization of a receiver PRBS with polynomial generator order r is achieved by sending r linearly independent source PRBS samples through the transmission channel as conveyed data samples. When received without error, these r samples are sufficient to synchronize the phase of the PRBS generator at the receiver to that of the transmitter PRBS generator.

A simple timing skew between the source PRBS samples and the conveyed PRBS samples serves as a means of decoupling the sample times of the source PRBS samples from the conveyed PRBS samples. This enables linearly independent PRBS samples and faster synchronization to be achieved, simply by taking samples at equal intervals of half an ATM cell (212 bits) from the source PRBS generator.

7.3.4.2.2 Transmitter operation

The transmitter pseudo-random binary sequence is added (modulo 2) to the complete cell bit by bit excepting the HEC field. The pseudo-random sequence polynomial is:

$$x^{31} + x^{28} + 1$$

The HEC field for each cell is then modified by modulo 2 addition of the HEC calculated on the 32 bits of the scrambler sequence coincident with the first 32 header bits. This is equivalent to calculation of the HEC on the first 32 bits of the scrambled header. The first two bits of the HEC field are then modified as follows by two bits from the PRBS generator. The two bits from the PRBS generator will be referred to as the PRBS source bits and the two bits of the HEC field onto which they are mapped will be referred to as the PRBS transport bits.

To the first HEC bit (HEC_8) is added (modulo 2) the value of PRBS generator that was added (modulo 2) 211 bits earlier to the previous cell payload. To the second bit of the HEC field is added (modulo 2) the current value of the PRBS generator. These samples are exactly half a cell apart (212 bits) and the first (U_{t-211}) is delayed by 211 bits before conveyance (requiring a one bit store, where 211 bits is 1 bit less than half a cell). See Tables 1 and 2.

Table 1/I.432.1 – PRBS phase (as added to payload and all header except HEC)

U_{t-1}	U_t	U_{t+1}	U_{t+2}	U_{t+3}	U_{t+4}	U_{t+5}	U_{t+6}	U_{t+7}	U_{t+8}	U_{t+9}

Table 2/I.432.1 – Resultant transmitted data element

CLP	HEC_8	HEC_7	HEC_6	HEC_5	HEC_4	HEC_3	HEC_2	HEC_1	1st payload bit	2nd payload bit
+ U_{t-1}	+ U_{t-211}	+ U_{t+1}							+ U_{t+8}	+ U_{t+9}

7.3.4.2.3 Receiver operation

Three basic states of receiver operation are defined:

1) Acquisition of scrambler synchronization.

2) Verification of scrambler synchronization.

3) Steady state operation.

Receiver state 1): Acquisition of scrambler synchronization

The principle of operation is as follows:

– *Cell delineation*

The cell delineation mechanism is independent of the descrambler synchronization mechanism. However while the descrambler is in acquisition or verification states, the cell delineation is determined by using only the last six bits of the HEC field. This is because the first two bits of the HEC field have been modified by the modulo 2 addition of the conveyed data samples and cannot therefore be used in delineation or HEC evaluation until the descrambler is synchronized (steady state).

When the cell delineation process returns to HUNT state, the descrambler process shall return to acquisition state.

– *Acquisition of scrambler synchronization*

In Acquisition state, the conveyed bits (U_{t-211}, U_{t+1}) are extracted by modulo 2 addition of the predicted values for HEC_8 and HEC_7 to the received values. The predicted values correspond to bits HEC_8 and HEC_7 of the HEC value calculated over the first four octets of the received header.

Scrambler synchronization may, for example, be achieved by comparing the conveyed sample every half cell interval (212 bits), with the local bit generated by a recursive descrambler (Figure II.1). If these two bits are not identical, a constant correction vector is applied to the recursive descrambler through feed-forward taps. At time t, the sample conveyed in HEC_8 (U_{t-211}) is compared to the descrambler bit V_{t-211} that has been stored for 211 bits. At time t + 212, the sample conveyed in HEC_7 (U_{t+1}) is compared to the descrambler bit V_{t+1} generated at time t + 1 (both U_{t+1} and V_{t+1} have been stored for 211 bits).

Because both samples are applied to the recursive descrambler 211 bits behind their point of modulo 2 addition to the transmitted data sequence, the recursive descrambler feed-forward taps are chosen to generate a sequence that is advanced by 211 samples. Similarly, the verification comparisons made in the recursive descrambler between the conveyed bits and their prediction is delay equalized using one bit stores as illustrated in Figure II.1.

– *Time to achieve descrambler synchronization*

Two bit samples are conveyed per cell, which are linearly independent. The minimum number of consecutive error free conveyed samples needed to synchronize the descrambler is equal to the degree of the scrambler polynomial, therefore 16 cells provide the 31 samples necessary to synchronize the descrambler.

The descrambler synchronization process is not disabled during cell delineation; however, the descrambler will not begin to converge until the cell delineation mechanism has located the true position of the HEC field in the header and is no longer in its HUNT state. Therefore the start of descrambler synchronization acquisition convergence will be coincident with the final transition from the HUNT state to the PRESYNC state of the cell delineation mechanism.

Receiver state 2): Verification of descrambler synchronization

The verification state differs from the acquisition state in that the recursive descrambler is no longer modified with synchronising samples. Verification is needed because errors undetectable by the 6 bits HEC check may have occurred in the conveyed bits during the acquisition phase. Verification tests the predicted PRBS in the receiver against the remote reference sequence given by the conveyed samples. To verify descrambler acquisition phase overall such that the probability of false

synchronization is less than 10^{-6} requires 16 verifications where the transmission error ratio is better than 10^{-3}.

Receiver State 3): Steady state operation (synchronized descrambler)

In this state the HEC_8 and HEC_7 bits can both be returned to normal use following their descrambling by the locally generated bits (V_{t-211}, V_{t+1}). Properties of error detection and correction are not affected by this process.

Both cell delineation and descrambler synchronization robustness to channel bit-slip are reliably monitored in this state by the existing cell delineation state machine. When the cell delineation process returns to HUNT state, the descrambler process shall return to Acquisition state.

– *HEC regeneration and header scrambling*

The HEC bits in the transmitted cell were modified prior to transmission to correspond to the HEC for the scrambled header. Optionally, to reverse this process where required and regenerate an HEC that corresponds to the unscrambled header, the HEC bits may be modified by modulo 2 addition of the CRC calculated on the 32 bits of the descrambler sequence coincident with the first 32 header bits.

7.3.4.2.4 State transition diagram and mechanism

The three states of the descrambler are acquisition, verification and steady state.

The transition between these states may be determined by reference to the value of a single confidence counter (C) as follows:

Initial state = acquisition, Confidence counter initial value = 0

State 1: Acquisition – Confidence counter range 0 to X–1

For every cell received correctly with no errors detected in HEC bits 1 to 6 the confidence counter is incremented by one and the two conveyed bits used to drive the recursive descrambler into synchronization.

Any error detected in the cell header (HEC bits 1 to 6) results in a return to the initial state (the confidence counter being reset to zero).

Transition to the verification state occurs when the counter reaches X (X = 16).

State 2: Verification – Confidence counter range X to Y–1

For every cell received without detected errors in HEC bits 1 to 6, the two conveyed bits are compared to their predicted values. For each cell with two correct predictions received, the confidence counter is incremented. If one or two incorrect predictions are made then the counter is decremented. If the counter falls below V (V = 8) the system returns to the acquisition initial state 1 and the confidence counter is reset.

Transition to the steady state occurs when the counter reaches Y (Y = 24).

State 3: Steady state – Confidence counter range Y to Z

When the cell delineation process detects a non-zero syndrome with error bits confined to HEC_8 or HEC_7 the confidence counter is decremented, else it is incremented. The acquisition state is returned to automatically should the counter drop below W (W = 16). The confidence counter has an upper limit of Z (Z = 24). See Figure 6. The descrambler process shall also return to the acquisition state if the cell delineation process returns to HUNT state.

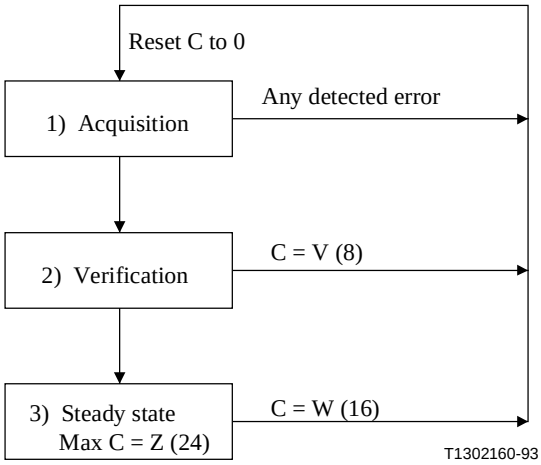


Figure 6/I.432.1 – State transition diagram

7.3.4.3 Scrambler for other systems

For other systems, refer to the relevant clause in the appropriate Recommendation of the I.432 series.

7.3.5 Idle cells

Idle cells cause no action at a receiving node except for cell delineation including HEC verification. They are inserted and discarded for cell rate decoupling. Idle cells are identified by the standardized pattern for the cell header shown in Table 3.

Table 3/I.432.1 – Header pattern for idle cell identification (before scrambling)

	Octet 1	Octet 2	Octet 3	Octet 4	Octet 5
Header pattern	0000 0000	0000 0000	0000 0000	0000 0001	HEC = Valid code 0101 0010
NOTE 1 – The content of the information field is "0110 1010" repeated 48 times. NOTE 2 – There is no significance to any of these individual header fields from the point of view of the ATM layer, as idle cells are not passed to the ATM layer.					

7.4 OAM Implementation

Refer to the appropriate bit rate specific Recommendation of the I.432 series for both SDH-based and cell-based systems.

8 Operational functions

Refer to the appropriate bit rate specific Recommendation of the I.432 series for both SDH-based and cell-based systems.

9 Power feeding

Refer to the appropriate bit rate specific Recommendation of the I.432 series for both SDH-based and cell-based systems.

APPENDIX I

Impact of random bit errors on cell delineation performance

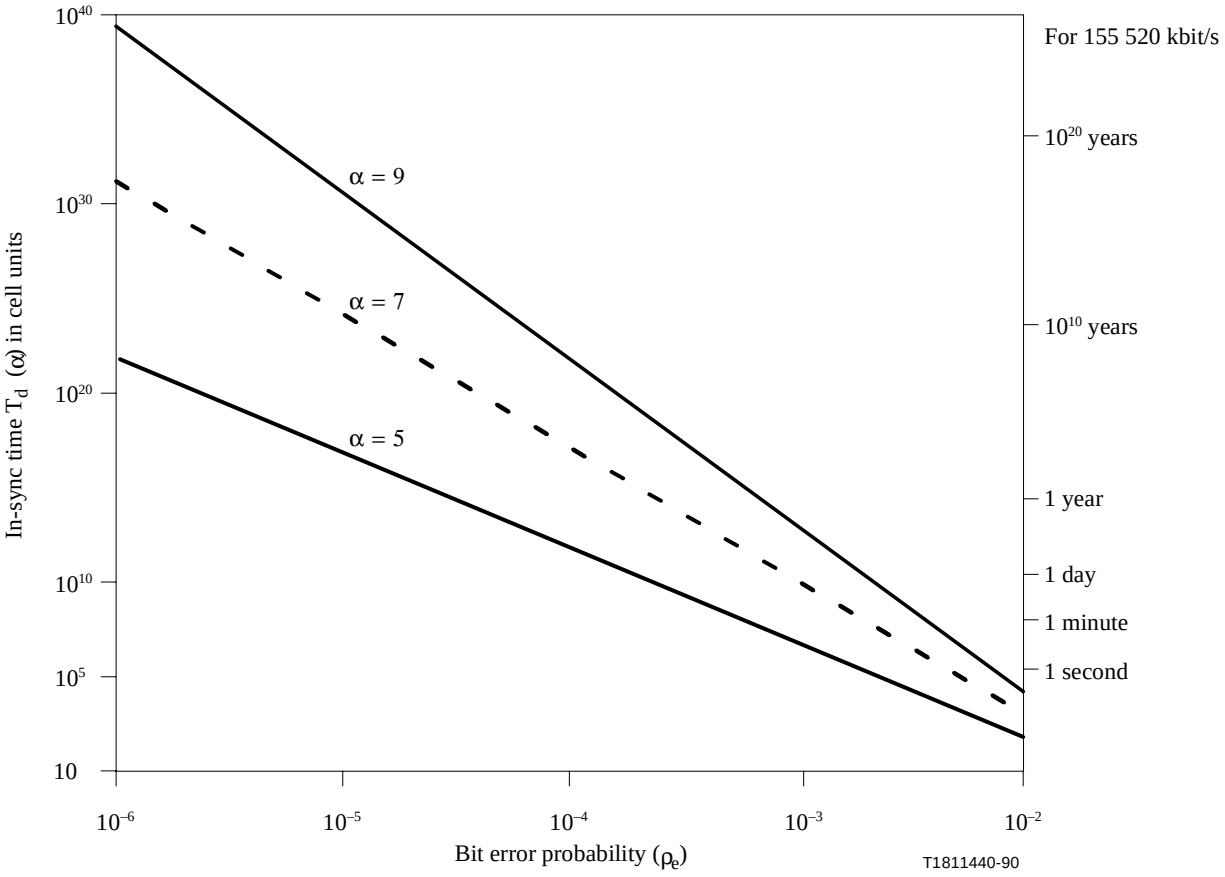


Figure I.1/I.432.1 – Mean in-sync time vs. bit error probability [$T_d(\alpha)$ vs. ρ_e]

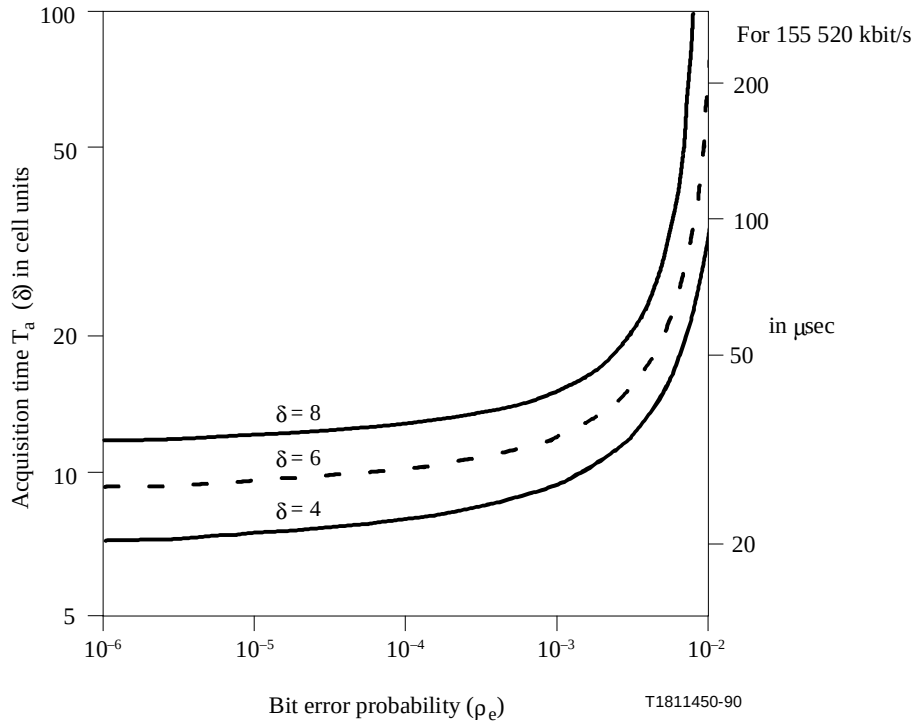


Figure I.2/I.432.1 – Mean acquisition time vs. bit error probability [$T_a(\delta)$ vs. ρ_e]

APPENDIX II

Distributed sample scrambler implementation example

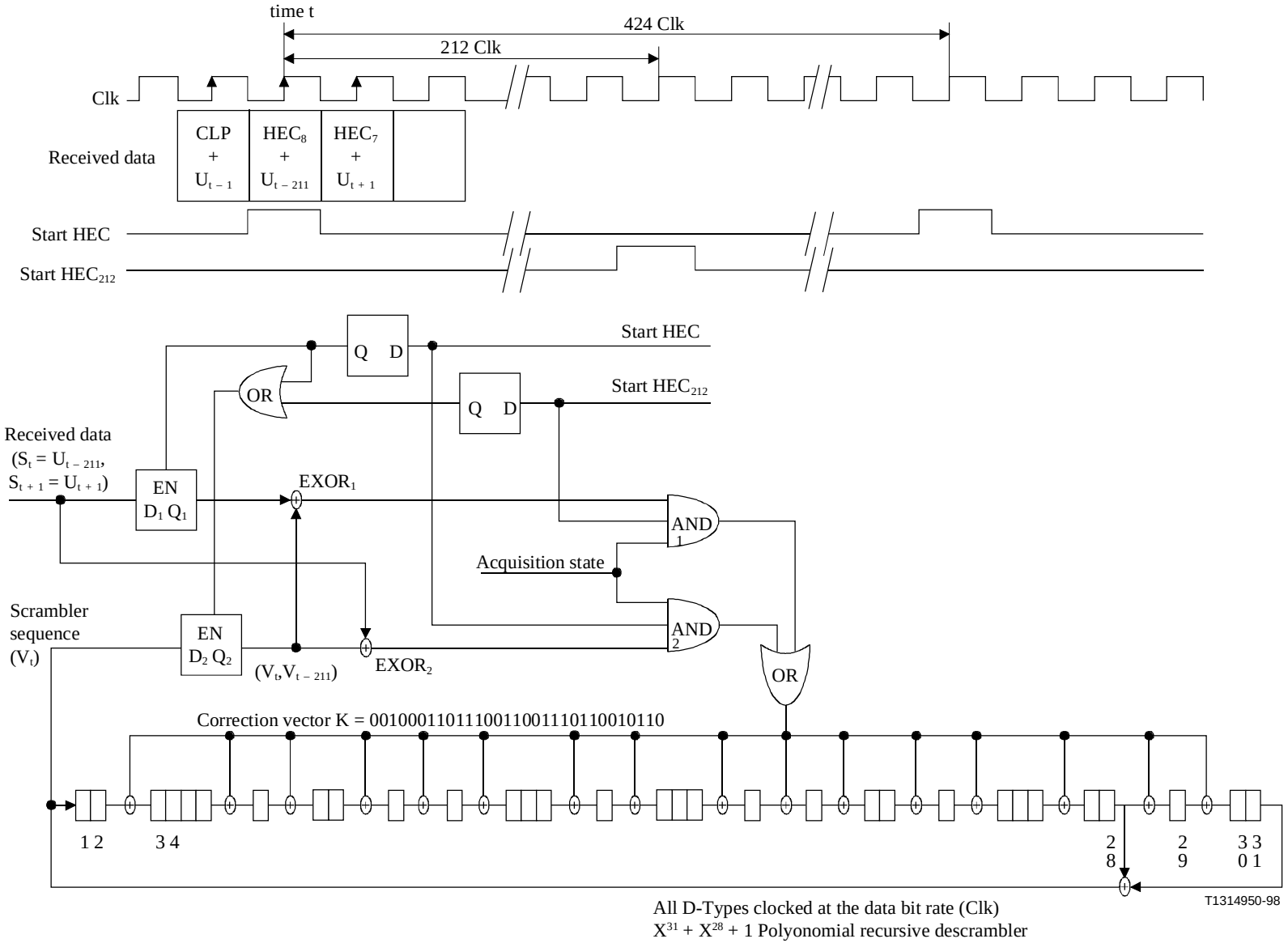
Acquisition of scrambler synchronization

The conveyed bits are extracted by modulo 2 addition of the predicted values for HEC_8 and HEC_7 from the received values. Scrambler synchronization is achieved by comparing the conveyed samples (U_{t-211}, U_{t+1}) at half cell intervals to the recursive descrambler sequence V_t (Figure II.1). In order to ensure the samples are compared with the recursive descrambler sequence at the same interval they were extracted from the source PRBS, the second sample $U_{(t+1)}$ (derived from HEC_7) is stored for 211 bits before it is used.

Additionally, because both samples are applied to the recursive descrambler 211 bits behind their point of modulo addition to the transmitted data sequence, the recursive descrambler feed-forward taps are chosen to generate a sequence that is advanced by 211 samples. Similarly, the verification comparison made in the recursive descrambler between the conveyed bits and their prediction is delay equalized using one bit stores as illustrated in Figure II.1.

Example: Implementation – The recursive descrambler

Figure II.1 illustrates the recursive descrambler implementation. Notation of sample values indicates the important sample values in each cell, time being referenced to the conveyed PRBS sample being received with HEC_8.



NOTE – Acquisition state is active when the cell delineation process is in HUNT or PRESYNC states

Figure II.1/I.432.1 – Example of receiver descrambler

At time t:

– the receiver PRBS generator sample V_t is at the input to the lower D-type D_2;

– the source PRBS sample $S_t = U_{t-211}$ conveyed via HEC_8 is at input D_1;

– the sample previously stored at the output of the lower D-type is $Q_2 = V_{t-211}$

$$EXOR_2 = D_1 + Q_2 = U_{t-211} + V_{t-211}$$

The multiplexer selects this output at time t. In the acquisition state the feed-forward taps (constant correction vector) are applied to the descrambler if the AND gate output is high, that is if $U_{t-211} \neq V_{t-211}$.

At time t + 1:

– the receiver sample V_{t+1} is at the input to D_2;

– the sample $S_{t+1} = U_{t+1}$ is at the input to D_1.

These values are latched on the following clock edge such that:

At time t + 2 through until t + 212:

– $EXOR_1 = Q_2 + Q_1 = V_{t+1} + U_{t+1}$

The multiplexer selects this output at time t + 212. In the acquisition state the feed-forward taps (constant correction vector) are applied to the descrambler if the AND gate output is high, that is if $U_{t+1} \neq V_{t+1}$.

At time t + 213 = L + t – 211 (L being the duration of a cell):

– $D_2 = V_{t+213} = V_{t-211+L}$ (which is latched on the following clock edge and held until the next cell cycle).

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