International Telecommunication Union

ITU-T

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

K.102

(08/2014)

SERIES K: PROTECTION AGAINST INTERFERENCE

Parameters of fixed-voltage thyristor overvoltage protector components used for the protection of telecommunication installations

Recommendation ITU-T K.102

Recommendation ITU-T K.102

Parameters of fixed-voltage thyristor overvoltage protector components used for the protection of telecommunication installations

Summary

Recommendation ITU-T K.102 defines the basic electrical parameters to be met by fixed-voltage thyristor overvoltage protector components used for the protection of telecommunications equipment or lines from surges. Examples of equipment include those located either within a telecommunications centre [b-ITU-T K.20], customer premises [b-ITU-T K.21], in access or in trunk networks [b-ITU-T K.45]. It is intended that this Recommendation be used for the harmonization of existing or future specifications issued by thyristor surge protective component manufacturers, telecommunication equipment manufacturers, administrations or network operators.

History

Edition	Recommendation	Approval	Study Group	Unique ID*
1.0	ITU-T K.102	2014-08-29	5	11.1002/1000/12292

Keywords

Electrical characteristics, electrical ratings, overvoltage protection, surge protective component (SPC), test methods, thyristor.

* To access the Recommendation, type the URL http://handle.itu.int/ in the address field of your web browser, followed by the Recommendation's unique ID. For example, http://handle.itu.int/11.1002/1000/11830-en.

FOREWORD

The International Telecommunication Union (ITU) is the United Nations specialized agency in the field of telecommunications, information and communication technologies (ICTs). The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of ITU. ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSA Resolution 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Compliance with this Recommendation is voluntary. However, the Recommendation may contain certain mandatory provisions (to ensure, e.g., interoperability or applicability) and compliance with the Recommendation is achieved when all of these mandatory provisions are met. The words "shall" or some other obligatory language such as "must" and the negative equivalents are used to express requirements. The use of such words does not suggest that compliance with the Recommendation is required of any party.

INTELLECTUAL PROPERTY RIGHTS

ITU draws attention to the possibility that the practice or implementation of this Recommendation may involve the use of a claimed Intellectual Property Right. ITU takes no position concerning the evidence, validity or applicability of claimed Intellectual Property Rights, whether asserted by ITU members or others outside of the Recommendation development process.

As of the date of approval of this Recommendation, ITU had not received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementers are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database at http://www.itu.int/ITU-T/ipr/.

Table of Contents

Recommendation ITU-T K.102

Parameters of fixed-voltage thyristor overvoltage protector components used for the protection of telecommunication installations

1 Scope

Thyristor surge protective components (SPCs) are specially formulated thyristors designed to limit overvoltages and divert surge currents by clamping and switching actions. This Recommendation applies to fixed-voltage thyristor overvoltage SPCs used in surge protective devices (SPDs) and telecommunications equipment ports to provide overvoltage protection for installations during lightning surges and AC power faults, in accordance with [b-ITU-T K.11]. Telecommunications equipment port test levels and criterion are defined by [b-ITU-T K.20], [b-ITU-T K.21] and [b-ITU-T K.45], as appropriate and are supported by [b-ITU-T K.44] with test circuit details and application guidance.

This Recommendation covers fixed-voltage thyristor SPCs with a switching characteristic in the first quadrant and a switching or blocking or conducting characteristic in the third quadrant.

This Recommendation contains information on:

a) terminology;

b) letter and circuit symbols;

c) essential electrical ratings and characteristics;

d) rating verification and characteristic measurement;

e) environmental tests on packaging;

f) identification and ordering information.

It does not deal with:

a) mountings and their effect on thyristor performance, the test results only apply for the mounting method used for that test;

b) system signal performance such as insertion loss, see [b-ITU-T G.117];

c) mechanical dimensions;

d) RoHS requirements;

e) electrical overload;

f) quality assurance requirements, see [b-IEC 60738-1];

g) specific cases of user agreed and regional values;

h) conventional thyristors as covered by [b-IEC 60747-6];

i) gated thyristor SPCs.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T K.96] Recommendation ITU-T K.96 (02/2014), *Surge protective components: Overview of surge mitigation functions and technologies*.

[IEC 60068-1] IEC 60068-1 ed5.0 (1988), *Environmental testing – Part 1: General and guidance, plus Amendment 1 (1992)*.

[IEC 60068-2-1] IEC 60068-2-1 ed6.0 (2007), *Environmental testing – Part 2-1: Tests – Test A: Cold*.

[IEC 60068-2-2] IEC 60068-2-2 ed5.0 (2007), *Environmental testing – Part 2-2: Tests – Test B: Dry heat*.

[IEC 60068-2-6] IEC 60068-2-6 ed7.0 (2007), *Environmental testing – Part 2-6: Tests – Test Fc: Vibration (sinusoidal)*.

[IEC 60068-2-13] IEC 60068-2-13 ed4.0 (1983), *Environmental testing – Part 2-13: Tests – Test M: Low air pressure*.

[IEC 60068-2-14] IEC 60068-2-14 ed6.0 (2009), *Environmental testing – Part 2-14: Tests – Test N: Change of temperature*.

[IEC 60068-2-20] IEC 60068-2-20 ed5.0 (2008), *Environmental testing – Part 2-20: Tests – Test T: Test methods for solderability and resistance to soldering heat of devices with leads*.

[IEC 60068-2-21] IEC 60068-2-21 ed6.0 (2006), *Environmental testing – Part 2-21: Tests – Test U: Robustness of terminations and integral mounting devices*.

[IEC 60068-2-27] IEC 60068-2-27 ed4.0 (2008), *Environmental testing – Part 2-27: Tests – Test Ea and guidance: Shock.*

[IEC 60068-2-29] IEC 60068-2-29 ed2.0 (1987), *Environmental testing – Part 2: Tests – Test Eb and guidance: Bump*.

[IEC 60068-2-30] IEC 60068-2-30 ed3.0 (2005), *Environmental testing – Part 2-30: Tests – Test Db: Damp heat, cyclic (12 h+12 h cycle)*.

[IEC 60068-2-45] IEC 60068-2-45 ed1.0 (1980), *Environmental testing – Part 2-45: Tests – Test XA and guidance: Immersion in cleaning solvents*.

[IEC 60068-2-54] IEC 60068-2-54 ed2.0 (2006), *Environmental testing – Part 2-54: Tests – Test Ta: Solderability testing of electronic components by the wetting balance method*.

[IEC 60068-2-58] IEC 60068-2-58 ed3.0 (2004), *Environmental testing – Part 2-58: Tests – Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD)*.

[IEC 60068-2-69] IEC 60068-2-69 ed2.0 (2007), *Environmental testing – Part 2-69: Tests – Test Te: Solderability testing of electronic components for surface mounting devices (SMD) by the wetting balance method*.

[IEC 60068-2-78] IEC 60068-2-78 ed1.0 (2001), *Environmental testing – Part 2-78: Tests – Test Cab: Damp heat, steady state*.

[IEC 60695-11-5] IEC 60695-11-5 ed1.0 (2004), *Fire hazard testing – Part 11-5: Test flames – Needle-flame test method – Apparatus, confirmatory test arrangement and guidance*.

3 Definitions

Where possible, terms, definitions, letter symbols and circuit diagram symbols are used from conventional thyristor [b-IEC 60747-6] and rectifier diode [b-IEC 60747-2] standards.

3.1 Terms defined elsewhere

This Recommendation uses the following terms defined elsewhere:

3.1.1 Types of semiconductor component

3.1.1.1 bidirectional diode thyristor [b-IEC 60050-521]: Two-terminal thyristor having substantially the same switching behaviour in the first and third quadrants of the current-voltage characteristic.

3.1.1.2 reverse conducting diode thyristor [b-IEC 60050-521]: Two-terminal thyristor which for negative anode voltage does not switch and conducts large currents at voltages comparable in magnitude to the forward on-state voltage.

3.1.1.3 reverse blocking diode thyristor [b-IEC 60050-521]: Two-terminal thyristor which for negative anode voltage does not switch, but exhibits reverse blocking state.

3.1.1.4 (semiconductor) rectifier diode [b-IEC 60050-521]: Semiconductor diode designed for rectification and including its associated mounting and cooling attachments if integral with it.

3.1.1.5 thyristor [b-IEC 60050-521]: Bi-stable semiconductor device comprising three or more junctions which can be switched from the off-state to the on-state or vice versa.

3.1.2 General terms for semiconductor components

3.1.2.1 avalanche breakdown (of a PN junction) [b-IEC 60050-521]: Breakdown that is caused by the cumulative multiplication of charge carriers in a semi-conductor under the action of a strong electric field which causes some carriers to gain enough energy to liberate new hole-electron pairs by ionization.

3.1.2.2 breakdown (of a reverse-biased PN junction) [b-IEC 60050-521]: Phenomenon, the initiation of which is observed as a transition from a state of high dynamic resistance to a state of substantially lower dynamic resistance for increasing magnitude of reverse current.

3.1.2.3 forward direction (of a PN junction) [b-IEC 60050-521]: Direction of current that results when the P-type semiconductor region is at a positive voltage relative to the N-type region.

3.1.2.4 reverse direction (of a PN junction) [b-IEC 60050-521]: Direction of current that results when the N-type semiconductor region is at a positive voltage relative to the P-type region.

3.1.2.5 Zener breakdown (of a PN junction) [b-IEC 60050-521]: Breakdown caused by the transition of electrons from the valence band to the conduction band due to tunnel action under the influence of a strong electric field in a PN junction.

3.1.3 Component packaging

3.1.3.1 dual in-line package (DIP) [b-IEC 61188-5-1]: Rectangular component package that has a row of leads extending from each of the longer sides of its body that are formed at right angles to a plane that is parallel to the base of its body.

3.1.3.2 guarded measurement (three terminal network) [b-ITU-T K.95]: Measurement technique that allows the direct impedance between two terminals to be measured correctly by applying a compensating voltage to the third terminal that removes the shunting effects of any impedances to the third terminal.

3.1.3.3 package [b-IEC 60050-521]: Enclosure for one or more chips, film elements or other components, that allows electrical connection and provides mechanical and environmental protection.

3.1.3.4 single in-line package (SIP) [b-IEC 61188-5-1]: Component package with one straight row of pins or wire leads.

3.1.3.5 surface mounting component [b-IEC 61760-1]: Electronic component designed for mounting on to terminal pads or conducting tracks on the surface of substrate.

3.1.3.6 surface-mount device, SMD [b-IEC 60749-20-1]: Plastic-encapsulated surface-mount devices made with moisture-permeable materials.

3.1.3.7 surface-mount technology (SMT) [b-IEC 61188-5-1]: Technology where electrical connection of components is made to the surface of a conductive pattern of a printed board and does not utilize component lead holes.

3.1.3.8 surge protective component (SPC) [ITU-T K.96]: Component specifically included in a device or equipment for the mitigation of the onward propagation of overvoltages or overcurrents or both.

3.1.3.9 surge protective device (SPD) [ITU-T K.96]: Device that mitigates the onward propagation of overvoltages or overcurrents or both.

3.1.3.10 terminal (of a semiconductor device) [b-IEC 60050-521]: Conductive element provided for external connection.

3.1.3.11 through-hole technology (THT) [b-IEC 61188-5-1]: Assembly process for mounting component packages where leads are passed through supported (plated-through) or unsupported (bare) holes in an interconnection substrate.

3.1.4 Specific terms for thyristors

3.1.4.1 anode-to-cathode (voltage-current) characteristic [b-IEC 60050-521]: Function, usually represented graphically, relating the anode voltage to the principal current, with the gate current, where applicable, as a parameter.

3.1.4.2 breakover point [b-IEC 60050-521]: Any point on the principal characteristic for which the differential resistance is zero and where the principal voltage reaches a maximum value.

3.1.4.3 critical rate of rise of off-state voltage [b-IEC 60050-521]: Lowest value of the rate of rise of principal voltage that will cause switching from the off-state to the on-state.

3.1.4.4 critical rate of rise of on-state current [b-IEC 60050-521]: Highest value of the rate of rise of on-state current which a thyristor can withstand without deleterious effect.

3.1.4.5 main terminal [b-IEC 60050-521]: Terminal through which the main current flows.

3.1.4.6 off-state [b-IEC 60050-521]: Condition of a thyristor corresponding to the portion of the principal characteristic between the origin and the breakover point or points.

3.1.4.7 on-state [b-IEC 60050-521]: Condition of a thyristor corresponding to the low-resistance low-voltage portion of the principal characteristic.

3.1.4.8 principal (voltage-current) characteristic [b-IEC 60050-521]: Function, usually represented graphically, relating the principal voltage to the principal current, with the gate current, where applicable, as a parameter.

3.1.4.9 principal current [b-IEC 60050-521]: Current which flows through the device excluding gate current.

3.1.4.10 principal voltage [b-IEC 60050-521]: Voltage between the main terminals.

3.1.4.11 reverse blocking state (of a reverse blocking thyristor) [b-IEC 60050-521]: Condition of a reverse blocking thyristor corresponding to reverse currents of lower magnitude than the current at the reverse breakdown voltage.

3.1.5 Thyristor characteristic terms and symbols

3.1.5.1 breakover voltage, $V_{(BO)}$ [b-IEC 60747-6]: Voltage at the breakover point.

3.1.5.2 breakover current, $I_{(BO)}$ [b-IEC 60747-6]: Anode, principal, or thyristor current at the breakover point.

3.1.5.3 forward current (diode), I_F [b-IEC 60747-6]: Current through the device in the forward conducting state.

3.1.5.4 forward recovery voltage (diode), V_{FRM} [b-IEC 60747-2]: Varying voltage occurring during the forward recovery time after instantaneous switching from zero or a specified reverse voltage to a specified forward current.

3.1.5.5 forward voltage (diode), V_F [b-IEC 60747-6]: Voltage across the terminals which results from the flow of current in the forward direction.

3.1.5.6 holding current, I_H [b-IEC 60747-6]: Minimum anode, principal, or thyristor current that will maintain the thyristor in the on state.

3.1.5.7 on-state current, I_T [b-IEC 60747-6]: Anode, principal, or thyristor current when the thyristor is in the on state.

3.1.5.8 on-state voltage, V_T [b-IEC 60747-6]: Anode, principal, or thyristor voltage when the thyristor is in the on state.

3.1.5.9 off-state capacitance, C_o, C_J [b-IEC 61643-341]: Differential capacitance at the specified terminals in the off-state measured at specified frequency, f, amplitude, V_d and d.c. bias, V_D.

3.1.5.10 off-state current, I_D [b-IEC 60747-6]: Anode, principal, or thyristor current when the thyristor is in the off state.

3.1.5.11 off-state voltage, V_D [b-IEC 60747-6]: Anode, principal, or thyristor voltage when the thyristor is in the off state.

3.1.5.12 repetitive peak off-state current, I_{DRM} [b-IEC 61643-341]: Maximum (peak) value of off-state current that results from the application of the repetitive peak off-state voltage, V_{DRM}.

3.1.5.13 repetitive peak reverse current, I_{RRM} [b-IEC 61643-341]: Maximum (peak) value of reverse current that results from the application of the repetitive peak reverse voltage, V_{RRM}.

3.1.5.14 reverse current I_R [b-IEC 60747-2]: Total conductive current flowing through the diode when specified reverse voltage is applied.

3.1.5.15 reverse voltage (of a unidirectional thyristor), V_R [b-IEC 60747-6]: Negative anode voltage.

3.1.6 Thyristor rating terms and symbols

3.1.6.1 critical rate of rise of on-state current, $(di/_T/dt)_{cr}$ [b-IEC 60747-6]: Highest value of the rate of rise of on-state current that a thyristor can withstand without deleterious effect.

3.1.6.2 non-repetitive peak impulse current, I_{PP} [b-IEC 61643-341]: Rated maximum value of peak impulse current of specified amplitude and waveshape that may be applied.

3.1.6.3 peak sinusoidal on-state current, I_{TM} [b-IEC 60747-6]: Peak value of a sinusoidal on-state current, excluding any transient currents.

3.1.6.4 repetitive peak forward current (diode), I_{FRM} [b-IEC 60747-2]: Peak value of the forward current including all repetitive transient currents.

3.1.6.5 repetitive peak off-state voltage, V_{DRM} [b-IEC 60747-6]: Highest instantaneous value of the off-state voltage, including all repetitive transient voltages, but excluding all non-repetitive transient voltages.

3.1.6.6 repetitive peak on-state current, I_{TRM} [b-IEC 60747-6]: Peak value of the on-state current, including all repetitive transient currents.

3.1.6.7 repetitive peak reverse voltage (of a unidirectional thyristor), V_{RRM} [b-IEC 60747-6]: Highest instantaneous value of the reverse voltage, including all repetitive transient voltages, but excluding all non-repetitive transient voltages.

3.1.6.8 surge forward current (diode), I_{FSM} [b-IEC 60747-2]: Peak value of the forward current including all repetitive transient currents.

3.1.6.9 surge on-state current, I_{TSM} [b-IEC 60747-6]: On-state current pulse of short duration and specified waveshape, whose application causes or would cause the maximum rated virtual junction temperature to be exceeded, but which is assumed to occur rarely and with a limited number of such occurrences during the service life of the device and to be a consequence of unusual circuit conditions.

3.1.7 Temperature related parameters

3.1.7.1 maximum junction temperature, T_{JM} [b-IEC 61643-341]: Maximum value of permissible junction temperature, due to self-heating, which a thyristor surge suppressor can withstand without degradation.

3.1.7.2 storage temperature range, T_{stgmin} to T_{stgmax} [b-IEC 61643-341]: Temperature range over which the device can be stored without any voltage applied.

3.1.7.3 temperature derating [b-IEC 61643-341]: Derating with temperature above a specified base temperature, expressed as a percentage, such as may be applied to peak pulse current.

3.1.7.4 thermal resistance, R_{th} [b-IEC 62590]: Quotient of the temperature difference between two specified points or regions and the heat flow between these two points or regions under conditions of thermal equilibrium.

3.1.7.5 transient thermal impedance, Z_{th} [b-IEC 62590]: Quotient of the variation of the temperature difference, reached at the end of a time interval between the virtual junction temperature and the temperature at a specified external reference point and the step function change of power dissipation at the beginning of the same time interval causing the change of temperature.

3.1.7.6 virtual temperature, T_{vj}, T_j [b-IEC 60747-1]: The temperature of the theoretical point or region in a simplified model of the thermal and electrical behaviour of a semiconductor device at or in which all the power dissipation within the device is assumed to occur.

3.2 Terms defined in this Recommendation

None.

4 Abbreviations and acronyms

This Recommendation uses the following abbreviations and acronyms:

ADSL Asymmetric Digital Subscriber Line

DFN Dual Flat No leads

GDT Gas Discharge Tube

JEDEC Joint Electronic Device Engineering Council

POTS Plain Old Telephone Service

QFN Quad Flat No leads

SIP Single In-line Package

SMD Surface Mounting Device

SPC Surge Protective Component

SPD Surge Protective Device

VDSL Very high speed Digital Subscriber Line

5 Conventions

This Recommendation uses the following circuit symbols, Figure 1, based on [b-IEC 60617] for fixed voltage thyristor SPC types:

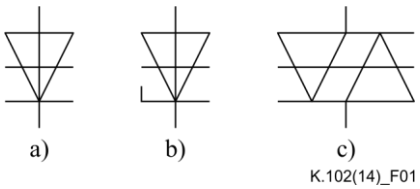


Figure 1 – Symbols for a) Reverse blocking diode thyristor (S00650), b) Reverse conducting diode thyristor (S00651) and c) Bidirectional diode thyristor (S00652)

The characteristics of the three types of fixed-voltage thyristor SPC are shown in Figures 2, 3 and 4. These figures show key component parameters.

Voltage-Current Quadrant 1 characteristics of Figure 2, Figure 3 and Figure 4 are measured with a positive voltage applied to the top terminal of the Figure 1 circuit symbols. Quadrant 3 characteristics are measured with a negative voltage applied to the top terminal.

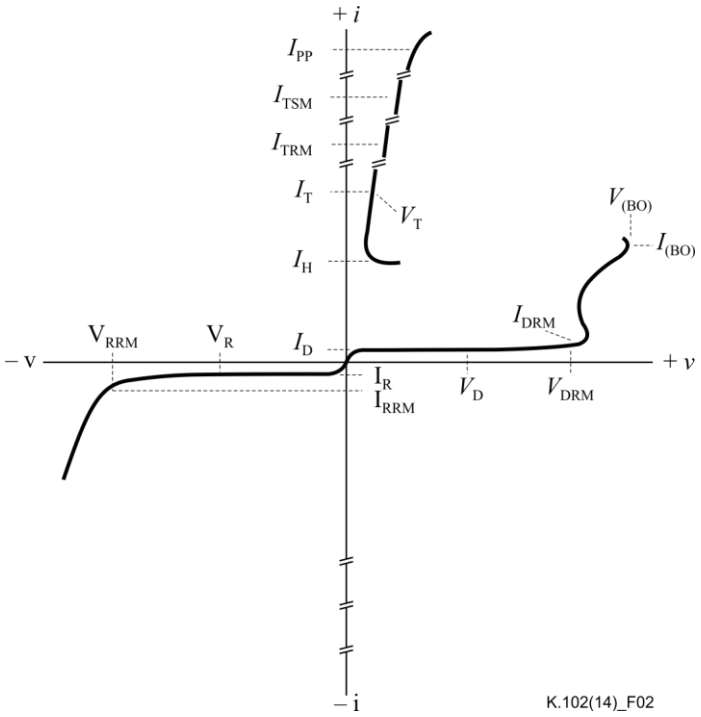


Figure 2 – Reverse blocking diode thyristor characteristic

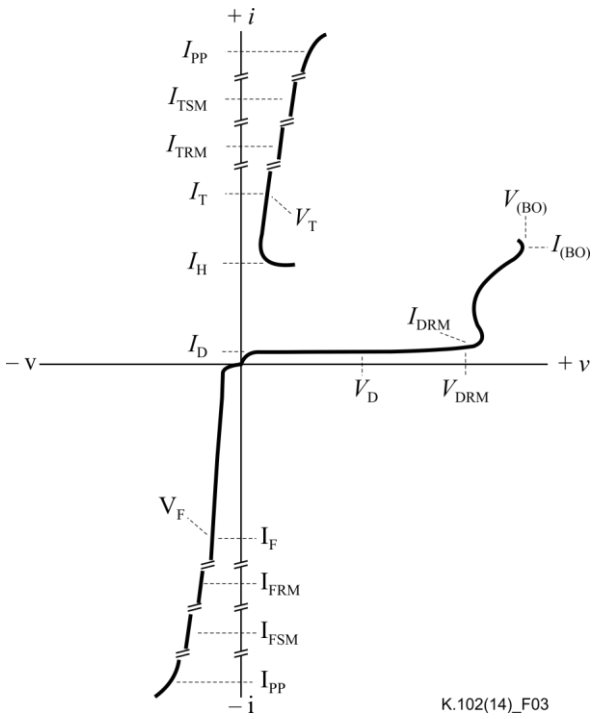


Figure 3 – Reverse conducting diode thyristor characteristic

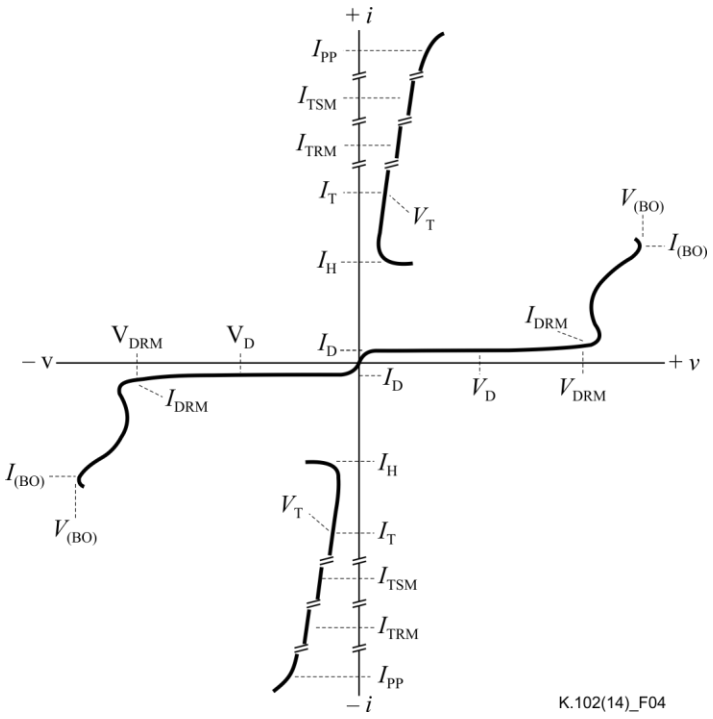


Figure 4 – Bidirectional diode thyristor characteristic

6 Service conditions

6.1 Normal service conditions

This Recommendation is for stationary telecommunications installations that are weather-protected [b-IEC 60721-3-3]. Two equipment microclimates [b-IEC 60721-3-9] defined:

a) Normal microclimate

   1) ambient air temperature within the range of 0°C to 70°C

2) air pressure within the range of 80 kPa to 106 kPa
3) relative humidity within the range of 25% to 75%.

b) Extended microclimate
1) ambient air temperature within the range of –40°C to 85°C
2) air pressure within the range of 70 kPa to 106 kPa
3) relative humidity 10% to 95%.

6.2 Storage temperature range, T_{stgmin} to T_{stgmax}

The temperatures over which the thyristor can be stored without any voltage applied has the following preferred temperature ranges (selected from [b-IEC 60747-1] and [b-IEC 60749-1]):

a) 0°C to 125°C

b) –55°C to 125°C

c) –65°C to 150°C.

7 Electrical requirements

7.1 Electrical characteristics

The electrical characteristic value of a thyristor is measured during the test, unlike ratings which are verified after the stress test (see clause 7.2). Testing shall be done at the standard test temperature of 25°C (see clause 9.3) and at any other temperatures specified in the product documentation.

7.1.1 Off-state current, I_D

This off-state parameter is the current flowing through the thyristor due to a d.c. voltage applied to the terminals at specified ambient conditions.

7.1.1.1 Values

The maximum current value in the product documentation reflects the quality of the tested reversed biased junction and the ability of the manufacturers' production test equipment. Typical limit values are 10 µA or lower.

The test method is given in clause 8.1.1.

7.1.1.2 Criteria

The measured value shall be within the specified limits given in the product documentation.

7.1.2 Repetitive peak off-state current, I_{DRM}

This off-state parameter is the current flowing through the thyristor due to the repetitive peak off-state voltage applied to the terminals at specified ambient conditions.

7.1.2.1 Values

The maximum current value in the product documentation reflects the quality of the tested reversed biased junction and the ability of the manufacturers' production test equipment. Typical limit values are 10 µA or lower.

The test method is given in clause 8.1.2.

7.1.2.2 Criteria

The measured value shall be within the specified limits given in the product documentation.

7.1.3 Reverse current, I_R

This reverse blocking parameter is the current flowing through the thyristor due to a d.c. voltage applied to the terminals at specified ambient conditions.

7.1.3.1 Values

The maximum current value in the product documentation reflects the quality of the tested reversed biased junction and the ability of the manufacturers' production test equipment. Typical limit values are 10 µA or lower.

The test method is given in clause 8.1.3.

7.1.3.2 Criteria

The measured value shall be within the specified limits given in the product documentation.

7.1.4 Repetitive peak reverse current, I_{RRM}

This reverse blocking parameter is the current flowing through the thyristor due to the repetitive peak reverse voltage applied to the terminals at specified ambient conditions.

7.1.4.1 Values

The maximum current value in the product documentation reflects the quality of the tested reversed biased junction and the ability of the manufacturers' production test equipment. Typical limit values are 10 µA or lower.

The test method is given in clause 8.1.4.

7.1.4.2 Criteria

The measured value shall be within the specified limits given in the product documentation.

7.1.5 Breakover voltage, $V_{(BO)}$ and current, $I_{(BO)}$

This off-state parameter is the peak limiting voltage developed before switching to the on-state and the current required to initiate switching at specified ambient conditions.

7.1.5.1 Values

There are no preferred values given can be specified as they are dependent on the intended application and thyristor ratings (see clause 9).

The test method is given in clause 8.1.5.

7.1.5.2 Criteria

The measured values shall be within the specified limits given in the product documentation.

7.1.6 On-state voltage, V_T

This on-state voltage developed when the thyristor is conducting a specified current at specified ambient conditions.

7.1.6.1 Values

There are no preferred values given as they are dependent on the thyristor ratings (see clause 9).

The test method is given in clause 8.1.6.

7.1.6.2 Criteria

The measured value shall be within the specified limits given in the product documentation.

7.1.7 Holding current, I_H

The holding current, I_H, is the minimum current that maintains a switched thyristor in the low-voltage on-state.

7.1.7.1 Values

Common values for I_H are: 150 mA and 250 mA measured at 25°C. The thyristor holding current decreases with temperature, typically 65% of the 25°C value at 70°C. If high ambient temperatures are expected, then the holding current test should be done at the highest expected ambient temperature.

The test method is given in clause 8.1.7.

7.1.7.2 Criteria

The measured value shall be within the specified limits given in the product documentation.

7.1.8 Off-state capacitance, C_o

Because thyristors have multiple PN junctions, the thyristor capacitance will vary with applied voltage. This voltage variable capacitance can distort digital subscriber line (DSL) signals, reduce data rates and cause line unbalance. Various manufacturing and circuit techniques are used to reduce the capacitance variation.

7.1.8.1 Values

Measuring the capacitance at 0 V d.c. usually gives the highest value of capacitance, for a thyristor with two switching quadrants. No matter what the applied voltage, the total capacitance variation cannot exceed the 0 V d.c. value.

As it is the capacitance variation is usually the most important factor, the capacitance change between two levels of d.c. bias is often measured. The amount of tolerable capacitance is system dependent and typical values are; Plain Old Telephone Service (POTS) < 200 pF, Asymmetric Digital Subscriber Line (ADSL) < 40 pF, Very high speed Digital Subscriber Line (VDSL) < 35 pF and VDSL2 < 10 pF.

The test method is given in clause 8.1.8.

7.1.8.2 Criteria

The measured value shall be within the specified limits given in the product documentation.

7.1.9 Forward voltage, V_F

This diode conduction voltage developed when the reverse conducting thyristor is conducting a specified current at specified ambient conditions.

7.1.9.1 Values

There are no preferred values given as they are dependent on the thyristor ratings (see clause 9).

The test method is given in clause 8.1.9.

7.1.9.2 Criteria

The measured value shall be within the specified limits given in the product documentation.

7.1.10 Peak forward recovery voltage, V_{FRM}

This diode dynamic conduction voltage developed when the reverse conducting thyristor is subjected to a rapidly rising current at specified ambient conditions.

7.1.10.1 Values

There are no preferred values given as they are dependent on the thyristor ratings.

The test method is given in clause 8.1.10.

7.1.10.2 Criteria

The measured value shall be within the specified limits given in the product documentation.

7.1.11 Critical rate of rise of off-state voltage, dv/dt

This parameter ensures that the thyristor does not falsely switch on due to fast rising voltages at specified ambient conditions.

7.1.11.1 Values

There are no preferred values given as they are dependent on the system signal dv/dt and the specified surge waveforms.

The test method is given in clause 8.1.11.

7.1.11.2 Criteria

The measured value shall be within the specified limits given in the product documentation.

7.2 Electrical ratings

The thyristor current ratings of this clause are verified by applying the defined current stress test, allowing the thyristor to cool back to ambient temperature, measuring some specified electrical characteristics and determining that the characteristics have not changed. Key indicators of change are usually I_{DRM} and $V_{(BO)}$ measured in all switching quadrants. Reverse blocking thyristors shall also be measured for I_{RRM}. If the characteristic values are only measured after the stress test, then the criteria is to meet the product documentation values. If the characteristic values are measured pre and post the stress test, then the criteria is for the characteristic change not to exceed defined limits such as twice the equipment measurement accuracy. Testing shall be done at the standard test temperature of clause 9 and at any other temperatures specified in the product documentation.

7.2.1 Repetitive peak on-state current, I_{TRM}

The rated repetitive peak on-state current is the maximum level of a.c. surge current that may be applied continuously without causing degradation or failure.

7.2.1.1 Values

There are no preferred values given as they are dependent on the thyristor ratings (see clause 10).

The test method is given in clause 8.2.1.

7.2.1.2 Criteria

After the rated parameter stress test, the thyristor is checked for degradation by measuring the electrical characteristics of I_{DRM} and $V_{(BO)}$ in all switching quadrants. The measured characteristic values shall be within the specified limits given in the product documentation.

7.2.2 Non-repetitive peak on-state current, I_{TSM}

The rated non-repetitive peak on-state current is the maximum level of a.c. surge current that may be applied for a specified time period without causing degradation or failure.

7.2.2.1 Values

There are no preferred values given as they are dependent on the thyristor ratings (see clause 10).

The test method is given in clause 8.2.2.

7.2.2.2 Criteria

After the rated parameter stress test, the thyristor is checked for degradation by measuring the electrical characteristics of I_{DRM} and $V_{(BO)}$ in all switching quadrants. The measured characteristic values shall be within the specified limits given in the product documentation.

7.2.3 Non-repetitive peak pulse current, I_{PP}

The rated non-repetitive peak impulse current is the maximum level of a defined impulse current that may be applied without causing degradation or failure.

7.2.3.1 Values

There are no preferred values given as they are dependent on the thyristor ratings, see clause 10.

The test method is given in clause 8.2.3.

7.2.3.2 Criteria

After the rated parameter stress test, the thyristor is checked for degradation by measuring the electrical characteristics of I_{DRM} and $V_{(BO)}$ in all switching quadrants. The measured characteristic values shall be within the specified limits given in the product documentation.

7.2.4 Non-repetitive peak forward current, I_{FSM}

The rated non-repetitive peak forward current is the maximum level of a.c. surge current that may be applied for a specified time period to a reverse conducting thyristor without causing degradation or failure.

7.2.4.1 Values

There are no preferred values given as they are dependent on the thyristor ratings, see clause 10.

The test method is given in clause 8.2.4.

7.2.4.2 Criteria

After the rated parameter stress test, the thyristor is checked for degradation by measuring the electrical characteristics of I_{DRM} and $V_{(BO)}$ in the switching quadrant. The measured characteristic values shall be within the specified limits given in the product documentation.

7.2.5 Repetitive peak forward current, I_{FRM}

The rated repetitive peak forward current is the maximum level of a.c. that may be applied continuously to a reverse conducting thyristor without causing degradation or failure.

7.2.5.1 Values

There are no preferred values given as they are dependent on the thyristor ratings, see clause 10.

The test method is given in clause 8.2.5.

7.2.5.2 Criteria

After the rated parameter stress test, the thyristor is checked for degradation by measuring the electrical characteristics of I_{DRM} and $V_{(BO)}$ in the switching quadrant. The measured characteristic values shall be within the specified limits given in the product documentation.

7.2.6 Critical rate of rise of on-state current, $(di_T/dt)_{cr}$

The rated critical rate of rise of on-state current is the maximum rate of impulse current rise that may be applied without causing degradation or failure.

7.2.6.1 Values

There are no preferred values given as they are dependent on the thyristor ratings, see clause 10.

The test method is given in clause 8.2.6.

7.2.6.2 Criteria

After the rated parameter stress test, the thyristor is checked for degradation by measuring the electrical characteristics of I_{DRM} and $V_{(BO)}$ in all switching quadrants. The measured characteristic values shall be within the specified limits given in the product documentation.

8 Test methods

For these tests, the component should be mounted as detailed in the product documentation.

Unless otherwise specified, all tests shall be carried out under standard atmospheric conditions for testing as given in clause 5.3 of [IEC 60068-1]:

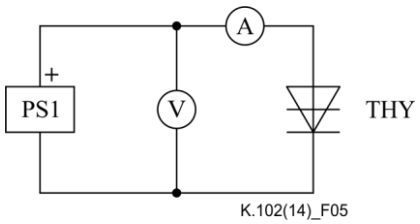
- temperature 15°C to 35°C
- relative humidity 25% to 75%
- air pressure 86 kPa to 106 kPa.

8.1 Electrical characteristics

8.1.1 Off-state current, I_D

The purpose of this test is to determine the off-state current of a thyristor when biased at a specified d.c. off-state voltage. The test circuit used shall be functionally equivalent to Figure 5.

The voltage output of the d.c. supply shall be ramped from zero to the specified value of d.c. off-state voltage, V_D, at a rate below the minimum value of the critical rate of rise of off-state voltage. The d.c. voltage is applied until the value of off-state current, I_D, stabilises. The final value of I_D shall be measured. Unless specified otherwise, each switching quadrant of the thyristor shall be separately tested and measured.



Key

THY	thyristor under test
A	microammeter
V	DC voltmeter
PS1	DC power supply ramped to V_D

Figure 5 – Test circuit for off-state current, I_D at V_D

8.1.2 Repetitive peak off-state current, I_{DRM}

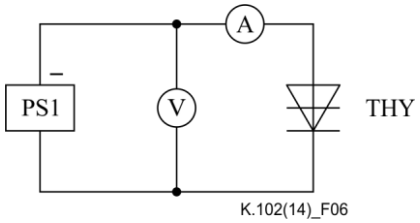
The purpose of this test is to determine the peak off-state current of a thyristor when biased at the specified repetitive peak off-state voltage. The rated value of the repetitive peak off-state voltage, V_{DRM}, shall be applied across the thyristor and the value of thyristor repetitive peak off-state current, I_{DRM}, is measured during the test using a circuit functionally equivalent to Figure 5.

Unless specified otherwise, each switching quadrant of the thyristor shall be separately tested and measured.

8.1.3 Reverse current, I_R

The purpose of this test is to determine the reverse blocking current of a thyristor when biased at a specified d.c. reverse voltage. The test circuit used shall be functionally equivalent to Figure 6.

The voltage output of the d.c. supply shall be ramped from zero to the specified value of d.c. reverse blocking voltage, V_R. The d.c. voltage is applied until the value of reverse blocking current, I_R, stabilises. The final value of I_R shall be measured.



Key

THY	thyristor under test
A	microammeter
V	DC voltmeter
PS1	DC power supply ramped to V_R

Figure 6 – Test circuit for off-state current, I_R at V_R

8.1.4 Repetitive peak reverse current, I_{RRM}

The purpose of this test is to determine the peak reverse current of a reverse blocking thyristor when biased at the specified repetitive peak reverse voltage. The rated value of repetitive peak reverse voltage, V_{RRM}, shall be applied across the thyristor in its blocking quadrant and the peak value of thyristor repetitive peak reverse current, I_{RRM}, is measured during the test using a circuit functionally equivalent to Figure 6.

8.1.5 Breakover voltage, $V_{(BO)}$ and current, $I_{(BO)}$

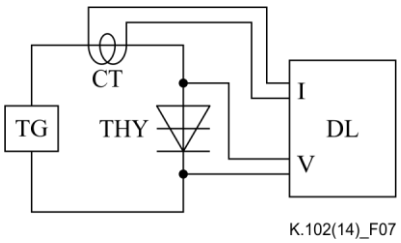
The purpose of this test is to determine the breakover parameters of a thyristor at a specified current ramp rate. The test circuit used shall be functionally equivalent to Figure 7.

The test generator shall apply to the thyristor the electrical test conditions specified for characteristic value measurement.

Alternatively, the test generator circuit diagram shall be given. The peak voltage, $V_{(BO)}$, that occurs across the thyristor in switching from the off-state to the on-state shall be measured together with the thyristor current at that instant ($I_{(BO)}$).

The test generators used by component manufacturers will often exercise the thyristor through the complete switching characteristic, recording the values of $V_{(BO)}$, $I_{(BO)}$, V_T (at I_T) and I_H that occur. An example showing test generator current and the thyristor voltage is shown in Figure 8. Figure 9 has three expansions of the Figure 8 waveforms to show the transition and measurement points. The test generator, TG, used for Figure 8 consists of a current source and a 300 Ω shunt resistor. Starting from zero, the current source ramped to 3 A at 3.33 A/ms (1000 V/ms open-circuit voltage); the current then stepped to 5 A for 200 µs before dropping down to 2 A, after which the current ramped to zero at a rate of –0.2 A/ms.

For multiple cycle a.c. testing, the measured value shall be the highest value of all individual cycle $V_{(BO)}$ values. The corresponding instantaneous thyristor current, $I_{(BO)}$, at $V_{(BO)}$ shall also be measured for a power frequency voltage ramp rate.



Key

THY thyristor under test
CT DC current probe or equivalent
TG test generator with specified characteristics switching THY from off-state to on-state
DL dual channel data logger or equivalent

Figure 7 – Test circuit for breakover, $V_{(BO)}$ and $I_{(BO)}$ and on-state voltage, V_T

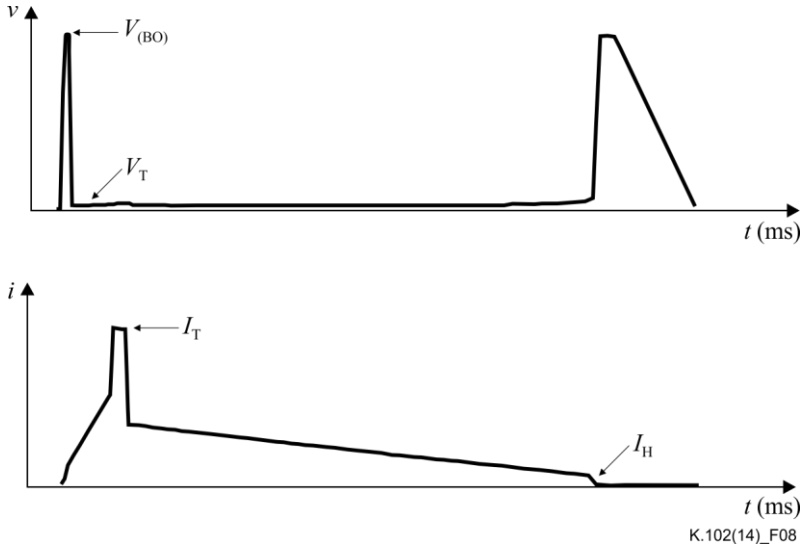


Figure 8 – Test generator current and the resultant thyristor voltage

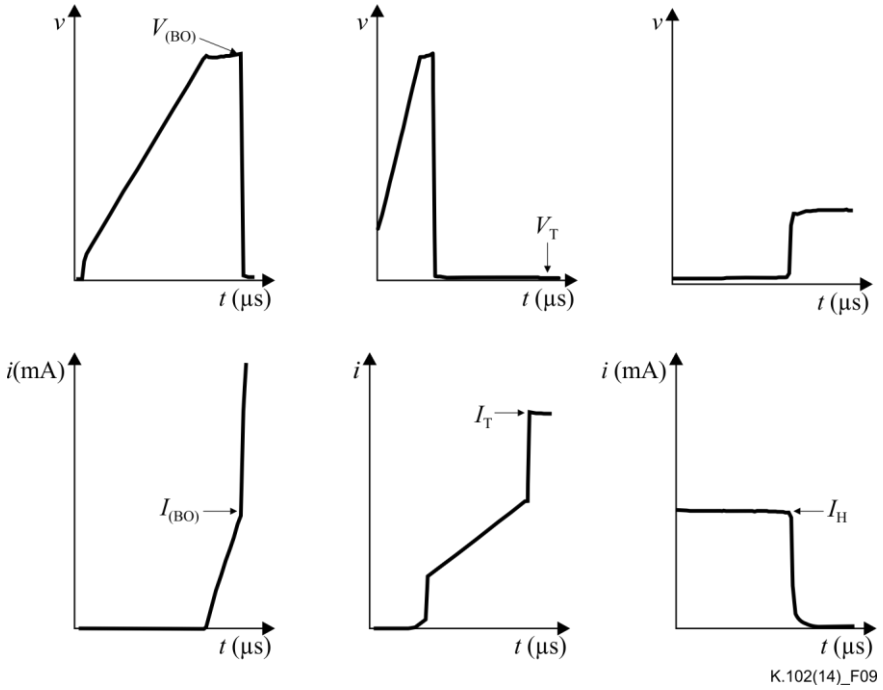


Figure 9 – Waveform expansions of Figure 8

8.1.6 On-state voltage, V_T

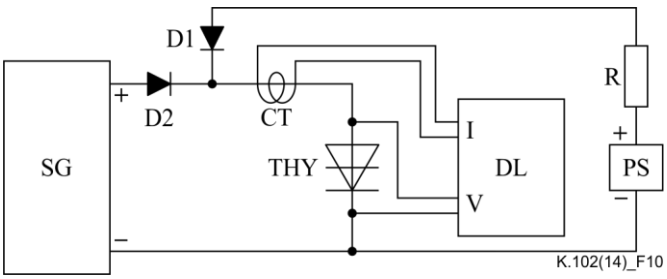
The purpose of this test is to determine the on-state voltage of a thyristor at a specified current; this voltage value is used to calculate the on-state power loss. The test circuit used shall be functionally equivalent to Figure 7 allowing the thyristor to be switched to the on-state and the value of on-state voltage, V_T, measured at a specified time and value of on-state current, I_T (see Figure 9).

Each switching polarity of the thyristor shall be separately tested and measured. The value of V_T will vary with the value of I_T and time. A low and high current value of V_T may be required to cover a.c. and impulse operation.

8.1.7 Holding current, I_H

The purpose of this test is to determine the holding current of a thyristor. A test sequence generator can be used as described in clause 8.1.5. Each switching quadrant of the thyristor shall be separately tested and measured. Alternatively a simple go/no-go circuit can be used as shown in Figure 10.

Figure 10 is based on a gas discharge tube holdover test circuit, (Figure 4 of [b-ITU-T K.12]) and the holding current test circuit of [b-ITU-T K.28]. The thyristor, THY, has two sources of current; the surge generator, SG, and the current limited d.c. power supply, PS. The generator surge is used to switch the thyristor into the on-state. When in the low-voltage on-state the thyristor will also draw current from the power supply. The power supply current level is set by resistor R to be the minimum specified value of I_H. Current flow between the two sources is blocked by the diodes D1 and D2. As the surge current decays to zero, the thyristor conduction current will only be from the power supply. The thyristor will switch off if the actual thyristor holding current is higher than the power supply current. Switch-off is detected by the thyristor voltage rising to the power supply voltage. If thyristor switch-off does not occur, the component fails the test as its actual holding current is lower than minimum specified value. Each switching quadrant of the thyristor shall be separately tested and measured.



Key

THY	thyristor under test
CT	DC probe or equivalent
SG	impulse generator with specified characteristics
PS	DC voltage power supply, set to specified voltage
R	resistor to define the maximum prospective d.c.
D1	reverse current blocking diode for PS
D2	reverse current blocking diode for SG
DL	dual channel data logger or equivalent

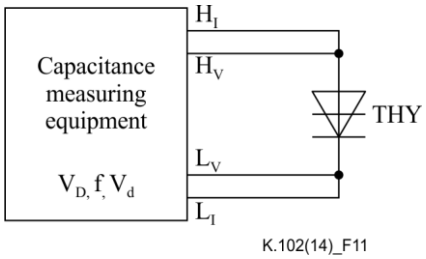
Figure 10 – Test circuit for holding current with additional d.c. bias

8.1.8 Off-state capacitance, C_o

The purpose of this test is to determine the capacitance of a thyristor under specified bias conditions. The test circuit used shall be functionally equivalent to Figure 11.

The test equipment shown has the addition capability of making guarded capacitance measurements on components with three or more active terminals. This allows only the capacitance between the two terminals of interest to be measured and the capacitance from the other terminals to be nulled out.

The THY off-state capacitance, C_o, shall be measured at specified d.c. (V_D) and a.c. (V_d and f) bias levels. In the absence of special requirements, it is recommended that an a.c. bias level of V_d = 1 V r.m.s at a frequency within the range of 100 kHz < f < 1 MHz be used. The d.c. bias level should be −2 V and any other levels that are representative of the intended application.

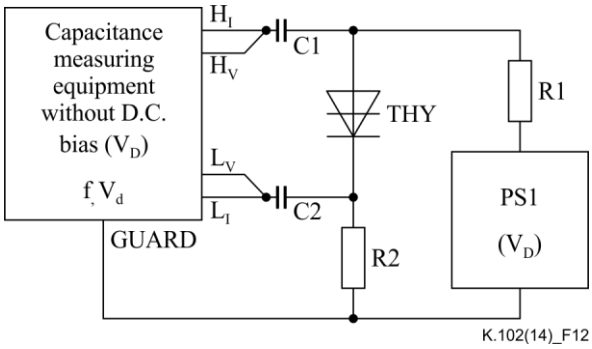


Key

THY	thyristor under test
H_V	H_i, voltage sense
H_i	H_i, current feed
L_V	L_o, voltage sense
L_i	L_o, current return

Figure 11 – Test circuit for capacitance measurement

If the capacitance measuring equipment cannot supply the required d.c. bias voltage, the circuit arrangement shown in Figure 12 can be used.



Key

THY	thyristor under test
C1, C2	DC blocking capacitors, C1 = C2 >> C_o
R1, R2	DC feed resistors, R1 = R2 << V_D / I_D
PS1	variable voltage d.c. power supply set to V_D
H_V	H_I, voltage sense
H_I	H_I, current feed
L_V	L_o, voltage sense
L_I	L_o, current return
Guard	Guard ground terminal (nulls components connected to the terminal from the measurement)

Figure 12 – Test circuit for capacitance measurement with external d.c. bias

8.1.9 Forward voltage, V_F

The purpose of this test is to determine the diode forward voltage of a reverse conducting thyristor at a specified current. The test circuit and waveforms used shall be consistent with those used for the determination of on-state voltage, V_T, clause 8.1.6.

The generator shall switch the THY diode into forward conduction and the value of forward voltage, V_F, shall be measured at a specified time or value of forward current, I_F. Rapidly rising current

waveforms may generate an additional forward recovery voltage; this should not be included in the V_F measurement (see Figure 13).

A low and high current value of V_F may be required to cover a.c. and impulse operation.

8.1.10 Peak forward recovery voltage, V_{FRM}

The purpose of this test is to determine the peak forward diode voltage of a reverse conducting thyristor under the condition of a fast rising current wavefront; this voltage value is the maximum stress imposed on the protected circuitry. The test circuit and levels used shall be consistent with those used for the determination of fast impulse breakover voltage, $V_{(BO)}$ (see Figure 7).

The generator shall switch the diode section on at a specified rate of forward current rise, dI_F/dt, and the value of peak forward recovery voltage, V_{FRM}, shall be measured (see Figure 13.

In the absence of special requirements, it is recommended that the test values for fast impulse rate of rise shall be 1 000 V/µs and 10 A/µs.

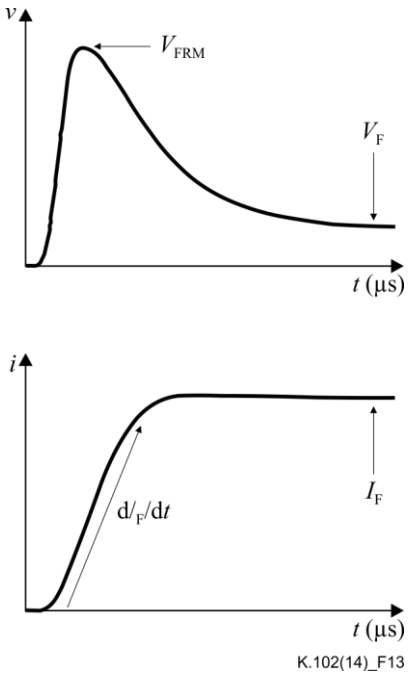
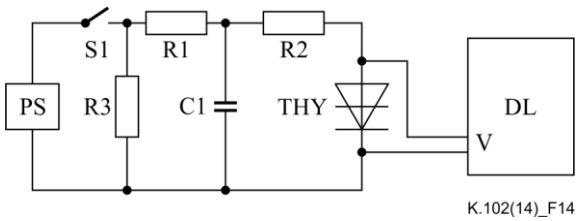


Figure 13 – Diode forward recovery waveforms

8.1.11 Critical rate of rise of off-state voltage, dv/dt

The purpose of this test is to verify that the thyristor will not switch on as a result of fast rising system voltages with peak amplitudes less than the V_{DRM} rating. A specified voltage ramp equal to the minimum value of critical dv/dt and of amplitude V_{DRM} shall be applied to the unenergized thyristor, THY. The peak ramp voltage shall be maintained for a period of at least 50 µs. The thyristor shall not switch on, even partially, during the test. The voltage ramp can be exponential or linear. Figure 14 shows an example of an exponential rate of rise test circuit. For an exponential ramp, the dv/dt value is calculated as 0.632 V_{DRM}/t, where t is the time from the ramp start until the voltage rises to 0.632 V_{DRM}. For a linear ramp, the dv/dt value is calculated as 0.8 $V_{DRM}/(t_{90} - t_{10})$, where t_{10} and t_{90} are the times at which the voltage has risen to 0.1 V_{DRM} and 0.9 V_{DRM}, respectively.

Each switching quadrant of the thyristor shall be separately tested and measured.



Key

THY	thyristor under test	R2	current limit resistor if THY switches
PS	DC voltage power supply	R3	discharge resistor after S1 opens
S1	start test switch	C1	charging capacitor
R1	charging resistor	DL	data logger or equivalent

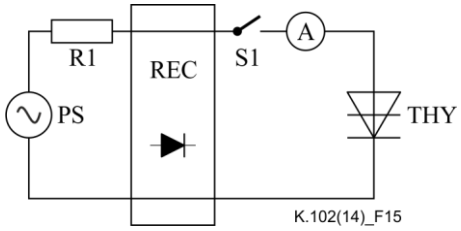
Figure 14 – Test circuit for exponential critical rate of off-state voltage rise, *dv/dt*

8.2 Electrical ratings

The thyristor current stress tests of this clause apply the thyristor rated current values under the defined environmental conditions. After stress testing, the thyristor shall be allowed to cool back to ambient temperature and some specified electrical characteristics measured, see clause 7.2.

8.2.1 Repetitive peak on-state current, I_{TRM}

The purpose of this test is to verify that the thyristor can continuously conduct its rated repetitive peak (quasi-sinusoidal) on-state current without failure or exceeding the maximum rated junction temperature (see Figure 15).



Key

THY	thyristor under test
A	ammeter, peak reading current monitor
PS	AC power supply, set at specified voltage
R1	resistor, defines peak short-circuit current
S1	switch, closed to perform test
REC	full or half-wave rectifier circuit, connected for reverse blocking thyristor testing

Figure 15 – Test circuit for verifying repetitive peak on-state current, I_{TRM}

The a.c. test generator shall be specified for the open-circuit voltage and short-circuit current values, or equivalents, of waveshape and waveshape peak value. The capability of the generator shall ensure that the thyristor will always switch into the on-state. Unidirectional thyristor which are not rated for bidirectional current operation will require a bridge or half-wave rectifier to be added to the a.c. voltage source for full or half wave testing. During the I_{TRM} test, a temperature-sensitive thyristor parameter, such as I_H, can be monitored (see Figure 16).

The average working junction temperature can be calculated from the measured parameter values, the parameter temperature coefficient and the THY initial temperature. After the I_{TRM} test, the thyristor shall not fail any of its specified characteristics. The test duration shall be long enough to establish the desired confidence in thyristor reliability. (Large changes between pre- and post-test characteristics are a possible indication of thyristor degradation.)

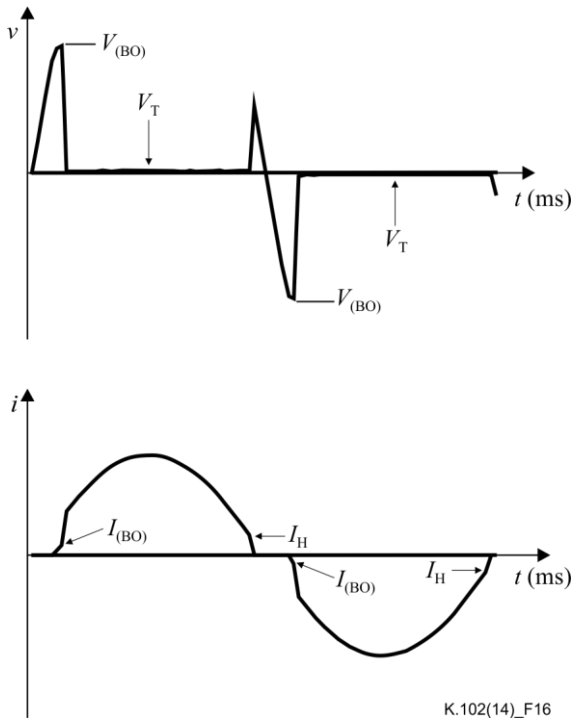
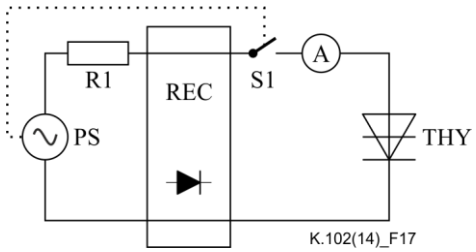


Figure 16 – Repetitive peak on-state current waveforms

8.2.2 Non-repetitive peak on-state current, I_{TSM}

The purpose of this test is to verify that the thyristor can survive a specified duration of (quasi-sinusoidal) a.c. surge current without failure. The test circuit used shall be functionally equivalent to Figure 17.



Key

THY	thyristor under test
A	ammeter, peak reading current monitor
PS	AC power supply, set at specified voltage
R1	resistor, defines peak short-circuit current
S1	switch, closes for specified duration, operation synchronized to a.c. voltage zero crossings
REC	full or half-wave rectifier circuit, connected for reverse blocking thyristor testing

Figure 17 – Test circuit for verifying non-repetitive peak on-state current, I_{TSM}

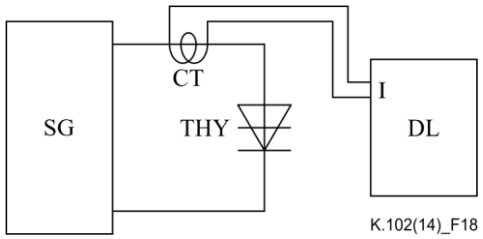
Switch S1 only opens or closes at the zero voltage crossings of the a.c. voltage source. This ensures that the thyristor will be tested with half or full a.c. cycles. The a.c. test generator shall be specified for the open-circuit voltage and short-circuit current values, or equivalent, of waveshape, waveshape peak value, and duration for which the switch S1 closes. The capability of the generator shall ensure that the thyristor will always switch to the on-state. Unidirectional thyristor which are not rated for bidirectional current operation, will require a bridge or half-wave rectifier to be added to the a.c. voltage source for full or half-wave testing. After switch S1 has operated for the specified test duration and the thyristor has returned to thermal equilibrium conditions, the thyristor shall not fail any of its

specified characteristics. (Large changes between pre- and post-test characteristics are a possible indication of thyristor degradation.)

The test duration may be specified as a time or number of a.c. cycles at a specified power frequency. A non-repetitive current rating test shall not be repeated until the thyristor has returned to thermal equilibrium conditions. In the absence of special requirements, it is recommended that the thyristor be capable of withstanding up to 100 such tests without failure during its lifetime. The I_{TSM} rating will vary with test duration time and several values may be needed to fulfil an application need; recommended time durations are one cycle at 0.1 s, 1 s and 10 s.

8.2.3 Non-repetitive peak pulse current, I_{PP}

The purpose of this test is to verify that a thyristor can survive a specified impulse waveshape of short-circuit current amplitude I_{PP} without failure. The test circuit used shall be functionally equivalent to Figure 18. The impulse test generator shall be specified for the open-circuit voltage and short-circuit current values, or equivalent, of waveshape and waveshape peak value. The capability of the generator shall ensure that the thyristor will always switch to the on-state. After the impulse and after the thyristor has returned to thermal equilibrium conditions, the thyristor shall not fail any of its specified characteristics. (Large changes between pre- and post-test characteristics are a possible indication of thyristor degradation.)



Key

THY	thyristor under test
CT	current transformer or equivalent
SG	impulse generator with specified characteristics
DL	data logger or equivalent

Figure 18 – Test circuit for verifying non-repetitive peak pulse current, I_{PP}

Each switching quadrant of the thyristor shall be separately tested and measured. A non-repetitive current rating test shall not be repeated until the thyristor has returned to thermal equilibrium conditions. In the absence of special requirements, it is recommended that the thyristor be capable of withstanding up to 100 such tests without failure during its lifetime. For the purpose of verification a smaller number of tests may be preferred. The I_{PP} rating will vary with waveshape and several waveshape values may be needed to fulfil an application need.

8.2.4 Non-repetitive peak forward current, I_{FSM}

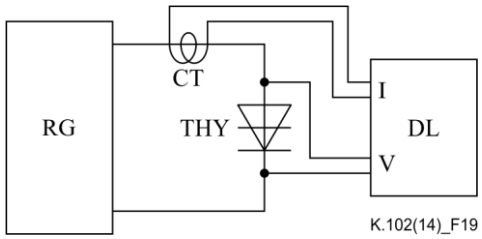
The purpose of this test is to verify that the diode section of a reverse conducting thyristor can survive a specified duration of a.c. surge current without failure. The test method used for non-repetitive peak on-state current, I_{TSM} (see clause 8.2.2 and Figure 17), shall be used for verifying the non-repetitive peak forward current, I_{FSM}. If the conduction period used is one full cycle or longer, then I_{TSM} (see clause 8.2.2) rather than I_{FSM}, is applicable. (I_{TSM} includes both diode and thyristor conduction) After the I_{FSM} test and after the thyristor has returned to thermal equilibrium conditions, the thyristor shall not fail any of its specified characteristics. (Large changes between pre- and post-test characteristics are a possible indication of thyristor degradation.)

8.2.5 Repetitive peak forward current, I_{FRM}

The purpose of this test is to verify that the diode section of a forward or reverse conducting thyristor can continuously conduct the rated repetitive peak forward current without failure or exceeding the maximum rated junction temperature. The test method for repetitive peak on-state current, I_{TRM} (see clause 8.2.1 and Figure 15), shall be used for verifying the repetitive peak forward current, I_{FRM}. In the absence of special requirements, it is recommended that I_{TRM} shall be specified instead of I_{FRM}, where I_{TRM} includes both diode and thyristor conduction.

8.2.6 Critical rate of rise of on-state current, $(di_T/dt)_{cr}$

The purpose of this test is to verify that a thyristor can survive a fast rising current, as may occur on the wavefront of an impulse. The test circuit used shall be functionally equivalent to Figure 19.



Key

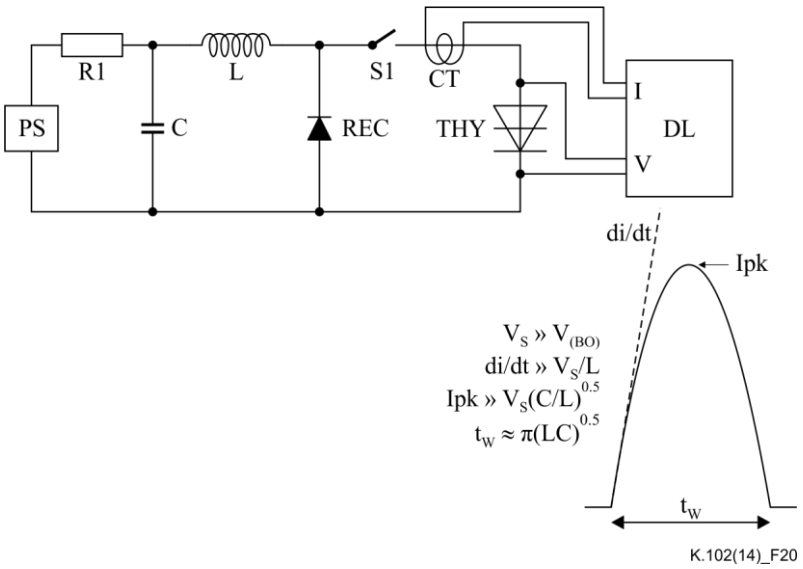
THY	thyristor under test
CT	current transformer or equivalent
RG	ramp generator with specified d*i*/d*t*
DL	dual channel data logger or equivalent

Figure 19 – Test circuit for verifying critical rate of rise of on-state current $(di_T/dt)_{cr}$

Voltage, *V*, and current, *I*, monitors (typically a digital or storage oscilloscope with voltage and current probes) are used to record the circuit conditions. After applying the $(di_T/dt)_{cr}$ impulse to the thyristor, and when it has returned to thermal equilibrium conditions, the thyristor shall not fail any of its specified characteristics. (Large changes between pre- and post-test characteristics are a possible indication of thyristor degradation.)

The $(di_T/dt)_{cr}$ test generator shall be specified for wavefront $(di_T/dt)_{cr}$ and peak (crest) current and waveshape (normally the wave tail will be relatively short). It is essential that the correct waveform is used for this test and the thyristor manufacturer should be contacted for the test circuit and waveform details. In the absence of special requirements, it is recommended that a generator based on the standard thyristor $(di_T/dt)_{cr}$ test circuit be used. The basic circuit diagram and its waveforms are shown in Figure 20.

Each switching quadrant of the thyristor shall be separately tested and measured. A non-repetitive current rating test shall not be repeated until the thyristor has returned to thermal equilibrium conditions. In the absence of special requirements, it is recommended that the thyristor shall be capable of withstanding up to 100 such tests, in each test polarity, without failure, during its lifetime. For the purpose of verification a smaller number of tests may be preferred.



Key

THY	thyristor under test
CT	current transformer or equivalent
PS	DC power supply, set to *Vs*
R1	resistor, limits charging current
S1	switch, closes to start test; opens at current zero crossing
REC	rectifier conducts the negative current
C	capacitor, energy storage and timing
L	inductor, sets d*i*/d*t*
DL	dual channel data logger or equivalent

Figure 20 – Half sine-wave di/dt test circuit

9 Preferred values

This clause lists parameter values for 2-terminal diode fixed voltage thyristor SPCs. Certain parameters such as $V_{(BO)}$ and V_{DRM}, will have a defined relationship, whereas parameters like I_H are essentially independent. Components like resistors, capacitors, inductors and breakdown diodes are available in a preferred series of values like the [b-IEC 60063] E12 series for ±10% tolerance components and the E24 series where a ±5% tolerance is needed. Thyristor SPCs have their parametric values set by the expected surge environment, the equipment withstand capability and the system voltage and current levels.

To meet these requirements, the thyristor parameters have to be customized to a spectrum of individual of unique requirements. Hence the use of a mathematically generated value series is impractical. Further, differences in manufacturing processes mean that limit parameters may not be the same. This is why manufacturers cannot offer a common set of limit parametric values. For some parameters, as in clauses 9.1 and 9.2 only a technology capability can be shown.

9.1 $V_{(BO)}$ and V_{DRM}

The $V_{(BO)}/V_{DRM}$ ratio is dependent on the manufacturing process and the value of V_{DRM}. Figure 21 shows how $V_{(BO)}/V_{DRM}$ varies with V_{DRM}.

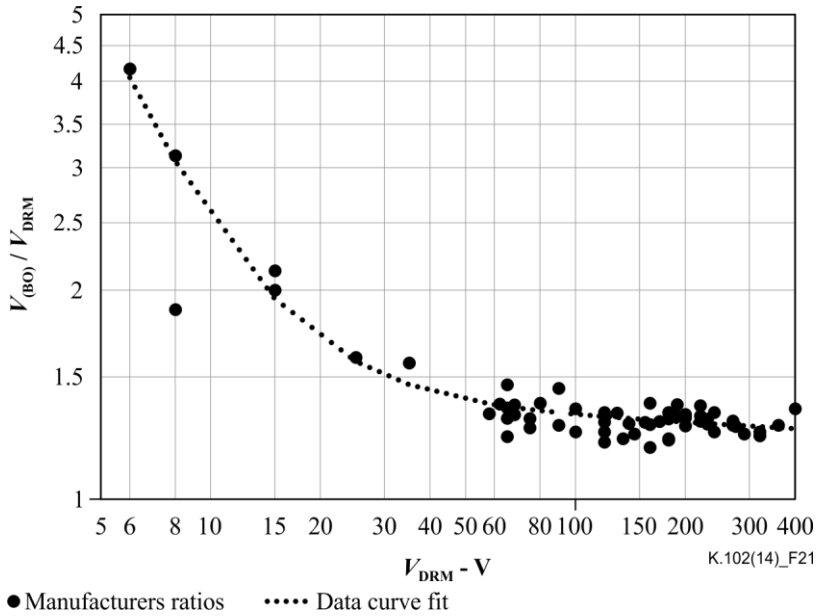


Figure 21 – $V_{(BO)}/V_{DRM}$ ratio against V_{DRM}

Below approximately 50 V, the manufacturing process changes to get the lower V_{DRM} voltages and this causes an increase in the $V_{(BO)}/V_{DRM}$ ratio. As guidance to what should be possible as a $V_{(BO)}$ value the data curve fit line is used to for the $V_{(BO)}$ plot in Figure 22.

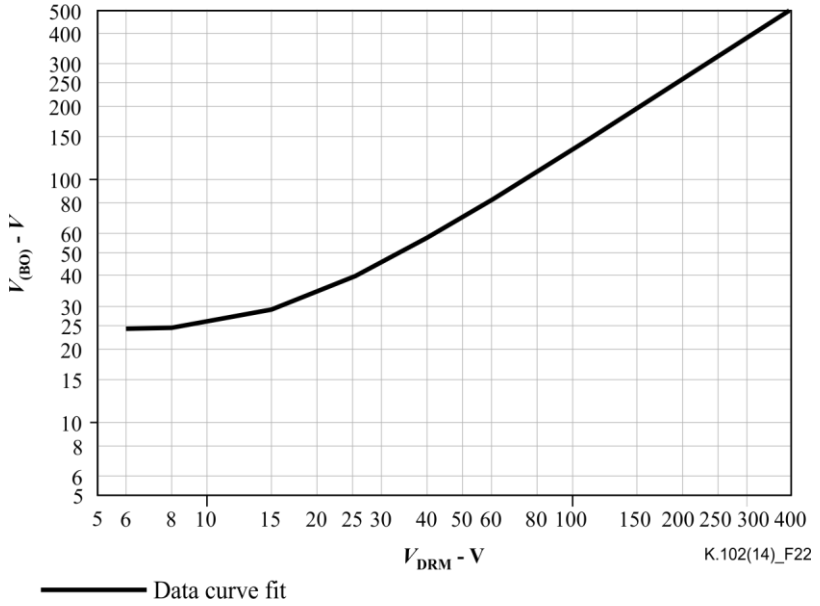


Figure 22 – $V_{(BO)}$ vs V_{DRM}

9.2 C_O, V_{DRM} and I_{PP}

The thyristor chip size will be related to the I_{PP} rating. The thyristor capacitance will depend on the breakdown area on the chip and the breakdown voltage. For the same chip structure, Figure 23 shows the capacitance, C_O, variation with DC bias, V_{DC}, for repetitive off-state voltages, V_{DRM}, of 58 V, 90 V and 180 V.

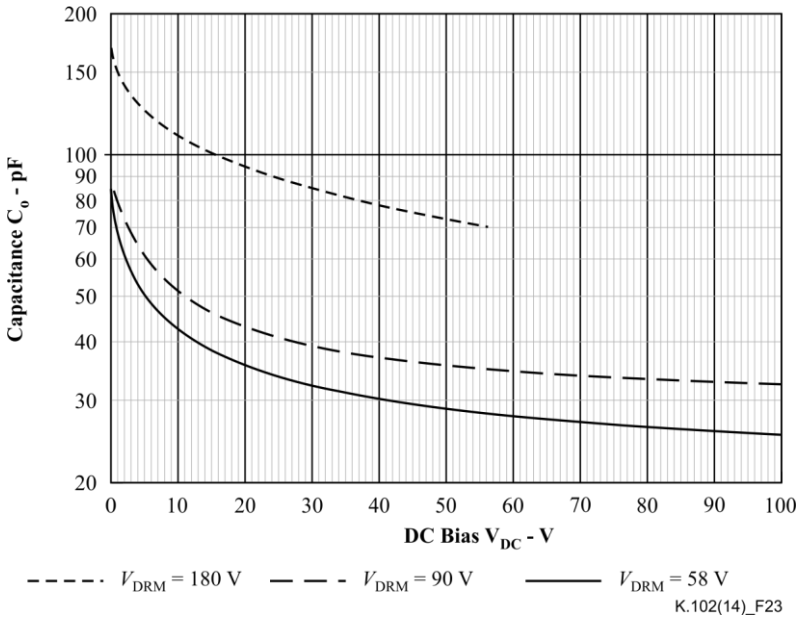


Figure 23 – Capacitance variation with DC bias

To cater for the various types thyristor SPC a preferred DC bias value of 2 V shall be used to prevent the AC measuring bias of 1 Vrms reversing the applied voltage polarity. It is the capacitance change with voltage that causes the distortion of digital signals rather than the absolute value of capacitance. The capacitance change between two levels of DC bias is a better criterion than a single capacitance value. A second capacitance measurement should be taken at V_{DC} = 50 V, assuming this is permitted by V_{DRM} of the thyristor. The capacitance change from 2 V to 50 V is more relevant capacitance value for digital applications.

9.3 I_H

The variation of holding current, I_H, with temperature is predictable. It is sufficient to specify the holding current measurement at an ambient of 25°C. Typical minimum current values are 150 mA and 225 mA for thyristor components with V_{DRM} values above 50 V and I_{PP} ratings of 100 A, for 10/1000 impulse waveshapes[1] or less. Due to the different manufacturing techniques and application use, thyristor components with V_{DRM} values below 50 V will often have typical I_H values of 50 mA. Due to application use, thyristor components with 200 A, 10/1000 I_{PP} ratings will often have typical I_H values of 50 mA.

9.4 I_{PP} and time to half value (duration)

Difference in chip sizes, evaluation techniques and applied safety margins means that there is not a universal normalized I_{PP} versus surge duration curve. Figure 24 shows the variance between several thyristor manufacturers. The symbols on a line represent the I_{PP} value at current waveshapes of 2/10, 8/20, 10/160, 5/320, 10/560 and 10/1000.

The preferred I_{PP} 10/1000 values used by manufacturers are 30 A, 45 A, 50 A, 80 A, 100 A and 200 A.

[1] Note, impulse wave shapes are designated as x/y having a rise time of x µs and a decay time to half value of y µs, for example 10/1000.

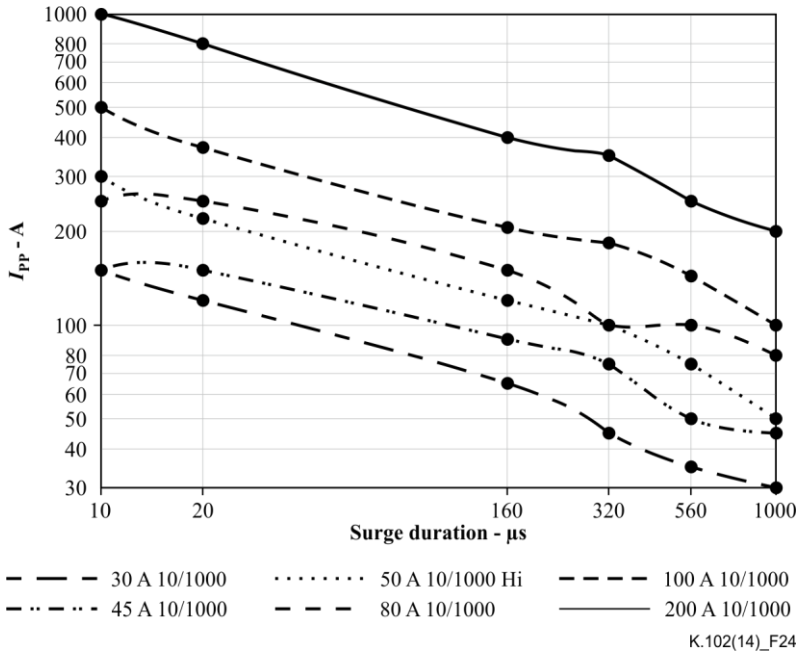


Figure 24 – I_{PP} versus Duration for various 10/1000 waveshape current ratings

10 Informative characteristics

For some electrical parameters, it is useful to have a general idea of how they vary over a wide range of conditions. Although not a product guarantee, many manufacturers provide details of the generic variation of some parameters. Holding current and breakover voltage variation with temperature are two commonly provided parameters.

10.1 Variation of holding current with temperature

The holding current value decreases with increasing temperature. Figure 25 allows the designer, knowing the expected maximum ambient temperature around the thyristor, to estimate the minimum I_H value at that temperature.

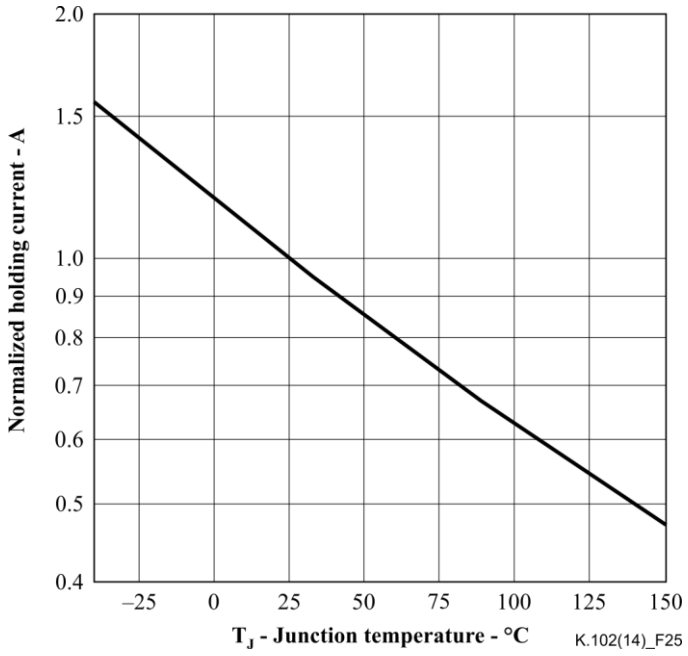


Figure 25 – Variation of normalized holding current versus temperature

10.2 Variation of breakover voltage with temperature

Breakover voltage increases with increasing temperature, typically at a rate of 0.5%/K. Figure 26 allows the designer to predict the likely value of breakover voltage at high junction temperatures.

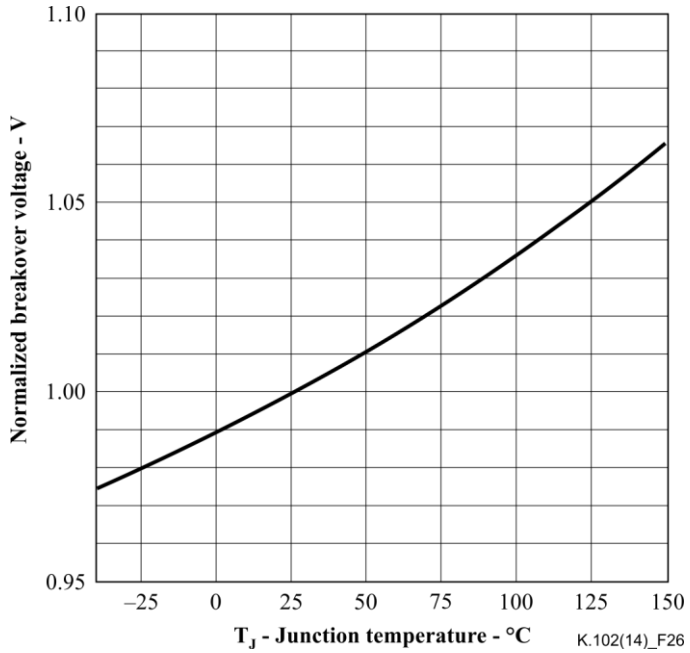


Figure 26 – Variation of normalized breakover voltage versus temperature

10.3 Variation of repetitive peak off-state voltage with temperature

The repetitive peak off-state voltage decreases with decreasing temperature, at a rate of about 1%/K. Figure 27 allows the designer to predict the likely value of peak off-state voltage at the lowest expected thyristor ambient temperature. The low temperature voltage value must be higher than the maximum service voltage to avoid clipping.

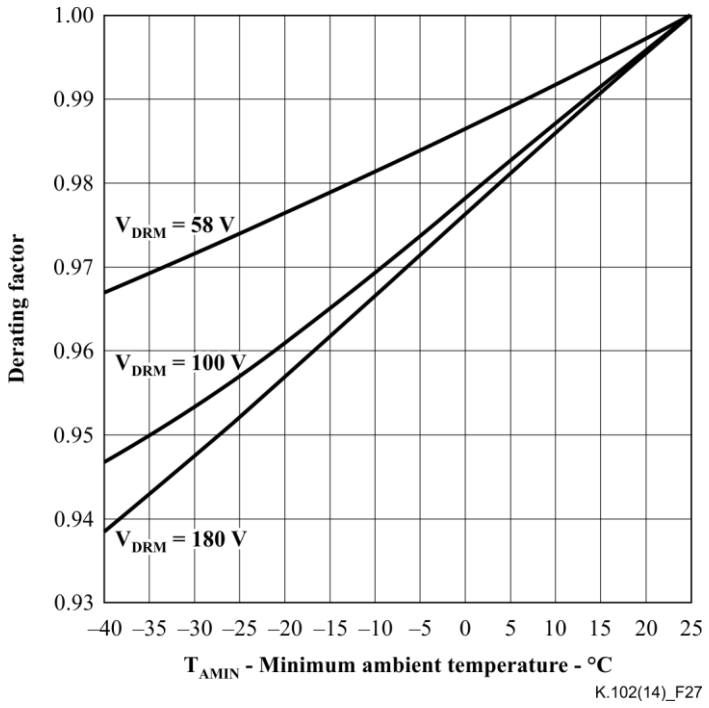


Figure 27 – Variation of normalized repetitive off-state voltage versus temperature

10.4 Variation of capacitance with voltage

Thyristor capacitance varies with applied voltage. Capacitance variation with voltage causes twisted pair line unbalance and intermodulation distortion of complex signals. Figure 28 allows the designer to estimate the levels of these effects.

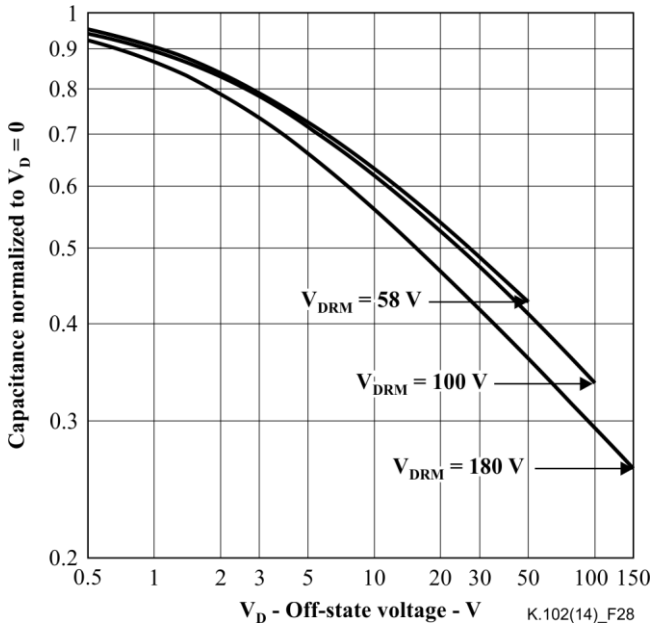


Figure 28 – Variation of normalized capacitance versus off-state voltage

10.5 Variation of non-repetitive a.c. surge current with time

The maximum value of non-repetitive a.c. surge current decreases with increasing current flow time. At long periods, when thermal equilibrium is reached, the I_{TSM} becomes the I_{TRM} value. Figure 29 allows the designer to select a series current limiter that operates before thyristor damage occurs due to the I_{TSM} value at that time being exceeded.

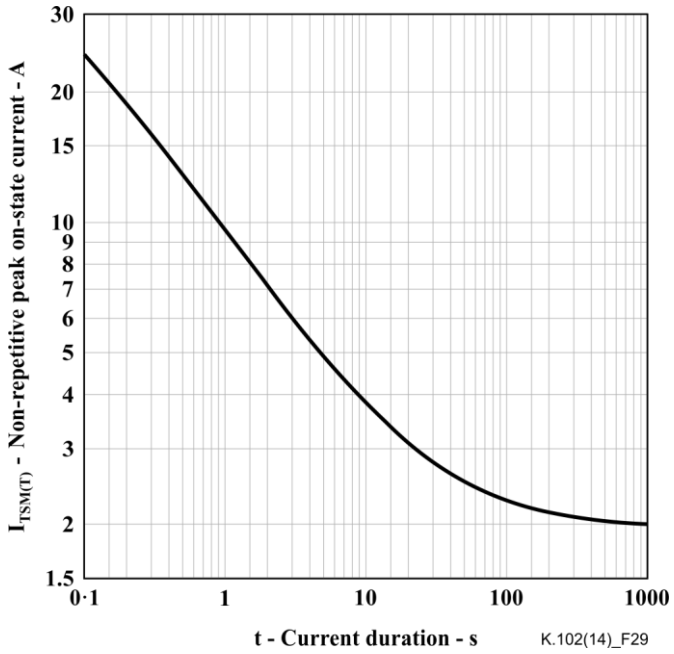


Figure 29 – Example of non-repetitive a.c. surge current with time

11 Environment tests

Prior to, and after, the tests in the subclauses below, measure the component resistance, and verify impulse voltage rating. Any change in value compared with that measured initially shall be recorded and the value after test shall stay within defined limits. Visual examinations shall show no evidence of damage, and the marking shall be legible.

11.1 Robustness of terminations

11.1.1 Through-hole lead terminations robustness

Components with wire terminations shall be subjected to tests U_{a1} and U_b of [IEC 60068-2-21] with the following details:

a) Test U_{a1} – Tensile

The force applied shall be 10N for wire diameter 0.6 mm and 0.8 mm, or 20N for wire diameter 1 mm for 1 min.

b) Test U_b – Bending.

Two consecutive bends shall be applied in each direction.

11.1.2 SMD termination robustness

Thyristors in two-terminal SMD resistor type packaging shall be subjected to the following test. Thyristors in multi-chip or multi-terminal packaging (DFN, QFN, SIP, etc.) should be tested in accordance with the relevant JEDEC or alternative standards.

a) Force application test

Surface mount components shall be soldered on the substrate using the method prescribed by the manufacturer, as given in Figure 30. The dimensions of the substrate are as shown in Table 4 and Figure 30. A force specified in Table 4 shall be smoothly applied on the sample for 5 s ± 1 s.

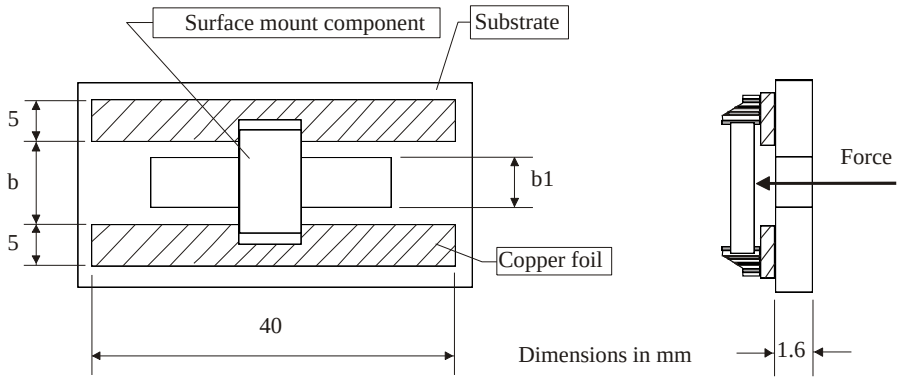


Figure 30 – Test arrangement for surface mount components

b) Test U_e of [IEC 60068-2-21]

Bend the substrate by 2 mm for 10 times. After the test, the component shall comply with the requirements of the first paragraph of clause 10.

Table 4 – Force and dimensions of the substrate

Surface mount device type	1005 (0402)	1608 (0603)	2012 (0805)	3210 (1206)	3225 (1210)	4532 (1812)	5750 (2220)
Force P, N	5	5	10	10	10	15	15
Dimension *b*, mm	0.5	1.0	1.2	2.2	2.2	3.2	4.0
Dimension b_1, mm	0.5	1.0	1.0	1.0	1.0	1.0	1.5

11.2 Solderability

11.2.1 Non-SMD package lead solderability

Tested in accordance with [IEC 60068-2-54], Test Ta, method 1 (solder bath), with the following details:

Depth of immersion (from component body): 2 mm for wire terminations. A thermal insulating screen of 1.5 mm ± 0.5 mm thickness shall be used for wire terminations.

Time of immersion: 2s ± 0.5 s

Temperature of the solder bath: 235°C ± 5°C, for P_b-Sn solder

260°C ± 5°C, for lead-free solder

Visual examination shall show free flowing of the solder with the wetted area of terminations not less than 80%. A magnifier capable of giving a magnification of (4~10) times may be used when visual examination is carried out.

11.2.2 SMD type solderability

Tested in accordance with [IEC 60068-2-58], Test Td with the following details:

Time of soldering: 4 s ± 1 s

Recovery time: 24 h ± 2 h

Visual examination shall show free flowing of the solder with the wetted area of terminations not less than 80%. A magnifier capable of giving a magnification of (4~10) times may be used when visual examination is carried out.

11.3 Resistance to soldering heat

11.3.1 Non-SMD package resistance to soldering heat

Tested in accordance with [IEC 60068-2-20], Test Tb, method 1 (solder bath), with the following details:

Depth of immersion (from component body): 2 mm for wire terminations.

Time of immersion: 5 s ± 0.5 s

Temperature of the solder bath: 235°C ± 5°C for P_b-Sn solder

260°C ± 5°C for lead-free solder

After recovery for 1 h, the component shall comply with the requirements of the first paragraph of clause 10.

11.3.2 SMD type resistance to soldering heat

Tested in accordance with [IEC 60068-2-58], Test Td with the following details:

Time of soldering: 10 s ± 1 s

Recovery time: 24 h ± 2 h

After recovery for 24 h, the component shall comply with the requirements of the first paragraph of clause 10. A magnifier capable of giving a magnification of (4~10) times may be used when visual examination is carried out.

11.4 Vibration

Tested in accordance with [IEC 60068-2-6], Test Fc, method B4, with the following details:

Frequency of sine wave: 10 Hz~55 Hz for 10 cycles

Acceleration: 98 m/s^2, or Amplitude: 0.75 mm, whichever is the less severe vibration

Duration: 6 h (2 h for each axis)

After the test, the component shall comply with the requirements of the first paragraph of clause 10.

11.5 Bump

Tested in accordance with [IEC 60068-2-29], Test Eb with the following details:

Pulse: half sine, duration 6 ms

Maximum acceleration: 400 m/s^2

Number of bumps: 4000

After the test, the component shall comply with the requirements of the first paragraph of clause 10.

11.6 Rapid changes of temperature

Tested in accordance with [IEC 60068-2-14], Test Na with the following details (Table 5):

The temperature cycle shall be repeated for 5 times as below:

Table 5 – Temperature cycle details

Step	Temperature	Period
1	–40°C ± 3 °C	(30 ± 3) min
2	(transition time)	< 10 s
3	+85°C ± 2 °C	(30 ± 3) min
4	(transition time)	< 10 s

After completion of 5 cycles, the samples shall be allowed to recover in room temperature for 1 h～2 h.

After the test, the component shall comply with the requirements of the first paragraph of clause 10.

11.7 Climatic sequence

The components shall be subjected to the following climatic sequence:

a) Dry heat, in accordance with [IEC 60068-2-2], Test Ba, at +85°C ± 2°C for 16 h;

b) damp heat, cyclic, in accordance with [IEC 60068-2-30], Test Db, first cycle, at 55°C/25°C, 93% relative humidity for 24 h;

c) cold, in accordance with [IEC 60068-2-1], Test Aa, at –40°C ± 3°C for 2 h;

d) damp heat, cyclic, in accordance with [IEC 60068-2-30], Test Db, remaining cycles: the single cycle is 55°C/25°C, 93% relative humidity, 24 h, that shall be repeated for 5 times.

NOTE – An interval of maximum 3 days is permitted between any of the tests in the period of climatic sequence, except that test b) shall be followed immediately by test c).

After completion of climatic sequence, the samples shall be allowed to recover in room temperature for 1 h～2 h.

After the test, the component shall comply with the requirements of the first paragraph of clause 10.

11.8 Damp heat, steady state

Tested in accordance with [IEC 60068-2-78], Test Ca, with the following details:

a) Tested at +40°C, (90-95)% relative humidity for 500 h.

b) After completion of the damp heat test, the samples shall be allowed to recover in room temperature for 1 h to 2 h.

After the test, the component shall comply with the requirements of the first paragraph of clause 10.

11.9 Fire hazard

The component shall be subjected to the needle flame test of [IEC 60695-11-5]. The needle flame application shall be on the side surface of the samples for 5 s. The burning of the sample shall be self-extinguishable within 30 s after removing the needle flame.

11.10 Solvent resistance of marking

Tested in accordance with [IEC 60068-2-45], Test XA with the following details:

a) Solvent to be used: see clause 3.1.1 of [IEC 60068-2-45].

b) Solvent temperature: 23°C ± 5°C

c) Conditioning: Method 1 (with rubbing)

d) Rubbing material: Cotton wool.

After the test, the marking shall be legible.

11.11 Component solvent resistance

Tested in accordance with [IEC 60068-2-45], Test XA with the following details:

a) Solvent to be used: see clause 3.1.1 of [IEC 60068-2-45]

b) Solvent temperature: 23°C ± 5°C

c) Conditioning: Method 2 (without rubbing)

d) Recovery time: 4 h

e) Post-test inspection.

After the test, the component shall comply with the requirements of the first paragraph of clause 10.

12 Identification

12.1 Marking

Legible and permanent marking shall be applied to the component, as necessary, to ensure that the user can determine the following information by inspection:

a) manufacturer

b) year of manufacture

c) component number or code.

If requested and agreed, the customer's identification should be marked on each component.

12.2 Documentation

Documents shall be provided to the user so that from the information in clause 12.1, the user can determine the following additional information:

a) full component parameters as set out in this Recommendation

b) component mounting requirements and process.

13 Ordering information

The following information should be supplied by the user:

a) drawing giving all dimensions, finishes and termination details

b) type or model

c) quantity

d) quality assurance requirements.

Bibliography

[b-ITU-T K.12] Recommendation ITU-T K.12 (2006), *Characteristics of gas discharge tubes for the protection of telecommunications installations*.

[b-ITU-T K.20] Recommendation ITU-T K.20 (2008), *Resistibility of telecommunication equipment installed in a telecommunications centre to overvoltages and overcurrents*.

[b-ITU-T K.21] Recommendation ITU-T K.21 (2008), *Resistibility of telecommunication equipment installed in customer premises to overvoltages and overcurrents*.

[b-ITU-T K.28] Recommendation ITU-T K.28 (1993), *Characteristics of semi-conductor arrester assemblies for the protection of telecommunications installations*.

[b-ITU-T K.44] Recommendation ITU-T K.44 (2008), *Resistibility tests for telecommunication equipment exposed to overvoltages and overcurrents – Basic Recommendation*.

[b-ITU-T K.45] Recommendation ITU-T K.45 (2008), *Resistibility of telecommunication equipment installed in the access and trunk networks to overvoltages and overcurrents*.

[b-ITU-T K.95] Recommendation ITU-T K.95 (2014): *Surge parameters of isolating transformers used in telecommunication devices and equipment*.

[b-IEC 60617] IEC 60617, *Graphical symbols for diagrams*. On-line database: http://std.iec.ch/iec60617.

[b-IEC 60721-3-3] IEC 60721-3-3 ed2.0 (1994-12), *Classification of environmental conditions – Part 3: Classification of groups of environmental parameters and their severities – Section 3: Stationary use at weatherprotected locations*.

[b-IEC 60721-3-9] IEC 60721-3-9 ed1.0 (1993-07), *Classification of environmental conditions – Part 3: Classification of groups of environmental parameters and their severities – Section 9: Microclimates inside products*.

[b-IEC 60747-1] IEC 60747-1 ed2.1 (2010-08), *Semiconductor devices – Part 1: General*.

[b-IEC 60747-2] IEC 60747-2 ed2.0 (2000-03), *Semiconductor devices – Discrete devices and integrated circuits – Part 2: Rectifier diodes*.

[b-IEC 60747-6] IEC 60747-6 ed2.0 (2000-12), *Semiconductor devices – Part 6: Thyristors*.

[b-IEC 60749-1] IEC 60749-1 ed1.0 (2002-08), *Semiconductor devices – Mechanical and climatic test methods – Part 1: General*.

[b-IEC 60749-20-1] IEC 60749-20-1 ed1.0 (2009-04), *Semiconductor devices – Mechanical and climatic test methods – Part 20-1: Handling, packing, labelling and shipping of surface-mount devices sensitive to the combined effect of moisture and soldering heat*.

[b-IEC 61188-5-1] IEC 61188-5-1 ed1.0 (2002-07), *Printed boards and printed board assemblies – Design and use – Part 5-1: Attachment (land/joint) considerations – Generic requirements*.

[b-IEC 61643-341] IEC 61643-341 ed1.0 (2001-11), *Components for low-voltage surge protective devices – Part 341: Specification for thyristor surge suppressors (TSS)*.

[b-IEC 61760-1] IEC 61760-1, ed2.0 (2006-04), *Surface mounting technology – Part 1: Standard method for the specification of surface mounting components (SMDs)*.

[b- IEC 62590] IEC 62590, ed1.0 (2010-06), *Railway applications – Fixed installations – Electronic power converters for substations*.

[b-IEV 521-04] IEV 521-04: *Types of semiconductor devices*, Part of IEC database related to semiconductor devices and integrated circuits, http://www.electropedia.org/iev/iev.nsf/index?openform&part=521

[b-IEV 521-05] IEV 521-05: *General terms for semiconductor devices*, Part of IEC database related to semiconductor devices and integrated circuits, http://www.electropedia.org/iev/iev.nsf/index?openform&part=521

[b-IEV 521-08] IEV 521-08: *Specific terms for thyristors*, Part of IEC database related to semiconductor devices and integrated circuits, http://www.electropedia.org/iev/iev.nsf/index?openform&part=521

SERIES OF ITU-T RECOMMENDATIONS

Series A	Organization of the work of ITU-T
Series D	General tariff principles
Series E	Overall network operation, telephone service, service operation and human factors
Series F	Non-telephone telecommunication services
Series G	Transmission systems and media, digital systems and networks
Series H	Audiovisual and multimedia systems
Series I	Integrated services digital network
Series J	Cable networks and transmission of television, sound programme and other multimedia signals
Series K	**Protection against interference**
Series L	Construction, installation and protection of cables and other elements of outside plant
Series M	Telecommunication management, including TMN and network maintenance
Series N	Maintenance: international sound programme and television transmission circuits
Series O	Specifications of measuring equipment
Series P	Terminals and subjective and objective assessment methods
Series Q	Switching and signalling
Series R	Telegraph transmission
Series S	Telegraph services terminal equipment
Series T	Terminals for telematic services
Series U	Telegraph switching
Series V	Data communication over the telephone network
Series X	Data networks, open system communications and security
Series Y	Global information infrastructure, Internet protocol aspects and next-generation networks
Series Z	Languages and general software aspects for telecommunication systems

Printed in Switzerland
Geneva, 2015