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Characteristics and ratings of solid-state, self-restoring overcurrent protectors for the protection of telecommunications installations

Recommendation ITU-T K.82

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Characteristics and ratings of solid-state, self-restoring overcurrent protectors for the protection of telecommunications installations

Summary

Recommendation ITU-T K.82 defines the basic requirements and parameters of solid-state, self-restoring overcurrent protectors (OCPs) for the protection of telecommunication installations (for example, exchange equipment, access equipment, telecommunication lines and subscriber or customer equipment).

This Recommendation should be used for the harmonization of existing or future specifications issued by solid-state, self-restoring overcurrent protector manufacturers, telecommunication equipment manufacturers, administrations or network operators.

History

Edition	Recommendation	Approval	Study Group
1.0	ITU-T K.82	2010-05-29	5

Keywords

CPTC, ECL, overcurrent protection, PPTC, PTC, self-restoring, surge protective component, surge protective device, thermistor.

FOREWORD

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Introduction

Unlike fuses and heat coils, self-restoring overcurrent protectors (OCPs) automatically reset after the end of the overcurrent condition without the need for manual intervention, generally after power is removed at the end of the overcurrent. All the OCPs covered are solid-state. Having no moving parts, these OCPs are at least four times more reliable than thermal circuit breakers and six times more reliable than mechanical disk switches.

The current reducing action is for the normally low (untripped) OCP resistance to transition to a very high tripped resistance value, which greatly reduces the circuit current flow. The positive temperature coefficient (PTC) thermistor OCPs transition is caused by the component body reaching a critical temperature. The body temperature rise is caused by the i^2R heating of the overcurrent flowing through the component. Being thermally operated, PTC thermistor OCPs generally do not operate for short duration lightning currents, but will operate for AC overcurrents caused by power faults. Electronic current limiter (ECL) OCPs operate on a preset current threshold level and will reduce both AC and lightning overcurrents. Under lightning surge conditions, both OCP types assist in the coordination function.

Many of the performance tests and values can be applied to the three types of OCP technology. Some tests are specific to OCP used in SPDs (surge protective devices) or in equipment connected to an SPD and others to OCPs used in equipment. Differences between technologies mean that some tests will be specific to a given technology.

Recommendation ITU-T K.82

Characteristics and ratings of solid-state, self-restoring overcurrent protectors for the protection of telecommunications installations

1 Scope

This Recommendation applies to 2-terminal, series connected, solid-state, self-restoring overcurrent protectors (OCPs) used in surge protective devices (SPDs) and telecommunications equipment. These OCPs are directly connected to a device or equipment port and provide overcurrent protection and coordination functions for telecommunications installations during lightning surges and AC power faults, in accordance with [b-ITU-T K.11]. The port test levels and criterion are defined by [ITU-T K.20], [ITU-T K.21] and [ITU-T K.45], as appropriate. [ITU-T K.44] supports these three equipment performance ITU-T Recommendations with test circuit details and application guidance.

This Recommendation provides the basic requirements, and parameter tests, for OCPs used in the protection of telecom installations. This Recommendation covers the following types of solid-state, self-restoring OCP:

a) polymer positive temperature coefficient (PPTC) thermistors;

b) ceramic positive temperature coefficient (CPTC) thermistors;

c) electronic current limiters (ECLs).

It does not deal with:

a) mountings and their effect on OCP performance, the test results only apply for the mounting method used for that test;

b) system signal performance such as insertion loss, see [b-ITU-T G.117];

c) mechanical dimensions;

d) RoHS requirements;

e) electrical overload;

f) quality assurance requirements, see [IEC 60738-1];

g) specific cases of user agreed and regional values.

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published. The reference to a document within this Recommendation does not give it, as a stand-alone document, the status of a Recommendation.

[ITU-T K.12] Recommendation ITU-T K.12 (2006), *Characteristics of gas discharge tubes for the protection of telecommunications installations*.

[ITU-T K.20] Recommendation ITU-T K.20 (2008), *Resistibility of telecommunication equipment installed in a telecommunications centre to overvoltages and overcurrents*.

[ITU-T K.21] Recommendation ITU-T K.21 (2008), *Resistibility of telecommunication equipment installed in customer premises to overvoltages and overcurrents*.

[ITU-T K.28] Recommendation ITU-T K.28 (1993), *Characteristics of semi-conductor arrester assemblies for the protection of telecommunications installations*.

[ITU-T K.44] Recommendation ITU-T K.44 (2008), *Resistibility tests for telecommunication equipment exposed to overvoltages and overcurrents – Basic Recommendation*.

[ITU-T K.45] Recommendation ITU-T K.45 (2008), *Resistibility of telecommunication equipment installed in the access and trunk networks to overvoltages and overcurrents*.

[IEC 60068-1] IEC 60068-1 (1988), *Environmental testing – Part 1: General and guidance, plus Amendment 1 (1992)*.

[IEC 60068-2-1] IEC 60068-2-1 (2007), *Environmental testing – Part 2-1: Tests – Test A: Cold*.

[IEC 60068-2-2] IEC 60068-2-2 (2007), *Environmental testing – Part 2-2: Tests – Test B: Dry heat*.

[IEC 60068-2-6] IEC 60068-2-6 (2007), *Environmental testing – Part 2-6: Tests – Test Fc: Vibration (sinusoidal)*.

[IEC 60068-2-13] IEC 60068-2-13 (1983), *Environmental testing – Part 2-13: Tests – Test M: Low air pressure*.

[IEC 60068-2-14] IEC 60068-2-14 (2009), *Environmental testing – Part 2-14: Tests – Test N: Change of temperature*.

[IEC 60068-2-20] IEC 60068-2-20 (2008), *Environmental testing – Part 2-20: Tests – Test T: Test methods for solderability and resistance to soldering heat of devices with leads*.

[IEC 60068-2-21] IEC 60068-2-21 (2006), *Environmental testing – Part 2-21: Tests – Test U: Robustness of terminations and integral mounting devices*.

[IEC 60068-2-27] IEC 60068-2-27 (2008), *Environmental testing – Part 2-27: Tests – Test Ea and guidance: Shock*.

[IEC 60068-2-29] IEC 60068-2-29 (1987), *Environmental testing – Part 2: Tests – Test Eb and guidance: Bump*.

[IEC 60068-2-30] IEC 60068-2-30 (2005), *Environmental testing – Part 2-30: Tests – Test Db: Damp heat, cyclic (12 h+12 h cycle)*.

[IEC 60068-2-45] IEC 60068-2-45 (1980), *Environmental testing – Part 2-45: Tests – Test XA and guidance: Immersion in cleaning solvents*.

[IEC 60068-2-54] IEC 60068-2-54 (2006), *Environmental testing – Part 2-54: Tests – Test Ta: Solderability testing of electronic components by the wetting balance method*.

[IEC 60068-2-58] IEC 60068-2-58 (2004), *Environmental testing – Part 2-58: Tests – Test Td: Test methods for solderability, resistance to dissolution of metallization and to soldering heat of surface mounting devices (SMD)*.

[IEC 60068-2-69] IEC 60068-2-69 (2007), *Environmental testing – Part 2-69: Tests – Test Te: Solderability testing of electronic components for surface mounting devices (SMD) by the wetting balance method*.

[IEC 60068-2-78] IEC 60068-2-78 (2001), *Environmental testing – Part 2-78: Tests – Test Cab: Damp heat, stead state*.

[IEC 60695-11-5] IEC 60695-11-5 (2004), *Fire hazard testing – Part 11-5: Test flames – Needle-flame test method – Apparatus, confirmatory test arrangement and guidance*.

[IEC 60738-1] IEC 60738-1 (2006), *Thermistors – Directly heated positive temperature coefficient – Part 1: Generic specification*.

3 Definitions

3.1 Terms defined elsewhere

This Recommendation uses the following terms defined elsewhere:

3.1.1 fault current, I_{fault} [b-IEC 62319-1]: Current used when measuring time-to-trip.

3.1.2 hold current, I_h [b-IEC 62319-1]: Maximum current at specified ambient temperature, which will not cause the trip event.

NOTE – Sometimes known as rated or non-tripping current.

3.1.3 maximum current AC, I_{max} [b-IEC 62319-1]: Value of current for the operating temperature range, which should not be exceeded.

3.1.4 maximum voltage AC, V_{max} [b-IEC 62319-1]: Maximum AC voltage that may be applied.

3.1.5 positive temperature coefficient thermistor [b-IEC 62319-1]: Thermistor that exhibits a very sharp increase in resistance over a narrow temperature range.

NOTE – In this Recommendation, the change of temperature that results in resistance increase is caused by the current flow through the PTC thermistor.

3.1.6 resistance 1 h after tripping (polymer PTC thermistor), R_1 [b-IEC 62319-1]: Resistance of a Polymer PTC thermistor 1 h after a trip event or 1 h after reflow for surface mounting devices.

NOTE – R_{1max} is the maximum allowed value of R_1.

3.1.7 time-to-trip, (PTC thermistor) t_{trip} [b-IEC 62319-1]: Under specified ambient conditions, starting from the time the fault current (I_{fault}) is applied, the time-to-trip is the time required for a device to transition into a tripped state.

NOTE – An OCP shall have passed into the tripped condition as indicated by the measured voltage exceeding 90% of the supply open-circuit voltage.

3.1.8 trip current, I_t [b-IEC 62319-1]: Lowest current which will cause a trip event at a specified temperature and within a time specified in the product specification.

3.1.9 trip event [b-IEC 62319-1]: Event of rapid increasing resistance in response to an overcurrent surge.

3.2 Terms defined in this Recommendation

This Recommendation defines the following terms:

3.2.1 electronic current limiter: A device based on transistor and related technology that automatically restricts the current amplitude when it exceeds a predetermined threshold level.

3.2.2 endurance test (life test) AC: Application of a specified number of trip events under specified temperature and trip cycle (on and off time) conditions.

NOTE – After the test, the product shall meet specified mechanical and electrical parameters.

3.2.3 endurance test (life test) impulse: Application of a specified number of impulses under specified temperature and impulse repetition rate conditions.

NOTE – After the test, the product shall meet specified mechanical and electrical parameters.

3.2.4 impulse generator charge voltage, V_C: Value of impulse generator charging voltage.

3.2.5 impulse resistance (ceramic PTC thermistor) R_{imp}: Quotient of the peak impulse voltage between the terminals by the peak impulse current through the PTC thermistor.

NOTE – Ceramic PTC thermistors are also voltage-dependent resistors and conduct higher currents (up to three times) under impulse conditions than predicted from the untripped resistance value.

3.2.6 impulse voltage, V_{imp}: Value of peak impulse voltage.

NOTE – V_{imp} is the impulse voltage across the OCP, not necessarily the impulse generator peak open-circuit voltage value.

3.2.7 regional values: AC test parameters to suit local conditions in accordance with the variations permitted in the ITU-T K-series Recommendations for equipment.

3.2.8 reset voltage (ECL), V_{reset}: Value of DC voltage at which there is a transition from a high-resistance tripped state to a low-resistance untripped state under specific test conditions.

3.2.9 resistance R: Untripped value of DC resistance measured at specified ambient temperature.

3.2.10 user agreed values: Test parameters and circuits agreed between major stakeholders (e.g., user and manufacturer) for a specific application.

4 Abbreviations, acronyms and symbols

This Recommendation uses the following abbreviations and acronyms:

CPTC Ceramic Positive Temperature Coefficient (thermistor)
DFN Dual Flat No leads
ECL Electronic Current Limiter
GDT Gas Discharge Tube
JEDEC Joint Electronic Device Engineering Council
OCP OverCurrent Protector
PPTC Polymer Positive Temperature Coefficient (thermistor)
PTC Positive Temperature Coefficient (thermistor)
QFN Quad Flat No leads
SIP Single In-line Package
SMD Surface Mounting Device
SPD Surge Protective Device

This Recommendation uses the following IEC 60617 graphical symbols for OCPs:

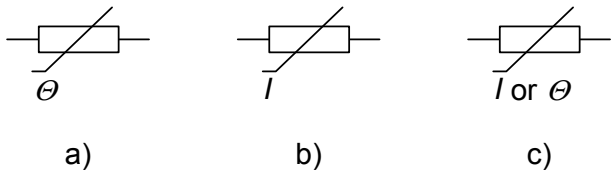


Figure 1 – Symbols for a) PTC thermistor, b) ECL and c) PTC thermistor or ECL

5 Storage conditions

OCPs shall be capable of withstanding the following conditions without damage:

– Temperature: –40°C to +70°C;

– Relative humidity: up to 95%.

Also see clause 8.7, Climatic sequence.

6 Electrical requirements

Following are the recommended values for OCPs. Suggested performance values relate to ITU-T K-series inherent protection requirements. All tests shall be run in accordance with the test procedures documented in clause 7.

6.1 resistance, *R*

This parameter is the untripped OCP resistance value with minimal self-heating, at specified ambient conditions.

6.1.1 Values

OCPs used in telecommunication applications have a typical resistance range of one ohm to fifty ohms. There are no preferred resistance values given, as the values appropriate for a given application are dependent on the signal performance requirements and the desired time-to-trip, see Table 1.

When the OCPs are provided as pairs, one in each wire of a twisted pair, an important characteristic is the resistance difference between the OCPs. For polymer PTC thermistors, the biggest resistance difference occurs after a trip event.

The test method is given in clause 7.1.

6.1.2 Criteria

The measured resistance value and, if necessary, the differential resistance value of a pair, shall be within the specified limits given in the product documentation.

6.2 hold current, I_h

This parameter defines the maximum current, which will not cause the trip event at specified ambient temperature.

6.2.1 Values

Example values of minimum hold current are listed in Table 1. The lowest value of hold current which occurs at the highest ambient temperature, see clause 9.1

The test method is given in clause 7.2.

6.2.2 Criteria

The OCP, conducting the specified I_h current value of the product documentation, shall not have tripped during the specified measurement time. This verifies that the tested component I_h is higher than the specified I_h value. For pairs of OCPs supplied as a single component, the test condition should be for both OCPs conducting current and neither OCP should trip.

6.3 trip current, I_t

This parameter defines the lowest current which will cause a trip event at a specified temperature and within a time specified in the product specification.

6.3.1 Values

Example values of trip current are listed in Table 1. Normally, the trip current value will be about twice the hold current value.

The test method is given in clause 7.3.

6.3.2 Criteria

The OCP, conducting the specified I_t current value of the product documentation, shall have tripped by the specified measurement time. This verifies that the tested component I_t is lower than the maximum value. For pairs of OCPs supplied as a single component, the measurement should be for the transverse condition with only a single OCP section conducting current.

6.4 time-to-trip, t_{trip}

The parameter defines the time taken from the start of the current flow for the OCP to transition into a tripped state.

The time-to-trip (t_{trip}) of a PTC thermistor is dependent on many factors such as: the resistance value (R), component thermal capacity, voltage rating (V_{max}), fault current (I_{fault}), hold current (I_h), ambient temperature to trip body temperature difference and component mounting. Manufacturers provide time-to-trip curves, see clause 9.2, to comprehend all these factors for an individual product. Because of all these factors, this clause does not define preferred time-to-trip values, instead some example values for OCP technologies are listed in Table 1. This table is not a definitive list of OCP technology capability.

Table 1 – Example values for OCP parameters (Note)

OCP type	Nominal resistance R (Ω)	Typical Time-to-trip @ I_{fault} = 1 A t_{trip} (s)	Typical Time-to-trip @ I_{fault} = 3 A t_{trip} (s)	Hold current I_h (A)	Trip current I_t (A)	AC voltage rating V_{ACmax} (V rms)
CPTC thermistor	50	0.8		0.09	0.19	245
	35	1.1		0.11	0.23	245
	25	1.5		0.13	0.26	245
	10	3.8		0.18	0.36	245
PPTC thermistor	10	7.5		0.160	0.32	600
	8	1.5		0.12	0.24	250
	2	10	0.6	0.18	0.65	250
	1.2	60	4	0.4	1.0	600
ECL	5-50	$< 1 \times 10^{-5}$	$< 1 \times 10^{-5}$	< 0.5	> 0.05	300
NOTE – An OCP may be tested to alternative values to ascertain maximum ratings or validate a product specification.						

6.4.1 Values

Example values of time-to-trip are listed in Table 1. A single point benchmark of the time-to-trip shall be done at a fault current of 1 A. If the typical time-to-trip is longer than 10 s at 1 A, then a higher fault current of 3 A shall be used.

The test method is given in clause 7.4. This test method is only for fault current values of 3 A or less. For characterizing the time-to-trip at higher fault currents circuits based on the AC power, fault testing should be used.

6.4.2 Criteria

The measured time-to-trip value shall be less than or equal to the specified value(s) given in the product documentation. For pairs of OCPs supplied as a single component, the measurement should be for the transverse condition with a single OCP carrying the fault current.

6.5 resistance 1 h after tripping, R_1 for polymer PTC thermistors

This parameter is only applicable to PPTC thermistors. PPTC thermistors show a large increase in resistance immediately after a trip event (trip jump) or reflow soldering. Thereafter, the resistance shows an exponential-like decrease with time towards the initial resistance value. Manufacturers sometimes provide typical resistance recovery curves, see clause 9.3.

6.5.1 Values

The preferred ratio of the maximum resistance 1 h after tripping, R_{1max}, to the maximum pre-trip resistance, R_{max}, is in the range of 1.3 to 2.3. Although the average ratio over all the resistance range is 1.7, generally the ratio decreases with higher values of maximum pre-trip resistance, R_{max}.

The test method is given in clause 7.5.

6.5.2 Criterion

The measured R_1 resistance shall be less than or equal to the R_{1max} value given in the product documentation.

6.6 reset voltage, V_{reset} for ECL

This parameter is only applicable to ECLs in DC line powered applications. The value of V_{reset} is the maximum value of DC voltage at which there is a transition from a high-resistance tripped state to a low-resistance untripped state under specific test conditions.

6.6.1 Values

Table 2 lists the preferred values of DC powering voltage used in [ITU-T K.12] for GDT holdover testing.

Table 2 – Preferred DC powering voltage and component values for Figure 5

Test #	DC powering voltage V_{DC} (V)	Hold current I_h (A)	Max. impulse voltage V_{imp} (V)
1	52	Selected value from clause 6.2	Whichever is the greatest value of clause 6.9
2	80		
3	135		
4	User agreed		
Figure 5 Circuit values	PS1 set to V_{DC}	R2 = V_{DC}/I_h	R1 = $V_{imp}/5$

The test method is given in clause 7.6.

6.6.2 Criterion

The ECL shall return to its conducting state after the test in clause 7.6 is applied using the specified DC powering voltage.

6.7 impulse resistance, R_{imp} for ceramic PTC thermistors

Ceramic PTC thermistors are also voltage-dependent resistors (VDRs). The effective ceramic PTC thermistor resistance decreases at high voltages. Under impulse conditions, the resistance can drop by nearly 70% allowing three times more current to flow than might be expected.

This parameter is measured under 10/700 generator impulse conditions.

6.7.1 Values

The values of 10/700 generator charging voltage used for the measurement are 1 kV and 1.5 kV (as in [ITU-T K.20], [ITU-T K.21] and [ITU-T K.45]) although other voltage levels may be appropriate for a given application.

The test method is given in clause 7.7.

6.7.2 Criteria

The calculated R_{imp} value shall not be less than or equal to the value(s) given in the product documentation for a specified test mode. No flashover or damage to the CPTC thermistor shall occur during the impulse test.

6.8 Impulse voltage withstand

This parameter is the maximum 10/700 impulse voltage that the OCP can withstand without failure.

6.8.1 Values

The values of 10/700 generator charging voltage are 1.0 kV and 1.5 kV (as in [ITU-T K.20], [ITU-T K.21] and [ITU-T K.45]) although other voltage levels may be applicable to a given application. The test method is given in clause 7.8.

6.8.2 Criteria

The measured post-test resistance value for all the modes tested and, if necessary, the differential resistance value of a pair shall be within the limits given in the product documentation. No flashover or damage to the OCP shall occur during the testing.

6.9 AC power fault

The OCP performance is verified for a range of AC power fault levels.

6.9.1 Values

The AC power fault generator values are listed below. (These values are for the non-primary AC power fault tests of [ITU-T K.20], [ITU-T K.21] and [ITU-T K.45].)

1) V_{AC} = 450 Vrms, R1, R2 = 200 Ω, t = 2 s;

2) V_{AC} = 600 Vrms, R1, R2 = 600 Ω t = 0.2 s;

3) V_{AC} = 230 Vrms, R1, R2 = 10 Ω, 20 Ω, 40 Ω, 80 Ω, 160 Ω, 300 Ω, 600 Ω and 1000 Ω, t = 15 min.

AC power fault conditions may be adapted to the local AC supply values, by variation of the test parameters, and may be adapted for a given application.

The test methods are given in clause 7.9.

6.9.2 Criteria

The measured OCP post-test resistance value and, if necessary, the differential resistance value of a pair, shall be within the specification limits given in the product documentation. When a trip event occurs, the R_1 resistance values shall be used for polymer PTC thermistors.

6.10 Impulse endurance test (life test)

This parameter is optional. The OCP performance is verified under the impulse voltage withstand conditions of clause 6.8, but with the number of impulses increased from 10 to 100.

6.10.1 Values

The test levels of clause 6.8 shall be used.

The test method is given in clause 7.10.

6.10.2 Criteria

The measured post-test resistance value for all the modes tested and, if necessary, the differential resistance value of a pair shall be within the specified limits given in the product documentation. No flashover or damage to the OCP shall occur during the testing.

6.11 AC endurance test (PTC thermistor) (life test)

This parameter is optional. The PTC thermistor performance is verified for 100 trip events under AC power fault conditions.

6.11.1 Values

Table 3 shows the preferred circuit values used for PTC thermistor testing.

Table 3 – Preferred test level values for PTC thermistor AC endurance

Test #	AC source voltage, V_{AC} (Vrms)	Short-circuit AC (Arms) (Note)	Current limit resistors, R1 & R2 (Ω)	Application timing On time/Off time (s/s)	Number of applications
1	120	$5I_h$	$24/I_h$	10/50	100
2	≥ 230	$5I_h$	$46/I_h$	10/50	100
3	User agreed	User agreed	User agreed	User agreed	User agreed
NOTE – To trip a device in less than 10 s, a current greater than $5I_h$ might be required.					

The test methods are given in clause 7.11.

6.11.2 Criteria

The measured post-test resistance value and, if necessary, the differential resistance value of a pair, shall be within the specified limits given in the product documentation. An R_1 resistance measurement shall be used for polymer PTC thermistors.

7 Test methods

For these tests, the OCP should be mounted as detailed in the product documentation. In the absence of manufacturer specific mounting recommendations, the mounting Recommendations of [IEC 60738-1] should be used. The mounting method shown in [IEC 60738-1], Figure B.2 will apply for components with wire terminations. The mounting method shown in [IEC 60738-1], Figure B.3 will apply for surface mount components.

Unless otherwise specified, all tests shall be carried out under standard atmospheric conditions for testing as given in clause 5.3 of [IEC 60068-1]:

- temperature 15°C to 35°C;
- relative humidity 25% to 75%;
- air pressure 86 kPa to 106 kPa.

Many test circuits are designed to test two OCPs simultaneously. This allows integrated components containing two OCPs to be correctly tested for the longitudinal condition. For single OCPs, the circuits allow two to be tested at once.

7.1 resistance, *R*

The resistance shall be measured when the component is in thermal equilibrium at the atmospheric conditions given in the product documentation. The default standard atmospheric conditions are given in clause 7. Components mounted by reflow soldering shall be measured 24 h or more after soldering.

Resistance measurement shall be made without any appreciable self-heating of the component ([IEC 60738-1], clause 7.5 Zero-power resistance), using low-current resistance measuring equipment such as a digital meter.

The measuring method shall be such that:

- the error does not exceed 10% of the resistance tolerance;
- the error does not exceed 10% of the specified maximum difference resistance of paired OCPs.

7.2 hold current, I_h

The OCP shall be connected and enclosed in a chamber as in Figure 2. The chamber temperature is adjusted to the value given for this test in the product documentation and the air allowed to become stationary.

The OCPs are connected to constant current supplies set to the I_h value in the product documentation. The maximum open-circuit voltage of a supply shall not exceed 50 V. The voltage across each OCP is measured and recorded at the time given in the product documentation. If no time is specified, the default test time is 30 minutes. For ECLs, the default time is 200 s. Bidirectional ECLs are to be tested twice, once in each polarity as they are not necessarily symmetrical in I_h value.

An OCP shall have passed into the tripped condition, as indicated by the measured voltage exceeding 90% of the supply open-circuit voltage.

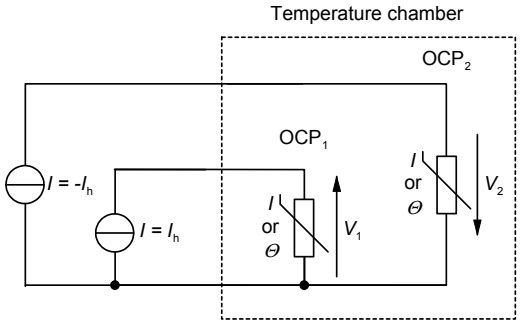


Figure 2 – Test arrangement for verifying minimum I_h

7.3 trip current, I_t

The OCPs shall be connected and enclosed in a chamber as in Figure 3. The chamber temperature is adjusted to the value given for this test in the product documentation and the air allowed to become stationary.

The OCPs are connected to constant current supplies set to the I_t value in the product documentation. For PTC thermistors, the maximum open-circuit voltage of a supply shall not exceed 50 V. To prevent instability, the maximum open-circuit voltage of a supply for ECLs shall

not be less than the maximum value of reset voltage. The voltage across each OCP is measured and recorded at the time given in the product documentation. If no time is specified, the default test time shall be 30 minutes; if tripping occurs the test may be terminated. For ECLs, the default time is 2 s. Bidirectional ECLs are to be tested twice, once in each polarity as they are not necessarily symmetrical in I_t value.

An OCP shall have passed into the tripped condition, as indicated by the measured voltage exceeding 90% of the supply open-circuit voltage.

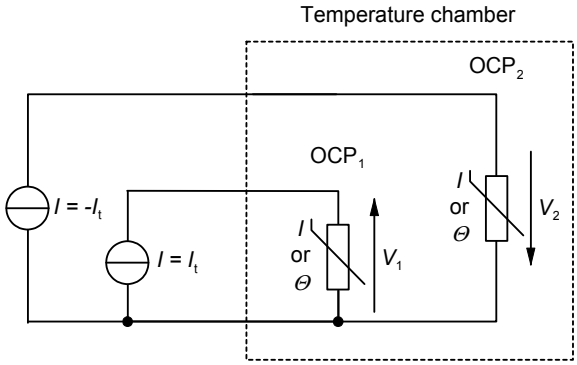


Figure 3 – Test arrangement for verifying maximum I_t

7.4 time-to-trip, t_{trip}

The thermistors shall be connected and enclosed in a chamber as in Figure 4. The chamber temperature is adjusted to the value given for this test in the product documentation and the air allowed to become stationary.

The OCPs are connected to constant current supplies set to the fault current, I_{fault}, value in the product documentation. For PTC thermistors the maximum open-circuit voltage of a supply shall not exceed 50 V. The current sources should reach 90% of the fault current value within 1 ms of the test start.

The OCP voltage shall be measured. An OCP shall have passed into the tripped condition as indicated by the measured voltage exceeding 90% of the supply open-circuit voltage.

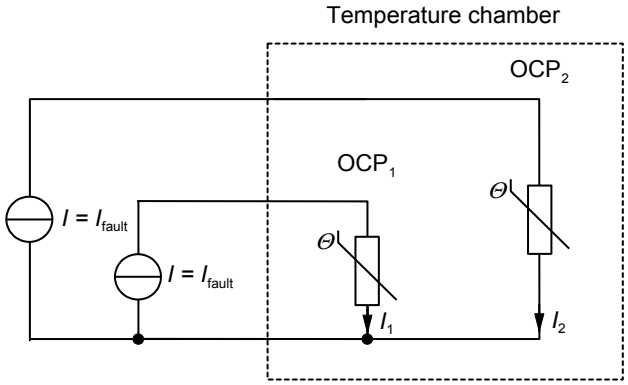


Figure 4 – Test arrangement for measuring PTC thermistors time-to-trip

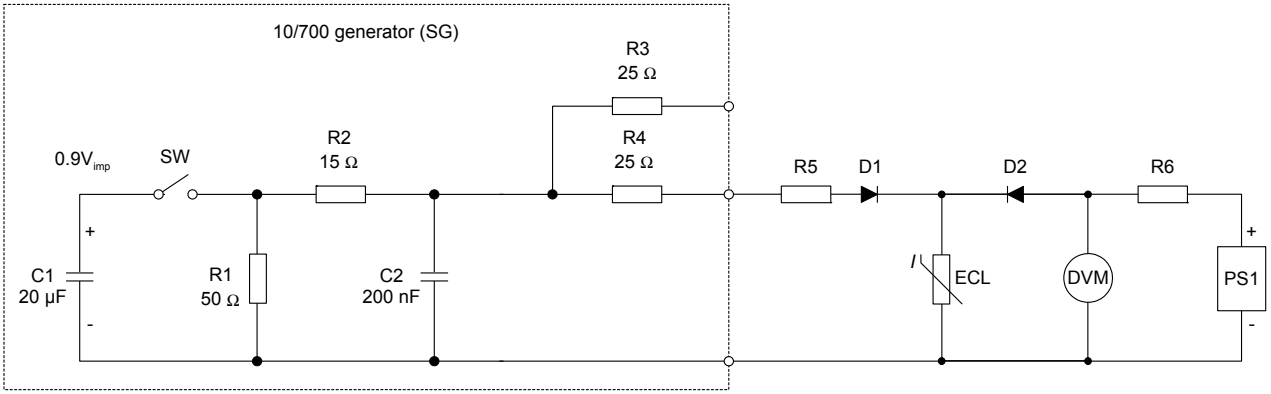
7.5 resistance 1 h after tripping, R_1, for polymer PTC thermistor

This test measures the thermistor resistance one hour after a trip event at specified ambient conditions.

After a test that causes a trip event and the post resistance needs to be measured, the tested component shall be placed in the specified ambient used for resistance measurement to reach thermal equilibrium. After the trip event, a period of not less than 1 hour shall elapse before the resistance of the polymer PTC thermistor is measured as described in clause 7.1.

7.6 reset voltage, V_{reset} for ECL

Testing shall be done using the circuit of Figure 5. Values of PS1, R2, and R3 shall be selected for each test condition from Table 2. Prior to applying the impulse, the digital voltmeter indicates the sum of the conducting ECL and diode D2 voltages. Applying the impulse causes conduction of diode, D1, which trips the ECL and pulls the ECL voltage up to 0.9 V_{imp}. As the impulse voltage decays, diode D2 will stop conducting as the impulse voltage falls below the voltage setting of power supply PS1. If the ECL has a reset voltage equal to or higher than the voltage setting of power supply PS1, the ECL conduction will result in a similar voltage reading to that before the impulse. This indicates the ECL has reset. If the digital voltmeter reading is similar to the voltage setting of power supply PS1, then the ECL has not reset. As bidirectional ECLs are not necessarily symmetrical in reset voltage, each is tested twice, once connected in one direction and once in the reverse connection.



D1	Impulse generator isolation diode
D2	DC supply isolation diode
ECL	ECL under test
DVM	Digital voltage meter
PS1	Constant voltage DC supply, set to line powering voltage V_{DC}
R1	Impulse current limiting resistor, R5 = $V_{imp}/5$
R2	DC supply current limiting resistor, R6 = V_{DC}/I_h
SG	10/700 impulse (surge) generator, charging voltage set to 0.9 V_{imp}

Figure 5 – Circuit for ECL V_{reset} verification (based on Figure 4)

7.7 impulse resistance, R_{imp} at V_{imp} for ceramic PTC thermistors

The ceramic PTC thermistors shall be tested in the circuit of Figure 6 using the generator settings of clause 6.7.1.

Five test impulses of the correct level shall be applied with a period of not less than one minute between impulses. The component current shall be monitored to detect any occurrence of flashover during the impulse causing higher than normal current. The R_{imp} values are calculated by dividing the maximum measured OCP voltage (V_1 and V_2) by the maximum measured OCP current (I_1 and I_2). The reported value for each component shall be the lowest calculated value of R_{imp} for the five impulses.

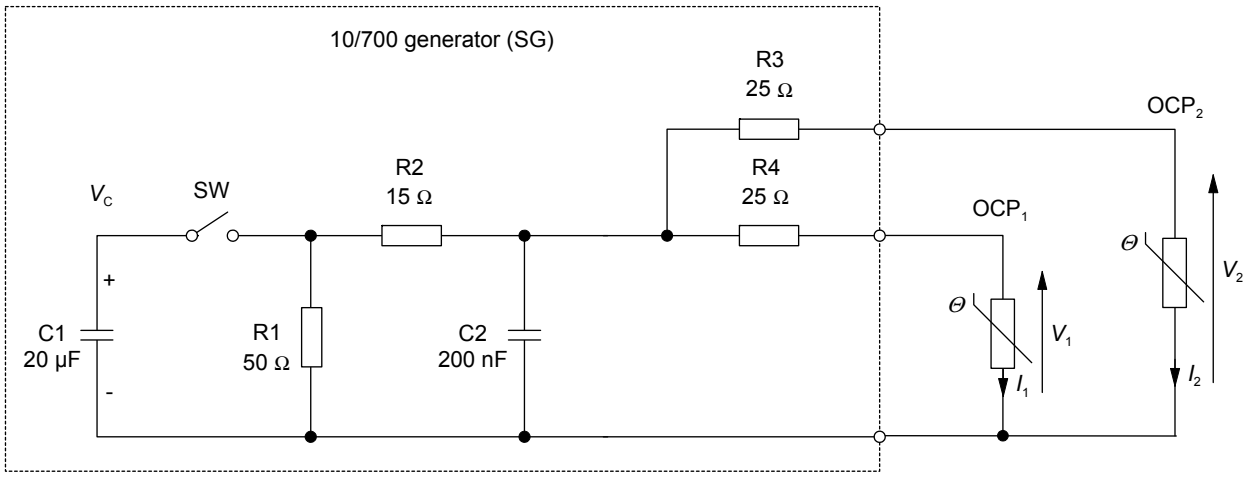


Figure 6 – Circuit for measurement of V_{imp} (V_1 and V_2) and I_{imp} (I_1 and I_2) to calculate R_{imp} (V_1/I_1 and V_2/I_2)

7.8 Impulse voltage withstand

Figure 7 shows the circuit used for impulse testing OCPs.

The generator charge voltage, V_C, is set to a selected value from clause 6.8.1. To make the values of measured maximum voltage, V_1 and V_2, reasonably equal, the resistance values of the OCP pairs tested should be within 10% of each other. Ten test impulses of the correct level and alternating polarity shall be applied with a period of not less than one minute between impulses. The component current (I_1 and I_2) shall be monitored to detect any occurrence of flashover during the impulse causing higher than normal current. The component voltage (V_1 and V_2) shall also be monitored to detect any occurrence of flashover and record the maximum value of component voltage, V_{imp}.

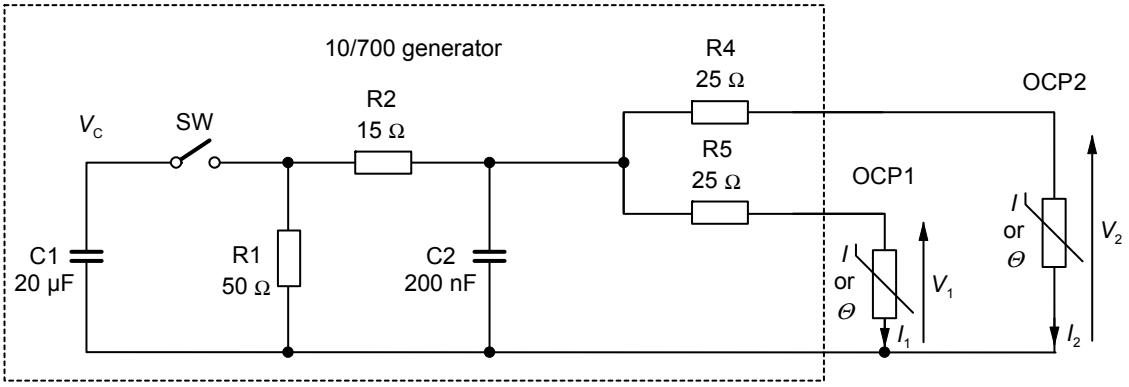


Figure 7 – Equipment impulse withstand test circuit

7.9 AC power fault tests

Figure 8 shows the circuit used for AC testing OCPs in equipment.

The generator voltage, V_{AC}, source resistance, R1 and R2, and test time, t, shall be set to the defined values. The tests are applied five times to each component. Fresh parts may be used for each voltage/resistance combination used. The component voltages (V_1 and V_2) and currents (I_1 and I_2) shall be monitored to detect any occurrence of flashover and trip events. The components shall be visually monitored during the test for any hazardous event and inspected after the test for any potentially hazardous condition that implies failure.

The rapid operation of an ECL may cause damaging voltage spikes and use of a voltage limiter may be necessary to limit the peak spike voltage to below V_{imp} of the ECL.

In all cases, the post test resistance (R_1 for polymer PTC thermistors) shall be measured as described in clause 7.1 or 7.5.

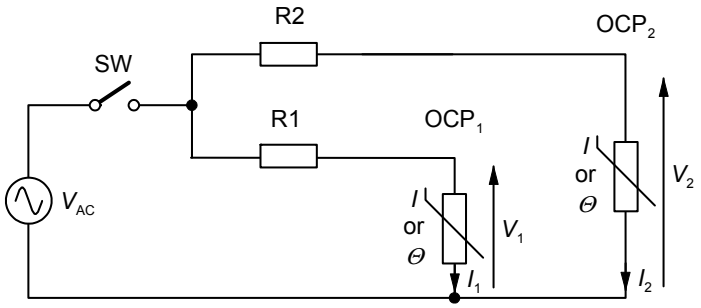


Figure 8 – Equipment power fault test circuit

7.10 Impulse endurance test (life test)

The test procedures of clause 7.8, impulse voltage withstand, shall be followed, with the exception that the number of impulses applied are increased from 10 to 100.

7.11 AC endurance test (life test)

The set-up of Figure 8 is used for AC endurance testing. The circuit values are given in Table 4. For testing large numbers of devices, switch SW can be made into a six-position rotary switch incrementing every 10 s. By having six separate resistor and OCP load circuits, twelve OCPs can be cycled every 60 s.

8 Environment tests

Prior to and after the following tests, measure the OCP resistance, and verify impulse voltage rating. Any change in value compared with that measured initially shall be recorded and the value after test shall stay within defined limits. Visual examinations shall show no evidence of damage, and the marking shall be legible.

8.1 Robustness of terminations

8.1.1 Wire terminations robustness

OCPs with wire terminations shall be subjected to Tests U_{a1} and U_b of [IEC 60068-2-21] with the following details:

a) Test U_{a1} – Tensile

The force applied shall be 10N for wire diameter 0.6 mm and 0.8 mm, or 20N for wire diameter 1 mm for 1 min.

b) Test U_b – Bending.

Two consecutive bends shall be applied in each direction.

8.1.2 SMD termination robustness

OCP in two-terminal SMD resistor type packaging shall be subjected to the following test. OCP in multi-chip or multi-terminal packaging (DFN, QFN, SIP, etc.) should be tested in accordance with the relevant JEDEC or alternative standards.

a) Force application test

Surface mount OCPs shall be soldered on the substrate using the method prescribed by the manufacturer, as given in Figure 9. The dimensions of the substrate are as shown in Table 4 and Figure 9. A force specified in Table 5 shall be smoothly applied on the sample for 5 s ± 1 s.

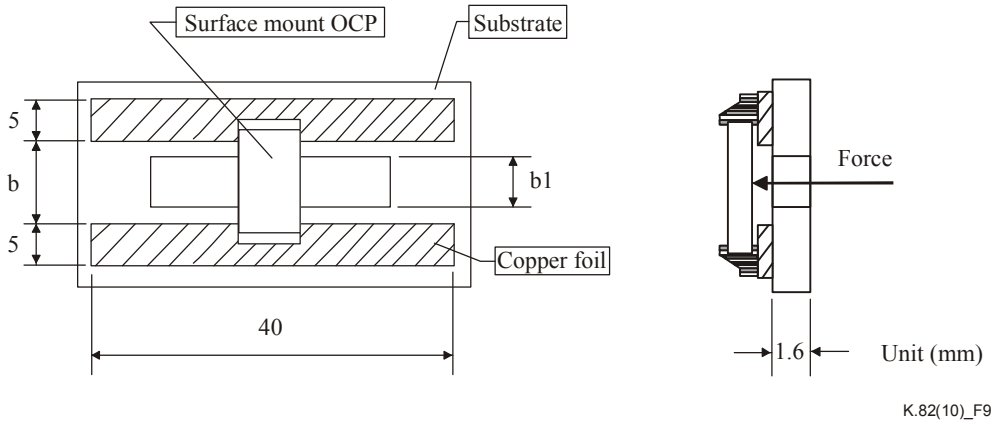


Figure 9 – Test arrangement for surface mount terminations

b) Test U_e of [IEC 60068-2-21]

Bend the substrate by 2 mm for 10 times. After the test, the OCP shall comply with the requirements of clause 8.

Table 4 – Force and dimensions of the substrate

Surface mount device type	1005 (0402)	1608 (0603)	2012 (0805)	3210 (1206)	3225 (1210)	4532 (1812)	5750 (2220)
Force P, N	5	5	10	10	10	15	15
Dimension *b*, mm	0.5	1.0	1.2	2.2	2.2	3.2	4.0
Dimension b_1, mm	0.5	1.0	1.0	1.0	1.0	1.0	1.5

8.2 Solderability

8.2.1 Wire leaded solderability

Tested in accordance with [IEC 60068-2-54], Test Ta, method 1 (solder bath), with the following details:

Depth of immersion (from component body): 2 mm for wire terminations. A thermal insulating screen of 1.5 mm ± 0.5 mm thickness shall be used for wire terminations.

Time of immersion:	2s ± 0.5 s	
Temperature of the solder bath:	235°C ± 5°C,	for P_b-Sn solder
	260°C ± 5°C,	for lead-free solder

Visual examination shall show free flowing of the solder with the wetted area of terminations not less than 80%. A magnifier capable of giving a magnification of (4~10) times may be used when visual examination is carried out.

8.2.2 SMD type solderability

Tested in accordance with [IEC 60068-2-58], Test Td with the following details:

Time of soldering: 4 s ± 1 s

Recovery time: 24 h ± 2 h

Visual examination shall show free flowing of the solder with the wetted area of terminations not less than 80%. A magnifier capable of giving a magnification of (4~10) times may be used when visual examination is carried out.

8.3 Resistance to soldering heat

8.3.1 Disc type resistance to soldering heat

Tested in accordance with [IEC 60068-2-20], Test Tb, method 1 (solder bath), with the following details:

- Depth of immersion (from component body): 2 mm for wire terminations.
- Time of immersion: 5 s ± 0.5 s
- Temperature of the solder bath for P_b-Sn solder: 235°C ± 5K
- Temperature of the solder bath for lead-free solder: 260°C ± 5K

After recovery for 1 h, the OCP shall comply with the requirements of clause 8.

8.3.2 SMD type resistance to soldering heat

Tested in accordance with [IEC 60068-2-58], Test Td with the following details:

- Time of soldering: 10 s ± 1 s
- Recovery time: 24 h ± 2 h

After recovery for 24 h, the OCP shall comply with the requirements of clause 8. A magnifier capable of giving a magnification of (4~10) times may be used when visual examination is carried out.

8.4 Vibration

Tested in accordance with [IEC 60068-2-6], Test Fc, Method B4, with the following details:

- Frequency of sine wave: 10 Hz~55 Hz for 10 cycles
- Acceleration: 98 m/s^2, or Amplitude: 0.75 mm, whichever is the less severe vibration
- Duration: 6 h (2 h for each axis)

After the test, the OCP shall comply with the requirements of clause 8.

8.5 Bump

Tested in accordance with [IEC 60068-2-29], Test Eb with the following details:

- Pulse: half sine, duration 6 ms
- Maximum acceleration: 400 m/s^2
- Number of bumps: 4000

After the test, the OCP shall comply with the requirements of clause 8.

8.6 Rapid changes of temperature

Tested in accordance with [IEC 60068-2-14], Test Na with the following details (Table 5):

The temperature cycle shall be repeated for 5 times as below:

Table 5 – Temperature cycle details

Step	Temperature	Period
1	–40°C ± 3 K	(30 ± 3) min
2	(transition time)	< 10 s
3	+85°C ± 2 K	(30 ± 3) min
4	(transition time)	< 10 s

After completion of 5 cycles, the samples shall be allowed to recover in room temperature for 1 h～2 h.

After the test, the OCP shall comply with the requirements of clause 8.

8.7 Climatic sequence

The OCPs shall be subjected to the following climatic sequence:

a) Dry heat, in accordance with [IEC 60068-2-2], Test Ba, at +85°C ± 2K for 16 h;

b) Damp heat, cyclic, in accordance with [IEC 60068-2-30], Test Db, first cycle, at 55°C/25°C, 93% relative humidity for 24 h;

c) Cold, in accordance with [IEC 60068-2-1], Test Aa, at –40°C ± 3K for 2 h;

d) Damp heat, cyclic, in accordance with [IEC 60068-2-30], Test Db, remaining cycles: the single cycle is 55°C/25°C, 93% relative humidity, 24 h, that shall be repeated for 5 times.

NOTE – An interval of maximum 3 days is permitted between any of the tests in the period of climatic sequence, except that Test b) shall be followed immediately by Test c).

After completion of climatic sequence, the samples shall be allowed to recover in room temperature for 1 h～2 h.

After the test, the OCP shall comply with the requirements of clause 8.

8.8 Damp heat, steady state

Tested in accordance with [IEC 60068-2-78], Test Ca, with the following details:

a) Tested at +40°C, (90-95)% relative humidity for 500 h.

b) After completion of the damp heat test, the samples shall be allowed to recover in room temperature for 1 h to 2 h.

After the test, the OCP shall comply with the requirements of clause 8.

8.9 Fire hazard

The OCP shall be subjected to the needle flame test of [IEC 60695-11-5]. The needle flame application shall be on the side surface of the samples for 5 s. The burning of the sample shall be self-extinguishable within 30 s after removing the needle flame.

8.10 Solvent resistance of marking

Tested in accordance with [IEC 60068-2-45], Test XA with the following details:

a) Solvent to be used: see clause 3.1.1 of [IEC 60068-2-45].

b) Solvent temperature: 23°C ± 5K

c) Conditioning: Method 1 (with rubbing)

d) Rubbing material: Cotton wool

After the test, the marking shall be legible.

8.11 Component solvent resistance

Tested in accordance with [IEC 60068-2-45], Test XA with the following details:

a) Solvent to be used: see clause 3.1.1 of [IEC 60068-2-45]

b) Solvent temperature: 23°C ± 5 K

c) Conditioning: Method 2 (without rubbing)

d) Recovery time: 4 h

e) Post-test inspection

After the test, the OCP shall comply with the requirements of clause 8.

9 Informative characteristics

For some characteristic values, it is useful to have a general idea of how they vary over a wide range of conditions. Although not a product guarantee, many manufacturers provide details of the generic variation of some characteristics.

9.1 Hold current variation with temperature

The hold current of all technologies decreases with increasing ambient temperature. The manufacturer should provide the designer with the device hold current variation with temperature. This information can be supplied as a graph or a table, as shown in Table 6. As a minimum, values for the nominal ambient and highest ambient values, typically 70°C or 85°C should be given.

Table 6 – Example of hold current variation with temperature

Temperature °C	–40	–20	0	25	40	60	70	85
Normalized I_h	1.70	1.40	1.21	1.00	0.86	0.66	0.55	0.39

9.2 Trip-time variation with fault current value for PTC thermistor OCPs

The trip-time of PTC thermistor OCPs has an inverse relationship with the prospective fault current. This information should be supplied and it is normally presented as a graphical curve at nominal ambient temperature, see Figure 10. Manufacturers may sometimes include other trip-time curves for the highest and lowest values of ambient temperature.

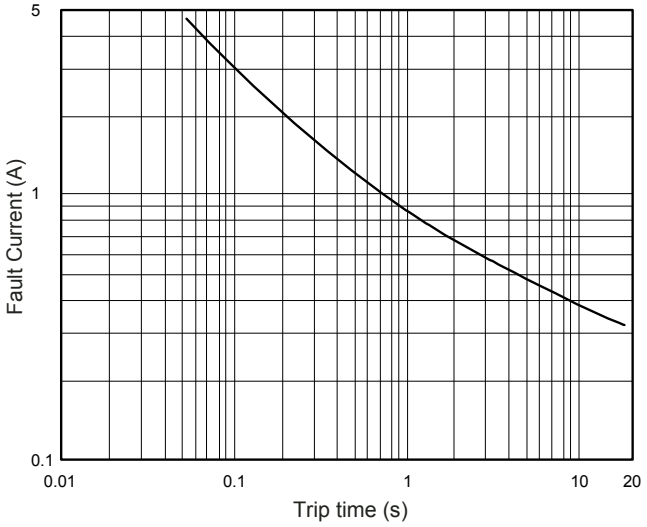


Figure 10 – Example of trip-time variation with fault current

9.3 Resistance recovery after a trip event for PPTC thermistor OCPs

Figure 11 shows an example of PPTC thermistor resistance recovery with time after a trip event. The pre-trip resistance, R, and R_{1max} are shown at the one-hour graph limit.

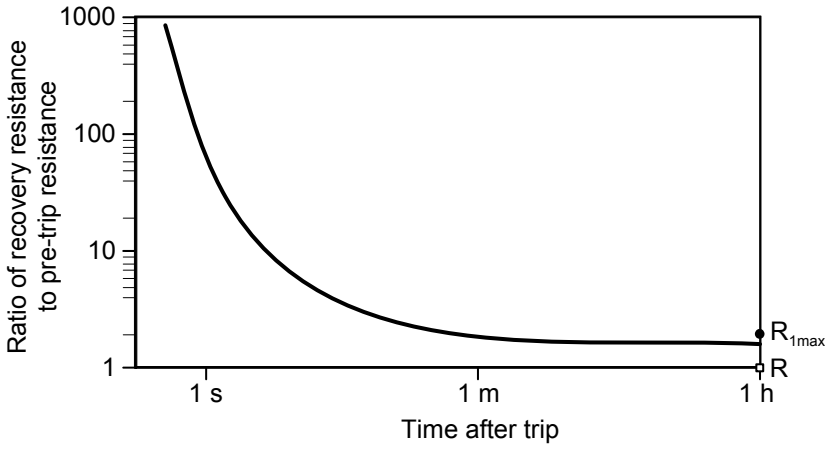


Figure 11 – Example of a PPTC thermistor resistance recovery after a trip event

10 Identification

10.1 Marking

Legible and permanent marking shall be applied to the OCP, as necessary, to ensure that the user can determine the following information by inspection:

a) manufacturer;

b) year of manufacture;

c) device number or code.

If requested and agreed, the customer's identification should be marked on each device.

10.2 Documentation

Documents shall be provided to the user so that from the information in clause 10.1, the user can determine the following additional information:

a) full device parameters as set out in this Recommendation;

b) component mounting requirements and process.

11 Ordering information

The following information should be supplied by the user:

a) drawing giving all dimensions, finishes and termination details;

b) type or model;

c) quantity;

d) quality assurance requirements.

Bibliography

[b-ITU-T G.117] Recommendation ITU-T G.117 (1996), *Transmission aspects of unbalance about earth*.

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[b-IEC 60060-2] IEC 60060-2 (1994), *High voltage test techniques – Part 2: Measuring systems*.

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[b-IEC 62319-1] IEC 62319-1 (2005), *Polymeric thermistors – Directly heated positive step function temperature coefficient – Part 1: generic specification*.

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