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SERIES L: ENVIRONMENT AND ICTS, CLIMATE CHANGE, E-WASTE, ENERGY EFFICIENCY; CONSTRUCTION, INSTALLATION AND PROTECTION OF CABLES AND OTHER ELEMENTS OF OUTSIDE PLANT

Examples of resource saving within the information and communication technology sector

ITU-T L-series Recommendations – Supplement 47

ITU-T L-SERIES RECOMMENDATIONS

ENVIRONMENT AND ICTS, CLIMATE CHANGE, E-WASTE, ENERGY EFFICIENCY; CONSTRUCTION, INSTALLATION AND PROTECTION OF CABLES AND OTHER ELEMENTS OF OUTSIDE PLANT

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Supplement 47 to ITU-T L-series Recommendations

Examples of resource saving within the information and communication technology sector

Summary

Supplement 47 to ITU-T L-series Recommendations provides various examples of resource saving in building systems, factories, plants, and home applications due to the progress of resource saving within the information and communications technology (ICT) sector. One example is the home network which uses the single-pair Ethernet (SPE) technology.

Another example is related to the semiconductor manufacturing technologies. Semiconductor dies (also known as chips) are currently mostly manufactured on disks (known as wafers) made of silicon, gallium arsenide or gallium nitride. These chips have a rectangular shape which lead to losses at the edge of the wafer. Bigger the die more important is the loss. Some techniques used in the current industries are also introduced for personal computers or server processors (CPU), and for graphics processing units (GPU) to reduce these losses.

To achieve sustainable growth under the constraints of the environment and resources, it is necessary to radically change conventional waste and recycling measures. Conventional waste countermeasures have mainly been recycling (reuse as a raw material), but in addition to this, reduction (control of waste generation) and reuse are also important.

Since twisted pair cables, such as 4-pairs of unshielded twisted pair (UTP) or shielded twisted pair (STP) cables, are mainly used in various local area networks (LANs), a large number of copper resources are still required to provide Internet services around the world. If fewer pairs can achieve the same communication performance as the 4-pair type, resource saving can be realized in the network.

History

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Keywords

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FOREWORD

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The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

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1 Scope

This Supplement provides various examples in building systems, factories, plants, and home applications due to the progress of resource savings within the information and communications technology (ICT) sector. With the development in the information and communication society, it is important to effectively use these resources and energy to provide information and communications technology (ICT) services. To achieve sustainable growth under the constraints of the environment and its resources, it is necessary to radically change conventional waste and recycling measures.

2 References

[ITU-T L.Sup.5]	ITU-T L-series Recommendations – Supplement 5 (2014), *Life-cycle management of ICT goods*.
[IEC 61156-11]	IEC 61156-11:2019, *Multicore and symmetrical pair/quad cables for digital communications – Part 11: Symmetrical single pair cables with transmission characteristics up to 600 MHz – Horizontal floor wiring – Sectional specification*.
[IEC 61156-13]	IEC 61156-13:2019, *Multicore and symmetrical pair/quad cables for digital communications – Part 13: Symmetrical single pair cables with transmission characteristics up to 20 MHz – Horizontal floor wiring – Sectional specification*.
[IEC 63171-6]	IEC 63171-6:2021, *Connectors for electrical and electronic equipment – Part 6: Detail specification for 2-way and 4-way (data/power), shielded, free and fixed connectors for power and data transmission with frequencies up to 600 MHz*.

3 Definitions

3.1 Terms defined elsewhere

This Supplement uses the following terms defined elsewhere:

3.1.1 reuse [b-EU WFD]: Operation by which products or parts that are not waste are used for the same purpose for which they were conceived by another user.

NOTE – The transfer of ownership is an essential part of the concept of reuse.

3.1.2 single pair Ethernet [b-IEEE 802.3]: Technology transmitting a signal using a single balanced twisted-pair of copper wires and associated power delivery.

3.2 Terms defined in this Supplement

This Supplement defines the following terms:

3.2.1 resource efficiency: Performance delivered per resources used.

NOTE – Not only controlling waste generation by promoting recycling and reuse at the stage of using ICT equipment and providing ICT services, but also the reduction of waste generation and the improvement of recyclability at the stage of developing and designing ICT equipment.

3.2.2 reduction: To reduce the amount of resources used when making products and to reduce the generation of waste. One of the efforts is to provide highly durable products and devise a maintenance system to extend the product life.

4 Abbreviations and acronyms

This Supplement uses the following abbreviations and acronyms:

ADP	Adapter
CCB	Cepi ContainerBoard
FEFCO	European Federation of Corrugated Board Manufacturers
HGW	Home Gateway
IoT	Internet of Things
ICT	Information and communications technology
JCMA	Japan Electric Wire & Cable Markers' Association
LAN	Local Area Network
LCA	Life Cycle Assessment
LCI	Life Cycle Inventory
ONU	Optical Network Unit
PVC	Polyvinyl Chloride
PBX	Private Branch Exchange
SPE	Single-Pair Ethernet
STP	Shielded Twisted Pair Cable
UTP	Unshielded Twisted Pair Cable

5 Conventions

None.

6 Examples of resource savings within the ICT sector

6.1 Resource saving by using single-pair Ethernet (SPE) technologies

Since twisted pair cables such as 4-pairs of unshielded twisted pairs (UTP) or shielded twisted pair (STP) cables are currently used in various local area networks (LANs), a large number of copper resources are still required to provide Internet services around the world. If fewer pairs can achieve the same communication performance as the 4-pair type, resource saving in the network can be realized. Clause 6.1.1 describes resource saving by using the single-pair Ethernet (SPE) technology.

6.1.1 Single-pair Ethernet technology

SPE technology has created a lot of new possibilities in the Internet of things (IoT). By transmitting a signal using a single balanced twisted pair of copper wires and its associated power delivery, various users can utilize the Ethernet communication with power supply for all systems.

The communication speed of SPE can support 10 Mbit/s to a maximum of 10 Gbit/s. The power supply capacity is DC48V with up to 50 W. This Ethernet capacity is the same as using a LAN cable.

Until now twisted pair cables, such as 4-pairs of unshielded twisted pair (UTP) or shielded twisted pair (STP) cables, are used in various local area networks (LANs). Since a twisted pair cable is comprised of bundling several pairs of insulated copper wires into a single cable, the 4-pair (8-wire) type of twisted pair cable uses four times as much copper as the single-pair (2-wire) type of cable.

Table 1 shows the typical specifications of the SPE unshielded twisted pair cable (UTP) and Ethernet (UTP, category 5) cables and Figures 1 and 2 show the appearance and cross-section of the SPE (UTP) and an Ethernet (UTP, Category 5) cable. Since the cross-sectional area of the SPE cable is a quarter of that of the Ethernet cable, the amount of copper used per unit length is reduced to a quarter (75% reduction). According to Table 1, replacing Ethernet (UTP) cables with SPE cables can save 11.25 grams of copper per meter. And in the case of 1 000 m, it can be reduced by 11.250 kg. According to Japan Electric Wire & Cable Markers' Association (JCMA), Japan's total conductor production of communication cables in 2020 was 15 015 tons and that of the power cables for equipment was 35 854 tons [b-JCMA], which implies that quite a large potential of conductor material reduction can be expected.

Figure 3 shows the comparison between the SPE connector and the LAN connector. The LAN connector is larger than the SPE because it uses a 4-pair cable, and the SPE can reduce the connector size.

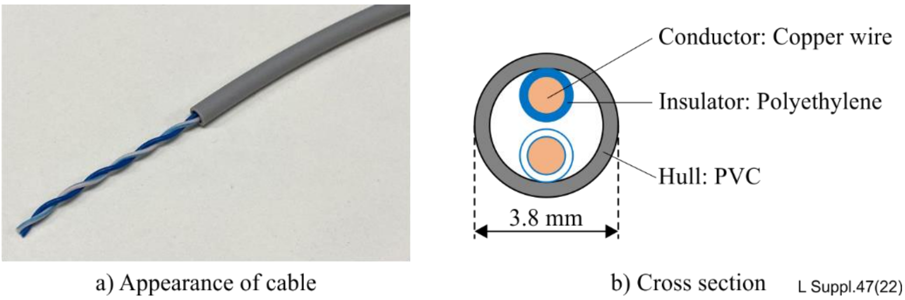
SPE cables can transfer both data and power. This also leads to resource savings as an extra power cable is unnecessary. As shown in Figure 4, SPE can reduce the two cables required for power supply and communication to one. Many IoT devices are DC-driven and power-saving, and it is possible to reduce these AC-ADP (adapters) by a DC power supply. Therefore, the SPE cables can be useful for the effectiveness of resource saving in most use cases with respect to its reductions in weight and size.

This Supplement introduces three main examples for resource savings by using the SPE technology in clause 6.1.2. The first example is a replacement of LAN cables. The second is the reuse of existing cables. This also includes the possibility of reusing existing telephone lines. The third one is the integration of a LAN cable and a power cable. The use cases are shown in Figures 5 to 11.

Table 1 – Typical specifications of SPE and Ethernet cables

	SPE (UTP) cable	**Ethernet (UTP, Category 5) cable**
Number of cores [pair]	1	4
Diameter of the conductor [mm]	0.51	0.51
Weight of the conductor [g/m]	3.75	15.0
Outer diameter [mm]	3.8	5.2

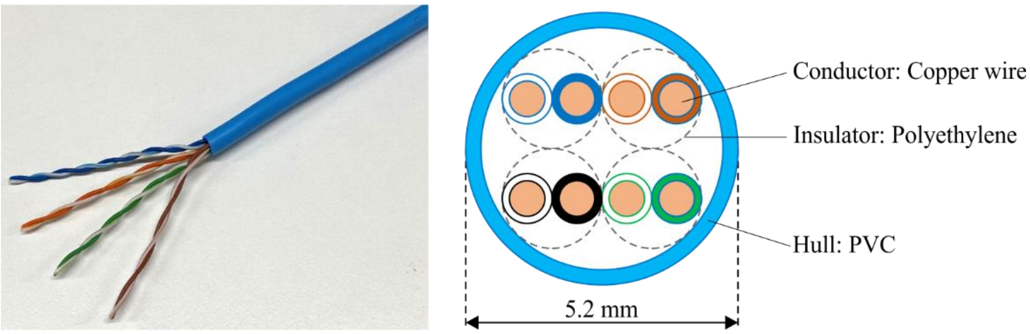
The values of SPE cables are specified in [IEC 61156-11] and [IEC 61156-13].



a) Appearance of cable

b) Cross section

Figure 1 – Appearance and cross section of an SPE (UTP) cable



a) Appearance of cable

b) Cross section

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Figure 2 – Appearance and cross section of an Ethernet (UTP, Category 5) cable

NOTE – Hull is also called a cable sheet or jacket.

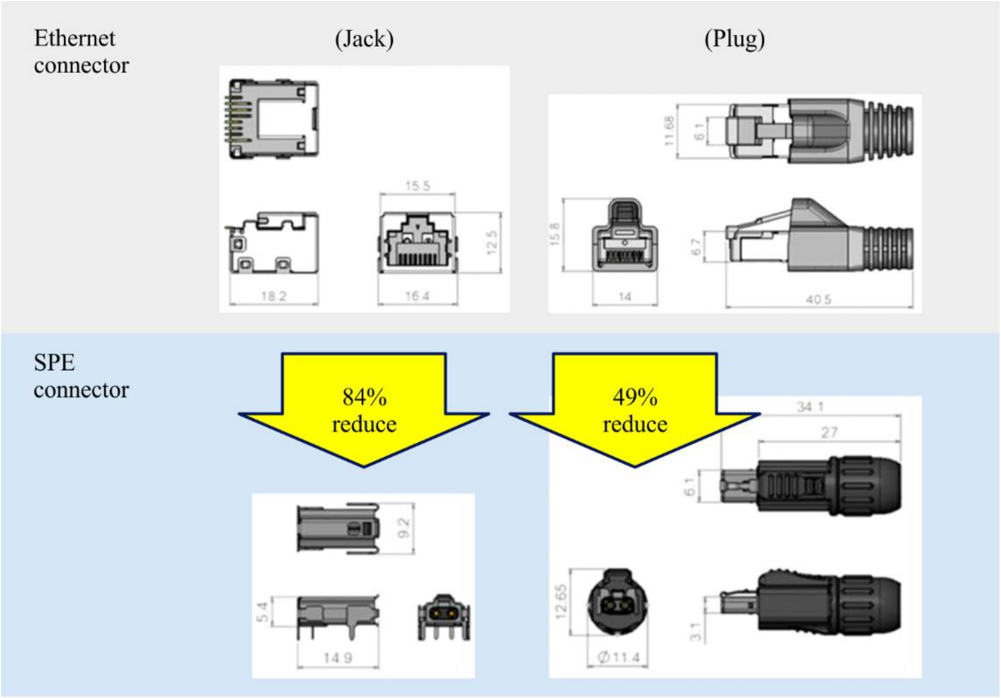

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Figure 3 – Comparison between the SPE and LAN (Ethernet) connectors

The connectors of the SPE are specified in [IEC 63171-6].

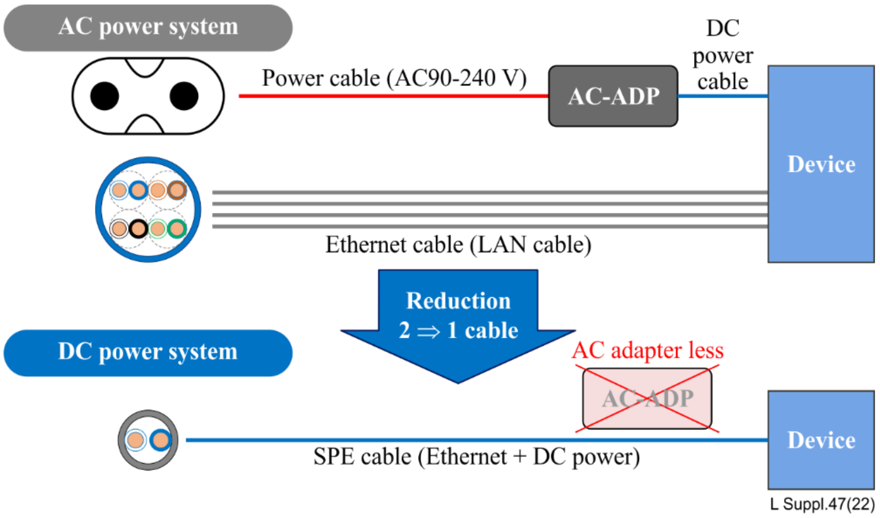


Figure 4 – Power cable and Ethernet cable replaced with an SPE cable

NOTE – SPE cables can transfer both data and power. This also leads to resource savings as an extra power cable is unnecessary.

6.1.2 Use cases of SPE technology

6.1.2.1 Example of LAN (4-pair)cable ⇨ SPE(1-pair) cable

SPE cables can replace LAN cables in the following examples of systems. This capability of replacement can be valid for both UTP and STP cables.

Many LAN (4-pair) cables are installed in data centres and communication centre buildings for connections between servers and communication devices. SPE can realize the same connection with a 1-pair cable.

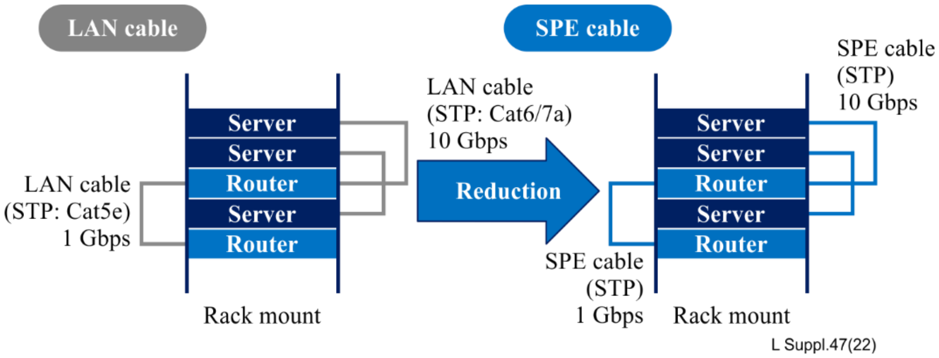


Figure 5 – Example (i) of reduction application using SPE cable in clause 6.1.2.1

The access line optical network unit (ONU) (or radio station) has a connection to the home gateway (HGW) and the router by a LAN (4-pair cable). SPE can realize the same connection with a 1-pair cable.

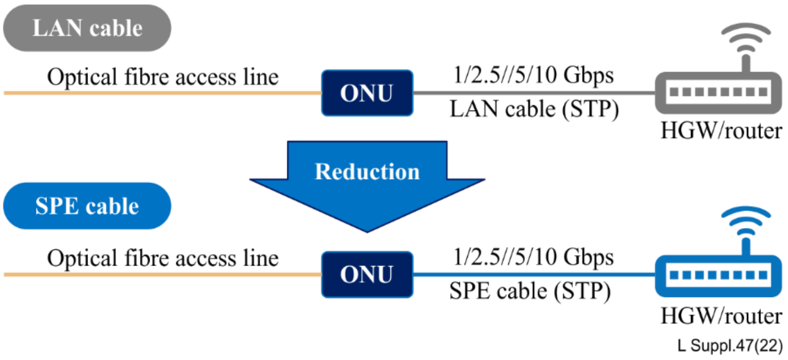


Figure 6 – Example (ii) of reduction application using SPE cable in clause 6.1.2.1

6.1.2.2 Example of reuse of existing 1-pair communication cable

SPE can reuse existing telephone cables or private communication cables for an apartment Internet service, building services in control and security systems, etc. These existing telephone and private communication cables are twisted cables. Screening is necessary for reuse because these are not new SPE cables.

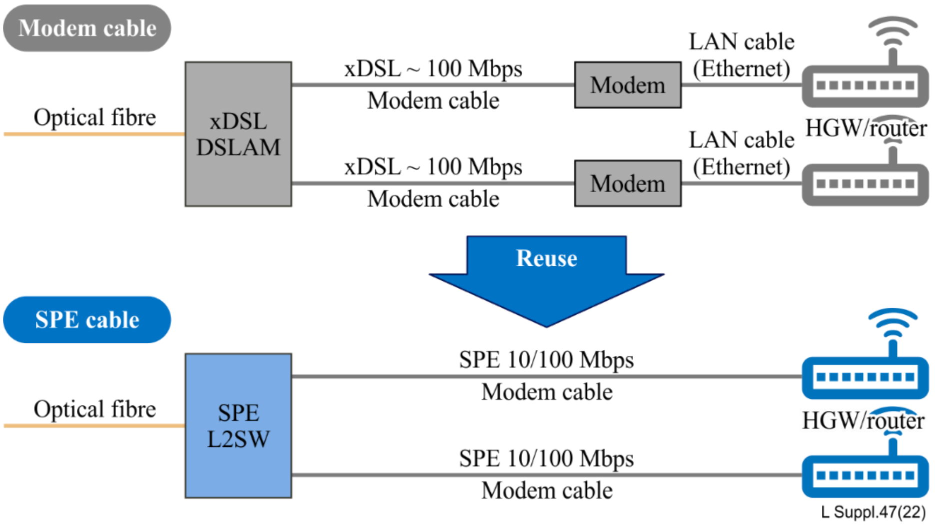


Figure 7 – Example (i) of reuse application using SPE cable in clause 6.1.2.2

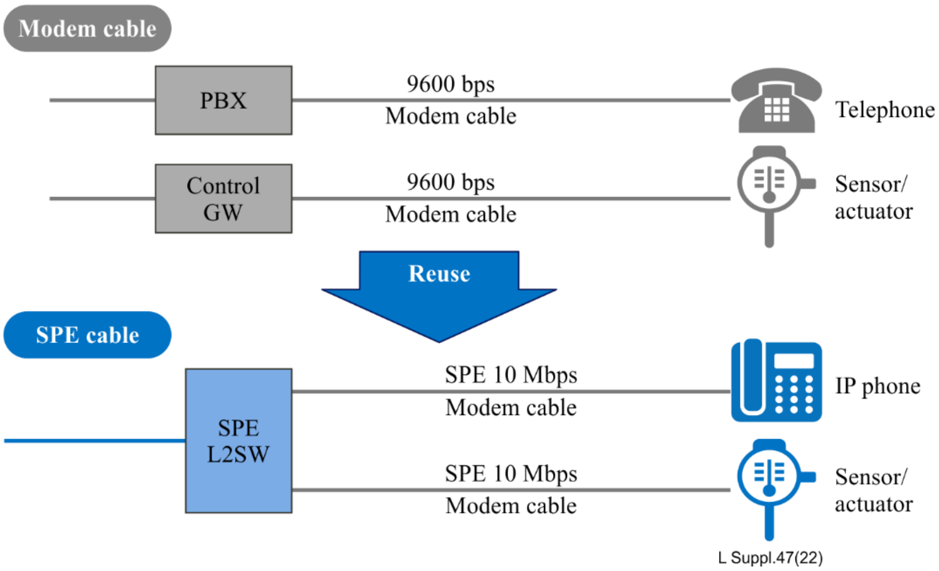


Figure 8 – Example (ii) of reuse application using SPE cable in clause 6.1.2.2

6.1.2.3 Example of power cable and LAN (4-pair) ⇨ integrated into one SPE(1-pair)

SPE can realize DC power supply and communication with a 1 pair cable and integrate the AC power cable and the LAN (4-pair) communication cable. Moreover, it is provided to various terminals without the use of the adapters (ADP).

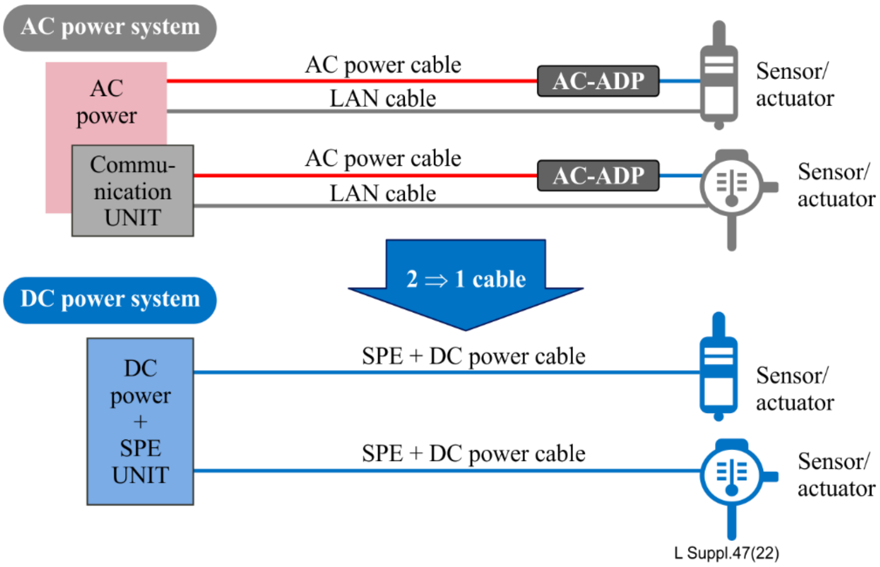


Figure 9 – Example (i) of an integrated application using SPE cable in clause 6.1.2.3

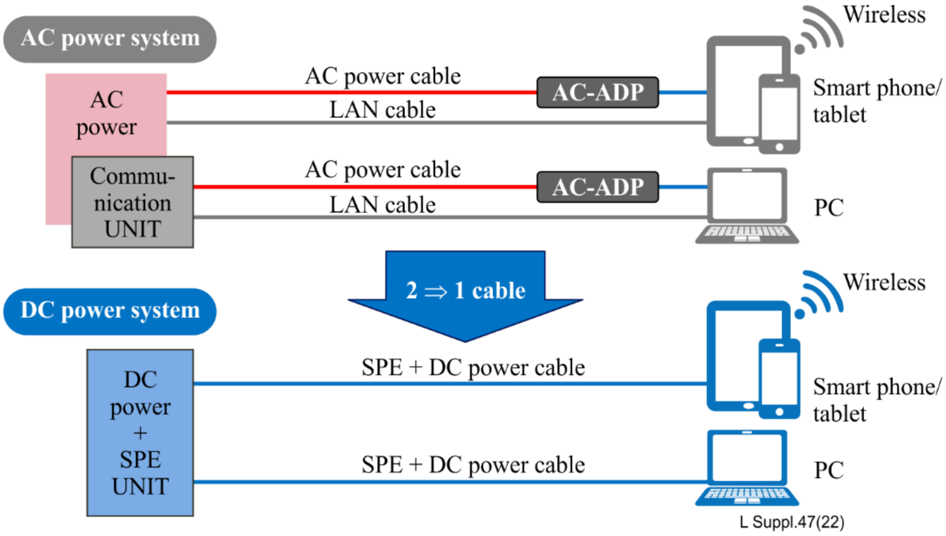


Figure 10 – Example (ii) of an integrated application using SPE cable in 6.1.2.3

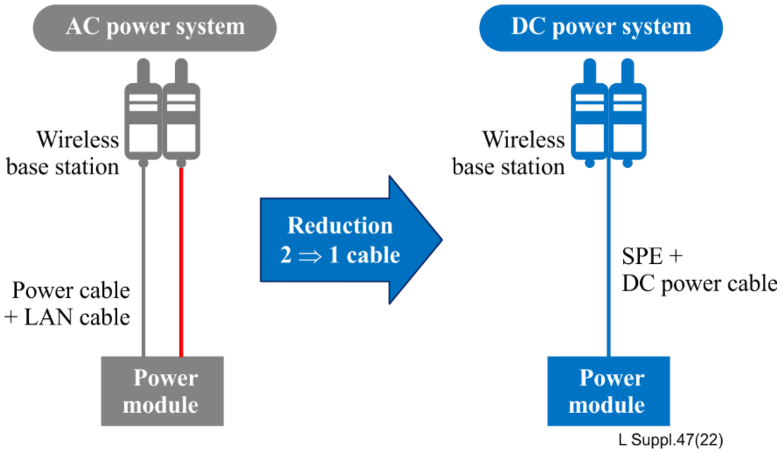


Figure 11 – Example (iii) of an integrated application using SPE cable in clause 6.1.2.3

6.1.3 Resource saving resulting from using the SPE technology

The resource saving of communication cables also contributes to the efficiency of packing and transportation as shown in Figure 12. Moreover, thinner communication cables also contribute to the reduction of installation space.

Figure 12 – An example of an outer box packed with SPE and Ethernet cables having a length of 300 m

Life cycle assessment (LCA) is based on life cycle thinking which means, taking into account the whole life cycle of the product. The core idea of life cycle thinking is to avoid eco-environmental burden shifting. This means minimizing the impact at one stage of the life cycle, or in one eco-environmental impact category, while avoiding increases elsewhere [ITU-T L.Sup.5].

Resource saving is generally realized by improving resource efficiency. In the design of a resource efficiency, three impact categories are very important for telecom goods: climate change, mineral resource depletion and fossil fuel depletion. Potential rebound effects of improved resource efficiency are outside the scope of this Supplement but may be considered in future works. Recycled material content is one attribute because enhancing the recycled material content when producing new raw materials is important. The main environmental benefits – of increasing the environmental attribute of recycled material content – are to reduce mineral resource usage and fossil fuel depletion. The next environmental attribute is embodied energy defined for materials as the primary energy (renewable and non-renewable) used to make one kilogram of material. The environmental benefit of minimizing embodied energy is fossil fuel depletion. Another environmental attribute is carbon dioxide (CO_2) and other greenhouse gases which are closely connected to embodied energy and climate change [ITU-T L.Sup.5].

[b-LCA Report 2019] describes a report and a database of life cycle inventory (LCI) data for corrugated base papers and corrugated products, issued by FEFCO (European Federation of Corrugated Board Manufacturers) and Cepi ContainerBoard (CCB). Following the calculations and data in the report, box sheet areas and CO_2 emissions of climate change environmental impact for corrugated products for SPE and Ethernet cables in Figure 12 are obtained and shown in Table 2. It is easily understood that the CO_2 emissions from corrugated products of an SPE cable with 300 m is lower than that of an Ethernet cable. The derivations of sheet areas and CO_2 emissions are described in Appendix I.

Table 2 – Box sheet areas and CO_2 emissions of climate change environmental impact for corrugated products of SPE cable and Ethernet cable with 300 m

	Cable Type		SPE cable's % of CO_2 decrease relative to Ethernet cable
	SPE cable	Ethernet cable	
Box sheet Area	0.7198 m^2/box	0.9179 m^2/box	
CO_2 emissions			
CO_2 (fossil)	142.2 g/box	188.1 g/box	24.4%
CO_2 (biomass)	122.3 g/box	155.8 g/box	21.5%

6.1.4 Summary of resource saving by using the SPE technology

Clause 6.1 shows that the SPE technology is used in a variety of situations from data centres to homes. Since the SPE is a very simple and smart technology, the technology should be available in all countries so that resource saving by the SPE technology could contribute to sustainable growth under the constraints of the environment and resources. SPE technology could be one of the key technologies that bring a new ecosystem in line with the sustainable development goals (SDGs).

6.2 Resource saving by semiconductor manufacturing technologies

6.2.1 Semiconductor area reduction achievable, due to a chiplet based design

Personal computers or server processors (CPU) are currently manufactured on a single monolithic die or several smaller dies (i.e., chiplets, for example 2 or 4 for the cores, and 1 additional for input / output functions). The second option i.e., several smaller dies, allows the manufacturer to improve the yield of the manufacturing process (i.e., have fewer losses per wafer). For example, AMD's Epyc server processors are based on 213 mm^2 dies (~22.05 mm × ~9.66 mm) for their Zen+ architecture (Zeppelin dies) [b-Tirias & AMD]. If 4 of these dies were combined, it would be an aggregate of 852 mm^2 of silicon. A hypothetical aggregate of these 4 dies would have an area of about 777 mm^2 due to some possible optimizations [b-Tirias & AMD].

To evaluate the resources savings between the manufacturing of 4 dies of 213 mm^2 versus a 777 mm^2 monolithic die the following parameters are applied:

- Manufacturing on a 300 mm wafer;
- D0 of 0.09 defect per square cm^2 (according to [b-IEEE Xplore]);
- Horizontal scribe lane and vertical scribe lane set at 0.2 mm;
- Edge loss set at 3 mm.

Figure 13 shows an estimation of how the 213 mm^2 dies would be distributed on a 300 mm wafer and the losses to be expected according to the D0 and edge loss values. A maximum of 404 dies could fit on the wafer but according to the assessment only 355 of them are entirely functional.

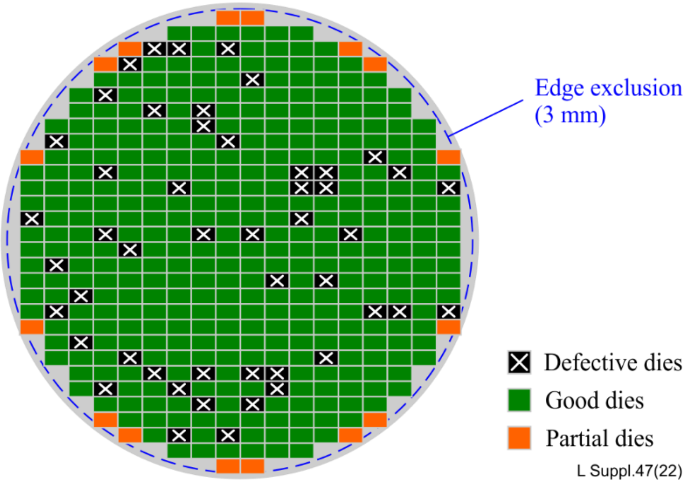


Figure 13 – Manufacturing of the 213 mm² (~22.05 mm × ~9.66 mm) dies on a 300 mm wafer, with losses due to manufacturing defects (e.g., D0) and edge losses (partial dies)

The hypothetical 777 mm² monolithic die dimensions are set to ~42.12 mm × ~18.45 mm (4 dies of 213 mm² aggregated on 2 dies×2 dies scheme and with the 10% surface reduction applied). Figure 14 shows an estimation of how those 777 mm² dies would be distributed on a 300 mm wafer and the losses to be expected according to the D0 and edge loss values. A maximum of 62 dies could fit on the wafer but according to the assessment only 32 of them are entirely functional.

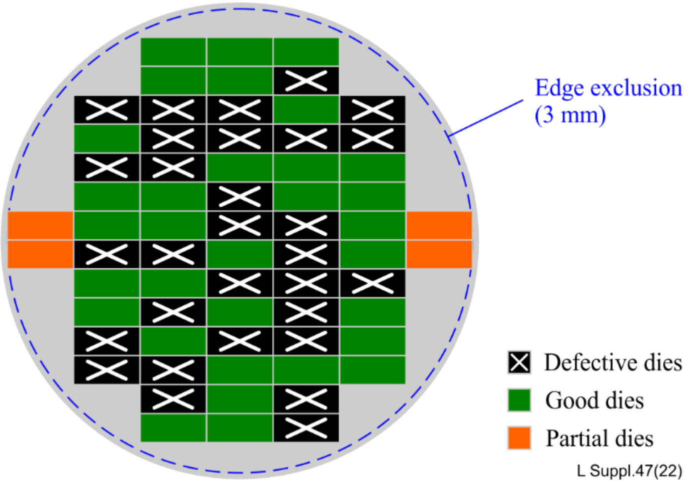


Figure 14 – Manufacturing of the 777 mm² (to ~42.12 mm × ~18.45 mm) dies on a 300 mm wafer, with losses due to manufacturing defects (e.g., D0) and edge losses (partial dies)

The semiconductor area to obtain the 777 mm² die can also be modelled with a square shape, i.e., ~27.88 × ~27.88 mm. Figure 15 shows an estimation of how those square shaped 777 mm² dies would be distributed on a 300 mm wafer and the losses to be expected according to the D0 and edge loss values. A maximum of 69 dies could fit on the wafer but according to the assessment only 36 of them are entirely functional.

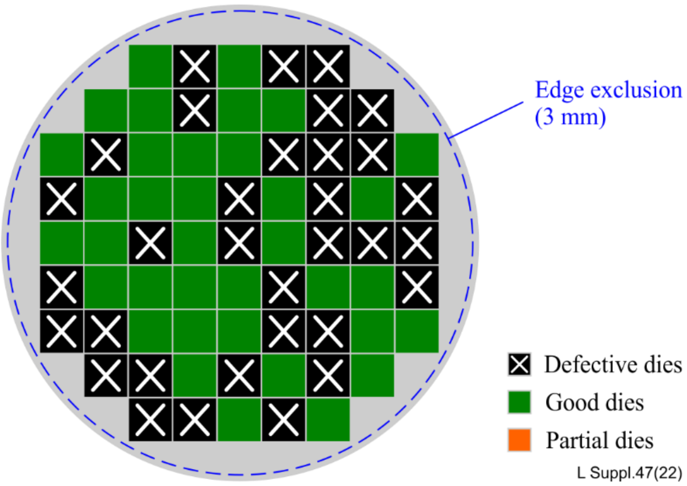


Figure 15 – Manufacturing of the 777 mm^2 (to ~27.88 mm × ~27.88 mm) dies on a 300 mm wafer, with losses due to manufacturing defects (e.g., D0) and edge losses (partial dies)

According to these three examples to obtain 1000 functional CPUs the area of processed semiconductor would be:

1) With the 4 × 213 mm^2 dies architecture

4 × 213 × 1000 × 404 / 355 = 969 600 mm^2 of semiconductor

2) With the monolithic 777 mm^2 die architecture

777 × 1000 × 62 / 32 = 1 505 437.5 mm^2 of semiconductor (~+55% of area compared to 1)

3) With the monolithic square shaped 777 mm^2 die architecture

777 × 1000 × 69 / 36 = 1 489 250 mm^2 of semiconductor (~+53 % of area compared to 1)

6.2.2 Estimation of GHG emissions reduction, due to a chiplet based design

The dies' dimensions (e.g., ~22.05 mm × ~9.66 mm for the 213 mm^2 dies) and their distributions on 300 mm wafers (displayed in Figure 13, Figure 14 and Figure 15) will be combined with two sources of data to calculate the environmental footprint reduction potential achievable due to the chiplet based design:

1) Data from the TSMC CSR report [b-TSMC 2020] which provide GHG emissions data in terms of "tonnes of CO_2 equivalent per 12 inches wafer-layer equivalent" for Scope 1 and 2. Scope 3 is given for the entire company and can then be reallocated per area of wafer produced during the year 2020.

2) Data from IC Knowledge [b-Scotten] which include data about logic mask counts for different technology nodes (e.g., 10, 7, 5 nm). All the dies will be considered as manufactured on a 7 nm process, which would require 76 masks.

The GHG emissions reduction potential calculated according to these reports and the figures from clause 6.2.1 is displayed in Figure 16.

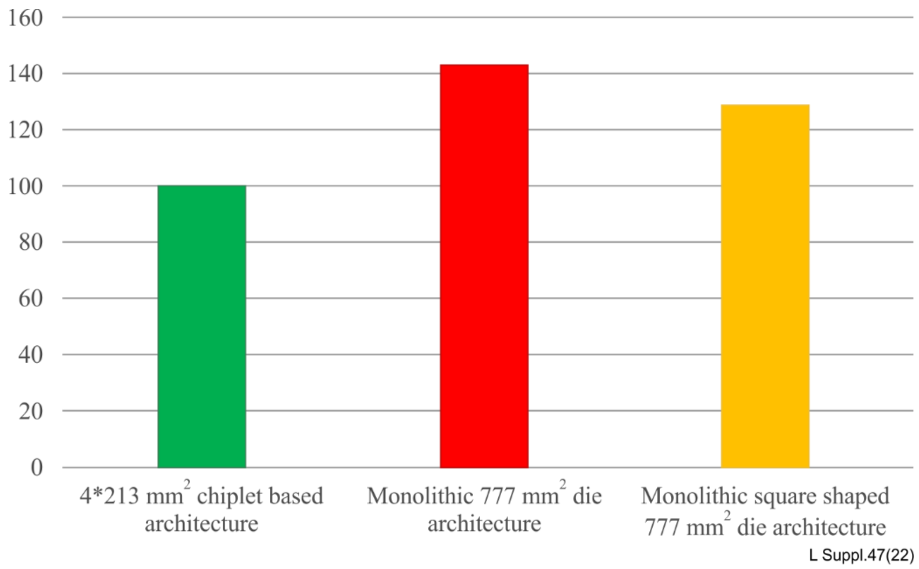


Figure 16 – Carbon footprint of each of the 3 architectures (the 4 × 213 mm² chiplet based architecture's carbon footprint is set at 100 as a reference)

In addition to the CPU, the chiplet based architecture has also been introduced to the GPU with a patent published in 2021, and a product featuring this architecture is expected to arrive in the market in 2022 [b-US 2021/0097013].

6.2.3 Panel-level manufacturing

This manufacturing process is about using a square shaped substrate (for example 610 × 456 mm, i.e., 24" × 18" as demonstrated in [b-Tanja]) instead of the traditional disks (i.e., wafers).

To investigate the losses mitigation between panel-level manufacturing and manufacturing on wafer, calculations were carried out for a 17.9 × 16.2 mm die. The following parameters were applied for both panel-level manufacturing and manufacturing on the wafer (300 mm one):

- D0 of 0.09 defect per square cm² (according to [b-IEEE Xplore]);
- Horizontal scribe lane and vertical scribe lane set at 0.2 mm;
- Edge loss set at 3 mm.

Figure 17 shows an estimation of how the 17.9 × 16.2 mm dies would be distributed on a 300 mm wafer and the losses to be expected according to the D0 and edge loss values. According to the assessment only 145 of the dies are entirely functional, which leads to the following calculation regarding the efficiency of the manufacturing process:

- 145 × 17.9 × 16.2 = 42 047.1 mm² of effective dies
- 300 mm wafer = 150 ×150 × Pi = 70 685.8 mm² of area
- Percentage of material used for dies manufacturing = 42 047.1 / 70 685.8 = 59.5%

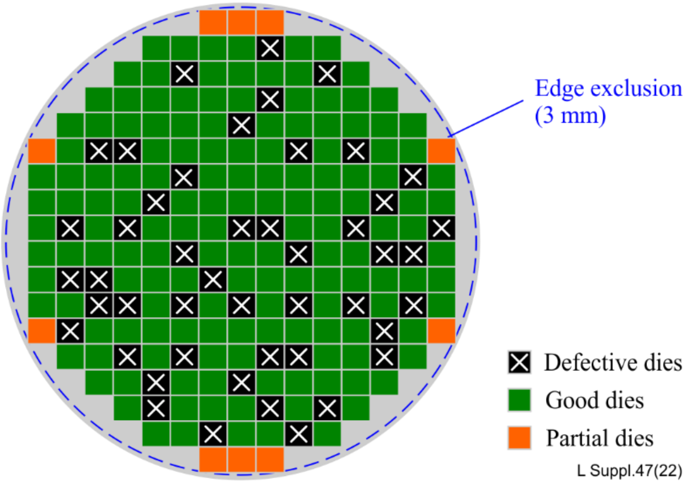


Figure 17 – Manufacturing of the 17.9 mm × 16.2 mm dies on a 300 mm wafer, with losses due to manufacturing defects (e.g., D0) and edge losses (partial dies)

Figure 18 shows an estimation of how the 17.9 × 16.2 mm dies would be distributed on a 510 mm × 515 mm panel and the losses to be expected according to the D0 and edge loss values.

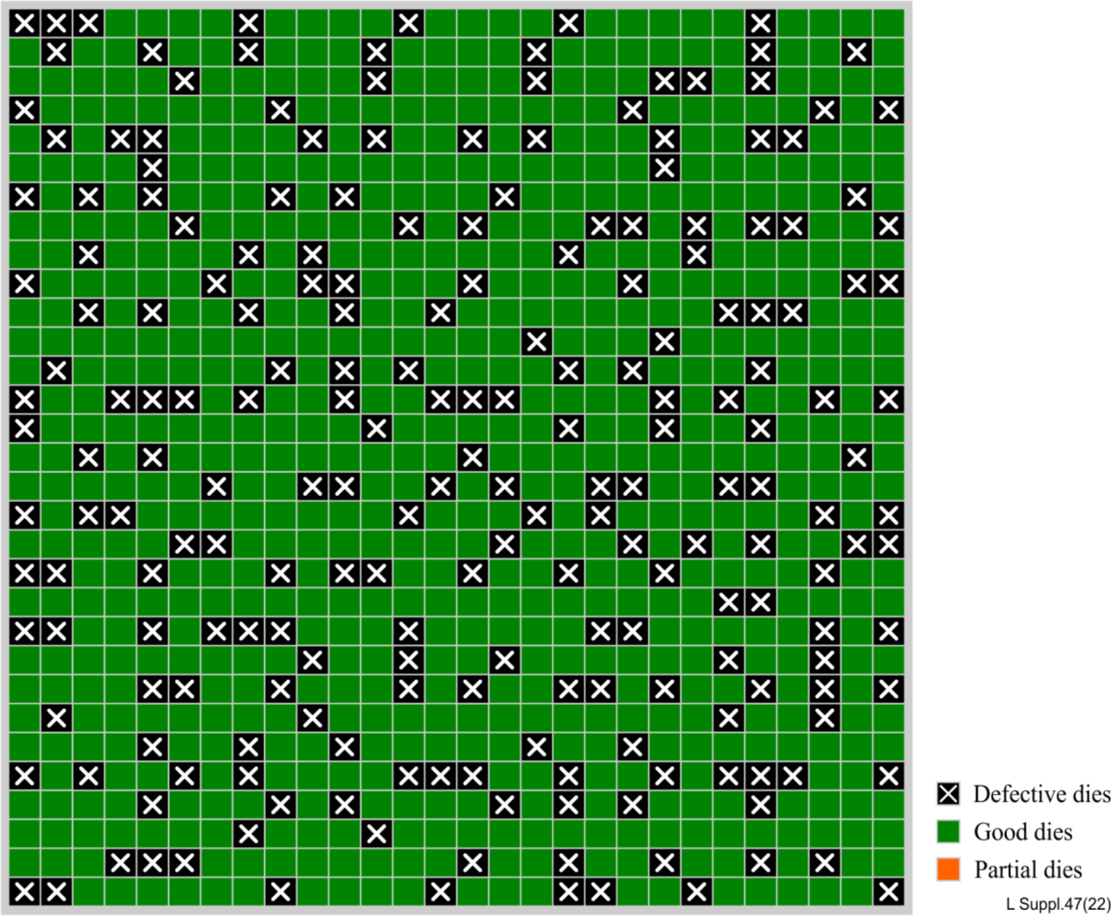


Figure 18 – Manufacturing of the 17.9 mm × 16.2 mm dies on a 510 mm × 515 mm panel, with losses due to manufacturing defects (e.g., D0) and edge losses (partial dies)

According to the assessment 653 of the dies are entirely functional, which leads to the following calculation regarding the efficiency of the manufacturing process:

- 653 good dies = 653 × 17.9 × 16.2 = 189 356.9 mm² of effective dies
- 510 × 515 mm panel = 262 650 mm² of area
- Percentage of material used for dies manufacturing = 189 356.9 / 262 650 = 72.09%

This simplified calculation shows the potential of panel-level manufacturing to save resources (e.g., silicon, chemicals such as photoresist and metals like tantalum, tungsten or titanium required for depositions). One interesting challenge is to adapt the size of the panel to the size of the dies that will be manufactured, to avoid significant losses on the edges of the panel.

6.3 Resource saving by using other technologies

Note that this Supplement collects examples and / or best practices due to the progress of resource saving within the ICT sector. Further contributions will improve this Supplement.

Appendix I

Calculation of CO_2 emissions of corrugated products

[b-LCA Report 2019] describes a report and a database of life cycle inventory (LCI) data for corrugated base papers and corrugated products, issued by FEFCO (European Federation of Corrugated Board Manufacturers) and the Cepi ContainerBoard (CCB). In order to analyse climate change environmental impacts for corrugated products based on the report, the following assumptions need to be considered:

1) Corrugated boards are manufactured from several specially conditioned layers of recycled and / or virgin papers, called fluting medium and linerboard. The corrugated fluting medium with one liner attached to it is called single face web and travels along the production machine towards the double backer where the single face web meets the outer liner and forms a corrugated board. Figure I.1 shows a single wall corrugated board with a double face consisting of one sheet of fluted paper.

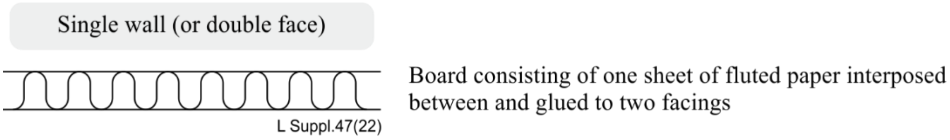


Figure I.1 – Corrugated board consisting of one sheet of fluted paper [b-LCA Report 2019]

2) A corrugated box is manufactured through the processes of printing, slotting, folding, and gluing the corrugated board. Figure I.2 shows an example of a box blank and Figure I.3 shows the result when this blank is erected as a converted box.

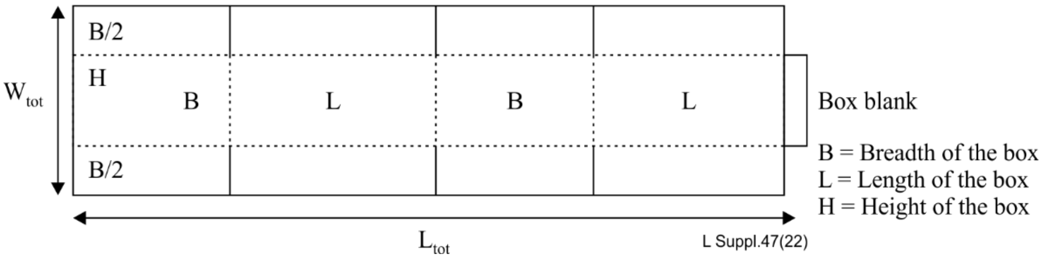


Figure I.2 – Box blank [b-LCA Report 2019]

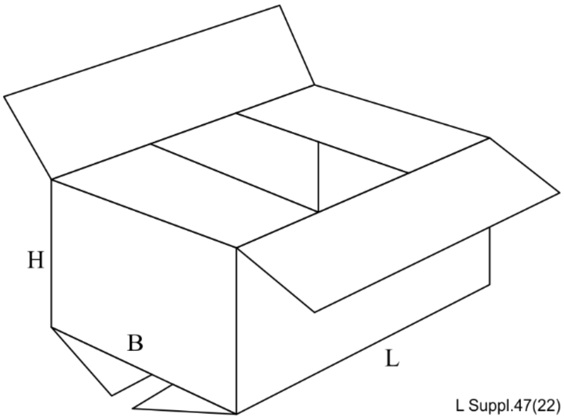


Figure I.3 – Converted box [b-LCA Report 2019]

3) The corrugated board composition of the corrugated box depends on the function that it has to fulfil. The consumption of liner and fluting can be calculated from the dimensions of the box, the weight of the liners and fluting, what kind of flute i.e., wave type used, and the

weight of the sheet before die cutting. Different wave types lead to different heights of the corrugated layer and different paper consumption. For example, 1.43m^2 of fluting (measured flat) is required to manufacture 1m^2 of converted corrugated board with C-flute, as shown in Figure I.4.

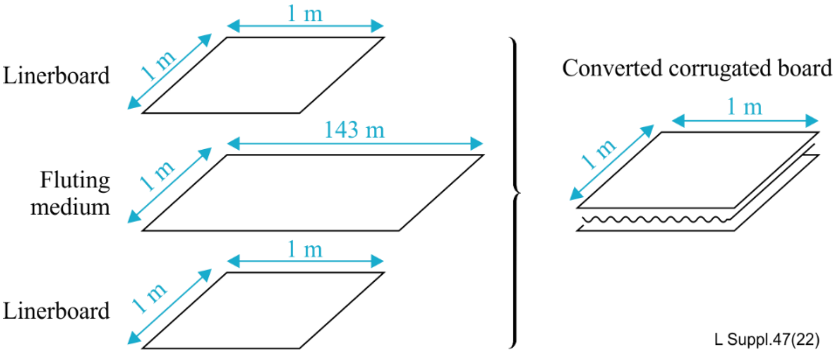


Figure I.4 – Corrugated board with C-flute type [b-LCA Report 2019]

The corrugated board manufacturer can give the weight of the sheet before die-cutting. For a standard type construction, the weight can also be calculated using the International fibreboard case code published by FEFCO. The example is shown below [b-LCA Report 2019]:

Example: FEFCO Code 0201

Facings: Corrugated board C flute, Kraftliner 175 g/m^2 and Testliner 175 g/m^2

Corrugating medium: Recycled Fluting 140 g/m^2

The composition of the corrugated board is then obtained below:

Kraftliner	175 g/m^2
Recycled fluting	1.43 × 140 = 200 g/m^2
Testliner	175 g/m^2
Glue	2 × 5 = 10 g/m^2
Total weight	560 g/m^2

In FEFCO code the form of the box blank is shown and by using the box dimensions it is possible to calculate the total length and width of the blank. Adding a 20 mm broad strip to the edges of the blank gives a fair estimate of the sheet area before die-cutting.

Considering the corrugated box of SPE cable of 300 m in clause 6.1.3 with L_{tot} = 1.140 m and W_{tot} = 0.570 m, the dimension of the sheet is:

$$(1.140 + 0.040) \times (0.570 + 0.040) = 0.7198 \text{ m}^2/\text{box}$$

Similarly, for the corrugated box of Ethernet cable of 300 m in clause 6.1.3 with L_{tot} = 1.306 m and W_{tot} = 0.642 m, the dimension of the sheet is:

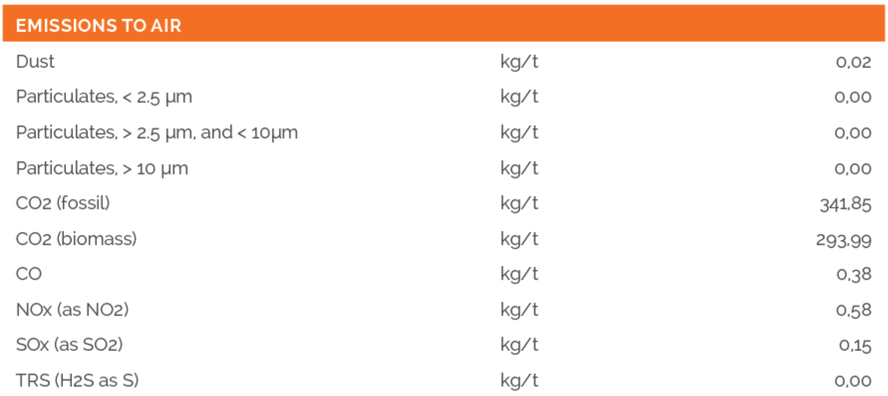
$$(1.306 + 0.040) \times (0.642 + 0.040) = 0.9179 \text{ m}^2/\text{box}$$

Assuming 3% as corrugator trimmings (0.97, a common value for modern corrugators), the consumption of liner and fluting can be calculated as:

Corrugated box of SPE cable	560 × 0.7198 / 0.97 = 416 g
Corrugated box of Ethernet cable	560 × 0.9179 / 0.97 = 530 g

[b-LCA Report 2019] collects data on emissions to air from fuel combustion at mill sites. For CO_2 the figures reported are based on calculations and are reported separately for fossil and biomass origin. Table I.1 shows the calculated inputs and outputs for the production of 1 ton of corrugated board in Europe with an average paper grade composition in terms of emissions to air.

Table I.1 – Data of emissions to air [b-LCA Report 2019]



EMISSIONS TO AIR		
Dust	kg/t	0,02
Particulates, < 2.5 µm	kg/t	0,00
Particulates, > 2.5 µm, and < 10µm	kg/t	0,00
Particulates, > 10 µm	kg/t	0,00
CO2 (fossil)	kg/t	341,85
CO2 (biomass)	kg/t	293,99
CO	kg/t	0,38
NOx (as NO2)	kg/t	0,58
SOx (as SO2)	kg/t	0,15
TRS (H2S as S)	kg/t	0,00

Using the data above, CO_2 emissions (fossil) for corrugated products of SPE cable and Ethernet cable with 300 m are calculated as follows:

Corrugated box of SPE cable	341.85 × .416 = 142.2 g
Corrugated box of Ethernet cable	341.85 × .530 = 181.1 g

CO_2 emissions (biomass) for corrugated products of SPE cable and Ethernet cable with 300 m are calculated as follows:

Corrugated box of SPE cable	293.99 × .416 = 122.3 g
Corrugated box of Ethernet cable	293.99 × .530 = 155.8 g

These results of CO_2 emissions are summarized in Table 2 in clause 6.1.3.

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