ITU

INTERNATIONAL TELECOMMUNICATION UNION

CCITT

THE INTERNATIONAL
TELEGRAPH AND TELEPHONE
CONSULTATIVE COMMITTEE

O.152
(11/1988)

SERIES O: SPECIFICATIONS FOR MEASURING EQUIPMENT

Equipment for the measurement of digital and analogue/digital parameters

ERROR PERFORMANCE MEASURING EQUIPMENT FOR 64 kbit/s PATHS

Reedition of CCITT Recommendation O.152 published in the Blue Book, Fascicle IV.4 (1988)

NOTES

1   CCITT Recommendation O.152 was published in Fascicle IV.4 of the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2   In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Recommendation O.152

ERROR PERFORMANCE MEASURING EQUIPMENT FOR 64 kbit/s PATHS

(Malaga-Torremolinos, 1984; amended, Melbourne, 1988)

The requirements for the characteristics of a bit-error performance measuring equipment which are described below must be adhered to in order to ensure compatibility between equipments standardized by the CCITT, and produced by different manufacturers.

1 General

The set is designed to measure the bit-error performance of digital paths (operating at 64 kbit/s) by the direct comparison of a pseudorandom test pattern with an identical locally generated test pattern.

2 Test patterns

2.1 *Pseudorandom pattern*

This pattern is to be produced by means of a shift register incorporating appropriate feedback (see Figure 1/O.152):

Number of shift register stages	11
Pattern length	$2^{11} - 1 = 2047$ bits
Feedback..	taken from the outputs of the 9th and 11th stage via an exclusive-OR-gate to the first stage
Longest sequence of zeros	10 (non-inverted signal)

Note 1 – In the case of international testing where the measurement includes systems based on 1544 kbit/s it is necessary to modify the test sequence in such a way that more than seven consecutive "0"-bits are avoided. This is achieved by forcing the output signal to "1" whenever the next 7 bits of the sequence are all zeros.

Note 2 – It is recommended to use the test pattern of 2047 bit length also at other bit rates in the range 48 kbit/s to 168 kbit/s.
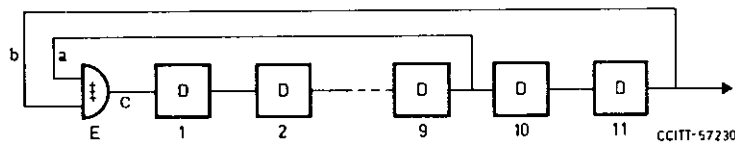
Note – The clock pulse connection is not shown.

a	b	c
1	0	1
0	1	1
0	0	0
1	1	0

Truth table for exclusive OR-gate (E):

a and b: gate inputs
c: gate output

FIGURE 1/O.152

Circuit example for an 11-stage shift register with D-flipflops and an executive-OR-gate

2.2 *Fixed patterns* (optional)

Fixed patterns of all ones (. . . 1111 . . .) and alternating ones and zeros (. . . 1010 . . .) may be provided.

3 Bit rate

Bit rate in accordance with CCITT Recommendations G.703, § 1 [1] and V.36 [2] of 64 kbit/s:

a)   bit rate tolerance (Recommendation G.703 [1]): ± 100 . 10^{-6},

b)   bit rate tolerance (Recommendation V.36 [2]), optional: ± 50 . 10^{-6}.

4 Interfaces

The interface characteristics (impedances, levels, codes, etc.) should be in accordance with Recommendations G.703 [1], I.430 [7] (optional) and V.11 [3] (optional).

In addition to providing for terminated measurements the measuring set shall also be capable of monitoring at protected test points on digital equipment. Therefore, a high impedance and/or additional gain must be provided to compensate for the loss at monitoring points already provided on some equipments.

4.1 *Interfaces corresponding to Recommendation G.703* [1]

Three interfaces shall be provided:

a)   a codirectional interface in accordance with Recommendation G.703, § 1.2.1 [1],

b)   a centralized clock interface in accordance with Recommendation G.703, § 1.2.2 [1],

c)   a contradirectional interface in accordance with Recommendation G.703, § 1.2.3 [1].

4.2 *Method of clock synchronization*

The following modes of synchronization shall be selectable:

a)   Lock the digital generator clock rate to that at the input of the receive side of the measuring set (for the codirectional interface).

b)   Allow the generator clock to free run within the overall allowed frequency tolerances.

c)   Lock the digital generator clock rate to an external clock signal. (Configuration of input for external clock in accordance with Recommendation G.703 [1].)

4.3 *Interface corresponding to Recommendation I.430 [7]*

For further study. This study should include means for obtaining access to the individual 64 kbit/s channels at the S and T interface points.

4.4 *Interface corresponding to Recommendation V.11 [3]*

As an option an interface in accordance with Recommendation V.11 [3] shall be provided.

5 Bit-error-ratio measuring range

The receiving equipment of the set should be capable of measuring bit-error ratios in the range 10^{-2} to 10^{-7}. The measurement time should be sufficiently long to achieve accurate measurements. In addition, it should be possible to measure bit-error ratios smaller than 10^{-7}; this can be achieved by providing the capability to count cumulative errors.

6 Block-error ratio measurements

Optionally, the instrument should be capable to perform block-error measurements in addition to the bit-error measurements. If provided it should be possible to measure block-error ratios in the range 10^{-0} to 10^{-5} when using the pseudorandom test pattern with a block length of 2047 bits.

7 Mode of operation

The mode of operation should be such that the signal to be tested is first converted into a unipolar (binary) signal in the error measuring instrument and subsequently the bit comparison is made also with a reference signal in binary form.

8   Error evaluation

8.1   *Measurement of errored time intervals*

The instrument shall be capable of detecting errored seconds and other errored or error-free time intervals as defined by Recommendation G.821 [4]. The number of errored or error-free time intervals in a selectable observation period from 1 minute to 24 hours, or continuous, shall be counted and displayed.

For this measurement the error detection circuits of the instrument shall be controlled by an internal timer which sets intervals of equal length and which operates independently of the occurrence of errors.

8.2   *Measurement of short-term mean error ratio*

8.2.1   It shall be possible to record the time intervals as defined in Recommendation G.821 [4], during which the bit-error ratio is less than $1 . 10^{-6}$.

8.2.2   It shall be possible to record the one-second intervals during which the bit-error ratio is less than $1 . 10^{-3}$.

9   Recording of measurement results

As an option an interface shall be provided which allows connecting external equipment for further processing the measuring results.

The interface shall comply with Recommendation V.24 [5] or the interface bus according to IEC Publication 625 [6].

10   Operating environment

The electrical performance requirements shall be met when operating at the climatic conditions as specified in Recommendation O.3, § 2.1.

References

[1]   CCITT Recommendation *Physical/electrical characteristics of hierarchical digital interfaces*, Vol. III, Rec. G.703.

[2]   CCITT Recommendation *Modems for synchronous data transmission using 60-108 kHz group band circuits*, Vol. VIII, Rec. V.36.

[3]   CCITT Recommendation *Electrical characteristics for balanced double-current interchange circuits for general use with integrated circuit equipment in the field of data communications*, Vol. VIII, Rec. V.11.

[4]   CCITT Recommendation *Error performance on an international digital connection forming part of an integrated services digital network*, Vol. III, Rec. G.821.

[5]   CCITT Recommendation *List of definitions for interchange circuits between data terminal equipment and data circuit-terminating equipment*, Vol. VIII, Rec. V.24.

[6]   IEC Publication 625 *An Interface system for programmable measuring instruments (byte serial, bit parallel)*.

[7]   CCITT Recommendation *Basic user-network interface-Layer/Specification*, Vol. III, Recommendation I.430.

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