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Equipment for the measurement of digital and analogue/ digital parameters

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EQUIPMENT TO PERFORM IN-SERVICE MONITORING ON 2048 kbit/s SIGNALS

Reedition of CCITT Recommendation O.162 published in the Blue Book, Fascicle IV.4 (1988)

NOTES

1 CCITT Recommendation O.162 was published in Fascicle IV.4 of the *Blue Book*. This file is an extract from the *Blue Book.* While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Recommendation O.162

EQUIPMENT TO PERFORM IN-SERVICE MONITORING ON 2048 kbit/s SIGNALS

(Geneva, 1980, amended Melbourne, 1988)

1 General

1.1 This specification describes an instrument for performing in-service error tests on 2 Mbit/s signals having frame structures that are in accordance with Recommendation G.704 [1].

1.2 The instrument is required to monitor a 2048-kbit/s HDB3 encoded signal, display any inherent alarm condition in the signal and be capable of counting errors in the frame alignment signal.

1.3 The instrument may also, if so desired, count and display HDB3 code violations as a separate facility.

1.4 The instrument is required to monitor any çcyclic redundancy check (CRC) procedure signals, in accordance with Recommendation G.704 [1], conveyed within the frame alignment signal, and çtime slot 0 (TSO) of frames not containing the frame alignment signal.

1.5 As an option the instrument may provide access to the information bits conveyed in any selected time slot.

1.6 *HDB3 decoding strategy*

When necessary, the received digital signal shall be decoded by the instrument in a manner such that, when sampling the signal, on recognition of 2 consecutive zeros (spaces) followed by a bipolar violation, the decoder shall substitute 4 consecutive zeros in place of the bipolar violation and the 3 preceding digits.

2 Input signal

2.1 *Interface*

The instrument shall be capable of operating with the interface at 2048 kbit/s corresponding to Recommendation G.703 [2], § 6.

2.2 *Input sensitivity*

2.2.1 The instrument is required to operate satisfactorily under the following input conditions.

2.2.1.1 Input impedances and levels in accordance with Recommendation G.703 [2].

2.2.1.2 The instrument shall also be capable of monitoring at protected test points on digital equipment. Therefore, a high impedance input and/or additional gain of 30 dB shall be provided to compensate for the loss at the monitoring points already provided on some equipment.

2.2.1.3 Additionally the instrument is required to operate satisfactorily, in both the terminated and monitor mode, when connected to an interface output in accordance with Recommendation G.703 [2] via a length of cable which can have an insertion loss of 0 dB to 6 dB at the half bit rate of the signal. The insertion loss of the cable at other frequencies will be proportional to $\sqrt{f}$.

2.3 *Input impedance*

2.3.1 The instrument shall have a return loss of better than 20 dB against a nonreactive 75/120/130-ohm resistor over a frequency range of 40 kHz to 2500 kHz.

2.4 *Signal input gating*

2.4.1 The instrument shall incorporate a timing recovery circuit, operated from the incoming digital signal, such that the instrument senses only the voltages which are present during a short gating period at the midpoint of each digit time slot.

2.5 *Input jitter tolerance*

2.5.1 The instrument shall be able to tolerate the lower limit of maximum tolerable input jitter specified in Recommendation G.823 [3].

3 Facilities

3.1 The instrument shall incorporate fault indications to meet the alarm strategies of equipments meeting Recommendation G.732 [4].

3.2 A possible fault indication plan is illustrated in § 3.3 below. All fault indicators are normally extinguished.

3.3 *Fault indication plan*

3.3.1 *Input signal failure*

A fault indication shall be given if more than 10 consecutive zeros are detected.

3.3.2 *Alarm indication signal (AIS)*

The instrument shall recognize a signal containing less than 3 zeros in a 2-frame period (512 bits) as a valid AIS signal and the appropriate indicator shall be lit.

The strategy for the detection of the presence of an AIS shall be such that the AIS is detectable even in the presence of a code violation rate of 1 in 10^3. However, a signal with all bits in the 1s state, except the çframe alignment signal (FAS), shall not be mistaken for a valid AIS.

3.3.3 *Frame*

3.3.3.1 In the event of a loss of frame alignment, as defined in Recommendation G.706 [5], § 4, the instrument shall recognize the loss and the appropriate indicator shall be lit.

3.3.3.2 In the event of recovery of frame alignment, as defined in Recommendation G.706 [5], § 4, the indicator shall be extinguished.

Note – The instrument shall be able to synchronize to frames with or without CRC bits.

3.3.4 *Errors in the frame alignment signal*

3.3.4.1 The instrument shall have a means of indicating bit error rates, e.g. $1 . 10^{-3}$, $1 . 10^{-4}$, $1 . 10^{-5}$ and illuminate the appropriate indicator.

The indication of bit error rates occurring in the received decoded signal and detected as incorrect frame alignment signals shall comply with the limits given in Table 1/O.162. The requirements in the table shall apply on the assumption that the average bit error rates are present for the whole of the counter measurement period.

TABLE 1/O.162

Bit error rate indication	Average bit error rates in decoded signal	Probability of indication illuminating or extinguishing within the periods stated below	
		Illuminate	Extinguish
$1 \cdot 10^{-3}$	$1 \cdot 10^{-3}$ $5 \cdot 10^{-4}$ $1 \cdot 10^{-4}$	50% within 0.3 s 5% within 0.3 s –	5% within 0.3 s – 95% within 0.3 s
$1 \cdot 10^{-4}$	$1 \cdot 10^{-4}$ $5 \cdot 10^{-5}$ $1 \cdot 10^{-5}$	50% within 3 s 5% within 3 s –	5% within 3 s – 95% within 3 s
$1 \cdot 10^{-5}$	$1 \cdot 10^{-5}$ $5 \cdot 10^{-6}$ $1 \cdot 10^{-6}$	50% within 30 s 5% within 30 s –	5% within 30 s – 95% within 30 s

3.3.4.2 It shall also be possible to count the sum of the errors indicated. The count capacity shall be 99 999. A separate indication shall be given if the count exceeds this figure.

3.3.5 *Multiframe*

3.3.5.1 In the event of a loss of multiframe alignment, as defined in Recommendation G.732 [4], § 5.2, the instrument shall recognize the loss and the appropriate indicator shall be lit.

3.3.5.2 In the event of recovery of multiframe alignment, as defined in Recommendation G.732 [4], § 5.2, the indicators shall be extinguished.

3.3.5.3 If time slot 16 is used for common channel signalling, the multiframe alignment signal is not present in a nominal input signal to the instrument. In this case it shall be possible to inhibit the loss of multiframe indicator in order to prevent false alarm indications.

3.3.6 *Distant alarm*

The instrument shall recognize the distant alarm condition as defined in Recommendation G.732 [4] (bit 3 of time slot 0 in frames alternate to those containing the frame alignment signal for at least 2 consecutive occasions and recognized within 4 consecutive occasions) and the appropriate indicator shall be lit.

3.3.7 *Distant multiframe alarm*

3.3.7.1 The instrument shall recognize the distant multiframe alarm condition as defined in Recommendation G.732 [4] (bit 6 of time slot 16, frame 0 for at least 2 consecutive occasions and recognized within 3 consecutive occasions) and the appropriate indicator shall be lit.

3.3.7.2 If time slot 16 is used for common channel signalling, bit 6 will be continuously in state 1. In this case it shall be possible to inhibit the distant multiframe alarm in order to prevent false alarm indications.

3.4 *Cyclic redundancy check procedure*

3.4.1 Where a cyclic redundancy check (CRC) procedure in accordance with Recommendation G.704 [1] is implemented within the 2 Mbit/s signal the instrument shall provide the features detailed in §§ 3.4.2, 3.4.3 and 3.4.4.

3.4.2 The instrument shall indicate the presence of CRC framing bits.

3.4.3 The instrument shall have a means of indicating bit error rates of $1 \cdot 10^{-5}$, $1 \cdot 10^{-6}$ and $1 \cdot 10^{-7}$ and shall cause the appropriate indicator to be illustrated under the conditions defined.

The indication of bit error rates occurring in the received decoded signal and detected by means of the CRC procedure information shall comply with the limits given in Table 2/O.162.

TABLE 2/O.162

Bit error rate indication	Average bit error rate in decoded signal	Probability of indication illuminating or extinguishing within the periods stated below	
		Illuminate	Extinguish
$1 \cdot 10^{-5}$	$1 \cdot 10^{-5}$ $5 \cdot 10^{-6}$ $1 \cdot 10^{-6}$	50% within 1 s 5% within 1 s –	5% within 1 s – 95% within 1 s
$1 \cdot 10^{-6}$	$1 \cdot 10^{-6}$ $5 \cdot 10^{-7}$ $1 \cdot 10^{-7}$	50% within 10 s 5% within 10 s –	5% within 10 s – 95% within 10 s
$1 \cdot 10^{-7}$	$1 \cdot 10^{-7}$ $5 \cdot 10^{-8}$ $1 \cdot 10^{-8}$	50% within 100 s 5% within 100 s –	5% within 100 s – 95% within 100 s

3.4.4 It shall also be possible to count the sum of errors indicated. The count capacity shall be 99 999. A separate indication shall be given if the count exceeds this figure.

3.5 *Code violation detection*

3.5.1 *Definition of an HDB3 code violation*

Two consecutive bipolar violations of the same polarity. This may not be the absolute number of errors.

3.5.2 When used as an HDB3 code violation detector the instrument shall incorporate an indicator to indicate the presence of a digital signal of correct amplitude and bit rate.

3.5.3 The code violation rate shall be indicated in the range 1 in 10^3 to at least 1 in 10^6. Indications of code violations occurring in the input signal and detected as defined in § 3.5.1 above, shall be determined by counting the number of code violations that occur during the period of at least 10^6 time slots.

3.5.4 It shall be possible to indicate the sum of the code violations. This facility will not be required at the same time as the code violation rate is being counted and displayed.

3.5.5 The count capacity shall be 99 999 and a separate indication shall be given if the count exceeds this figure.

3.6 *Performance indications*

As an option the instrument shall be capable of providing performance information in accordance with G.821 [6].

3.7 *Lamp lock – Lamp auto reset*

A facility shall be provided whereby the fault indication lamps either clear automatically when the fault condition clears or remain lit until a manual reset is operated.

3.8 *Time slot access*

As an option it shall be possible to access, at an external interface, the contents of any selected time slot, including time slot 16. An external interface meeting the requirements of a co-directional interface, as defined in Recommendation G.703 [2], is preferred.

4 Display

4.1 The counting sequence shall be started by operating a “start” control and shall be stopped by a “stop” control.

4.2 References to counters and displays being illuminated and extinguished does not imply that “light emitting” displays are essential.

4.3 The counter, and its display, shall be capable of being reset.

5 Alarm function check

A method of introducing fault conditions into the incoming digital signal, in order to check the correct functioning of the instrument, shall be considered.

6 Alarm output signal

As an option, an interface shall be provided to enable an external device, e.g. printer, to be connected to the instrument to allow recording of the status of the digital signal input to the instrument.

An interface in accordance with Recommendation V.24 [7] or V.28 [8], carrying suitably abbreviated, plain text messages in ASCII/T.50 [9] coded format according to the requirements of Recommendation V.4 [10] is preferred.

7 Operating environment

The electrical performance requirements shall be met when operating within the climatic conditions specified in Recommendation O.3, § 2.1.

References

[1] CCITT Recommendation *Synchronous frame structures used at primary and secondary hierarchical levels*, Vol. III, Rec. G.704.

[2] CCITT Recommendation *Physical/electrical characteristics of hierarchical digital interfaces*, Vol. III, Rec. G.703.

[3] CCITT Recommendation *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy* Vol. III, Rec. G.823.

[4] CCITT Recommendation *Characteristics of primary PCM multiplex equipment operating at 2048 kbit/s*, Vol. III, Rec. G.732.

[5] CCITT Recommendation *Frame alignment and CRC procedures relating to frames defined in Rec. G.704*, Vol. III, Rec. G.706.

[6] CCITT Recommendation *Error performance of an international digital connection forming part of an integrated digital network*, Vol. III, Rec. G.821.

[7] CCITT Recommendation *List of definitions for interchange circuits between data terminal equipment and data circuit-terminating equipment*, Vol. VIII, Rec. V.24.

[8] CCITT Recommendation *Electrical characteristics or unbalanced double-current interchange circuits*, Vol. VIII, Rec. V.28.

[9] CCITT Recommendation *International Alphabet No. 5*, Vol. VII, Rec. T.50.

[10] CCITT Recommendation *General structure of signals of International Alphabet No. 5 code for character oriented data transmission over public telephone networks*, Vol. VIII, Rec. V.4.

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