INTERNATIONAL TELECOMMUNICATION UNION

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TELECOMMUNICATION
STANDARDIZATION SECTOR
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V.33

DATA COMMUNICATION OVER THE TELEPHONE NETWORK

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14 400 BITS PER SECOND MODEM STANDARDIZED FOR USE ON POINT-TO-POINT 4-WIRE LEASED TELEPHONE-TYPE CIRCUITS

ITU-T Recommendation V.33

(Extract from the *Blue Book*)

NOTES

1 ITU-T Recommendation V.33 was published in Fascicle VIII.1 of the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Recommendation V.33

14 400 BITS PER SECOND MODEM STANDARDIZED FOR USE ON POINT-TO-POINT 4-WIRE LEASED TELEPHONE-TYPE CIRCUITS

(Melbourne, 1988)

1 Introduction

This modem is intended to be used primarily on special quality leased circuits, e.g. Recommendation M.1020 [1] or M.1025 [2] circuits but this does not preclude the use of this modem over circuits of lower quality at the discretion of the administration concerned (see Notes 1 and 2).

On leased circuits, considering that there exist and will come into being many modems with features designed to meet the requirements of the administrations and users, this Recommendation in no way restricts the use of any other modems.

The principal characteristics of this modem are as follows:

a) fallback rate of 12 000 bits per second;

b) capable of operating in a duplex mode with continuous carrier;

c) combined amplitude and phase modulation with synchronous mode of operation;

d) inclusion of an eight state trellis coded modulation;

e) optional inclusion of a multiplexer for combining data rates of 12 000, 9600, 7200, 4800 and 2400 bits per second (see Note 3).

Note 1 - The principal use of this recommended modem is on 4-wire leased circuits. Other applications, such as stand-by operation on the switched telephone network, half duplex or multipoint operation are for further study. Circuits should be of the special quality type, e.g. M.1020 [1] or M.1025 [2]. However, administrations and users may wish to note that modems conforming to this Recommendation, even assuming proper implementations, will not necessarily operate satisfactorily on all circuits conforming to M.1020 and M.1025; particularly where noise is at or near the specified limiting magnitude.

Note 2 - Attention should be given to the selection of appropriate equalization techniques in the modem implementation, if acceptable performance on circuits conforming to Recommendation M.1025 is desired.

Note 3 - When the multiplexer option is installed, provisions in section 10 may supersede provisions given in other sections.

2 Line signals

2.1 The carrier frequency is to be 1800 ± 1 Hz. The power levels used will conform to Recommendation V.2.

2.2 *Signal space coding*

2.2.1 At 14 400 bits per second, the scrambled data stream to be transmitted is divided into groups of six consecutive data bits. As shown in Figure 1/V.33, the first two bits in time Ql_n, and $Q2_n$ in each group, are first differentially encoded into Yl and Y2 according to Table 1A/V.33. The two differentially encoded bits Yl_n and $Y2_n$ are used as input to a systematic convolutional encoder which generates a redundant bit $Y0_n$. This redundant bit and the six information-carrying bits Yl_n, $Y2_n$, $Q3_n$, $Q4_n$, $Q5_n$, and $Q6_n$ are then mapped into the coordinates of the signal element to be transmitted according to the signal space diagram shown in Figure 2/V.33.

2.2.2 At the fallback rate of 12 000 bit/s, the scrambled data stream to be transmitted is divided into groups of five consecutive data bits. The trellis coding scheme shown in Figure 1/V.33, is used with the modification that first, the line designated by $Q6_n$ is removed and second, the signal element mapping is now as shown in Figure 3/V.33.

2.2.3 Table 1 B/V.33 describes the differential encoding used for the 4800 bit/s rate signal in segment 3 of synchronizing signals (§ 8.3).

TABLE 1A/V.33

Differential encoding for use with trellis coding

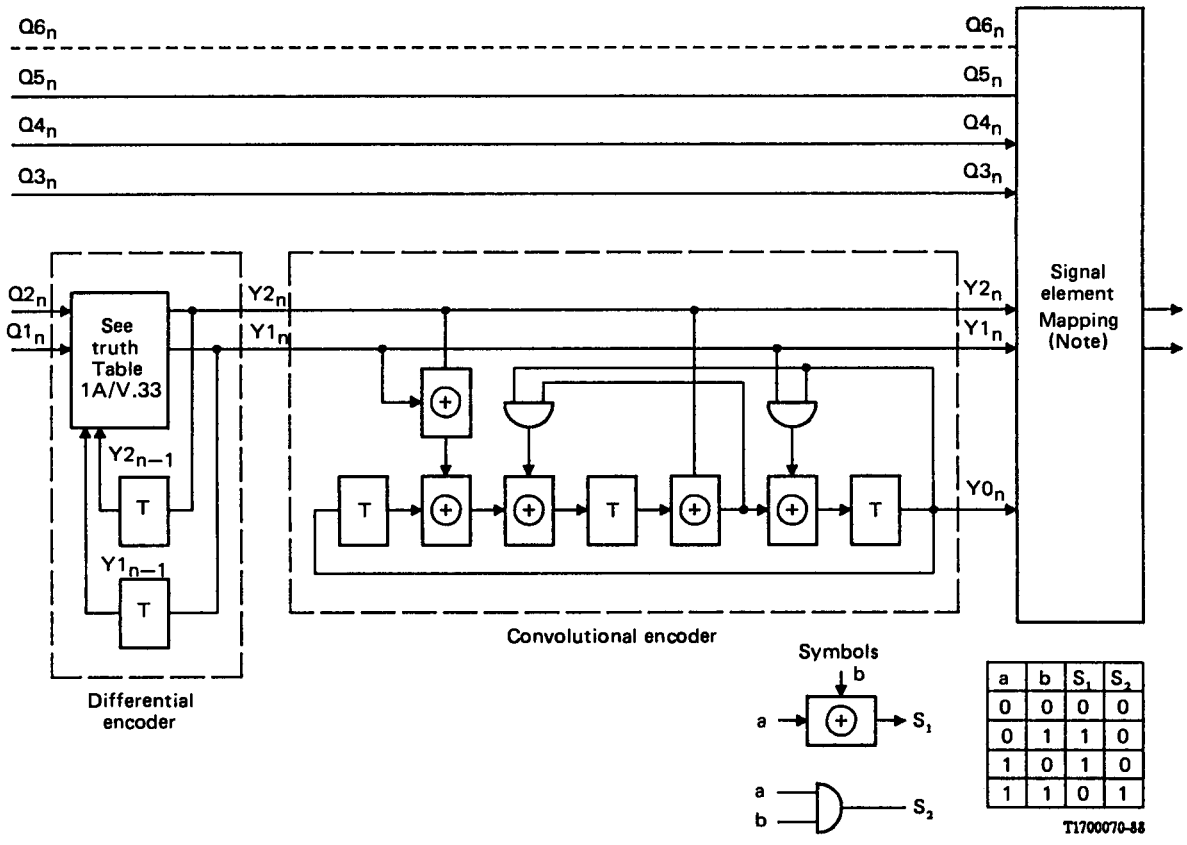
Inputs		Previous outputs		Outputs	
$Q1_n$	$Q2_n$	$Y1_{n-1}$	$Y2_{n-2}$	$Y1_n$	$Y2_n$
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	1	0	0
1	1	0	0	1	1
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	1	0	1

TABLE 1B/V.33

Differential quadrant coding for 4800 bit/s rate signal

Inputs		Previous outputs		Phase quadrant	Outputs		Signal element for	Coordinates	
$Q1_n$	$Q2_n$	$Y1_{n-1}$	$Y2_{n-1}$		$Y1_n$	$Y2_n$	4800 bit/s	Re	Im
0	0	0	0	+90°	0	1	D	-2	+6
0	0	0	1		1	1	A	-6	-2
0	0	1	0		0	0	C	+6	+2
0	0	1	1		1	0	B	+2	-6
0	1	0	0	0°	0	0	C	+6	+2
0	1	0	1		0	1	D	-2	+6
0	1	1	0		1	0	B	+2	-6
0	1	1	1		1	1	A	-6	-2
1	0	0	0	+180°	1	1	A	-6	-2
1	0	0	1		1	0	B	+2	-6
1	0	1	0		0	1	D	-2	+6
1	0	1	1		0	0	C	+6	+2
1	1	0	0	+270°	1	0	B	+2	-6
1	1	0	1		0	0	C	+6	+2
1	1	1	0		1	1	A	-6	-2
1	1	1	1		0	1	D	-2	+6

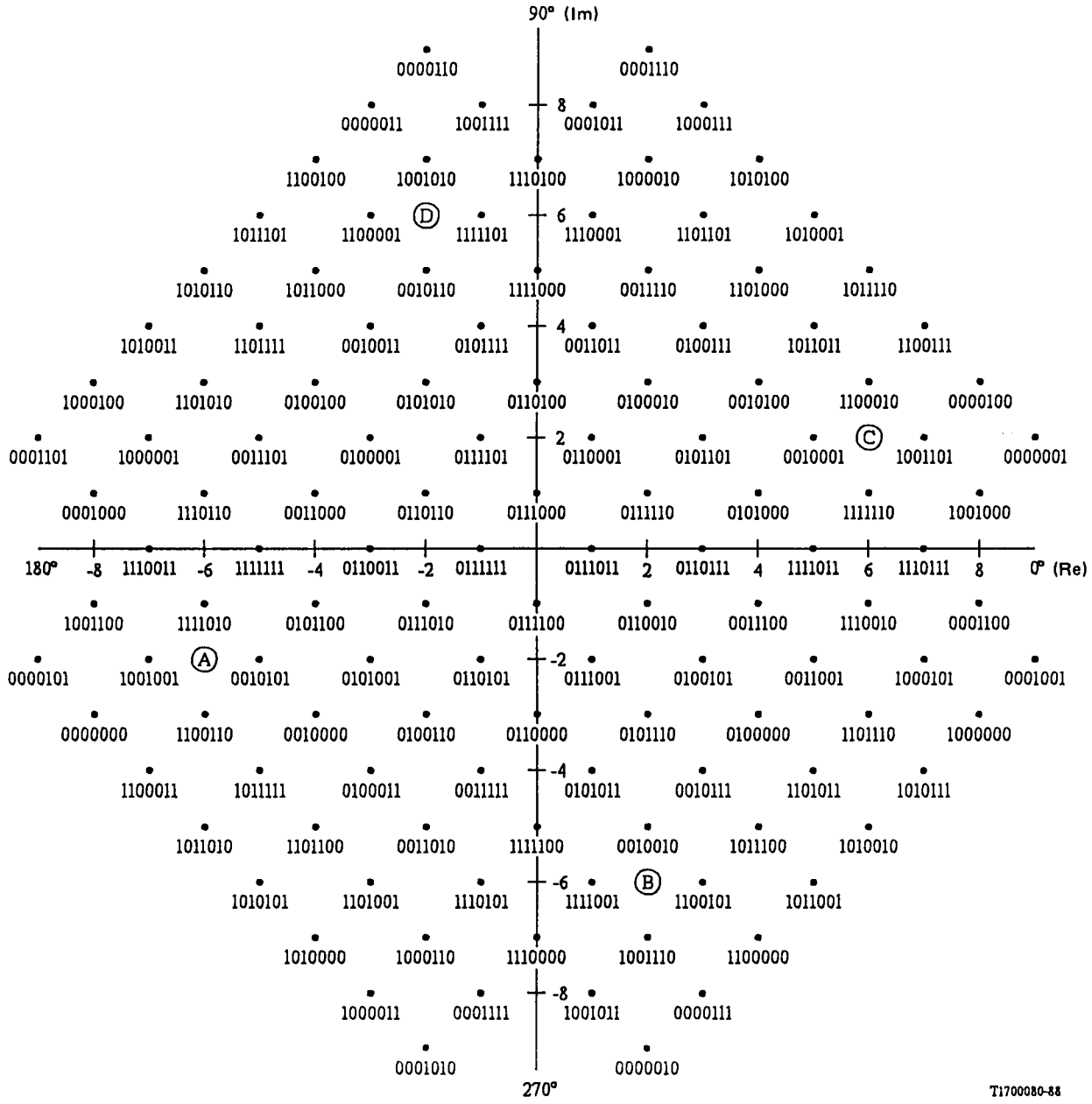
Note - Q1 is the first bit in time.



Note - See Figure 2/V.33 for 14 400 bit/s rate, Figure 3/V.33 for 12 000 bit/s.

FIGURE 1/V.33

Trellis coder at 14 400 bit/s and 12 000 bit/s

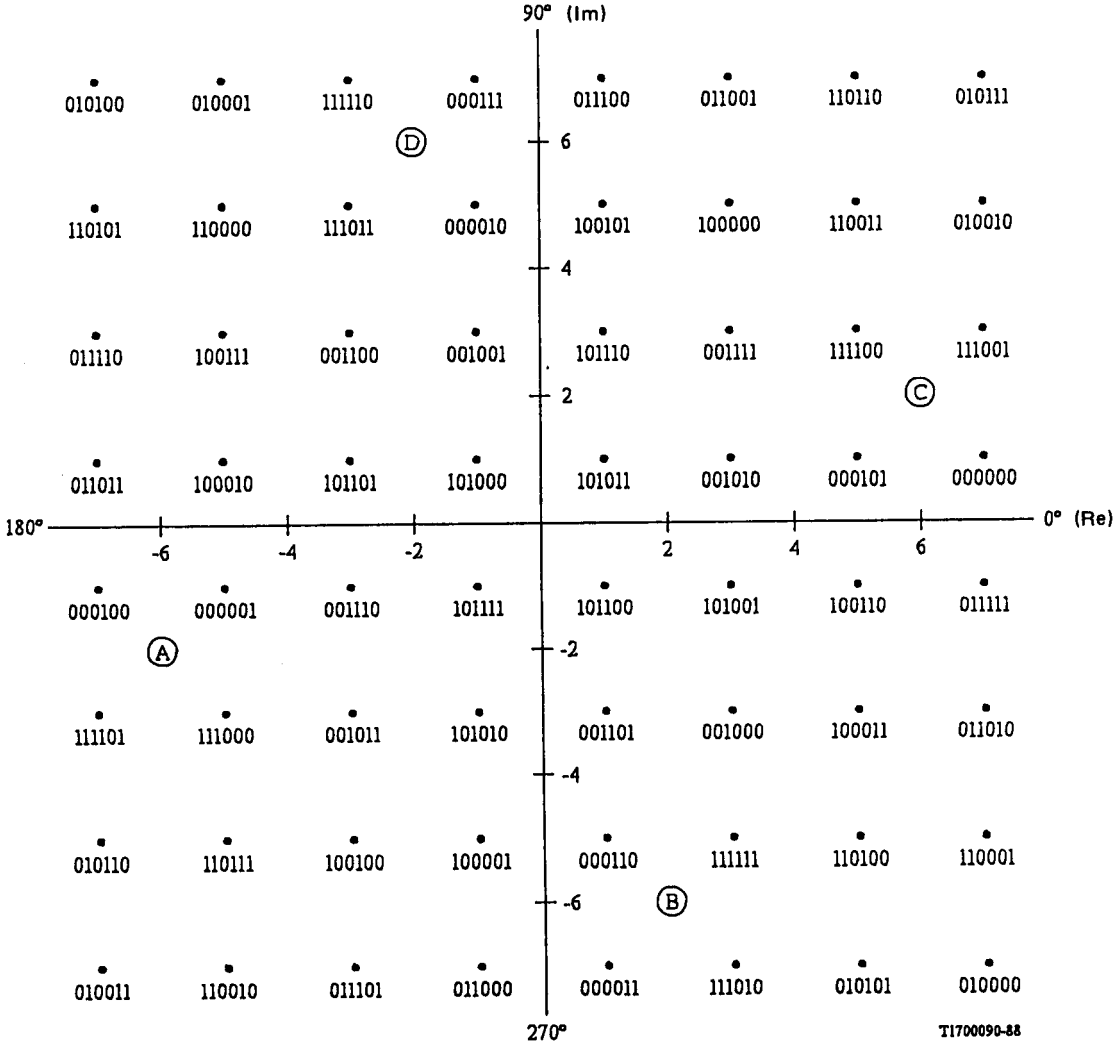


Binary numbers refer to $Q6_n$, $Q5_n$, $Q4_n$, $Q3_n$, $Y2_n$, Yl_n, $Y0_n$,

A, B , C, D refer to synchronizing signal elements

FIGURE 2/V.33

Signal space diagram and mapping for trellis-coded modulation at 14 400 bit/s



Binary numbers refer to $Q5_n$, $Q4_n$, $Q3_n$, $Y2_n$, Yl_n, $Y0_n$,

A, B , C, D refer to synchronizing signal elements

FIGURE 3/V.33

Signal space diagram and mapping for trellis-coded modulation at 12 000 bit/s

3 Data signalling and modulation rates

The data signalling rates shall be 14 400 and 12 000 bit/s ± 0.01%. The modulation rate is 2400 bauds ± 0.01%.

4 Received signal frequency tolerance

The carrier frequency tolerance allowance at the transmitter is ± 1 Hz. Assuming a maximum frequency drift of ± 6 Hz in the connection between the modems, then the receiver must be able to accept errors of at least ± 7 Hz in the received signal frequency.

5 Interchange circuits

5.1 *List of interchange circuits* (Table 2/V.33)

TABLE 2/V.33

Interchange circuit (see Note 1)

No.	Designation	Notes
102	Signal ground or common return	
103	Transmitted data	
104	Received data	
105	Request to send	Note 2
106	Ready for sending	
107	Data set ready	
109	Data channel received line signal detector	
111	Data signalling rate selector (DTE source)	
112	Data signalling rate selector (DCE source)	
113	Transmitter signal element timing (DTE source)	
114	Transmitter signal timing (DCE source)	
115	Receiver signal element timing (DCE source)	
140	Loopback/Maintenance test	Note 3
141	Local loopback	Note 3
142	Test indicator	

Note 1 - All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits provided shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 6).

Note 2 - Not essential for continuous carrier operation.

Note 3 - Interchange circuits 140 and 141 are optional.

5.2 *Threshold and response times of circuit 109*

5.2.1 *Threshold*

- greater than -26 dBm: circuit 109 ON
- less than - 33 dBm: circuit 109 OFF

The condition of circuit 109 for levels between -26 dBm and -33 dBm is not specified except that the signal detector shall exhibit a hysteresis action, such that the level at which the OFF to ON transition occurs is at least 2 dB greater than that for the ON to OFF transition.

5.2.2. *Response times*

- ON to OFF: 40 ± 10 ms:
- OFF to ON:
  1) for initial equalization, circuit 109 must be ON prior to user data appearing on circuit 104;
  2) for re-equalization during data transfer, circuit 109 will be maintained in the ON condition; during this period, circuit 104 may be clamped to the binary 1 condition;

3) after a line signal interruption that lasts more than the ON to OFF response time:
   a) when no new equalization is needed, 25 ± 10 ms;
   b) when a new equalization is needed, circuit 109 must be ON prior to user data appearing on circuit 104.

Response times of circuit 109 are the times that elapse between the connection or removal of a line signal, generated by applying binary one to circuit 103, to or from the modem receive line terminals and the appearance of the corresponding ON or OFF condition on circuit 109.

Note - Circuit 109 ON to OFF response time should be suitably chosen within the specified limits to ensure that all valid data bits have appeared on circuit 104.

5.3 *Response time for circuit 106*

Following the complete training procedure, the time between the OFF to ON transition of circuit 105 and the OFF to ON transition of circuit 106 shall be 15 ms ± 5 ms.

The time between the ON to OFF transition of circuit 105 and the ON to OFF transition of circuit 106 shall be suitably chosen to ensure that all valid signal elements have been transmitted.

6 Electrical characteristics of interchange circuits

6.1 Use of electrical characteristics conforming to Recommendation V.28 is recommended together with the connector pin assignment plan specified by ISO 2110 [3].

6.2 *Fault condition on interchange circuits*

(See § 7 of Recommendation V.28 for association of the receiver failure detection types).

6.2.1 The DTE should interpret a fault condition on circuit 107 as an OFF condition using failure detection type 1.

6.2.2 The DCE should interpret a fault condition on circuit 105 as an OFF condition using failure detection type 1.

6.2.3 All other circuits not referred to above may use failure detection types 0 or 1.

6.3 *Timing arrangements*

Clocks shall be included in the modem to provide the data terminal equipment with transmitter signal element timing, circuit 114, and receiver signal element timing, circuit 115. In this arrangement, the transmitter may either run as an independent timing source or with loopback timing (transmit timing slaved to receive timing). Loopback timing may be desirable in some network applications.

Alternatively, the transmitter signal element timing may be originated in the data terminal equipment and be transferred to the modem via interchange circuit 113.

7 Scrambler

A self-synchronizing scrambler/descrambler having the generating polynomial $1 + x^{-18} + x^{-23}$, shall be included in the modem.

At the transmitter the scrambler shall effectively divide the message polynomial, of which the input data sequence represents the coefficients in descending order, by the scrambler generating polynomial to generate the transmitted sequence. At the receiver the received polynomial, of which the received data sequence represents the coefficients in descending order, shall be multiplied by the scrambler generating polynomial to recover the message sequence.

The detailed scrambling and descrambling processes are described in the Annex.

8 Synchronizing signals

Transmission of synchronizing signals may be initiated by the modem. When the receiving modem requires resynchronizing, it shall turn circuit 106 OFF and generate a synchronizing signal sequence.

The synchronizing signals for all data signalling rates are divided into four segments as in Table 3/V.33.

TABLE 3/V.33

	Segment 1	Segment 2 TRN	Segment 3	Segment 4	Total
Type of line signal	Alternations ABAB	Equalizer condition pattern	Rate sequence	Scrambled all binary ONEs	Total synchronizing signal time
Number of symbol intervals	256	2976	64	48	3344
Approximate time in ms	106	1240	27	20	1393

8.1 Segment 1 consists of alternations between states A and B as shown in Figures 2 and 3/V.33 for a duration of 256 symbol intervals.

8.2 *Segment 2: Equalizer conditioning pattern*

The segment consists of the sequential transmission of four signal elements A, B, C and D. These signal elements are shown in Figures 2/V.33 and 3/V.33. The equalizer conditioning pattern is a pseudo-random sequence at 4800 bit/s generated by the $1 + x^{-18} + x^{-23}$ data scrambler. During segment 2 any differential quadrant encoding is disabled and the scrambled dibits are encoded as follows:

00 = C 01 = D 11 = A 10 = B

With a binary 1 applied to the input, the initial state of the scrambler shall be selected to produce the following scrambler output pattern and corresponding signal elements:

00	01	00	01	00	01	00	01	00	01	00	01	10	01	10	01
C	D	C	D	C	D	C	D	C	D	C	D	B	D	B	D

Segment 2 continues for 2976 symbol intervals.

8.3 *Segment 3: Rate signal*

The rate signal consists of a 16-bit binary sequence repeated 8 times. The sequence is defined in Table 4/V.33, scrambled and transmitted at 4800 bit/s with dibits differentially encoded as in Table 1B/V.33. The differential encoder shall be initialized using the final symbol of the previous segment.

The first two bits and subsequent dibits of each rate sequence shall be encoded as one signal state.

The rate signal may be used for establishing the data signalling rate between the modems, and providing information regarding multiplexer configuration, or other configuration information (subject to further study). When B14 = 0, only data signalling rate information is conveyed according to Table 4A/V.33. When B14 = 1, the bit assignment of Table 4B/V.33 applies.

The minimum requirement for detection is the receipt of two consecutive identical 16-bit sequences each with bits B0-3, B7, Bll and B15 conforming with Table 4/V.33. Following the detection of the rate sequence, the receiver shall be conditioned to receive data at the highest common rate with the indicated multiplexer configuration.

TABLE 4A/V.33

Bit designations

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0				1				1			0	1

B0-3,	B7,	B11,	B15	For synchronizing on a received rate signal
B4-6				Not yet defined (for further study)
B8			1	Denotes ability to transmit and receive data at 12 000 bit/s (Note)
B9			1	Denotes ability to transmit and receive data at 14 000 bit/s (Note)
B10,	B12,	B13		Not yet defined (for further study)

Note - When transmitting a rate signal, the modern will transmit bits B8 B9 equal to 11 or 01 when the data signalling rate of segment 4 equals 14.4 kbit/s and B8 B9 = 10 when the data signalling rate of segment 4 equals 12 kbit/s.

TABLE 4B/V.33

Bit designations

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0				1				1			0	1

B0-3,	B7,	B11,	B15	For synchronzing on a received rate signal
B4,	B5		00	Denotes that B6, B10, B12, B13 define multiplexer configuration select (Note 1)
B8			1	Denotes ability to transmit and receive data at 12 000 bit/s (Notes 1 and 3)
B9			1	Denotes ability to transmit and receive data at 14 000 bit/s (Notes 1 and 3)
B6,	B10,	B12,	B13	Multiplexer configuration select (see Note 2 and Tables 5A, 5B/V.33)

Note 1 - Other combinations of B4, B5 may be used to denote that B6, B8, B9, B10, B12 and B13 define other configuration information (for further study).

Note 2 - a) B6, B10, B12, B13 = all ZEROs: Manual Mode;

b) B6, B10, B12, B13 Binary representation of 1 through 11 (B6 = MSB, most significant bit) denotes desired multiplexer configuration as shown in Tables 5A and 5B/V.33;

c) B6, B10, B12, B13 = all ONEs: Remotely Programmable Mode. If a modem is so configured it will always transmit this pattern.

d) B6, B10, B12, B13 The unused combinations are available for use as manufacturer’s option;

e) It is recommended that either both modems be configured with the identical multiplexer Mode or one modem be configured in the remotely programmable multiplexer Mode.

Note 3 - When transmitting a rate signal, the modems will transmit bits B8 B9 equal to 11 or 01 when the data signalling rate of segment 4 equals 14.4 kbit/s and B8 B9 = 10 when the data signalling rate of segment 4 equals 12 kbit/s.

8.4 *Segment 4*

The differential encoding to be used during this segment is defined in Table 1A/V.33. The differential encoder shall be initialized using the first symbol of the previous segment. Segment 4 shall begin with the initial states of the delay elements of the convolutional encoder shown in Figure 1/V.33 set to zero.

This segment initiates transmission at the highest rate indicated by segment 3 according to the encoding described in § 2.2 above with continuous binary ONEs applied to the input of the data scrambler. The duration of segment 4 is 48 symbol intervals. At the end of segment 4, circuit 106 is turned ON and user data are applied to the input of the data scrambler.

9 Training-retraining procedure

An automatic adaptive equalizer shall be provided in the receiver.

The receiver shall incorporate a means of detecting loss of equalization and initiating a synchronizing signal sequence in its associated local transmitter.

The receiver shall incorporate a means of detecting a synchronizing signal and the rate sequence from the remote transmitter and initiating a synchronizing signal sequence in its associated local transmitter, which may be initiated at any time during the reception of the synchronizing signal sequence, regardless of the state of circuit 105.

Either modem may initiate a synchronizing signal sequence. The synchronizing signal is initiated when the receiver has detected a loss of equalization, or upon detecting a change in data rate or multiplexer configuration selection (made by a switch or by circuit 111). Having initiated a synchronizing signal, the modem expects a synchronizing signal from the remote transmitter.

Following the end of the transmitted synchronizing signal sequence, if the modem does not receive a synchronizing signal from the remote transmitter within a time interval equal to the maximum expected two-way propagation delay, it transmits another signal. A time interval of 1.2 seconds is recommended.

If the modem fails to synchronize on the received signal sequence, or fails to detect the rate signal, or is unable to provide the requested rate, or is transmitting at a rate higher than the requested rate, it transmits another synchronizing signal with rate sequence and data signalling rate conforming with the highest common rate, provided that it had not been sending a synchronizing sequence within the last 1.2 seconds.

If the modem receives a synchronizing signal when it had not initiated a synchronizing signal and the receiver properly synchronizes, it returns only one synchronizing sequence.

Note - When a synchronizing sequence is initiated due to loss of equalization, the previous multiplexer configuration should be maintained.

10 Multiplexing (See Tables 5A/V.33 and 5B/V.33)

A multiplexing option may be included to combine 12 000, 9600, 7200, 4800, and 2400 bit/s data subchannels into a single aggregate bit stream for transmission. Identification of the individual modulator bits is accomplished by assignment to the modulator as defined in § 2.2 above.

TABLE 5A/V.33

Aggregate data rate (bit/s)	Multiplex configuration	Sub-channel data rate (bit/s)	Multiplex channel	Modulator bits					
				Q1	Q2	Q3	Q4	Q5	Q6
14 400	1	14 400	A	X	X	X	X	X	X
14 400	2	12 000 2 400	A B	X	X	X	X	X	 X
14 400	3	9 600 4 800	A B	X	X	 X	X	X	 X
14 400	4	9 600 2 400 2 400	A B C	X	X	 X	X	X	 X
14 400	5	7 200 7 200	A B	X	 X	X	 X	X	 X
14 400	6	7 200 4 800 2 400	A B C	X	 X	X	 X	X	 X
14 400	7	7 200 2 400 2 400 2 400	A B C D	X	 X	X	 X	X	 X
14 400	8	4 800 4 800 4 800	A B C	X	 X	 X	X	 X	 X
14 400	9	4 800 4 800 2 400 2 400	A B C D	X	 X	 X	X	 X	 X
14 400	10	4 800 2 400 2 400 2 400 2 400	A B C D E	X	 X	 X	X	 X	 X
14 400	11	2 400 2 400 2 400 2 400 2 400 2 400	A B C D E F	X	 X	 X	 X	 X	 X

Note - When more than one modulator bit is assigned to a sub-channel, the first bit in time of the sub-channel is assigned to the first available bit in time of the modulator.

TABLE 5B/V.33

Aggregate data rate (bit/s)	Multiplex configuration	Sub-channel data rate (bit/s)	Multiplex channel	Modulator bits					
				Q1	Q2	Q3	Q4	Q5	Q6
12 000	1	12 000	A	X	X	X	X	X	
12 000	2	9 600 2 400	A B	X	X	X	X	 X	
12 000	3	7 200 4 800	A B	X	 X	X	 X	X	
12 000	4	7 200 2 400 2 400	A B C	X	 X	X	X	 X	
12 000	5	4 800 4 800 2 400	A B C	X	 X	X	 X	 X	
12 000	6	4 800 2 400 2 400 2 400	A B C D	X	 X	X	 X	 X	
12 000	7	2 400 2 400 2 400 2 400 2 400	A B C D E	X	 X	 X	 X	 X	

Note - When more than one modulator bit is assigned to a sub-channel, the first bit in time of the sub-channel is assigned to the first available bit in time of the modulator.

10.1 *List of interchange circuits concerned with multiplexer ports*

TABLE 6/V.33

Interchange circuits (see Note 1)		Port A	Port B, C, D, E and F	Notes
No.	Designation			
102	Signal ground or common return	X	X	
103	Transmitted data	X	X	
104	Received data	X	X	
105	Request to send	X	X	Note 2
106	Ready for sending	X	X	Note 3
107	Data set ready	X	X	
109	Data channel received line signal detector	X	X	
111	Data signalling rate selector (DTE source)	X		Note 4
113	Transmitter signal element timing (DTE source)	X	X	
114	Transmitter signal element timing (DCE source)	X	X	
115	Receiver signal element timing (DCE source)	X	X	
140	Loopback/Maintenance test	X	X	Note 5
141	Local loopback	X		Notes 5 & 6
142	Test indicator	X	X	Note 7

Note 1 - All essential interchange circuits and any others which are provided shall comply with the functional and operational requirements of Recommendation V.24. All interchange circuits indicated by X shall be properly terminated in the data terminal equipment and in the data circuit-terminating equipment in accordance with the appropriate Recommendation for electrical characteristics (see § 6).

Note 2 - Circuit 105 is not necessary for continuous carrier transmission. The transmitted line signal will not be controlled by this interchange circuit. If needed, circuit 105 (when the multiplexer is present) is used to control circuit 109 at the remote DCE. See § 10.4 below.

Note 3 - During the synchronization process of the main DCE the OFF condition of circuit 106 is signalled at all port interfaces.

Note 4 - Circuit 111 is optionally present on port A. If present, circuit 111 is activated in multiplexer configuration 1 in the same way as if no multiplexer were present.

Note 5 - Circuits 140 and 141 are optional.

Note 6 - Circuit 141 is present only on port A. When used in multiplexer configurations other than configuration 1, the looping occurs on all ports.

Note 7 - Circuit 142 is present on all ports of the multiplexer, but may be activated on an individual port basis for individual port tests. All are activated simultaneously for entire DCE test.

10.2 *Transmit buffers*

In the transmitter of each multiplexer port, there shall be a data buffer of suitable capacity. In this way, both phase variations and, within certain limits, frequency deviations are absorbed. The buffer shall be initialized when the OFF to ON transition of circuit 105 occurs and may be repositioned in the event of the buffer overflow.

Note - The buffer may be initialized upon the DCE sending a synchronizing signal.

10.3 *Transmit port timing arrangements*

Table 7/V.33 shows all possible combinations of port and main DCE transmit timing clock arrangements.

TABLE 7/V.33

Source of port : transmitter signal element timing (used to clock in circuit 103)	Source of DCE : internal transmitter element timing (internal transit clock)	Port transmit buffer
114 (DCE source)	Internal (Independent timing)	Not required
	External [a] (circuit 113 of selected port)	Not required
	Receiver timing (loopback timing)	Not required
113 (DTE [a] source)	Internal (Independent timing)	Required
	External [a] (Circuit 113 of selected port)	Required for all ports except port supplying circuit 113 to DTE
	Receiver timing (loopback timing)	Required

[a] In these applications a source could also be another DCE.

10.4 *Port simulated circuit 105 to circuit 109 operation* (optional)

Simulated circuits 105 to 109 operation on an individual port interface may optionally be provided in accordance with Recommendation V.13.

ANNEX A

(to Recommendation V.33)

Detailed scrambling, descrambling and pseudo-random sequence generation processes

A.1 *Scrambling*

The message polynomial is divided by the generating polynomial $1 + x^{-18} + x^{-23}$ (see Figure A.1/V.33).

The coefficients of the quotient of this division taken in descending order form the data sequence to be transmitted. The shift register shall be preconditioned to produce the output pattern defined in § 8.2 (the initial state of the scrambler required to generate that pattern is: 1010, 1011, 1011 0011, 0111, 010). The scrambler shall be clocked at 4 800 Hz during segments 2 and 3 and shall be clocked at the data rate during segment 4. During segments 2, 3 and 4 and during normal data transmission, the shift register is fed with scrambled data D_s:

$$D_s = D_i + D_s \, x^{-18} + D_s \, x^{-23}$$

where D_i is binary one during segments 2 and 4 and the rate sequence during segment 3.

A.2 *Descrambling*

The polynomial represented by the received sequence is multiplied by the generating polynomial (Figure A.2/V.33) to form the recovered message polynomial. The coefficients of the recovered polynomial, taken in descending order, form the output data sequence D_o:

$$D_o = D_i = D_s (1 + x^{-18} + x^{-23})$$

A.3 *Elements of the scrambling process*

The polynomial $1 + x^{-18} + x^{-23}$ generates a pseudo-random sequence of length $2^{23} - 1 = 8{,}388{,}607$. This long sequence does not require the use of a guard polynomial to prevent the occurrence of repeated patterns and is particularly simple to implement with integrated circuits.

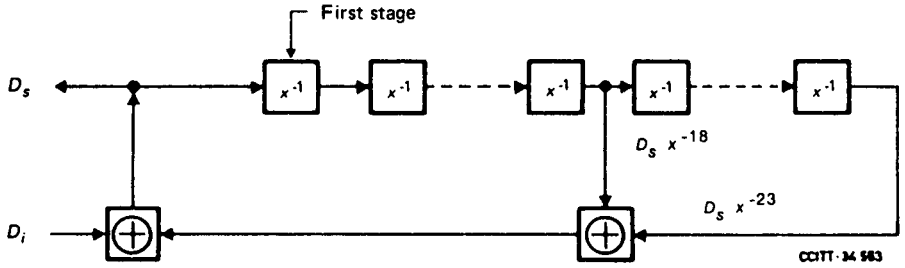


FIGURE A-1/V.33

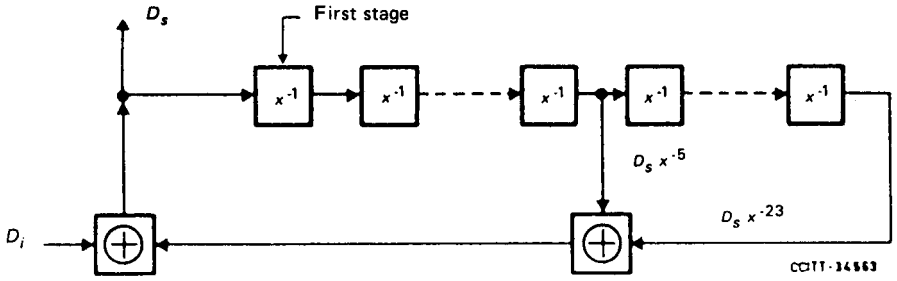


FIGURE A-2/V.33

References

[1] CCITT Recommendation *Characteristics of special quality international leased circuits with special bandwidth conditioning,* Vol. IV, Fascicle IV.2, Rec. M.1020.

[2] CCITT Recommendation *Characteristics of special quality international leased circuits with basic bandwidth conditioning,* Vol. IV, Fascicle IV.2, Rec. M.1025.

[3] Data communication - *25-pin DTE/DCE interface connector and pin assignments,* ISO Standard 2110.