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V.41

DATA COMMUNICATION OVER THE TELEPHONE NETWORK

CODE-INDEPENDENT ERROR-CONTROL SYSTEM

ITU-T Recommendation V.41

(Extract from the *Blue Book*)

NOTES

1 ITU-T Recommendation V.41 was published in Fascicle VIII.1 of the *Blue Book*. This file is an extract from the *Blue Book*. While the presentation and layout of the text might be slightly different from the *Blue Book* version, the contents of the file are identical to the *Blue Book* version and copyright conditions remain unchanged (see below).

2 In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Recommendation V.41

CODE-INDEPENDENT ERROR-CONTROL SYSTEM

(Mar del Plata, 1968, amended at Geneva, 1972)

1 General

This Recommendation is primarily intended for error control when implemented as an intermediate equipment which may be provided either with data terminal equipment or with the data circuit-terminating equipment. The appropriate interfaces are shown in Figures 1/V.41 and 2/V.41. The system is not primarily intended for use with multi-access computing systems. The Recommendation does not exclude the use of any other error-control system that may be better adapted to special needs.

The modems used must provide simultaneous forward and backward channels. The system uses synchronous transmission on the forward channel and asynchronous transmission on the backward channel. When modems to Recommendation V.23 are used with data signalling rates of 1200 or 600 bit/s in the general switched telephone network, Recommendation V.5 applies, the error-control equipment being classed as communication equipment. The margin of the synchronous receiver should be at least ± 45%.

The system employs block transmission of information in fixed units of 240, 480, 960 or 3840[1)] bits and is therefore most suited to the transmission of medium or long data messages, but a fast starting procedure is incorporated to improve the transmission efficiency for shorter messages.

Error control is achieved by means of automatic repetition of a block upon request (ARQ) from the data receiver. If storage is provided at the receiver, detected errors can be removed before the system output (clean copy). Storage for at least two data blocks must be provided at the transmitter.

The forward bit stream is divided into blocks each consisting of four service bits, the information bits, and 16 error-detection (or check) bits in that order, the check bits being generated in a cyclic encoder. Thus each block transmitted to line contains 260, 500, 980 or 3860[1)] bits.

The system will detect:

a) all odd numbers of errors within a block;

b) any error burst not exceeding 16 bits in length and a large percentage of other error patterns.

Assuming a distribution of errors as recorded in reference [1], the error-rate improvement factor has been indicated by a computer simulation to be of the order of 50 000 for a block size of 260 bits.

The fixed block system employed limits the use of the system to those lines having a loop propagation time not greater than the figures given in Table 1/V.41. Allowances of 40 ms for total modem delay and 50 ms for the detection of the RQ signal have been made.

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1) This block length is suitable for circuits provided by means of geostationary orbit satellites.

TABLE 1/V.41

Maximum permissible line loop propagation times (ms)

Block size (bits) \ Data signalling rate (bit/s)	200	600	1200	2400	3600	4800
260	1 210	343	127	18	-	-
500	2 410	743	327	118	49	14
980	4 810	1543	727	318	182	114
3860	19 210	6343	3127	1518	982	714

2 Encoding and checking process

The service bits and information bits, taken in conjunction, correspond to the coefficients of a message polynomial having terms from x^{n-1} (n = total number of bits in a block or sequence) down to x^{16}. This polynomial is divided, modulo 2, by the generating polynomial $x^{16} + x^{12} + x^5 + 1$. The check bits correspond to the coefficients of the terms from x^{15} to x^0 in the remainder polynomial found at the completion of this division. The complete block, consisting of the service and information bits followed by the check bits, corresponds to the coefficients of a polynomial which is integrally divisible in modulo 2 fashion by the generating polynomial.

At the transmitter the service bits and information bits are subjected to an encoding process equivalent to a division by the generator polynomial. The resulting remainder is transmitted to line immediately after the information bits, commencing with the highest order bits.

At the receiver, the incoming block is subjected to a decoding process equivalent to a division by the generator polynomial which in the absence of errors will result in a zero remainder. If the division results in other than a zero remainder, errors are indicated.

The above processes may conveniently be carried out by a 16-stage cyclic shift register with appropriate feedback gates (see Figures I-1/V.41 and I-2/V.41) which is set to the all 0 position before starting to process each block; at the receiver the all 0 condition after processing a block indicates error-free reception.

Use of scramblers - Where self-synchronizing scramblers (i.e. scramblers which effectively divide the message polynomial by the scrambler polynomial at the transmitter and multiply the received polynomial by the scrambler polynomial at the receiver) are used, in order to ensure satisfactory performance of the error-detecting system, the scrambler polynomial and the Recommendation V.41 generating polynomial must have no common factors. Where this condition cannot be maintained, the scrambling process must precede the error detection encoding process and the descrambler process must follow the error detection decoding process. Where additive (i.e. non-self-synchronizing) scramblers are used, this precaution need not be observed.

3 The service bits

3.1 *Block sequence indication*

The four service bits at the beginning of each block transmitted to the line indicate the block sequence and convey control information external to the message information. One of these control functions is to ensure that the information block order can be checked during repetitions, thus ensuring that information is not lost, gained or transposed. Three block sequence indicators A, B and C are used cyclically in that order.

Once a sequence indicator has been attached to an information block it remains with that block until the block is received correctly. Examination of the sequence indication is an additional part of the checking process.

3.2 *Allocation of service bits*

The allocation of the 16 possible combinations of the four service bits is given in Tables 2/V.41 and 3/V.41. Table 2/V.41 lists essential and therefore mandatory combinations and Table 3/V.41 optional combinations.

TABLE 2/V.41

Essential combinations

Group	Combination	Function
a	0011	Block A sequence indicator
b	1001	Block B sequence indicator
c	1100	Block C sequence indicator
d	0101	Synchronizing sequence prefix

Note - The digit on the left occurs first.

TABLE 3/V.41

Optional combinations

Group	Combination	Function
e	0110	Hold block
f	1000	End of transmission (this block contains no data)
g	0001	Start of message 1 (five-unit codes)
h	1010	Start of message 2 (six-unit codes)
j	1011	Start of message 3 (seven-unit codes)
k	0010	start of message 4 (eight-unit codes)
l	0100	End of message (this block contains no data)
m	0111	Data link escape (general control block)
n	1101	}
p	1110	} To be allocated
q	1111	} by bilateral agreement
r	0000	}

3.3 *Control functions*

Synchronization is the only essential control function catered for in the service bits.

The optional *Data link escape* (general control) block contains data which are special in some way agreed to by the users.

Additional optional functions are *Start of message 1* (or for five-unit codes), *Start of message 2* (or for six-unit codes), *Start of message 3* (or for seven-unit codes), *Start of message 4* (or for eight-unit codes), *End of message*, and *End of transmission.*

Four additional service bit combinations are available for allocation by bilateral agreement.

The message information part of the non-data blocks *(Hold, End of transmission* and *End of message)* is of no significance, but such blocks will still be checked at the receiver.

When the optional facilities groups g to k are not used, the first data block following the OFF to ON transition of *Ready for sending* is automatically prefixed *Block A sequence indicator, group a.* Data blocks BCABC, etc. then follow sequentially unless one (or more) of the other types of block are inserted.

When the optional facilities groups g to k are used, the first data block is prefixed by one of the *Start of message indicators* 1, 2, 3 or 4 (groups g to k), depending on the number of bits per character which will be used during transmission. Data blocks ABCAB, etc. then follow. Should an interruption to a leased type connection occur during transmission or should an operator interrupt the transmission to change to the speech mode, the transmission will be resumed with the sequence indicator following that of the last block to be accepted before the interruption. A *Start of message* indicator should not be used after such an interruption.

In the case of switched connections, special measures may be necessary to ensure that an interrupted message is not continued by a new message without appropriate indication.

4 Correction procedure

A binary 1 condition on the backward channel (the supervisory channel) indicates the need for repetition of information (RQ). Conversely, a binary 0 implies acceptance of the transmitted information. The rules governing the transmission and reception of these conditions are given in the following and §§ 5 and 6 below.

4.1 *Data transmitter sequence*

Starting and resynchronizing conditions are given in §§ 5 and 6 below, only normal operations being dealt with here.

Data are transmitted block by block, but the contents of each transmitted block together with its service bits are held in store at the transmitter until correct reception has been ensured. Storage for at least two blocks must be provided.

During transmission of a block the condition of the backward channel (circuit 119) is monitored for a period of 45-50 milliseconds immediately prior to transmission of the last check bit. If any RQ is found within this period the block is rendered invalid by inverting this last bit. The transmitter then recommences transmission from the beginning of the previous block by reference to the store. During the retransmission of the block which follows the detection of the RQ signal, the state of the backward channel is ignored.

4.2 *Receiver procedure*

In normal operation a binary 0 is maintained on the backward channel as long as blocks are received with correct check bits and permissible service combinations. Any data contained in these blocks are passed to the receiver output. If a clean copy output is required, data storage for at least one block should be provided since a block cannot be checked until it has been completely received.

When a block has been received which does not meet the error check condition, binary 1 is transmitted on the backward channel and the expected service bit combination is noted in the receiver.

Usually, the first received data block in the repetition cycle having correct check bits also will have an acceptable service bit combination and any data within it will be processed. Occasionally the first block which checks correctly may bear an abnormal service bit combination due to a line transmission error in the backward channel (causing either a mutilated or imitated binary 0 signal). In either case the data in this first block are discarded. In the case that the block checks correctly but the service bit combination indicates the block preceding the expected block, a binary 0 should be applied to the backward channel.

If the next block checks correctly and bears an acceptable service bit combination, its data should be processed and normal operation resumed. In the case that the service bit combination indicates an invalid block, a binary 1 should be applied; moreover, if the service bit combination indicates the block following the expected block, it is implied that a binary 0 has been imitated for the whole of the 45 ms period specified in § 4.1 above and an alarm must be given since it is not possible to recover from this (rare) condition automatically.

5 Starting procedures

5.1 *Transmitter procedures and synchronizing pattern*

During the delay between *Request to send and Ready for sending*, line idle conditions (binary 1) are emitted by the modem. The first data signals, after the modem is ready for sending, are the synchronizing sequence prefix (0101), followed by the synchronizing filler, followed by the synchronizing pattern. The filler may be of any length provided it includes at least 28 transitions and does not include the synchronizing pattern. The synchronizing pattern is 0101000010100101 starting from the left-hand digit (see Appendix I for a possible derivation). The 28 transitions are provided for bit synchronization purposes. These synchronizing signals are followed by *Block A* or a *Start of message* block (groups g to k in Table 3/V.41). During the whole of this sequence from the beginning of the synchronizing prefix the transmitter ignores the condition of the backward channel, acting as though binary 0 were present. The condition of the backward channel then assumes its normal significance (see § 4 above). Should this be binary 1 during the examination period of the second block, this block must be completed with the last bit inverted and the starting procedure must be recommenced from the beginning of the synchronizing sequence prefix.

5.2 *Receiver procedures*

Binary 1 is emitted on the backward channel at the receiving terminal until the synchronizing pattern (0101000010100101) is detected, at which time binary 0 is emitted and block timing is established. The only acceptable service bit combinations to follow the synchronizing pattern are the *Block A* sequence indicator or a *Start of message* indicator (when used). If other service bit combinations are received, binary 1 is returned and the search for the synchronizing pattern is resumed.

6 Resynchronization procedure

6.1 *Recovery of synchronization*

Should the receiver fail to recognize an acceptable block within a reasonable time, then it must examine the incoming bit stream continuously to find the synchronization pattern. When this pattern is found, block timing is re-established and the binary 0 condition applied to the backward channel; the procedure is identical to the starting procedure except that the expected service bit combination is that following the last sequence indicator to have been accepted.

6.2 *Emission of synchronization pattern*

If the normal repetition cycle has continued for a number of times consecutively (typically 4 or 8) the transmitter must assume that resynchronization is necessary. The normal repetition cycle is replaced by a three-block cycle including a synchronization block and the two blocks previously repeated. The synchronization block contains the synchronization sequence prefix, filler and pattern as described in § 5.1 above.

Note - A short filler should result in quicker resynchronization, particularly when long blocks are used. However, the short filler has the disadvantage that correct synchronization can be lost if the prefix is imitated or disturbed by noise or should the synchronization pattern be disturbed. The use of the longer filler, making the block the same length as the data block, overcomes this difficulty. There is the option to choose either length, both lengths being compatible.

6.3 *Use of synchronization block for delay in transmission*

The information flow may be suspended by the insertion of a synchronizing "block". In the case of the short filler it is essential that the receiving terminal should recognize the synchronizing prefix and change itself immediately into the synchronizing search mode, otherwise synchronization will be lost. In the case of the filler which produces a normal block length it is desirable to change into the search mode without abandoning block timing, a backward binary 0 being returned at the end of the block if the prefix is recognized and the check bits correspond to the synchronization pattern.

It may happen that the transmitter emits a resynchronization cycle before the receiver has changed into the synchronization search condition. The procedure at the receiver is identical to that just described for the use of a synchronization block for suspending the information flow.

7 Interfaces

7.1 *Modem interfaces*

In the normal case where the modems are not an integral part of the data terminal, the modem interfaces are as shown at points A-A in Figures 1/V.41 and 2/V.41. Where synchronous modems are employed, the appropriate signal element timing circuits will also be included in these interfaces.

7.2 *Data terminal interfaces*

Where the error control equipment (including stores) is not an integral part of the data terminal, the error control equipments are interposed between the data terminals and the modem. The data terminal interfaces are then as indicated at B-B and C-C in Figures 1/V.41 and 2/V.41 respectively. A signal element timing circuit is included in each of these interfaces.

7.2.1 In the case of the transmitting terminal all the interchange circuits perform their usual functions but *ready-for-sending* also takes advantage of the final paragraph of its definition in Recommendation V.24 and performs in the following manner:

Ready-for-sending circuit (see Figure 1/V.41)

This circuit, in conjunction with the signal element timing circuit, will inform the data terminal equipment when data are required in response to the *request-to-send* circuit. The *ready-for-sending* circuit will go to the ON condition when data are required and to the OFF condition when data are not required (in general this will be during the service and check bit transmissions and any repetition). This circuit will not go to the ON condition until the *request-to-send* circuit has gone to the ON condition. All transitions of this circuit will coincide with the signal element timing transition from ON to OFF. The transition from ON to OFF will thus coincide with the signal element timing transition from ON to OFF during the 240th, 480th, 960th or 3840th bit of the information within a block, as appropriate.

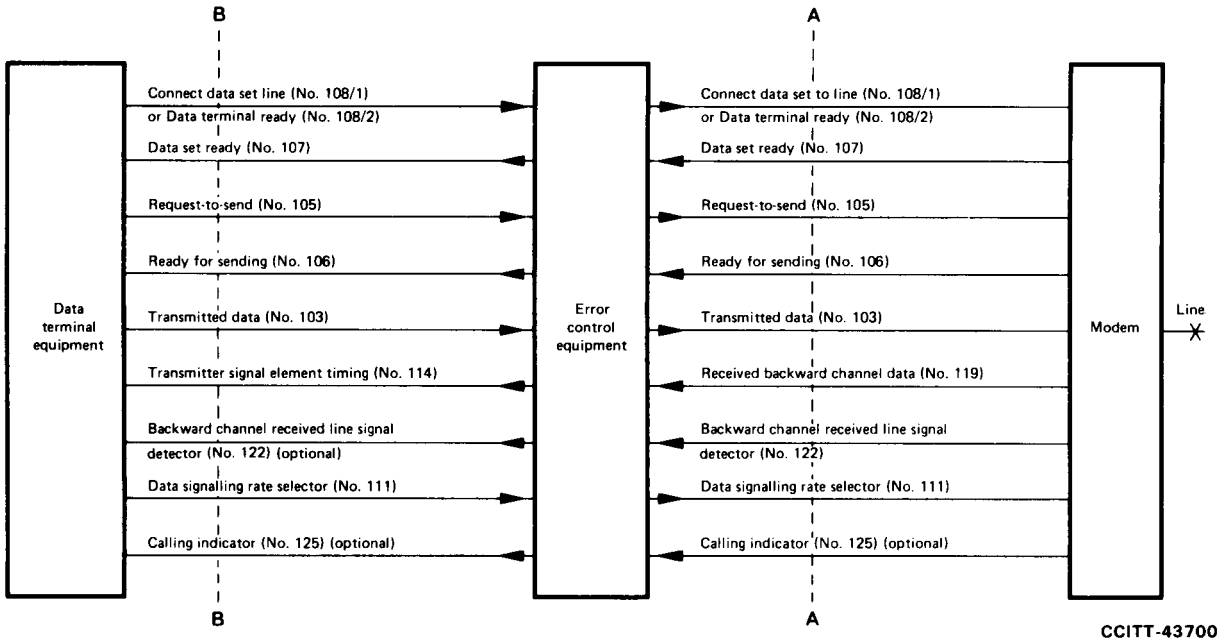

FIGURE 1/V.41

Interchange circuits – Transmitting terminal

7.2.2 In the case of the receiving terminal two new circuits are introduced, but since two (or more) of the modem interface circuits are not used in this interface, the number of circuits is not increased. Circuit 118 - *Transmitted backward channel data* is not available at this interface.

A *Ready for receiving* function must be provided to inform the error control equipment of the status of the data terminal. This function may be performed by circuit 108, in which case a connection on the switched telephone network will be released when the circuit goes from ON to OFF. Alternatively, a separate function control circuit may be provided in order to retain the line connection for short periods when the data terminal is unable to accept data. This new circuit may be assumed to take the place of circuit 120 and functions in the following manner:

Ready-for-receiving (see Figure 2/V.41)

Direction: to error control equipment from data terminal equipment

The data terminal equipment shall maintain the ON condition on this circuit when the data terminal equipment is ready to receive data. Since the error control equipment will receive data in blocks, the data terminal equipment must be capable of receiving data also in blocks. Therefore, the data terminal equipment shall change this circuit to the ON condition only if the data terminal equipment is capable of accepting a block of data (240, 480, 960 or 3840 elements) and shall return to the OFF condition if the data terminal equipment cannot accept another block within 15 element intervals after the end of the previous block of transferred data.

Note - If this *Ready for receiving* circuit is OFF at the end of this 15-element period, an RQ condition will be generated.

The other new circuit performs the function of responding to the ready-for-receiving function and is therefore analogous to circuit 121 - *Backward channel ready.* This new circuit functions as below:

Received-data-present (see Figure 2/V.41)

Direction: from error control equipment to data terminal equipment

This circuit, in conjunction with the signal element timing circuit, will inform the data terminal equipment when data are going to be output in response to the receive data terminal's connect data set to line (and separate *Ready for receiving* circuit when provided) and the incoming data from the distant end being adjudged correct. *The Received data present* circuit will go to the ON condition when data are going to be output and to the OFF condition at all other times. All transitions of this circuit will coincide with the signal element timing transition from ON to OFF. The transition from ON to OFF will thus coincide with the signal element timing transition from ON to OFF during the 240th, 480th, 960th or 3840th bit of information within a block as appropriate.

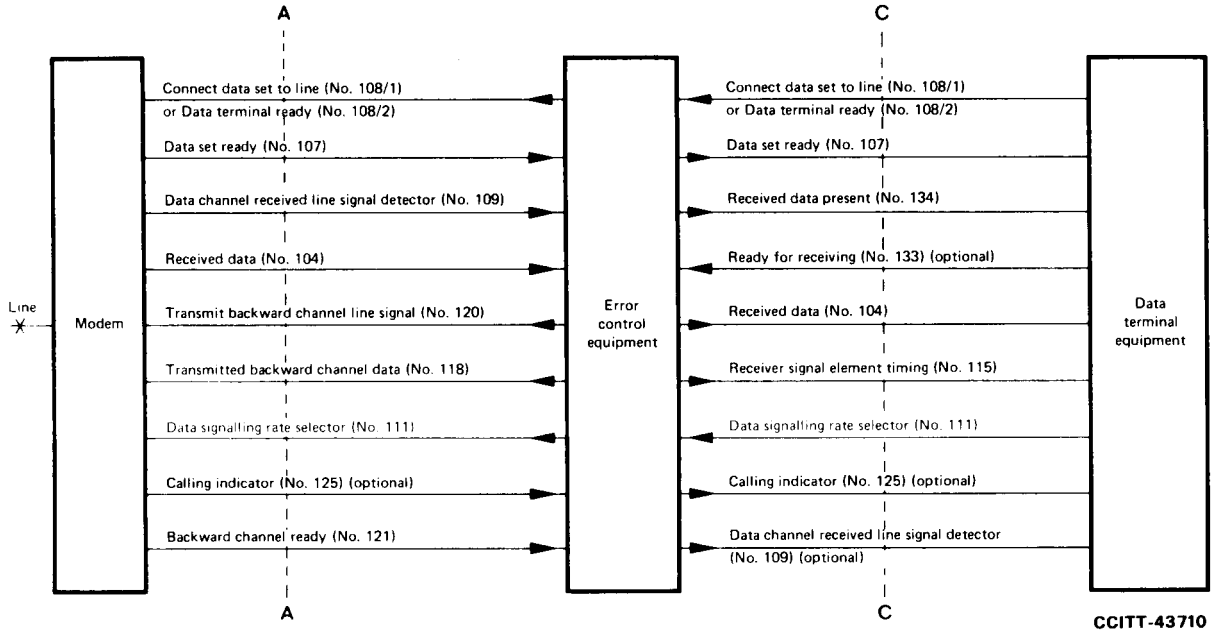

FIGURE 2/V.41

Interchange circuits – Receiving terminal

7.2.3 Additional interchange circuits may be provided at the data terminal interface by bilateral agreement of the users. These additional circuits may be used to introduce service bit control functions other than those provided as a basic necessity. Such circuits should not interfere with the operation of the recommended circuits.

8 Use of service functions

Data link escape is included in Table 3/V.41 as an optional indicator and its use is left to be agreed between operators. It may, for instance, be used to signal to a receiving station that the sending station wishes to speak over the connection. In this case the receiving equipment would operate a bell or similar calling device and transfer the line from the modem to a telephone. Alternatively, it may cause a short message to be printed on a teleprinter for the attention of an operator.

End of transmission is envisaged as giving a positive indication to the receiver that the transmission has ended and that the connection may be released. This is an alternative to the data terminal equipment interpreting the received data to know when to release the connection.

The optional start of message indicators together with the end of message indicator may be used to route messages to different destinations or terminal equipment at the receiving end, which may include the selection of equipment appropriate to the code used.

The hold block need not be used at a transmitter since synchronization sequences may be used as packing between data blocks in the event of data not being ready at the transmitting data terminal equipment, but if required a hold block may be used for this purpose.

APPENDIX I

(to Recommendation V.41)

Encoding and decoding realization for cyclic code system

I.1 *Encoding*

Figure I-1/V.41 shows an arrangement for encoding using the shift register. To encode, the storage stages are set to zero, gates A and B are enabled, gate C is inhibited and k service and information bits are clocked into the input. They will appear simultaneously at the output.

After the bits have been entered, gates A and B are inhibited and gate C is enabled, and the register is clocked a further 16 counts. During these counts the required check bits will appear in succession at the output.

Generation of the synchronizing pattern may be achieved by making $k = 4$, the four bits being 0101. Clocking is suspended for the duration of the synchronizing filler.

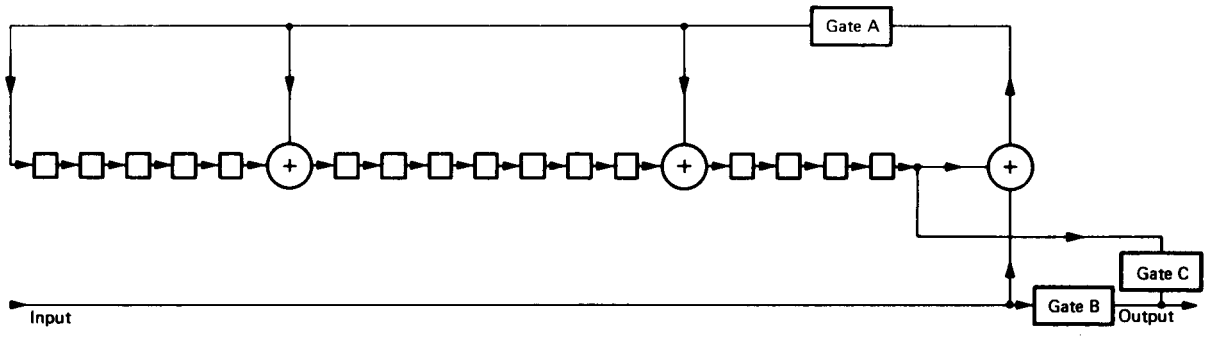

FIGURE I-1/V.41

Encoder

1.2 *Decoding*

Figure I-2/V.41 shows an arrangement for decoding using the shift register. To decode, gates A, B and E are enabled, gate D is inhibited and the storage stages are set to zero.

The *k* information or prefix bits are then clocked into the input and after *k* counts gate B is inhibited, the 16 check bits are then clocked into the input and the contents of the storage stages are then examined. For an error-free block the contents will be zero. A non-zero content indicates an erroneous block.

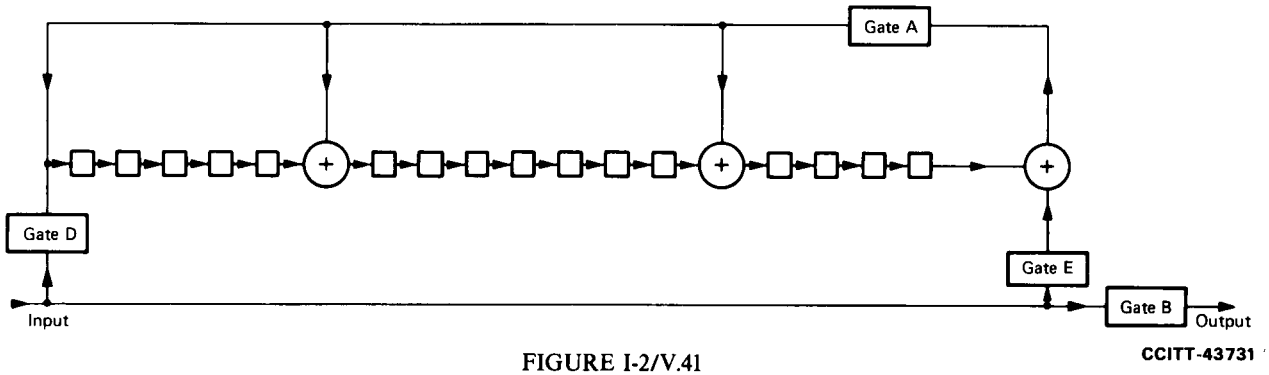

FIGURE I-2/V.41

Decoder

1.3 *Synchronizing at receiver*

For block synchronizing gate D is enabled (Figure I-2/V.41 and gates A, B and E are inhibited and the register is examined in successive bit intervals for the required 16-bit pattern. When the pattern is recognized the register and bit counter are set to zero and decoding proceeds normally.

Reference

[1] *Measurements on switched and leased telephone lines transmitting data at speeds of 250, 800 and 1000 bauds*, Blue Book, Vol. VIII, Supplement No. 22, ITU, Geneva, 1964.